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October 2013

# FCH47N60F\_F085

# N-Channel MOSFET 600V, 47A, 75m $\Omega$

### **Features**

- Typ  $r_{DS(on)}$  = 66mΩ at  $V_{GS}$  = 10V,  $I_D$  = 47A
- Typ  $Q_{q(tot)}$  = 190nC at  $V_{GS}$  = 10V,  $I_D$  = 47A
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

## Description

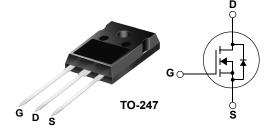
SuperFET<sup>TM</sup> is Fairchild's proprietary new generation of high voltage MOSFETs utilizing an advanced charge balance mechanism for outstanding low on-resistance and lower gate charge performance.

This advanced technology has been tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy.

Consequently, SuperFET is suitable for various automotive DC/DC power conversion.

## **Applications**

- Automotive On Board Charger
- Automotive DC/DC converter for HEV



For current package drawing, please refer to the Fairchild website at www.fairchildsemi.com/packaging



# **MOSFET Maximum Ratings** $T_J = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter		Ratings	Units
$V_{DSS}$	Drain to Source Voltage		600	V
V <sub>GS</sub>	Gate to Source Voltage		±30	V
-	Drain Current - Continuous (V <sub>GS</sub> =10) (Note 1)	T <sub>C</sub> = 25°C	47	^
ID	Pulsed Drain Current	T <sub>C</sub> = 25°C	See Figure4	Α
E <sub>AS</sub>	Single Pulse Avalanche Energy	(Note 2)	810	mJ
1	Power Dissipation		417	W
$P_D$	Derate above 25°C		3.3	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature		-55 to + 150	°C
$R_{\theta JC}$	Thermal Resistance Junction to Case		0.3	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance Junction to Ambient	(Note 3)	50	°C/W

## **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCH47N60F	FCH47N60F_F085	TO-247	-	-	30 units

#### Notes:

- 1: Current is limited by bondwire configuration.
- 2: Starting  $T_J = 25^{\circ}C$ , L = 5mH,  $I_{AS} = 18A$ ,  $V_{DD} = 100V$  during inductor charging and  $V_{DD} = 0V$  during time in avalanche
- 3:  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in<sup>2</sup> pad of 2oz copper.

Units

Max

# **Electrical Characteristics** $T_J = 25^{\circ}C$ unless otherwise noted

**Parameter** 

Off Characteristics							
B <sub>VDSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = 250μA, V	<sub>'GS</sub> = 0V	600	-	-	V
	Desire to Course I calcare Course	V <sub>DS</sub> =600V,	$T_J = 25^{\circ}C$	-	-	10	μА
DSS	I <sub>DSS</sub> Drain to Source Leakage Current		$T_J = 150^{\circ}C(Note 4)$	-	-	1	mA
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 30V$		-	-	±100	nA

**Test Conditions** 

Min

Тур

### On Characteristics

Symbol

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$		3.0	4.0	5.0	V
-	r <sub>DS(on)</sub> Drain to Source On Resistance	I <sub>D</sub> = 47A,	$T_{\rm J} = 25^{\rm o}{\rm C}$	-	66	75	$m\Omega$
DS(on)		V <sub>GS</sub> = 10V	$T_J = 150^{\circ}C(Note 4)$	-	180	223	mΩ

# **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	), OE), ),	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V, f = 1MHz		5900	8000	pF
C <sub>oss</sub>	Output Capacitance				3200	4200	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 1101112			250	-	pF
$R_g$	Gate Resistance	f = 1MHz	f = 1MHz		1	-	Ω
$Q_{g(ToT)}$	Total Gate Charge at 10V	V <sub>GS</sub> = 0 to 10V	V <sub>DD</sub> = 300V	-	190	250	nC
$Q_{g(th)}$	Threshold Gate Charge	V <sub>GS</sub> = 0 to 2V	$V_{GS} = 0 \text{ to } 2V$ $I_D = 47A$		12	18	nC
$Q_{gs}$	Gate to Source Gate Charge				40	-	nC
$Q_{qd}$	Gate to Drain "Miller" Charge			-	96	-	nC

# **Switching Characteristics**

t <sub>on</sub>	Turn-On Time		-	-	410	ns
t <sub>d(on)</sub>	Turn-On Delay Time		-	110	-	ns
t <sub>r</sub>	Rise Time	V <sub>DD</sub> = 300V, I <sub>D</sub> = 47A,	-	160	-	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS} = 10V, R_G = 25\Omega$	-	540	-	ns
t <sub>f</sub>	Fall Time		-	125	-	ns
t <sub>off</sub>	Turn-Off Time		-	-	1000	ns

### **Drain-Source Diode Characteristics**

V	Source to Drain Diade Voltage	I <sub>SD</sub> = 47A, V <sub>GS</sub> = 0V	-	-	1.4	٧
$V_{SD}$	Source to Drain Diode Voltage	$I_{SD} = 23.5A, V_{GS} = 0V$	-	-	1.25	V
T <sub>rr</sub>	Reverse Recovery Time	$I_F = 47A$ , $dI_{SD}/dt = 100A/\mu s$ ,	-	207	350	ns
Q <sub>rr</sub>	Reverse Recovery Charge	V <sub>DD</sub> =480V	-	2.0	3.6	uC

#### Notes

4: The maximum value is specified by design at  $T_J$  = 150°C. Product is not tested to this condition in production.

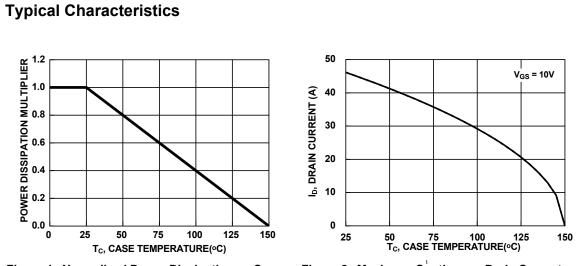


Figure 1. Normalized Power Dissipation vs Case Temperature

Figure 2. Maximum Continuous Drain Current vs Case Temperature

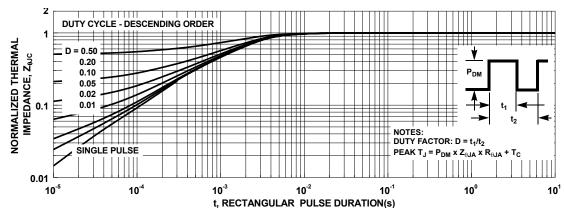


Figure 3. Normalized Maximum Transient Thermal Impedance

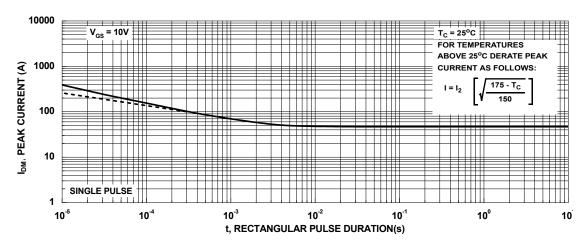


Figure 4. Peak Current Capability

# **Typical Characteristics**

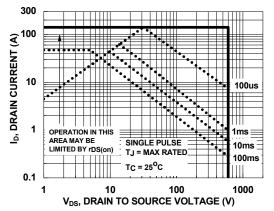


Figure 5. Forward Bias Safe Operating Area

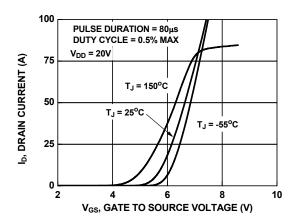


Figure 6. Transfer Characteristics

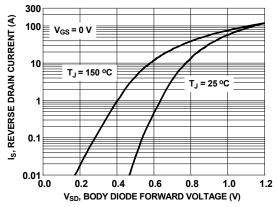


Figure 7. Forward Diode Characteristics

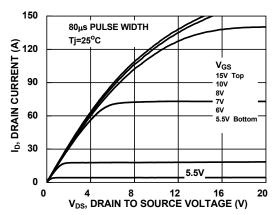


Figure 8. Saturation Characteristics

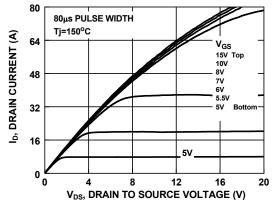


Figure 9. Saturation Characteristics

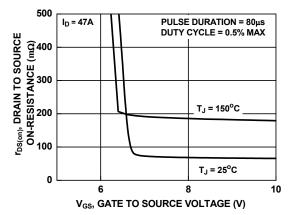


Figure 10. Rdson vs Gate Voltage

# **Typical Characteristics**

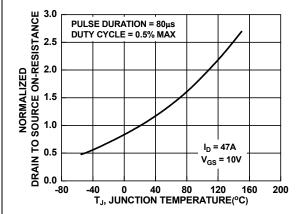


Figure 11. Normalized Rdson vs Junction **Temperature** 

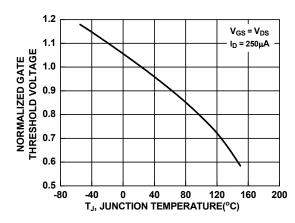


Figure 12. Normalized Gate Threshold Voltage vs **Temperature** 

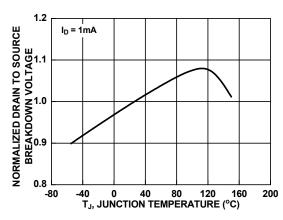


Figure 13. Normalized Drain to Source **Breakdown Voltage vs Junction Temperature** 

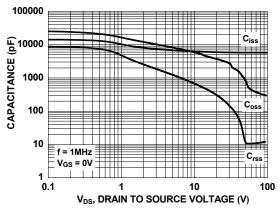


Figure 14. Capacitance vs Drain to Source Voltage Figure 16.

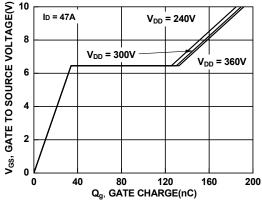


Figure 15. Gate Charge vs Gate to Source Voltage





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