





#### 20V P-CHANNEL ENHANCEMENT MODE MOSFET

## **Product Summary**

V <sub>(BR)DSS</sub>	R <sub>DS(on) max</sub>	I <sub>D</sub> T <sub>A</sub> = +25°C		
-20V	$95mΩ @ V_{GS} = -4.5V$	3.0A		
-20V	130mΩ @ V <sub>GS</sub> = -2.5V	2.5A		

#### **Description**

This new generation MOSFET has been designed to minimize the on-state resistance ( $R_{DS(ON)}$ ) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

### **Applications**

- DC-DC Converters
- Power Management Functions
- Analog Switch

### **Features and Benefits**

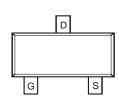
- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 standards for High Reliability

#### **Mechanical Data**

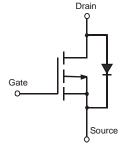
- Case: SOT23
- Case Material: Molded Plastic, "Green" Molding Compound.
  UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish Matte Tin annealed over Copper leadframe.
  Solderable per MIL-STD-202, Method 208 (3)
- Weight: 0.0072 grams (approximate)







Pin Configuration



Internal Schematic

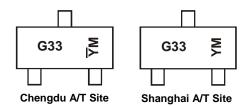
#### **Ordering Information** (Note 4)

<u> </u>		
Part Number	Case	Packaging
DMG3413L-7	SOT23	3,000/Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- 2. See http://www.diodes.com/quality/lead\_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

## **Marking Information**



G33 = Marking Code

YM = Date Code Marking for SAT (Shanghai Assembly/ Test site)  $\overline{Y}M$  = Date Code Marking for CAT (Chengdu Assembly/ Test site) Y or  $\overline{Y}$  = Year (ex: A = 2013) M = Month (ex: 9 = September)

Date Code Kev

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Year	2010	20	11	2012	2013	20	14	2015	2016	20	17	2018
Code	Χ	,	<b>′</b>	Z	Α		В	С	D	I	E	F
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	0	N	D



## **Maximum Ratings** (@ $T_A = +25$ °C, unless otherwise specified.)

Characteristic		Symbol	Value	Units	
Total Power Dissipation (Note 5)		$P_{D}$	0.7	W	
The small Beginter as Austine to Austine (Nets 5)		D	184	°C/W	
Thermal Resistance, Junction to Ambient (Note 5)	t<10s	R <sub>θJA</sub>	115	C/VV	
Total Power Dissipation (Note 6)		$P_{D}$	1.3	W	
Thermal Desistance Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	94	°C/W	
Thermal Resistance, Junction to Ambient (Note 6)	t<10s		61		
Thermal Resistance, Junction to Case		$R_{ heta JC}$	25		
Operating and Storage Temperature Range		$T_{J_i} T_{STG}$	-55 to +150	°C	

## Thermal Characteristics (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Units	
Drain-Source Voltage		$V_{DSS}$	-20	V	
Gate-Source Voltage			V <sub>GSS</sub>	±8	V
		$T_A = +25$ °C $T_A = +70$ °C	I <sub>D</sub>	3.0 2.4	А
Continuous Drain Current (Note 6) V <sub>GS</sub> = -4.5V	t<10s	$T_A = +25$ °C $T_A = +70$ °C	I <sub>D</sub>	3.7 2.9	А
Continuous Drain Current (Note 6) // 25/	Steady State	$T_A = +25$ °C $T_A = +70$ °C	I <sub>D</sub>	2.5 2.0	А
Continuous Drain Current (Note 6) V <sub>GS</sub> = -2.5V	t<10s	$T_A = +25$ °C $T_A = +70$ °C	I <sub>D</sub>	3.2 2.5	А
Maximum Continuous Body Diode Forward Current	(Note 6)	I <sub>S</sub>	1.9	Α	
Pulsed Drain Current (10µs pulse, duty cycle = 1%)	)	I <sub>DM</sub>	20	Α	

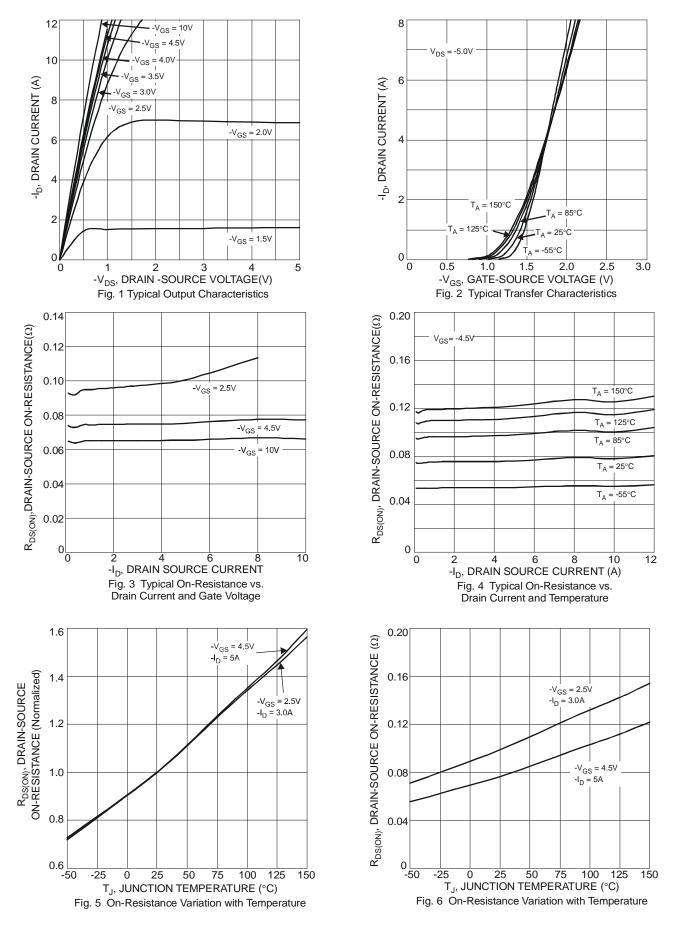
## **Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 7)							
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-20		_	V	$V_{GS} = 0V, I_D = -250\mu A$	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	_	_	-1.0	μA	$V_{DS} = -16V, V_{GS} = 0V$	
Gate-Source Leakage	I <sub>GSS</sub>	_	_	±100	nA	$V_{GS} = \pm 8V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 7)							
Gate Threshold Voltage	V <sub>GS(th)</sub>	-0.6	-0.55	-1.3	V	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	
			73	95		$V_{GS} = -4.5V$ , $I_D = -3.0A$	
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	_	95	130	mΩ	$V_{GS} = -2.5V$ , $I_D = -2.6A$	
			146	190		$V_{GS} = -1.8V, I_D = -1A$	
Forward Transfer Admittance	Y <sub>fs</sub>	_	8	-	S	$V_{DS} = -5V, I_{D} = -3A$	
Diode Forward Voltage	V <sub>SD</sub>	_	-0.8	-1.25	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = -1A	
DYNAMIC CHARACTERISTICS (Note 8)							
Input Capacitance	C <sub>iss</sub>	_	857	_	pF	101/11/	
Output Capacitance	Coss	_	54	_	pF	$V_{DS} = -10V, V_{GS} = 0V$ - f = 1.0MHz	
Reverse Transfer Capacitance	C <sub>rss</sub>	_	49		pF	T = 1.0WHZ	
Gate Resistnace	Rg	_	12.3	_	Ω	$V_{DS} = 0V$ , $V_{GS} = 0V$ , $f = 1.0MHz$	
Total Gate Charge	Qg	_	9.0	_	nC		
Gate-Source Charge	Qgs	_	1.6	_	nC	$V_{GS} = -4.5V$ , $V_{DS} = -15V$ , $I_{D} = -4A$	
Gate-Drain Charge	Q <sub>gd</sub>	_	1.1	_	nC		
Turn-On Delay Time	t <sub>D(on)</sub>	_	9.7	_	ns		
Turn-On Rise Time	tr	_	17.7	_	ns	$V_{DS} = -15V, V_{GS} = -10V,$	
Turn-Off Delay Time	Off Delay Time t <sub>D(off)</sub> -		268.8	_	ns	$R_L = 15\Omega$ , $R_G = 6.0\Omega$ , $I_D = -1A$	
Turn-Off Fall Time	tf	_	64.2	_	ns	7	

Notes:

- Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
  Device mounted on FR-4 substrate PC board, 2oz copper, with thermal vias to bottom layer 1inch square copper plate
  Short duration pulse test used to minimize self-heating effect.
  Guaranteed by design. Not subject to production testing.







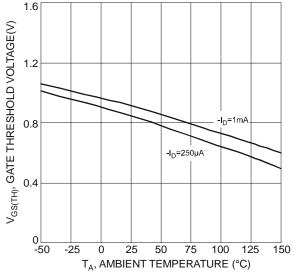
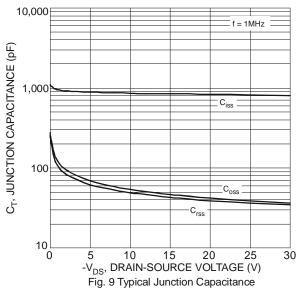


Fig. 7 Gate Threshold Variation vs. Ambient Temperature



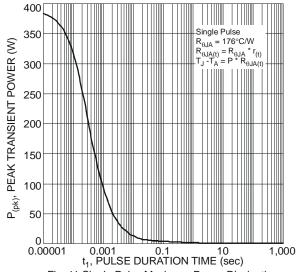
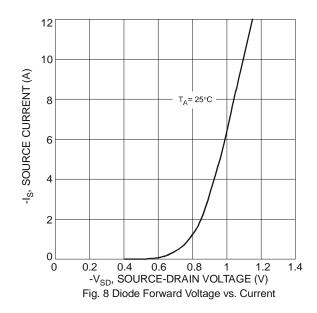
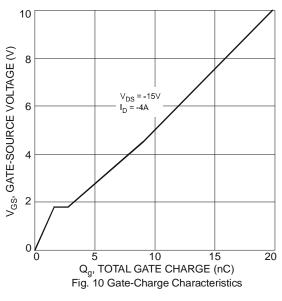
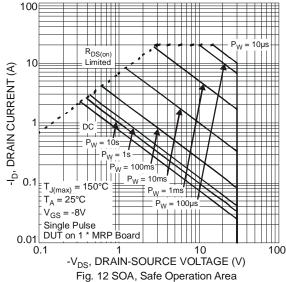


Fig. 11 Single Pulse Maximum Power Dissipation









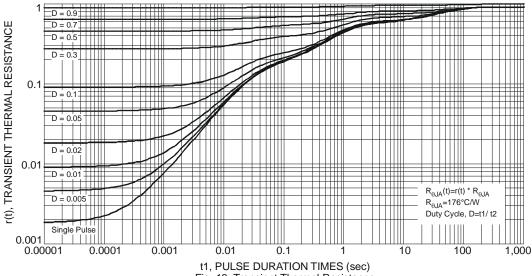
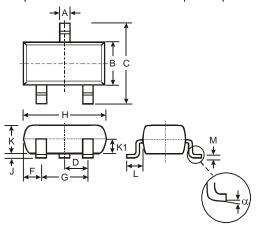


Fig. 13 Transient Thermal Resistance

## **Package Outline Dimensions**

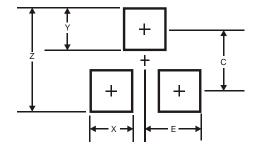
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.



SOT23							
Dim	Min	Max	Тур				
Α	0.37	0.51	0.40				
В	1.20	1.40	1.30				
C	2.30	2.50	2.40				
D	0.89	1.03	0.915				
F	0.45	0.60	0.535				
G	1.78	2.05	1.83				
H	2.80	3.00	2.90				
7	0.013	0.10	0.05				
K	0.903	1.10	1.00				
K1	-	-	0.400				
L	0.45	0.61	0.55				
М	0.085	0.18	0.11				
α	0°	8°	-				
All Dimensions in mm							

## **Suggested Pad Layout**

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.



Dimensions	Value (in mm)
Z	2.9
Х	0.8
Y	0.9
С	2.0
E	1.35



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