EQCO62R20.3 6.25 Gbps Asymmetric Coax Equalizer
EQCO31R20.3 3.125 Gbps Asymmetric Coax Equalizer

1.1 Introduction

The EQCO62X20[1] chipset is a driver/equalizer chipset that forms a bidirectional full duplex communication link over a single coax cable.

The EQCO62X20 chipset is designed to transport up to 6.25 Gbps over the downlink channel and to transport 21 Mbps over the uplink channel. The EQCO62T20 is designed to transmit the downlink signal up to 6.25 Gbps and receive the uplink signal. The EQCO62R20 is designed to receive the downlink signal up to 6.25 Gbps and to transmit the uplink signal. Power can be transferred over the same cable via external inductors.

The chipset is designed to work with several types of 75 Ω coaxial cables including legacy cables as well as thin flexible lightweight cables.

1.2 Applications

This solution is useful and economical for many markets and applications, including the following:

- High definition Camera links
- Machine Vision, Military, Aerospace, Medical, Broadcast & Surveillance cameras
  - Single coax cable carries power, video data and camera control stream

1.3 Features

- Complies with CoaXPress v1.1 camera standard [1]
- Supports up to 68 meters of cable at 6.25 Gbps using high quality coax
- Supports up to 212 meters of cable at 1.25 Gbps using high quality coax
- Single chip solutions for both the camera side and the frame grabber side, making a bidirectional connection over a single 75 Ω coax cable
- Full duplex bidirectional data channel
  - Downlink speeds from 1.25 Gbps up to 6.25 Gbps; differential interfacing straightforward with internal termination resistors
  - Flexible, protocol agnostic uplink supporting up to 21 Mbps, allowing nanoseconds precise triggering events driven by the frame grabber
- Supports Power distribution over the coax up to 900 mA, on top of the data signals allowing to power the camera through the same coax
- Low power consumption (<70 mW, 1.2 V supply)
- 16-pin, 0.65 mm pin pitch, 4 mm QFN package
- Small PCB footprint for EQCO62R20 and off-chip components, with guaranteed RF-performance
- -40 - +85 ˚C industrial temperature range
- Pb-free and RoHS compliant

[1] The EQCO31T20 and EQCO31R20 are lower speed versions of the EQCO62T20 and EQCO62R20, with a maximum bit rate of 3.125 Gbps for the high speed downlink and the same uplink speed.

1.4 Typical Link Performance

Table 1 gives an overview of typical link performance at room temperature for the link containing the EQCO62T20 coax driver in conjunction with the EQCO62R20 receiver, using the downlink channel, uplink channel and power transmission simultaneously.
Performance for EQCO62X20 and EQCO31X20 is equal for bit rates up to 3.125 Gbps.

BELDEN

Name		Belden 7731A	Belden 1694A	Belden 1505A	Belden 1505F	Belden 1855A
	Type	Long Distance	Industry Standard	Compromis Coax	*Flexible*	Thinnest cable
Diameter	(mm)	10.3	6.99	5.94	6.15	4.03
1.25 Gbps	(m)	194	130	107	80	55
2.5 Gbps	(m)	162	110	94	66	55
3.125 Gbps	(m)	147	100	86	60	55
5.0 Gbps	(m)	87	60	52	35	38
6.25 Gbps	(m)	58	40	35	23	25

GEPCO

Name		Gepco VHD1100	Gepco VSD2001	Gepco VPM2000	Gepco VHD2000M	Gepco VDM230
	Type	Long Distance	Industry Standard	Compromis Coax	*Flexible*	Thinnest cable
Diameter	(mm)	10.3	6.91	6.15	6.15	4.16
1.25 Gbps	(m)	212	140	109	81	66
2.5 Gbps	(m)	185	120	94	67	66
3.125 Gbps	(m)	169	110	86	61	62
5.0 Gbps	(m)	102	66	53	36	38
6.25 Gbps	(m)	68	44	35	24	25

CANARE*

Name		Canare L-7CFB	Canare L-5CFB	Canare L-4CFB	Canare L-3CFB	Canare L-2.5CFB
	Type	Long Distance	Industry Standard	Compromis Coax	Thin Cable	Thinnest Cable
Diameter	(mm)	10.2	7.7	6.1	5.5	4
1.25 Gbps	(m)	165	118	94	72	43
2.5 Gbps	(m)	135	98	79	66	43
3.125 Gbps	(m)	122	88	71	60	43
5.0 Gbps	(m)	71	52	42	36	30
6.25 Gbps	(m)	46	34	28	24	20

* specs from Canare only up to 2GHz, 5 Gbps and 6.25 Gbps performance are by extrapolation!

Table 1: Typical link performance

2 Functional Description

2.1 Overview

The EQCO62X20 single coax chipset is designed to simultaneously transmit and receive signals on a single 75 Ω coax cable. In one direction a downlink signal is transmitted. In the opposite direction a lower speed uplink is provided. The EQCO62X20 chipset consists of 2 chips. The EQCO62T20 is a high speed line driver with integrated low speed receiver. The EQCO62R20 is a high speed receiver with integrated low speed transmitter. Figure 1 illustrates a typical EQCO62X20 link set-up.

The downlink signal is transmitted with 600 mV transmit amplitude at the EQCO62T20 side. This signal is attenuated in the coax and recovered by an equalizer [2] integrated in the EQCO62R20. The low speed uplink is transmitted with a lower amplitude of 130 mV to limit the crosstalk with the downlink channel.

The downlink channel is intended for 8B/10B NRZ coded data with bitrates from 1.25 Gbps up to 6.25 Gbps. The low speed uplink [3] has a maximum bit rate of 21 Mbps and has a single ended LVTLL input and output. The uplink can operate with DC balanced, DC unbalanced or even burst mode data.

On top of the downlink channel and the low speed uplink the system allows power transmission over the coax by using ferrite beads and external inductors [4]. These external inductors give the communication channel a high pass characteristic. The uplink receiver inside the EQCO62T20 chip recovers the signal lost by this high pass filter. Appropriate inductors need to be selected for correct operation of the link. Correct operation is only guaranteed with the inductor combination used in our evaluation board, even though other components might be suited.

The EQCO62X20 chipset is compatible with the CoaXPress v1.0 camera standard.

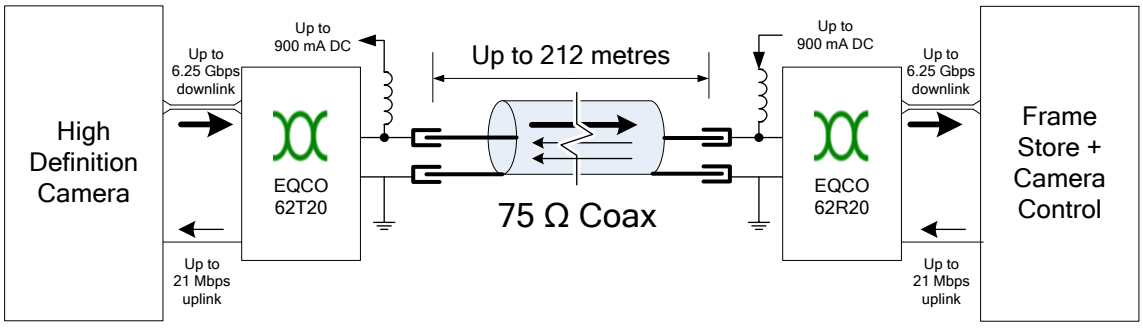

Figure 1: Typical EQCO62X20 link set-up

2.2 Package and Pinout

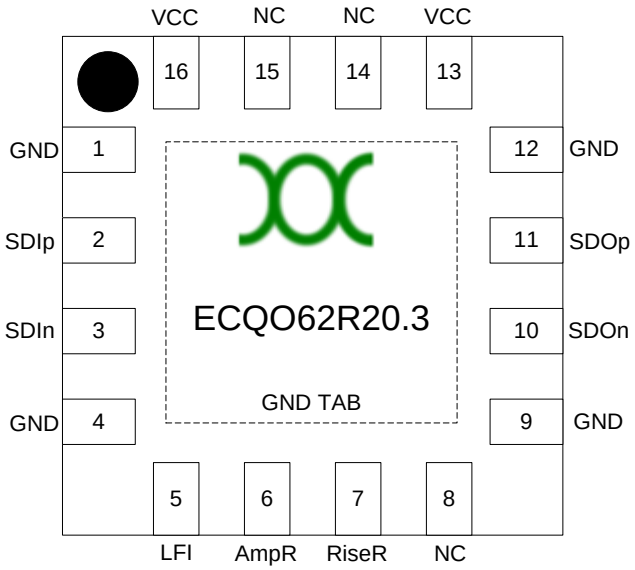

Figure 2: EQCO62R20.3 Pin Layout (viewed from top)

2.3 Pin Descriptions

Pin Number	Pin Name	Signal Type	Description
(TAB)	GND	Power	Use as single point Ground
13,16	VCC	Power	+1.2 V of power supply
1,4,9,12	GND	Power	connect to ground of power supply
2,3	SDIp,SDIn	CML Input	Serial Input Positive/Negative Differential serial input, connect SDIn to shield of cable via termination network. External 15 Ω resistors required.
11, 10	SDOp/ SDOn	CML Output	Serial Output Positive/Negative -Differential serial output. Output has a swing of 2x600 mV and has 2x50 Ω on chip termination resistors.
5	LFI	input	Uplink input signal. LVTTL signal with 1.2 V input swing. External series resistor is required for 2.5 V (3.9 kΩ) or 3.3 V (6.2 kΩ) input swing.
6	AmpR	input	Connected to VCC by a resistor that selects output swing of the uplink signal. Typical value is R_{amp} = 1.2 kΩ for 130 mV output swing
7	RiseR	input	Connected to VCC by a resistor to VCC that selects rise time of the uplink signal. Typical value is R_{rise} = 10 kΩ for rise/fall times of 11ns.
8,14,15	NC		DO NOT CONNECT, leave these pins floating. Used for internal testing.

Table 2: EQCO62R20.3 Device Pin List

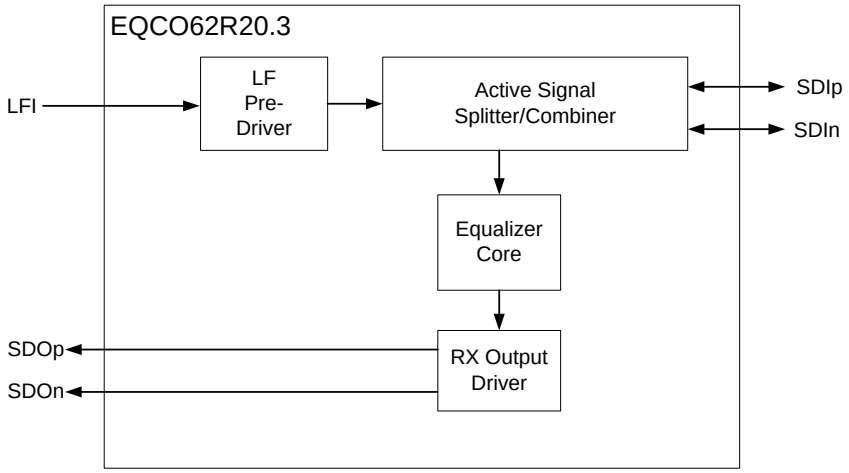

Figure 3: EQCO62R20.3 block diagram showing electrical connections

2.3.1 SDIp/SDIn

SDIp/SDIn together form a differential input pair. It is the differential voltage between these pins that the EQCO62R20 analyses and adaptively equalizes for signal level and frequency response. The equalizer automatically detects and adapts to signals with different edge rates, different attenuation levels and different cable characteristics. Both SDIp and SDIn inputs are terminated by 60 Ω to VCC on chip. For each input an external 15 Ω resistor is required in series.

2.3.2 SDOp/SDOn

SDOp/SDOn together form a differential pair outputting the reconstructed far end transmit signal. SDOp/SDOn are terminated on chip with 2x50 Ω resistors.

2.3.3 LFI

The uplink input signal that will be transmitted on the SDIp/SDIn pair. LFI must be a 1.2 V LVTTL signal. For 2.5 V and 3.3 V input swing an external resistor is needed in series at the input of the chip.

2.3.4 AmpR

Resistor to VCC that sets the transmit amplitude of the uplink output driver. Typical value for CoaXPress is R_{amp} = 1.2 kΩ for 130 mV transmit amplitude.

2.3.5 RiseR

Resistor to VCC that selects the rise/fall time of the uplink output driver. Typical value for CoaXPress is R_{rise} = 10 kΩ for rise/fall time of 11 ns.

If no R_{amp} and R_{rise} are placed the LF driver is disabled.

2.1 Circuit Operation

2.1.1 LF pre-driver

The uplink pre-driver converts the incoming LVTTL signal at the LFI pin to a signal with well controlled amplitude and rise/fall times, that will be transmitted onto the cable by the active splitter/combiner.

2.1.2 Active signal splitter/combiner

The active splitter/combiner transmits the outgoing coax signal via an internal 60 Ω output termination resistor. The total (60 Ω + 15 Ω) output resistor when balanced with the coax characteristic impedance also forms part of a hybrid splitter circuit which subtracts the TX output from the signal on the SDIO output to give yield the far end TX signal.

2.1.3 Equalizer Core

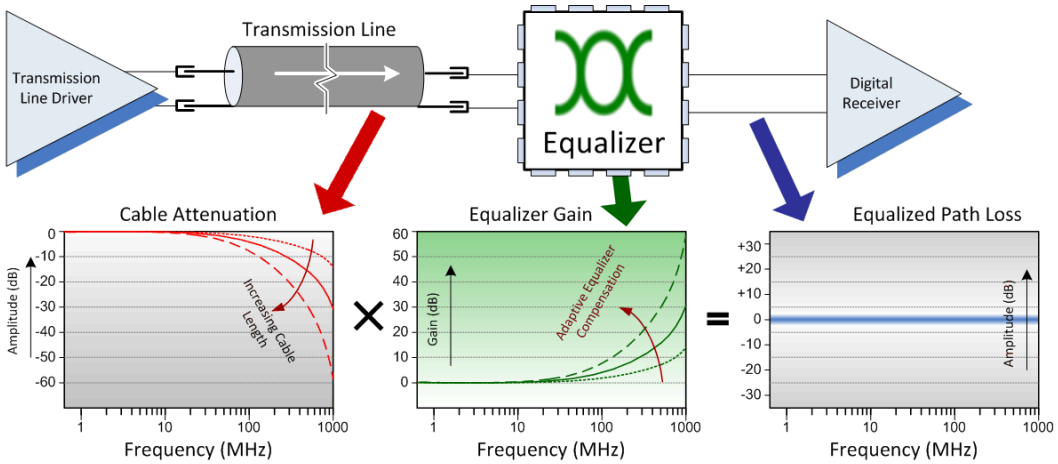

Figure 4: Principal of Equalizer Operation

The EQCO62R20 has an embedded equalizer in the receive path with following characteristics:

- Auto-adaptive

  The equalizer controls a multiple pole analog filter which compensates for attenuation of the cable, as illustrated in 4. The filter frequency response needed to restore the signal is automatically determined by the device using a time-continuous feedback loop that measures the frequency components in the signal. Upon the detection of a valid signal, the control loop converges within a few microseconds.

- Variable gain

  The EQCO62R20 equalizer has variable gain to compensate for low frequent attenuation through the coax and variations in transmit amplitude.

- Multi-speed

  The EQCO62R20 works at data-rates from 1.25 Gbps to 6.25 Gbps with 8B/10B coding.

Example equalizer performance measurements can be found in Appendix 1.

2.1.4 Rx output driver

The output driver converts the output of the equalizer core to a LVDS like signal and sends it onto a 100 Ω differential transmission line.

3 Electrical Specifications

3.1 Absolute Maximum Ratings

Stresses beyond those listed under this section may cause permanent damage to the device. These are stress ratings only and are not tested. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Conditions	Min	Typ	Max	Units
Storage Temperature		-65		+150	°C
Ambient Temperature	Power Applied	-55		+125	°C
Operating Temperature	Normal Operation (VCC=1.2V±5%)	-40		+85	°C
Supply Voltage to Ground		-0.5		+1.4	V
DC Input Voltage		-0.5		+1.6	V
DC Voltage to Outputs		-0.5		+1.6	V
Current into Outputs	Outputs Low			90	mA
Electro Static Discharge (ESD) HBM	JEDEC EIA/JESD-A114A	>2.2			kV
Electro Static Discharge (ESD) contact	IEC 61000-4-2	>8			kV
Latch-Up Current		>100			mA(DC)

Table 3: Absolute Maximum Ratings

3.2 Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit
Power supply					
VCC	Supply Voltage	1.15	1.2	1.25	V
I_s	Supply Current, both transmitting and receiving		60		mA
I_{sr}	Supply Current when only receiving		50		mA
LFI Input (LVTTL like)					
V_{ih}	Input HIGH Voltage		1.2	1.6	V
V_{il}	Input LOW Voltage	-0.5	GND		V
R_{input}	Resistance to GND		3.6		kΩ
SDIp connection to Coax					
Z_{coax}	Coax Cable Characteristic Impedance		75		Ω
R_{SDIp}	Input impedance between SDIp/SDIn and VCC		60		Ω
V_{LF}	Uplink transmit amplitude for R_{amp} = 1.2 kΩ, measured inside cable after external 15 Ω resistor	110	130	160	mV
t_{rise_lf}	Rise /fall time 20% to 80% of LF output on V_{SDIp} with R_{rise} = 10 kΩ and R_{amp} = 1.2 kΩ	7	11	15	ns
RL_{loss}	Coax Return-loss as seen on SDIp pin Frequency range = 5 MHz - 1 GHz			-15	dB

Parameter	Description	Min	Typ	Max	Unit
RL_{loss}	Coax Return-loss as seen on SDIp pin Frequency range = 1 GHz - 1.5 GHz			-10	dB
RL_{loss}	Coax Return-loss as seen on SDIp pin Frequency range = 1.5 GHz - 3.2 GHz			-7	dB
ΔV_{TX}	Transmit Amplitude for downlink signal	500	600	700	mV
SDOp/SDOn Outputs					
ΔV_o	Output amplitude $V_{SDOp,n}$ (into 2x50 Ω)		2x600		mV
R_{output}	Termination between SDOp/SDOn and GND/VCC		2x50		Ω
t_{rise_o}	Rise /fall time 20% to 80% of $V_{SDOp,n}$		40		ps

Table 4: Electrical Characteristics (Over the Operating VCC and -40 to 85 ^{o}C Range)

3.3 Jitter Numbers

Parameter	Conditions	Min	Typ	Max	Units
Additive jitter on LF output	8B/10B coded signal at 21 Mbps over full VCC and temperature range.			1	ns
DCD in LF output	8B/10B coded signal at 21 Mbps over full VCC and temperature range.			3	ns
Jitter in equalizer output	8B/10B coded signal over full transmit amplitude, VCC and temperature range. Including uplink and power supply transmission. At 1.25 Gbps from 0 to 135 m Belden 1694A = -22dB attenuation at 0.625 GHz			0.3	UI
"	At 2.5 Gbps from 0 to 115 m Belden 1694A = -27.2 dB attenuation at 1.25 GHz			0.3	UI
"	At 3.125 Gbps from 0 to 105 m Belden 1694A = -28.1 dB attenuation at 1.5625 GHz			0.3	UI
"	At 5 Gbps form 0 to 65 m Belden 1694A = -22.6 dB attenuation at 2.5 GHz (For EQCO62R20 only)			0.3	UI
"	At 6.25 Gbps from 0 to 45 m Belden 1694A = -17.8dB attenuation at 3.125 GHz (For EQCO62R20 only)			0.35	UI

Table 5: Jitter numbers

4 Package Drawing

A 16 pin Micro Lead frame Package (MLP) also known as Quad Flat No Lead (QFN) package is used. The package outline conforms to JEDEC MO-220.

Dimensions in 5 are in millimeters.

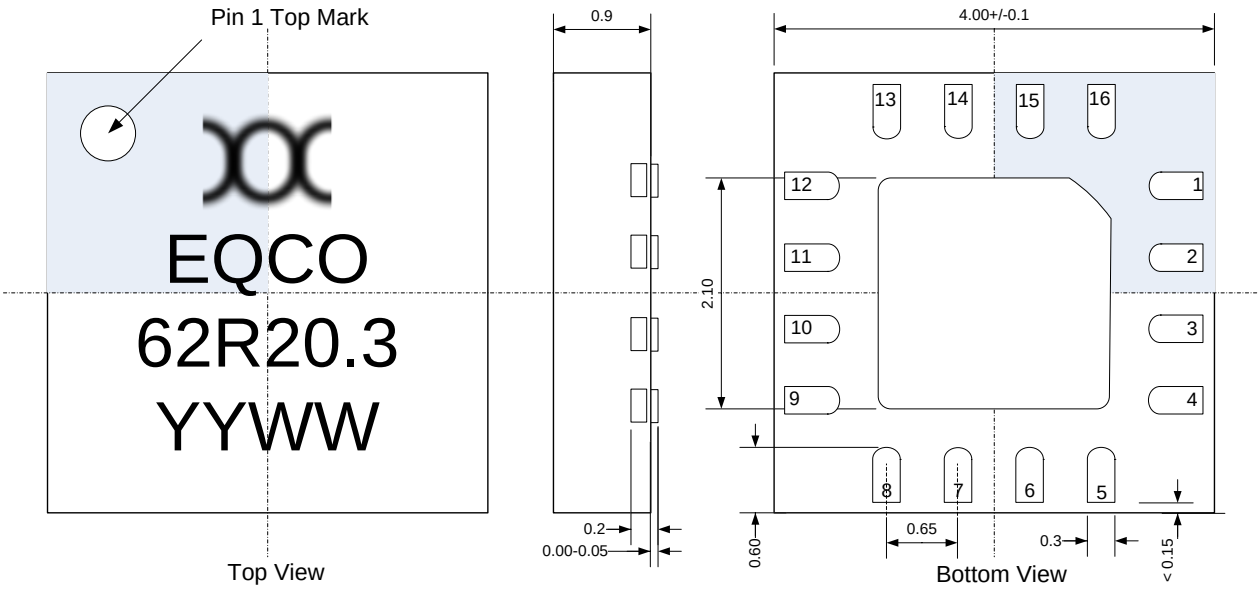

Figure 5: Package Drawing

5 Application Information

5.1 Typical Application Circuit

Figure 6 illustrates a typical schematic implementation:

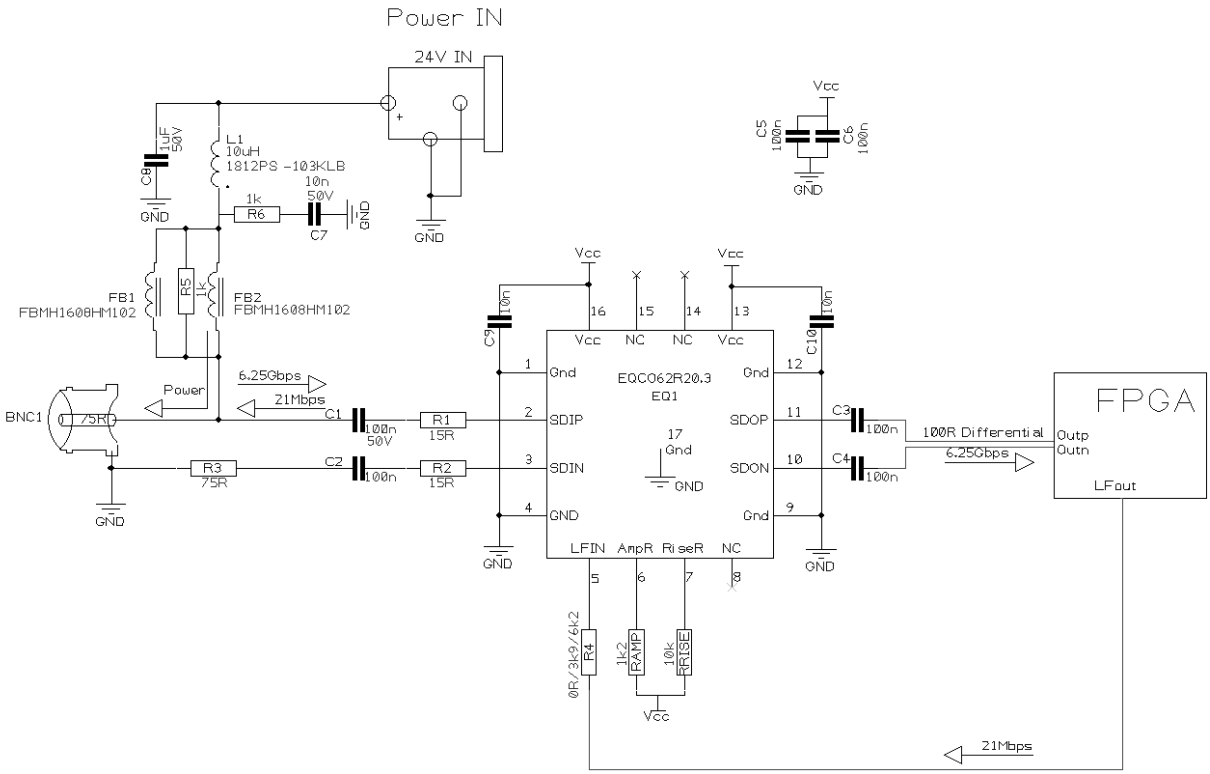

Figure 6: EQCO62R20.3 typical application circuit

5.2 Component recommendation

Element	Value	Size	Recommended component
Fb1, Fb2	1 kΩ @ 100 MHz ferrite bead	0603	FBMH1608HM102 from Taiyo Yuden (CRITICAL)
L1	10 µH	1812	1812PS_103 or JA4644-AL from Coilcraft (CRITICAL)
R1, R2	15 Ω ±1 %	0402	
R3	75 Ω ±1 %	0402	
R4	0 Ω (1.2 V input swing) 3.9 kΩ (2.5 V input swing)		

Element	Value	Size	Recommended component
	6.2 kΩ (3.3 V input swing)		
Ramp	1.2 kΩ ±1 %		
Rrise	10 kΩ ±1 %		
R5	1 kΩ	0402	
C1	100 nF, 50V, X7R	0603	
C2, C3, C4, C5, C6	100 nF, X7R	0402	
C7	10 nF, 50V, X7R	0402	
C8	1 µF, 50 V, X7R	0805	
BNC1	75 Ω right angle BNC connector		BNC-RA C-SX-090 from Cambridge Connectors

Table 5: Component recommendation for the EQCO62R20.3 board layout

Ferrite Beads Fb1, Fb2 = FBMH1608HM102 from Taiyo Yuden and inductor L1 = 1812PS_103 from Coilcraft (10 µH) are recommended for CoaXPress. For other applications the inductor value can be larger leading to a physical larger inductor.

Connector BNC1 = 75 Ω right angle BNC C-SX-090 from Cambridge "0310Precision75ohmcoaxialconnectorscatalogue" page8, recommended for CoaXPress.

Other inductor/ferrite bead/BNC connector can possibly be used, however, they must be selected carefully for their RF-performance since performance can decrease significantly!

5.3 Guidelines for PCB layout

Important Guidance Note: Using the EQCO62X20 chipset at its full purpose, i.e. including low speed uplink and power-supply transmission it is important not to disturb the RF-performance of the high speed downlink channel. Implementing the circuit of Figure 6 with a different PCB layout will in first instance not deliver full data-sheet performance. The simplest way of meeting optimal performance (including jitter and return-loss requirements) is to precisely follow the component and layout recommendations. Note that at multi-Gigabit speeds, using "equivalent" components or small PCB layout changes (even moving a via) can have significant detrimental effects.

For CoaXPress: The easiest way for achieving the requirements of the CoaXPress 1.0 specification is to merely use the recommended circuits, components and layout of the PCB.

5.3.1 Rightangle BNC

The figure below shows the 4 layers of the recommended footprint for the EQCO62R20.3 chip and the off-chip components that are critical for the RF-performance of the system.

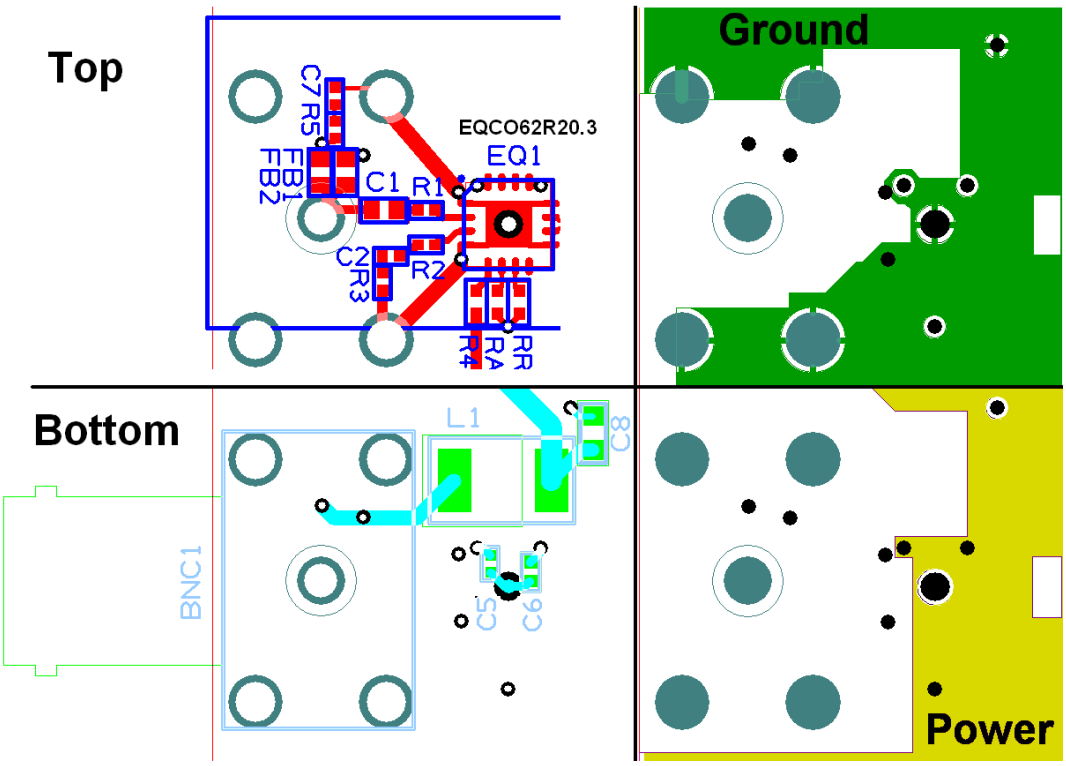

Figure 7: Recommended PCB layout for EQCO62R20.3

In this layout the size of the PCB area needed for the chip is minimized. Approximately the double of the BNC footprint area is required for the full bidirectional system including the necessary elements for the power transport.

The differential output of the chip must be a 100 Ω differential transmission line. To minimize the parasitic capacitance of the input pins a cut-out of the ground and power plane underneath the input pins is recommended. For best performance no via's should be used in this high speed signal path.

A large cut-out underneath the right angle BNC connector, the AC coupling capacitors, ferrite beads and inductor is needed for minimal parasitic.

This proposed layout is designed to be largely independent of the used PCB-layer stack. This will work as well for 4, 6 or even higher numbers of layers. Possible extra layers should have cut-outs as large as the full proposed footprint.

For easy implementation EqcoLogic will provide the Gerber file, please ask for it by email[2]. Changes to the proposed PCB layout can be reviewed by EqcoLogic on request.

[2] Email address: coaxpress@eqcologic.com

5.3.2 Multilane CoaXPress 4+1 layout with DIN1.0/2.3 Connectors

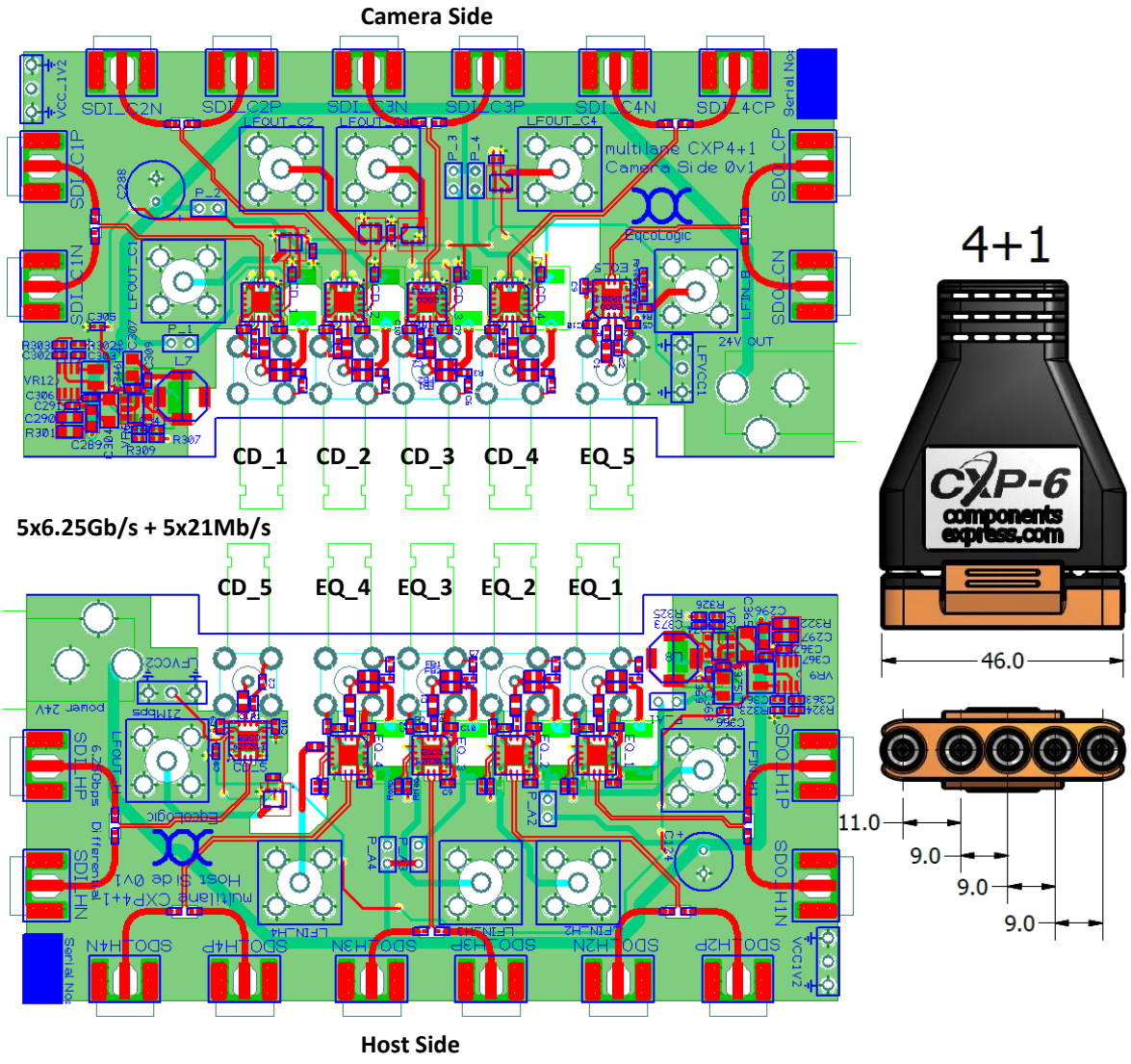

Figure 8: PCB layout of Multilane CoaXPress 0v1 demo board pair

Figure 8

shows an example of a Multilane CoaXPress 4+1setup. The recommended Din1.0/2.3 connector is the NPF 4076 from Cambridge Connectors. The cable example shows the pitches in mm. Figure 9 shows the 4 layers of the recommended footprints and off-chip components that are critical for RF-performance of the cable drivers CD_1 to CD_4 at the camera side, which have Power over CoaXPress (PoCXP). Figure 10 shows the variant without PoCXP used for CD_5 at the host side. The exact dimensions in mm are given in appendix4. It is recommended to copy these dimensions, especially the connection between the DIN1.0/2.3 connector and the chip, as this is a complex entity with coupled currents and compensated parasitic capacitances.

Despite the critical layout, this proposed layout is designed to be largely independent of the used PCB-layer stack, as the critical parts are mainly the top-layer only. This will work as well for 4, 6 or even higher numbers of layers. Possible extra layers should have cut-outs as large as the full proposed footprint.

In these layouts the size of the PCB area needed for the chip is minimized. This allows multiple lanes close together.

Only 2 of 4 connecter GND pins are connected to the GND plane to reduce the capacitance.

The differential CD inputs must be a 100 Ω differential transmission line. A cut-out of the ground and power plane underneath the input pins is recommended to minimize the parasitic capacitance. For best performance no via's should be used in this high speed signal path.

The Components Express 4+1 connector of Figure 8 is only shown as example. Other connector configurations are available with DIN1.0/2.3 connector such as 6+1, 2+1, 1+1, dual or single lane configurations.

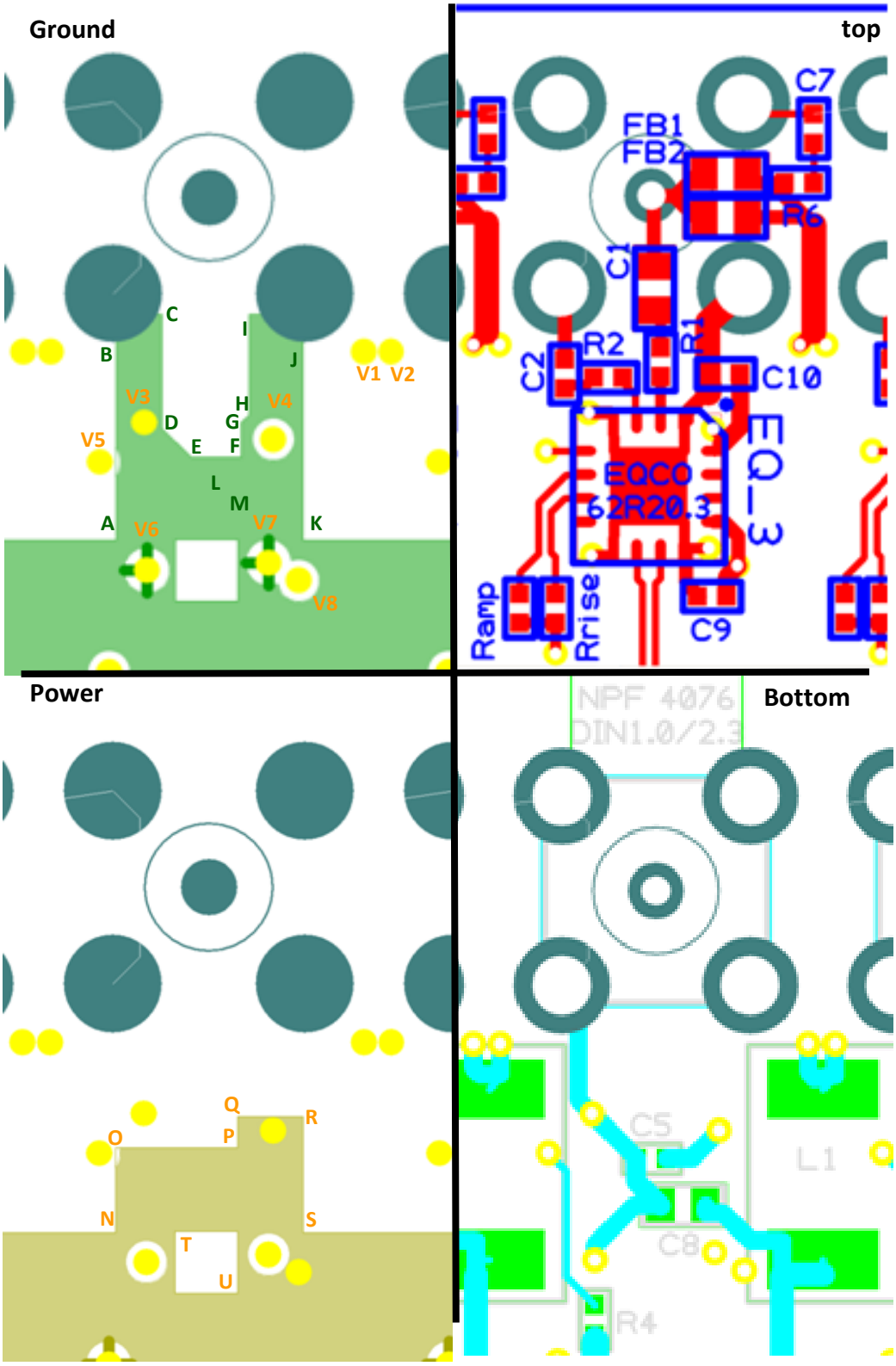

Figure 9: Recommended PCB layout for EQCO62R20.3 with DIN1.0/2.3 connector *with PoCXP*

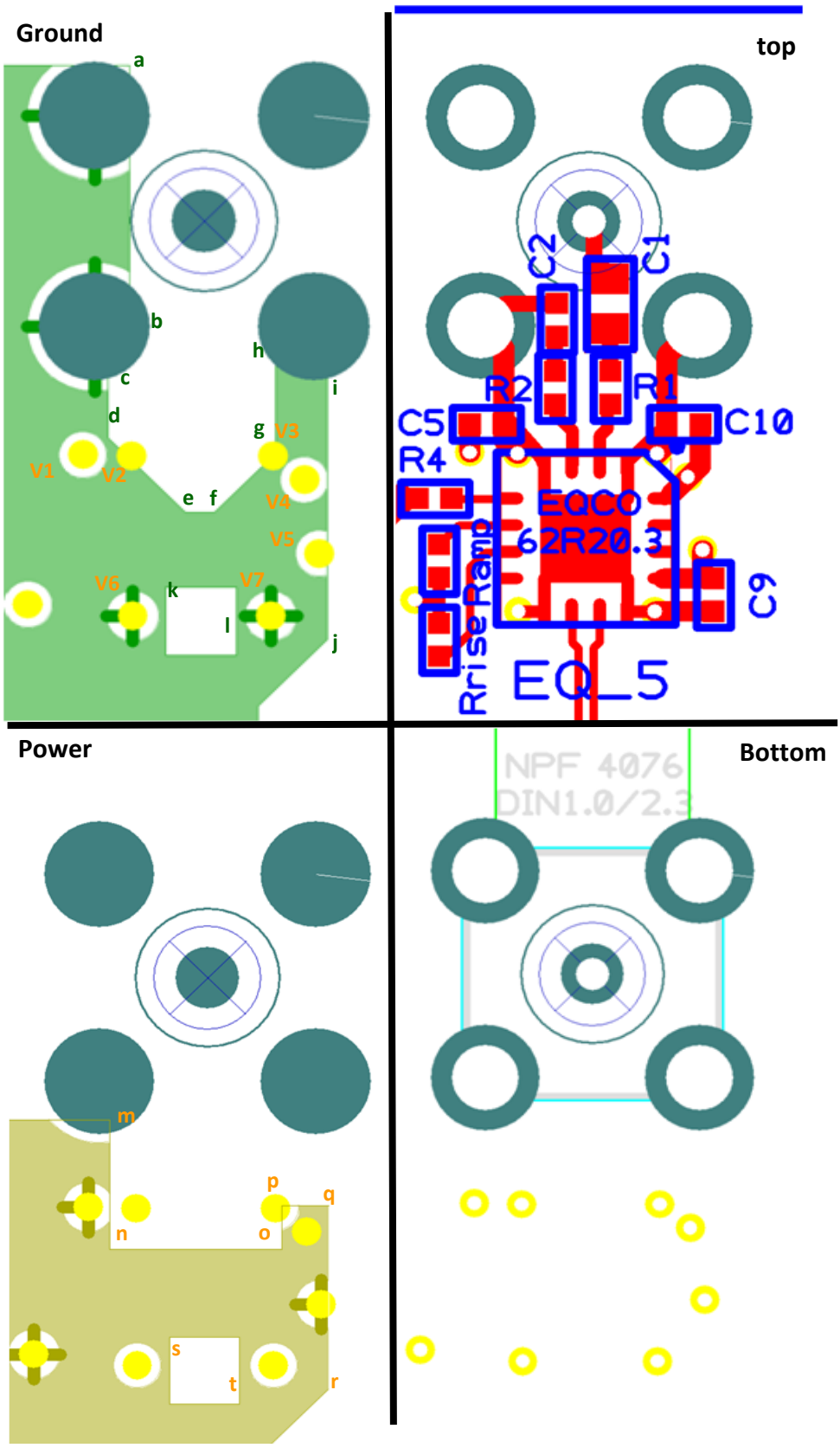

Figure 10: Recommended PCB layout for EQCO62R20.3 with DIN1.0/2.3 connector *without PoCXP*

5.4 Guidelines for Power Transmit Unit

At the Power-IN connection, a voltage supply is expected for powering a device (e.g. a camera) at the other end of the cable.

This voltage supply should have low ripple. High frequency ripple will be rejected by C8/L1/FB1/FB2 filtering in the reference circuit. However, mid frequency ripple is to be avoided by the power supply itself.

In a typical application one could want to step-up from a 12 V supply (e.g. in a PC) to a 24 V power supply for CoaXPress. It is in this case preferred to use a DC-to-DC converter that has a high switching frequency (e.g. 2 MHz) above one that has lower switching frequency (200 kHz). The latter typically induces larger voltage spikes at the Power-IN connection. These will only be partially filtered out by said filter, the remainder being cross-talk for the uplink channel.

When too much cross-talk remains on the uplink channel, additional power-supply filtering is required. This may be achieved by placing an extra filter network (not shown) in series with the Power-IN node.

5.5 Power over CoaXPress

The EQCO62R20.3 is compatible with the power over CoaXPress system (PoCXP) using the circuit from Fig. 7. Hence power can be switched ON and OFF by the host (e.g. frame grabber) through the 10-μH inductor specified by the CXP standard. This switching is supported through a relay and through an electronic switch.

Powering through a wide-band bias-T is also supported.

The EQCO62R20.3 is also protected against following events:

- Hot plugging by frame grabber: in case the frame grabber has already applied its 24V on the coax when connecting the cable, no damage will occur to the EQCO62R20.3 when connecting the powered coax cable.
- Fast turn-on and turn-off of power supply by frame grabber

6 Document Control

6.1 Version History

Version	Date	Author	Comments
1v2	27 Jan 2014	M. Kuijk	Added references
1v1	10 April 2012	X.Maillard	Added Multilane CoaXPress 4+1 layout with DIN1.0/2.3 connectors
1v0	9 February 2012	B.Devuyst	New document, taken from EQCO62R20.2 Most important changes with respect to EQCO62R20.2 Parasitic input capacitance has been reduced

6.2 References

[1] CoaXPress V1.1 standard. Free download from the JIIA website: http://jiia.org/en/standardization/list/
[2] Patents: US7894515B2 & EP2182688B1
[3] Patents & Patents Pending: EP2247047B1, US20110103267A1, EP12174398.3 & US20110103267A1
[4] Patents & Patents Pending: EP12153028.1, EP2648378A1 & US2013/301483A1

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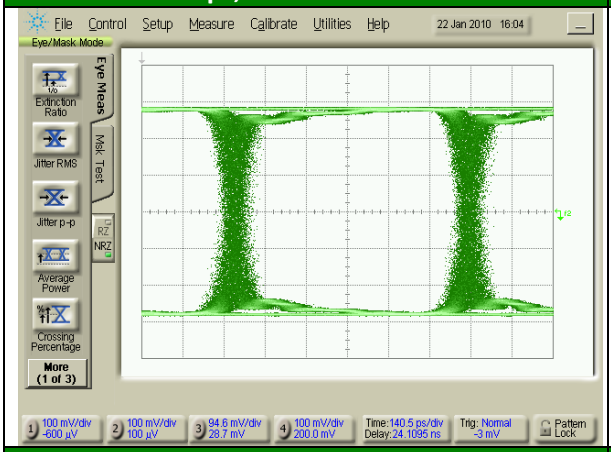
EqcoLogic NV
c/o ETRO/VUB dept.
Pleinlaan 2
1050 Brussels

Phone: +32 2 629 1301
Email: techsupport@eqcologic.com
www: www.eqcologic.com

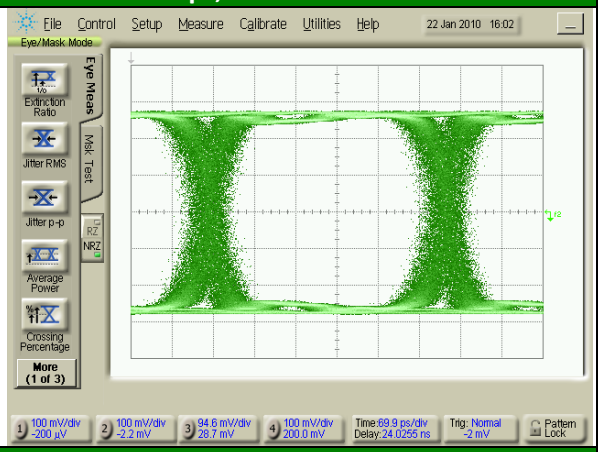
Appendix 1: Typical Equalizer Characteristics

All measurements at VCC = 1.2 V, Temp = +25 ºC, data pattern = 8B/10B test pattern, 600 mV transmit amplitude, and include uplink and power-supply transmission over the cable. Differential measurement into 2x50 Ω.

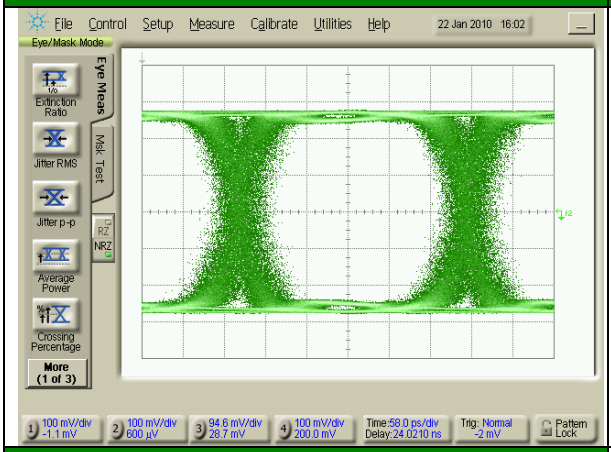
1.25 Gbps, 135 m Belden 1694A



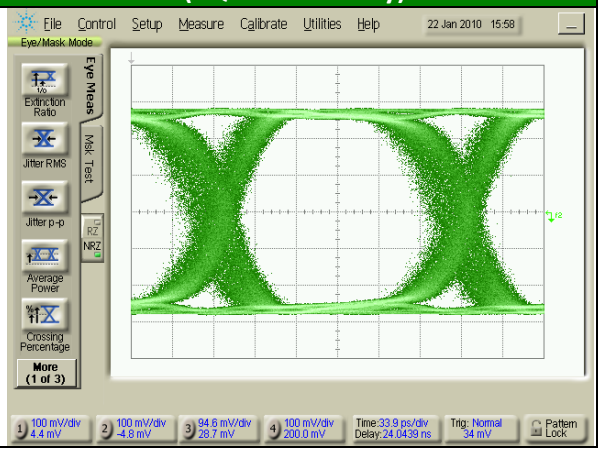
2.5 Gbps, 115 m Belden 1694A



3.125 Gbps, 105 m Belden 1694A



5 Gbps, 65 m Belden 1694A (EQCO62R20 only)



6.25 Gbps, 45m Belden 1694A (EQCO62R20 only)

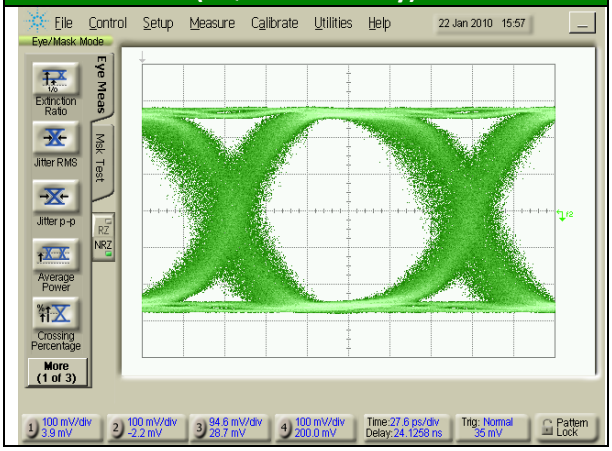


Figure 11: Typical system link EYE-diagram at room temperature for different speeds.

Appendix 2: Typical Uplink Characteristics

All measurements at VCC = 1.2 V, Temp = +25 ºC, data pattern = 8B/10B test pattern at 21 Mbps, typical R_{amp} and R_{rise}, measured into 75 Ω.

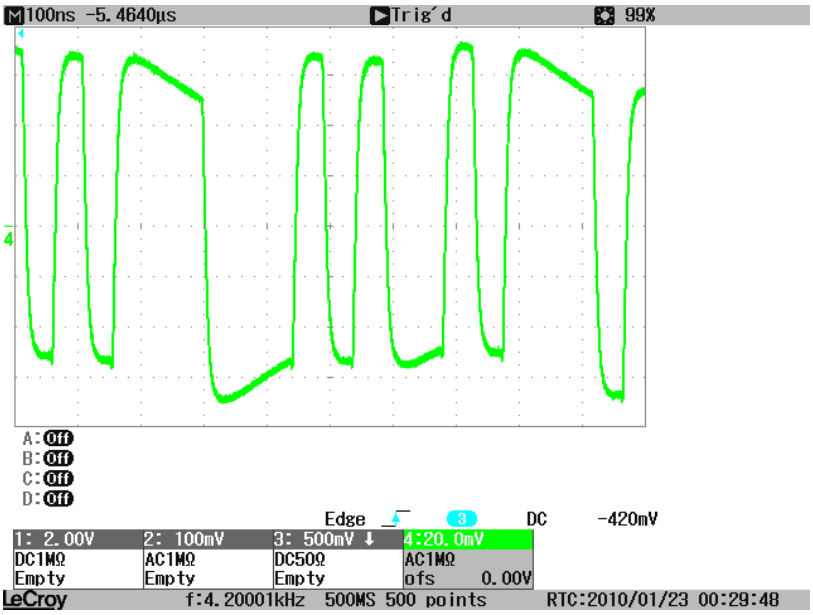


Figure 12: Signal transmitted by low speed driver showing baseline wander due to external 10 µH inductor and ferrite beads[4].

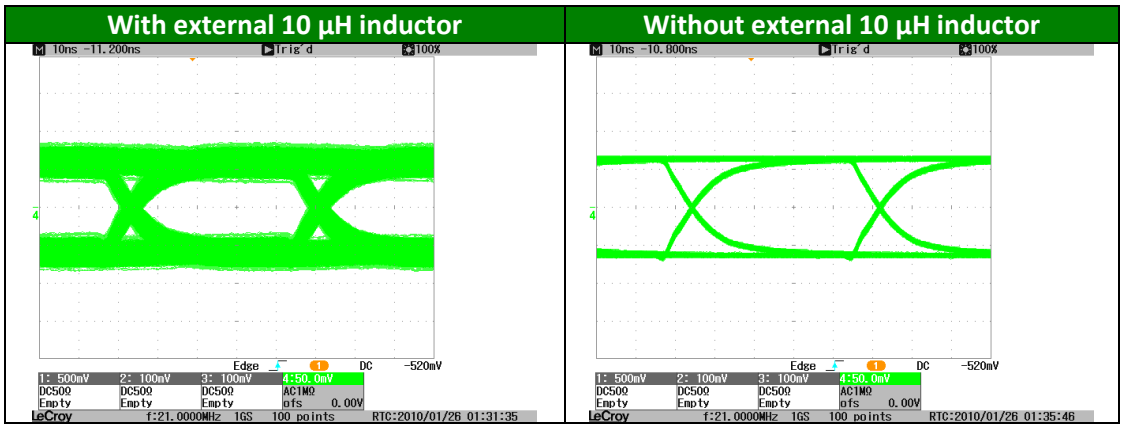


Figure 13: output eye of LF driver with and without external 10 µH inductor

[4] Inductor and ferrite beads at camera side of the link will double the baseline wandering: this is taken care of by the LF-receiver in the EQCO62T20 chip.

Appendix 3: Typical return-loss

Figure 14 shows the return-loss at the BNC connector of the EQCO62R20.3 evaluation board as shown in section 5.1 and 0 with supply current of 0 mA and 703 mA (maximum supply current for CoaXPress) through the inductor (L1) and the ferrite beads (Fb1 & Fb2) and compares it with the CoaXPress (Full Speed) return-loss specification.

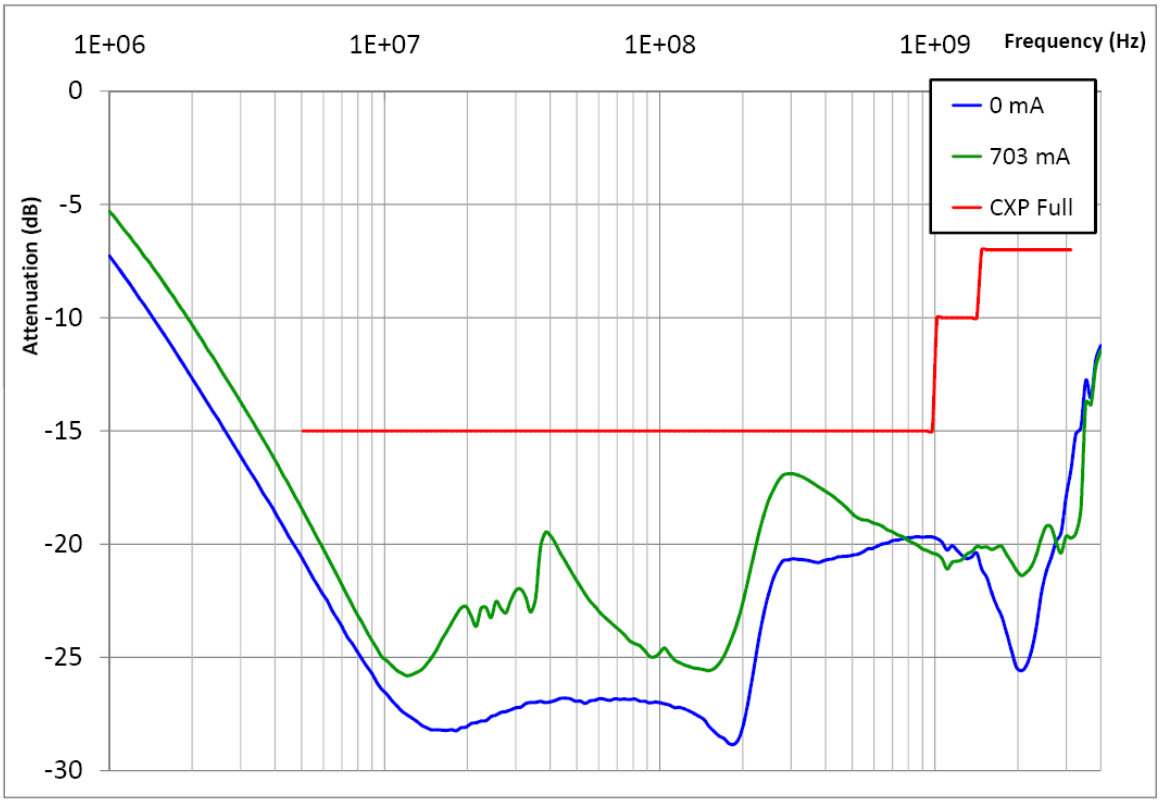


Figure 14: Return-loss of the EQCO62R20.3 evaluation board with and without supply current

Appendix 4: Footprints used for the multilane CoaXPress layout

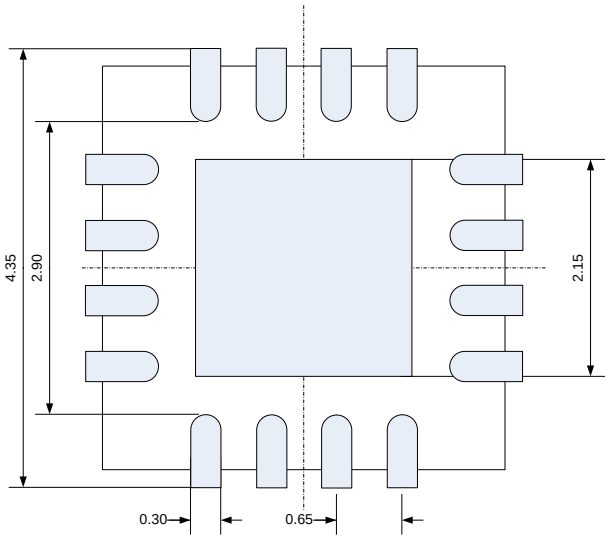


Figure 15: QFN footprint of EQCO62R20.3

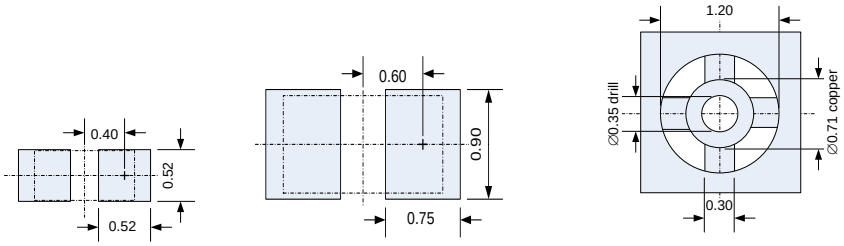


Figure 16: 0402, 0603 and VIA with thermal isolation footprints

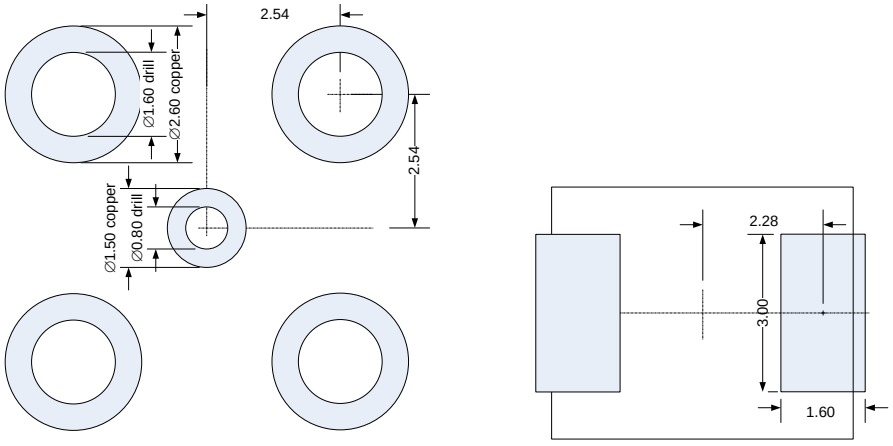


Figure 17: DIN1.0/2.3 and L1 inductor 1812 footprints

Component	Footprint	X	Y	Angle	
NPF 4076	DIN1.0/2.3	0	0		Bottom
EQCO62R20.3	QFN	-0.075	-8		
C1 (50 V)	0603	0.075	-2.55	90°	

Component	Footprint	X	Y	Angle	
C2	0402	2.4	-4.9	90°	
R1 (16 Ω)	0402	0.25	-4.575	90°	
R2 (91 Ω)	0402	-1.2	-5		
FB1	0603	-2.05	0.6		
FB2	0603	-2.05	-0.6		
R6	0402	4.075	0.35		
C7(50 V)	0402	4.475	1.850	90°	
C9	0402	1.675	-11.025		
C10	0402	2.05	-4.9		
L1	1812	4.5	-7.6	90°	Bottom
C8(50 V)	0603	-0.725	-8.425		Bottom
C5	0402	-0.125	-7.175		Bottom

Table 2 component positions of Figure 9

VIA	Thermal	X	Y	Connected to
1		4.1	-4.1	Top-bottom
2		4.825	-4.1	Top-bottom
3	Not isolated	-1.725	-5.975	Top-GND-bottom
4	Not isolated	1.7	-6.425	Top-power-bottom
5		-2.9	-7.025	Top-bottom
6	isolated	1.65	-9.9	Top-GND-bottom
7	Isolated	1.575	-9.7	Top-GND
8	Not Isolated	2.375	-10.175	Top-power

Table 3 via positions of Figure 9

GND plane Coordinates	X	Y	VCC plane Coordinates	X	Y
A	-2.475	-9.1	N	-2.475	-9.125
B	-2.475	-3.1	O	-2.475	-6.875
C	-1.25	-3.1	P	0.75	-6.875
D	-1.25	-6.125	Q	0.75	-6.05
E	-0.475	-6.9	R	2.475	-6.05
F	0.85	-6.9	S	2.475	-9.125
G	0.85	-5.975			
H	1.05	-5.775			
I	1.05	-3.1			
J	-2.475	-3.1			
K	2.475	-9.1			
L	-0.9	-9.075	T	-0.9	-9.075
M	0.75	-10.725	U	0.75	-10.725

Table 4 Ground and VCC plane position of Figure 9

Track	Width	Connected to
1	0.3	QFN.1 to TAB (GND)
2	0.4	QFN.1 to C10 (GND)
3	0.3	QFN.2 (SDIp)
4	0.2	QFN.3 (SDIn)
5	0.3	QFN.4 (GND)
6	0.2	QFN.5 (LFin)

Track	Width	Connected to
7	0.2	QFN.6 (ampR)
8	0.2	QFN.7 (riseR)
9	0.3	QFN.9 (GND)
10	100Ω diff[5].	QFN.10-11 (SDIp-SDIn)
11	0.3	QFN.12 to V8/TAB (GND)
12	0.4	QFN.12 to C9 (GND)
13	0.4	QFN.13 (VCC)
14	0.5	C9 to V9 (VCC)
15	0.5	QFN.16
16	0.4	C2 to DIN1.0/2.3
17	0.7	C10 to DIN1.0/2.3
18	0.3	R1
19	0.4	C1 to DIN1.0/2.3
20	0.4/0.7	FB
21	0.2	C7
22	0.5	Bottom tracks

Table 5 Track dimensions of Figure 9

component	Footprint	X	Y	angle	
NPF 4076	DIN1.0/2.3	0	0		Bottom
EQCO62R20.3	QFN	-0.075	-7.725		
C1 (50V)	0603	0.5	-2	90°	
C2	0402	-0.75	-2.4	90°	
R1 (16Ω)	0402	0.5	-4.05	90°	
R2 (91Ω)	0402	-0.8	-4.05	90°	
C5	0402	-2.4	-4.925		
C9	0402	2.925	-9.1	90°	
C10	0402	2.225	-4.925		

Table 6 component positions of Figure 10

VIA	Thermal	X	Y	Connected to
1	Isolated	-2.8	-5.625	Top-power
2	Not isolated	-1.675	-5.65	Top-GND
3	Not isolated	1.6	-5.65	Top-GND
4	Not isolated	2.325	-6.225	Top-power
5	isolated	2.675	-8	Top-power
6	isolated	-1.65	-9.5	Top-GND
7	Isolated	1.55	-9.5	Top-GND

Table 7 via positions of Figure 10

GND plane Cooardinates	X	Y	VCC plane Coordinates	X	Y
a	-1.725	3.75	m	-2.3	-3.475
b	-1.725	-3	n	-2.3	-6.65
c	-2.25	-3	o	1.75	-6.65
d	-2.25	-5.2	p	1.75	-5.575
e	-0.425	-7	q	2.85	-5.575

[5] Width and spaces between lines needs to be calculated based on PCB layer stack. Impedance should be 100Ω differential.

GND plane Cooardinates	X	Y	VCC plane Coordinates	X	Y
f	0.225	-7	r	2.85	-10.075
g	1.65	-5.575			
h	1.65	-3			
i	2.85	-3			
j	2.85	-10.075			
k	-0.9	-8.8	s	-0.9	-8.8
l	0.75	-10.45	t	0.75	-10.45

Table 8 Ground and VCC plane position of Figure 10

Track	Width	
1	0.3	QFN.1; QFN.4 (GND)
2	0.3	QFN.2 (SDIp)
3	0.3	QFN.3 (SDIn)
4	0.2	QFN.5 (LFin)
5	0.2	QFN.6 (ampR)
6	0.2	QFN.7 (riseR)
7	0.3	QFN.9; QFN.12 (GND)
8	100Ω diff[6].	QFN.10-11 (SDIp-SDIn)
9	0.5	QFN.13; QFN.16 (VCC)
10	0.5	C9; C10; C5
11	0.4	C1; C2

Table 9 Track widths of Figure 10

Figure 18: Used layer stack

[6] Width and spaces between lines needs to be calculated based on PCB layer stack. Impedance should be 100Ω differential.

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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9