



100V 175°C N-CHANNEL ENHANCEMENT MODE MOSFET PowerDI5060-8

Product Summary

BV _{DSS}	R _{DS(ON)} Max	I _D T _C = +25°C	
100V	8.9mΩ @ V _{GS} = 10V	88A	

Description

This new generation N-Channel Enhancement Mode MOSFET is designed to minimize $R_{DS(ON)}$, yet maintain superior switching performance. This device is ideal for use in notebook battery power management and load switch.

Applications

- Motor Control
- DC-DC Converters
- Power Management

Features

- Rated to +175°C Ideal for High Ambient Temperature Environments
- 100% Unclamped Inductive Switching (UIS) Test in Production Ensures More Reliable and Robust End Application
- Thermally Efficient Package-Cooler Running Applications
- High Conversion Efficiency
- Low R_{DS(ON)} Minimizes On-State Losses
- Low Input Capacitance
- Fast Switching Speed
- <1.1mm Package Profile Ideal for Thin Applications (PowerDI[®])
- Lead-Free Finish; RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)

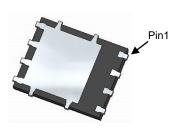
Mechanical Data

- Case: PowerDI5060-8
- Case Material: Molded Plastic, "Green" Molding Compound.
 UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram Below
- Terminal Finish Matte Tin Annealed over Copper Leadframe.
 Solderable per MIL-STD-202, Method 208 ⁽³⁾
- Weight: 0.097 grams (Approximate)

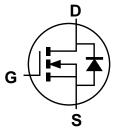
PowerDI5060-8



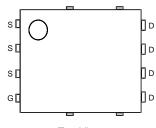
Top View



Bottom View



Internal Schematic



Top View Pin Configuration

Ordering Information (Note 4)

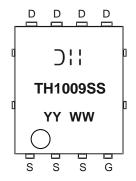
Part Number	Case	Packaging
DMTH10H009SPS-13	PowerDI5060-8	2,500 / Tape & Reel

Notes:

- 1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/



Marking Information



] | | = Manufacturer's Marking TH1009SS = Product Type Marking Code YYWW = Date Code Marking YY = Last Two Digits of Year (ex: 19 = 2019) WW = Week Code (01 to 53)

Characteristic	Symbol	Value	Unit		
Drain-Source Voltage	V_{DSS}	100	V		
Gate-Source Voltage			V _{GSS}	±20	V
Continuous Drain Current V _{GS} = 10V (Note 6)	Steady State	$T_A = +25$ °C $T_A = +100$ °C	I _D	16 11	А
Continuous Drain Current V _{GS} = 10V (Note 7)	ΙD	88 62	А		
Pulsed Drain Current (10µs Pulse, T _C = +25°C, Package Lin	I _{DM}	350	Α		
Maximum Continuous Body Diode Forward Current	Is	83	Α		
Pulsed Body Diode Current (10μs Pulse, T _C = +25°C, Package Limited)			I _{SM}	350	Α
Avalanche Current (Note 8), L = 3mH			I _{AS}	11	Α
Avalanche Energy (Note 8), L = 3mH			E _{AS}	181.5	mJ

Thermal Characteristics

Characteristic	Symbol	Value	Unit	
Total Power Dissipation (Note 5)	$T_A = +25^{\circ}C$	P_{D}	1.6	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{ heta JA}$	94	°C/W
Total Power Dissipation (Note 6)	$T_A = +25^{\circ}C$	P_{D}	3.2	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{ heta JA}$	47	°C/W
Total Power Dissipation (Note 7)	$T_{C} = +25^{\circ}C$	P_{D}	100	W
Thermal Resistance, Junction to Case (Note 7)		$R_{\theta JC}$	1.5	°C/W
Operating and Storage Temperature Range		T _{J,} T _{STG}	-55 to +175	°C

Notes:

- 5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
- 6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.
- 7. Thermal resistance from junction to soldering point (on the exposed drain pad).
- 8. I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep $T_J = +25^{\circ}C$.



Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

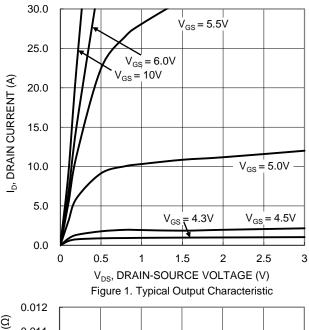
Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 9)							
Drain-Source Breakdown Voltage	BV _{DSS}	100	_	_	V	$V_{GS} = 0V$, $I_D = 1mA$	
Zero Gate Voltage Drain Current	I _{DSS}	_	_	1	μΑ	$V_{DS} = 80V, V_{GS} = 0V$	
Gate-Source Leakage	I _{GSS}	_	_	±100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 9)							
Gate Threshold Voltage	V _{GS(TH)}	2	_	4	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$	
Static Drain-Source On-Resistance	R _{DS(ON)}	_	6.7	8.9	mΩ	$V_{GS} = 10V, I_D = 20A$	
Diode Forward Voltage	V_{SD}	_	0.8	1.2	V	$V_{GS} = 0V, I_{S} = 13A$	
DYNAMIC CHARACTERISTICS (Note 10)							
Input Capacitance	C _{iss}	_	2085	_		$V_{DS} = 50V$, $V_{GS} = 0V$ f = 1MHz	
Output Capacitance	Coss	_	609	_	pF		
Reverse Transfer Capacitance	C_{rss}	_	13	_			
Gate Resistance	R_{g}	_	1.7	_	Ω	$V_{DS} = 0V$, $V_{GS} = 0V$, $f = 1MHz$	
Total Gate Charge	Q_g	_	30	_			
Gate-Source Charge	Q _{gs}	_	9.5	_	nC	$V_{DD} = 50V, I_{D} = 13A,$ $V_{GS} = 10V$	
Gate-Drain Charge	Q_{gd}	_	7.3	_			
Turn-On Delay Time	t _{D(ON)}	_	9.7	_		$V_{DD} = 50V, V_{GS} = 10V,$ $I_{D} = 13A, R_{g} = 6\Omega$	
Turn-On Rise Time	t _R	_	13.7	_	ns		
Turn-Off Delay Time	t _{D(OFF)}	_	25.1	_	115		
Turn-Off Fall Time	t _F	_	17.3	_			
Reverse Recovery Time	t _{RR}		45	_	ns	I_ 12.4 di/dt 100.4/v.o	
Reverse Recovery Charge	Q _{RR}	_	68	_	nC	$I_F = 13A$, di/dt = 100A/ μ s	

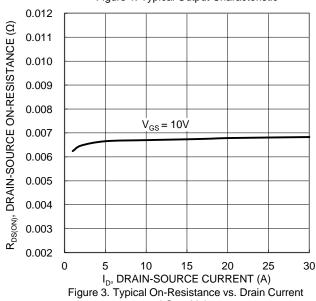
Notes:

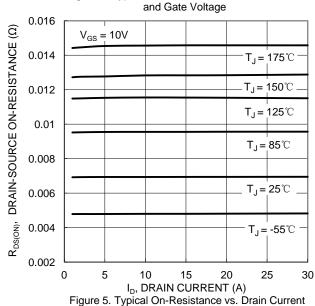
Short duration pulse test used to minimize self-heating effect.
 Guaranteed by design. Not subject to product testing.



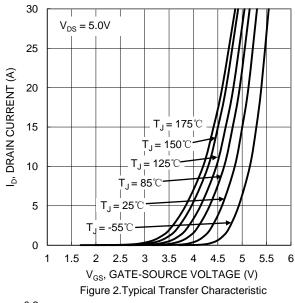


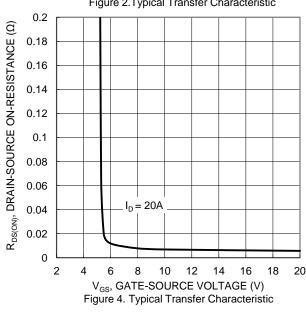






and Temperature





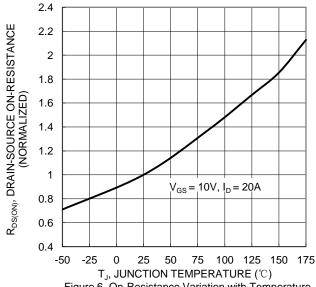


Figure 6. On-Resistance Variation with Temperature





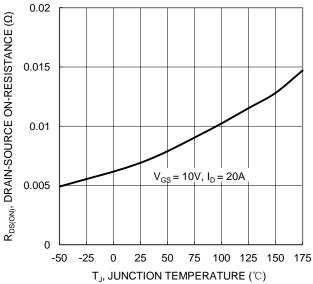
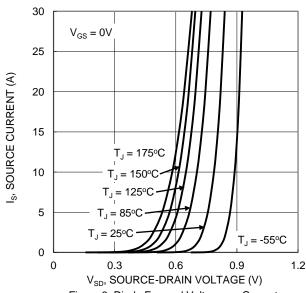


Figure 7. On-Resistance Variation with Temperature



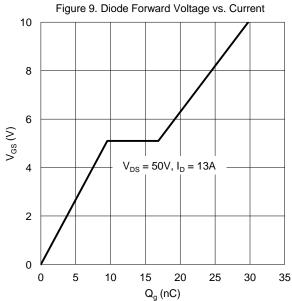


Figure 11. Gate Charge

4 $V_{GS(TH)},$ GATE THRESHOLD VOLTAGE (V) 3.5 $I_D = 1mA$ 3 2.5 2 $I_{D} = 250 \mu A$ 1.5 1 0.5 -50 -25 0 25 50 75 100 125 150 175 T_.I, JUNCTION TEMPERATURE (°C)

Figure 8. Gate Threshold Variation vs. Junction Temperature

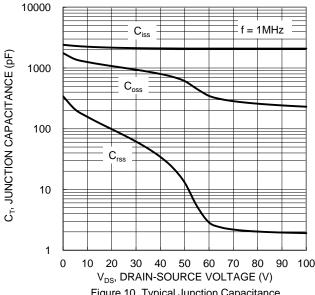
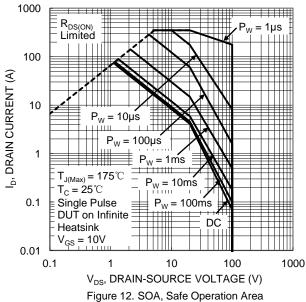


Figure 10. Typical Junction Capacitance





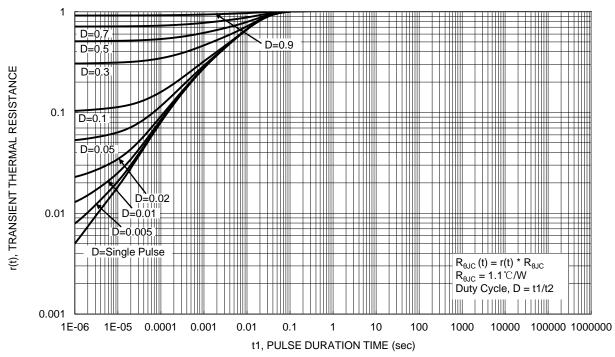


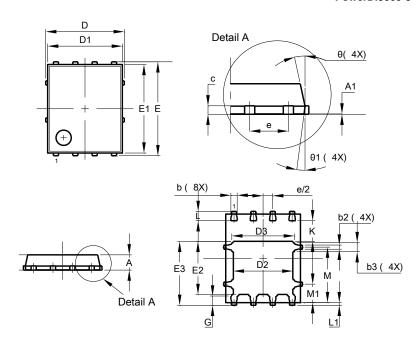
Figure 13. Transient Thermal Resistance



Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8

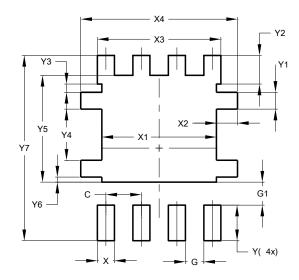


PowerDI5060-8						
Dim	Min					
Α	0.90	1.10	1.00			
A1	0.00	0.05	_			
b	0.33	0.51	0.41			
b2	0.200	0.350	0.273			
b3	0.40	0.80	0.60			
С	0.230	0.330	0.277			
D	;	5.15 BSC	;			
D1	4.70	5.10	4.90			
D2	3.70	4.10	3.90			
D3	3.90	4.30 4.1				
Е	(6.15 BSC				
E1	5.60	6.00	5.80			
E2	3.28	3.68	3.48			
E3	3.99					
е		1.27 BSC				
G	0.51	0.71	0.61			
K	0.51	-	_			
L	0.51	0.71	0.61			
L1	0.100	0.200	0.175			
М	3.235	4.035	3.635			
M1	1.00	1.40	1.21			
Θ	10°	12°	11°			
Θ1	6°	8°	7°			
All Dimensions in mm						

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8



Dimensions	Value (in mm)			
С	1.270			
G	0.660			
G1	0.820			
X	0.610			
X1	4.100			
X2	0.755			
Х3	4.420			
X4	5.610			
Y	1.270			
Y1	0.600			
Y2	1.020			
Y3	0.295			
Y4	1.825			
Y5	3.810			
Y6	0.180			
Y7	6.610			



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