

## ISL6617A

PWM Doubler with Output Monitoring Feature

FN7844  
Rev.2.00  
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The [ISL6617A](#) uses Intersil's proprietary Phase Doubler scheme to modulate two-phase power trains with single PWM input. It doubles the number of phases that 3.3V multiphase controllers can support.

The ISL6617A is designed to minimize the number of analog signals that interface between the controller and drivers in high phase count scalable applications. The common COMP signal, which is usually seen in conventional cascaded configurations, is not required; this improves noise immunity and simplifies the layout. Furthermore, the ISL6617A provides low part count and low cost advantage over the conventional cascaded technique.

By cascading the ISL6617A with another ISL6617 or ISL6611A, it can quadruple the number of phases that 3.3V multiphase controllers can support.

The ISL6617A also features tri-state inputs and outputs that recognize a high-impedance state, working together with Intersil multiphase PWM controllers and driver stages to prevent negative transients on the controlled output voltage when operation is suspended. This feature eliminates the need for the Schottky diode that may be utilized in a power system to protect the load from excessive negative output voltage damage.

### Applications

- High current, low voltage DC/DC converters
- High frequency and high efficiency VRM and VRD
- High phase count and phase shedding applications
- 3.3V PWM input integrated power stage or DrMOS

### Phase Doubler Selection Guide

| PART NUMBER | PWM INPUT | PWM OUTPUT | INTEGRATED DRIVER | CASCADED DEVICES                                 | COMPATIBLE CONTROLLERS   |
|-------------|-----------|------------|-------------------|--|--|
| ISL6617A    | 3.3V      | 5.0V       | N/A               | 5.0V PWM DrMOS/SPS; ISL6617, ISL6611A, ISL99227B | 3.3V PWM digital controllers with phase doubler compatibility; ISL691x7, ISL691x4, ISL691x8, ISL681x7, ISL681x4, and ISL6388/98 with 3.3V PWM option |
| ISL6617     | 5.0V      | 5.0V       | N/A               | 5.0V PWM DrMOS/SPS; ISL6617, ISL6611A, ISL99227B | ISL6388/98 with 3.3V or 5V PWM option  |
| ISL6611A    | 5V        | N/A        | 5.0V              | Discrete MOSFET; Dual FETs                       |  |

### Features

- Proprietary phase doubler scheme
- Enhanced light- to full-load efficiency
- Double or quadruple phase count
- Patented current balancing with DCR current sensing and adjustable gain
- Current monitoring output ( $I_{OUT}$ ) to simplify system interface and layout
- Triple-level enable input for mode selection
- Dual PWM output drives for two synchronous rectified bridges with single PWM input
- Channel synchronization and two interleaving options
- Support 3.3V PWM input
- Support 5V PWM output
- Compatible with DCR sensing or smart power stage sensing
- Tri-state PWM input and outputs for output stage shutdown
- Overvoltage protection
- Dual Flat No-lead (DFN) package
  - Near chip-scale package footprint; improves PCB utilization, thinner profile
  - Pb-free (RoHS compliant)

### Related Literature

- For a full list of related documents, visit our website
  - [ISL6617A](#) product page

## Internal Block Diagram

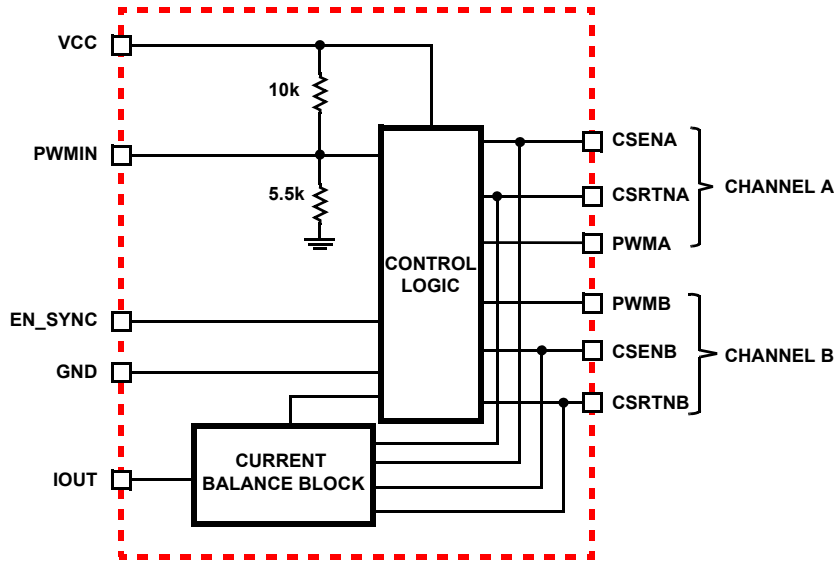


FIGURE 1. BLOCK DIAGRAM

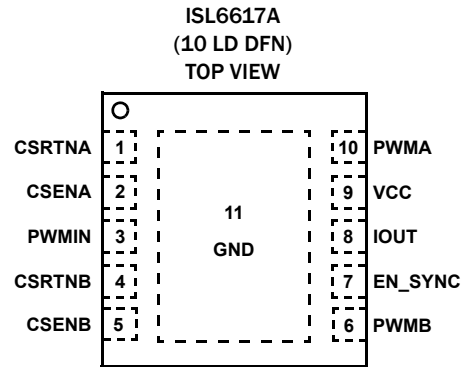
## Ordering Information

| PART NUMBER<br>(Notes 1, 2, 3) | PART MARKING | TEMP. RANGE<br>(°C) | PACKAGE<br>(RoHS COMPLIANT) | PKG.<br>DWG. # |
|--------------------------------|--------------|---------------------|-----------------------------|----------------|
| ISL6617AFRZ                    | 17AF         | -40 to +125         | 10 Ld 3x3 DFN               | L10.3x3        |

NOTES:

1. Add "-T" suffix for 6k unit tape and reel option. Refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see product information page for [ISL6617A](#). For information on MSL see techbrief [TB363](#).

## Pin Configuration



## Functional Pin Descriptions

| PIN # | PIN SYMBOL | FUNCTION   |
|-------|------------|--|
| 1     | CSRTNA     | Output of the differential amplifier for Channel A. Connect a resistor on this pin to the negative rail of the sensed voltage to set the current gain.   |
| 2     | CSENA      | Input of the differential amplifier for Channel A. Typically, the positive rail of sensed voltage via DCR sensing network connects to this node.   |
| 3     | PWMIN      | The PWM input signal (3.3V) triggers the J-K flip flop and alternates its input to Channel A and B. Both channels are effectively modulated. The PWM signal can enter three distinct states during operation; see <a href="#">"Operation" on page 9</a> for further details. Connect this pin to the PWM output of the controller. |
| 4     | CSRTNB     | Output of the differential amplifier for Channel B. Connect a resistor on this pin to the negative rail of the sensed voltage to set the current gain.   |
| 5     | CSENB      | Input of the differential amplifier for Channel B. Typically, the positive rail of sensed voltage via DCR sensing network connects to this node.   |
| 6     | PWMB       | PWM output of Channel B with 5V PWM tri-state compatibility.   |
| 7     | EN_SYNC    | Driver enable and mode selection input. See <a href="#">"EN_SYNC Operation" on page 9</a> for more details.  |
| 8     | IOUT       | Current monitoring output. It sources out the average current of both Channel A and B.   |
| 9     | VCC        | Connect this pin to a +5V bias supply. It supplies power to internal analog circuits. Place a high quality low ESR ceramic capacitor from this pin to GND.   |
| 10    | PWMA       | PWM output of Channel A with 5V PWM tri-state compatibility.   |
| 11    | GND        | Bias and reference ground. All signals are referenced to this node. Place a high quality low ESR ceramic capacitor from this pin to VCC. Connect this pad to the power ground plane (GND) via thermally enhanced connection.   |



## Typical Application II (2-Phase Controller for 4-Phase Operation)

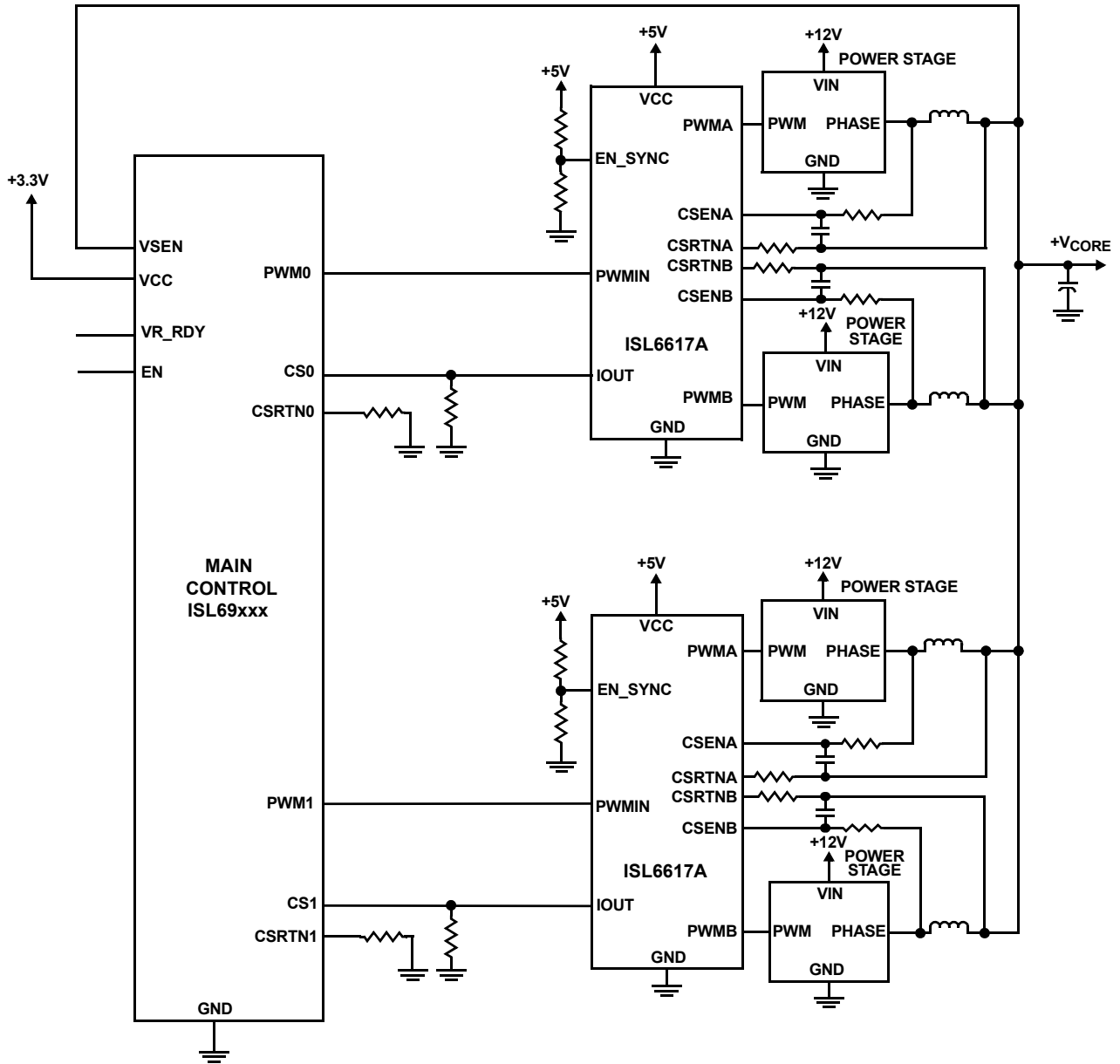


FIGURE 3. TYPICAL APPLICATION II

# Typical Application III (2-Phase Controller to 8-Phase Operation)

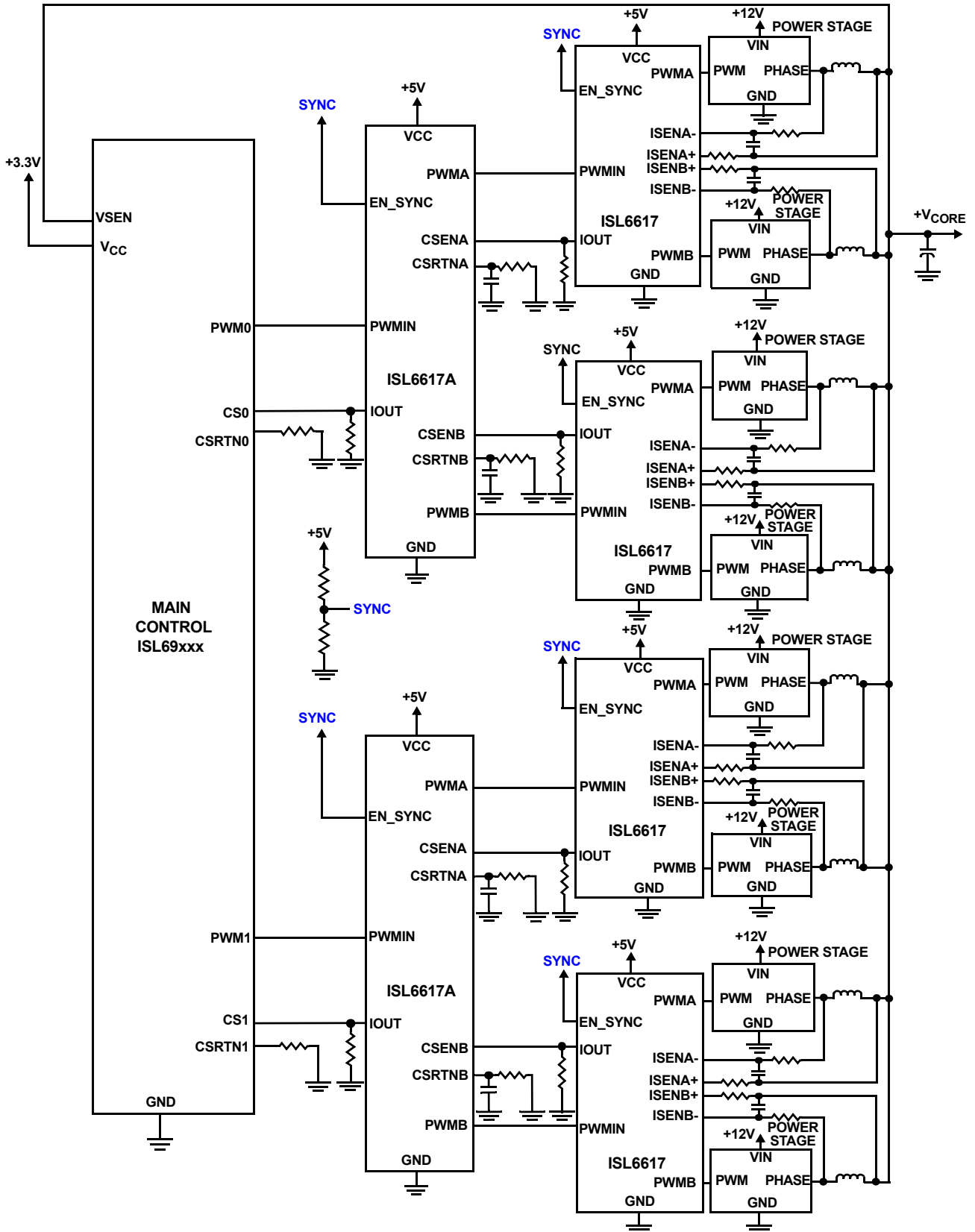


FIGURE 4. TYPICAL APPLICATION III

## Absolute Maximum Ratings

|  |                     |
|--|---------------------|
| Supply Voltage (VCC)                                   | -0.3V to 6.7V       |
| Input Voltage ( $V_{ENx}$ , $V_{PWMIN}$ , $I_{SENx}$ ) | -0.3V to VCC + 0.3V |
| Ambient Temperature Range                              | -40 °C to +125 °C   |
| <b>ESD Rating</b>                                      |                     |
| Human Body Model (JEDEC Class 2)                       | 2kV                 |
| Machine Model (JEDEC Class B)                          | 200V                |
| Charged Device Model (JEDEC Class IV)                  | 2kV                 |
| Latch-Up (JEDEC Class II)                              | +85 °C              |

## Thermal Information

|                                   |                           |                      |
|-----------------------------------|---------------------------|----------------------|
| Thermal Resistance (Typical)      | $\theta_{JA}$ (°C/W)      | $\theta_{JC}$ (°C/W) |
| 10 Ld DFN (Notes 4, 5)            | 48                        | 7                    |
| Maximum Junction Temperature      | +150 °C                   |                      |
| Maximum Storage Temperature Range | -65 °C to +150 °C         |                      |
| Pb-Free Reflow Profile            | see <a href="#">TB493</a> |                      |

## Recommended Operating Conditions

|  |                   |
|--|-------------------|
| Ambient Temperature                    | -40 °C to +125 °C |
| Maximum Operating Junction Temperature | +125 °C           |
| Supply Voltage, VCC                    | 5V ±10%           |

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

### NOTES:

- $\theta_{JA}$  is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See Tech Brief [TB379](#).
- $\theta_{JC}$ , “case temperature” location is at the center of the package underside exposed pad.

**Electrical Specifications** These specifications apply for recommended ambient temperature, unless otherwise noted. **Boldface limits apply across the operating temperature range.**

| PARAMETER                         | SYMBOL         | TEST CONDITIONS  | MIN<br>(Note 6) | TYP | MAX<br>(Note 6) | UNIT       |
|-----------------------------------|----------------|--|-----------------|-----|-----------------|------------|
| <b>SUPPLY CURRENT</b>             |                |  |                 |     |                 |            |
| Bias Supply Current               | $I_{VCC}$      | PWM pin floating, $V_{VCC} = 5V$ , $EN\_SYNC = 5V$       |                 | 5   | <b>6.5</b>      | mA         |
|                                   |                | PWM pin floating, $V_{VCC} = 5V$ , $EN\_SYNC = 0V$       |                 | 5   | <b>6.5</b>      | mA         |
|                                   |                | $F_{PWM} = 600kHz$ , $V_{VCC} = 5V$ , $EN\_SYNC = 5V$    |                 | 6   | <b>7.5</b>      | mA         |
|                                   |                | $F_{PWM} = 600kHz$ , $V_{VCC} = 5V$ , $EN\_SYNC = 4.25V$ |                 | 6   | <b>7.5</b>      | mA         |
|                                   |                | $F_{PWM} = 300kHz$ , $V_{VCC} = 5V$ , $EN\_SYNC = 3.25V$ |                 | 6   | <b>7.5</b>      | mA         |
| <b>POWER-ON RESET</b>             |                |  |                 |     |                 |            |
| POR Rising                        |                |  |                 | 3.4 | <b>4.2</b>      | V          |
| POR Falling                       |                |  | <b>2.3</b>      | 3.0 |                 | V          |
| Hysteresis                        |                |  |                 | 350 |                 | mV         |
| <b>EN_SYNC INPUT</b>              |                |  |                 |     |                 |            |
| ENx Minimum LOW Threshold         | $V_{ENx}$      |  |                 |     | <b>0.8</b>      | V          |
| ENx Maximum HIGH Threshold        | $V_{ENx}$      |  | <b>2.0</b>      |     |                 | V          |
| <b>SYNC AND INTERLEAVING MODE</b> |                |  |                 |     |                 |            |
| Interleaving Mode 1 Window        | $V_{ENx}$      |  | <b>97%</b>      |     |                 | VCC        |
| Interleaving Mode 2 Window        | $V_{ENx}$      |  | <b>78%</b>      |     | <b>85%</b>      | VCC        |
| Synchronous Mode Window           | $V_{ENx}$      |  | <b>54%</b>      |     | <b>64%</b>      | VCC        |
| Typical Threshold Hysteresis      |                |  |                 | -5% |                 | VCC        |
| Minimum SYNC Pulse                |                |  |                 |     | <b>40</b>       | ns         |
| Maximum Synchronization Delay     |                |  | <b>50</b>       |     |                 | ns         |
| Interleaving Mode Phase Shift     |                | SYNC = 5V, PWM = 300kHz, 10% Width                       |                 | 180 |                 | °          |
| Synchronization Mode Phase Shift  |                | SYNC = 0V, PWM = 300kHz, 10% Width                       |                 | 0   |                 | °          |
| <b>PWM INPUT (PWMIN)</b>          |                |  |                 |     |                 |            |
| Sinking Impedance                 | $R_{PWM\_SNK}$ |  |                 | 5.5 |                 | k $\Omega$ |
| Source Impedance                  | $R_{PWM\_SRC}$ |  |                 | 10  |                 | k $\Omega$ |

**Electrical Specifications** These specifications apply for recommended ambient temperature, unless otherwise noted. **Boldface limits apply across the operating temperature range. (Continued)**

| PARAMETER   | SYMBOL               | TEST CONDITIONS   | MIN<br>(Note 6) | TYP  | MAX<br>(Note 6) | UNIT     |
|---|----------------------|---|-----------------|------|-----------------|----------|
| Tri-State to PWM High Rising Threshold                          |                      | $V_{VCC} = 5V$  |                 | 2.50 | 2.70            | V        |
| Tri-State to PWM High Falling Threshold                         |                      | $V_{VCC} = 5V$  | 2.00            | 2.25 |                 | V        |
| Tri-State to PWM Low Rising Threshold                           |                      | $V_{VCC} = 5V$  |                 | 0.95 | 1.15            | V        |
| Tri-State to PWM Low Falling Threshold                          |                      | $V_{VCC} = 5V$  | 0.50            | 0.75 |                 | V        |
| <b>CURRENT SENSE (CSENA, CSENB, IOUT) AND PROTECTION (IOUT)</b> |                      |   |                 |      |                 |          |
| Sensed Current Tolerance  | I <sub>OUT</sub>     | CSENA = CSENB = 0 $\mu$ A   | <b>-6</b>       | 0    | <b>6</b>        | $\mu$ A  |
|   |                      | CSENA = CSENB = 20 $\mu$ A  | <b>14</b>       | 20   | <b>26</b>       | $\mu$ A  |
|   |                      | CSENA = CSENB = 50 $\mu$ A  | <b>43</b>       | 50   | <b>57</b>       | $\mu$ A  |
|   |                      | CSENA = CSENB = 100 $\mu$ A   | <b>90</b>       | 100  | <b>110</b>      | $\mu$ A  |
| Un-Tri State Trip for OVP                                       | I <sub>OUT</sub>     | ENx = LOW TO HIGH, PWM = LOW  | <b>40</b>       | 60   | <b>90</b>       | $\mu$ A  |
| <b>PWM OUTPUT (PWMA AND PWMB)</b>                               |                      |   |                 |      |                 |          |
| Sourcing Impedance  | R <sub>PWM_SRC</sub> | VCC = 5V, PWMIN = HIGH  | <b>30</b>       | 100  | <b>200</b>      | $\Omega$ |
| Sink Impedance  | R <sub>PWM_SNK</sub> | VCC = 5V, PWMIN = LOW   | <b>30</b>       | 100  | <b>150</b>      | $\Omega$ |
| PWM Output High Level   | V <sub>PWMA/B</sub>  | VCC = 5V, PWMIN = HIGH, 2.5mA Load  | <b>4.5</b>      |      |                 | V        |
| PWM Output Low Level  | V <sub>PWMA/B</sub>  | VCC = 5V, PWMIN = LOW, 2.5mA Load   |                 |      | <b>0.4</b>      | V        |
| PWM Tri-State Level   | V <sub>PWMA/B</sub>  | VCC = 5V, EN_PH = LOW, 0.5mA Load   | <b>1.65</b>     | 2.00 | <b>2.6</b>      | V        |
| <b>SWITCHING TIME</b> (See <a href="#">Figure 5 on page 9</a> ) |                      |   |                 |      |                 |          |
| PWMA/B Low to High Rise Time                                    | t <sub>R1</sub>      | Unloaded, 10% to 90%  |                 | 4.5  |                 | ns       |
| PWMA/B Tri-State to High Rise Time                              | t <sub>R2</sub>      | Unloaded, 10% to 90%  |                 | 4.5  |                 | ns       |
| PWMA/B High to Low Fall Time                                    | t <sub>F1</sub>      | Unloaded, 90% to 10%  |                 | 4.0  |                 | ns       |
| PWMA/B High to Tri-state Fall Time                              | t <sub>F2</sub>      | 100% to 60% (3V), assume equivalent loading of RC = 50k $\Omega$ * 10pF = 500ns |                 | 255  |                 | ns       |
| PWMA/B Turn-On Propagation Delay                                | t <sub>PDH</sub>     | Outputs unloaded  |                 | 35   |                 | ns       |
| PWMA/B Turn-Off Propagation Delay                               | t <sub>PDL</sub>     | Outputs unloaded, excluding extension   |                 | 35   |                 | ns       |
| PWMA/B Extension  | t <sub>EXT</sub>     | ENx = VCC, I <sub>PWMA</sub> > I <sub>PWMB</sub>                                |                 | 70   |                 | ns       |
|   |                      | ENx = VCC, I <sub>PWMA</sub> < I <sub>PWMB</sub>                                |                 | 70   |                 | ns       |
|   |                      | ENx = 80% * VCC, I <sub>PWMA</sub> > I <sub>PWMB</sub>                          |                 | 190  |                 | ns       |
|   |                      | ENx = 80% * VCC, I <sub>PWMA</sub> < I <sub>PWMB</sub>                          |                 | 190  |                 | ns       |
| Tri-State to High or Low Propagation Delay                      | t <sub>PTS</sub>     | Outputs unloaded, excluding extension   |                 | 10   |                 | ns       |
| Tri-State Shutdown Hold-Off Time                                | t <sub>TSSHD</sub>   | Including propagation delay   |                 | 65   |                 | ns       |

**NOTE:**

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.



## Timing Diagram

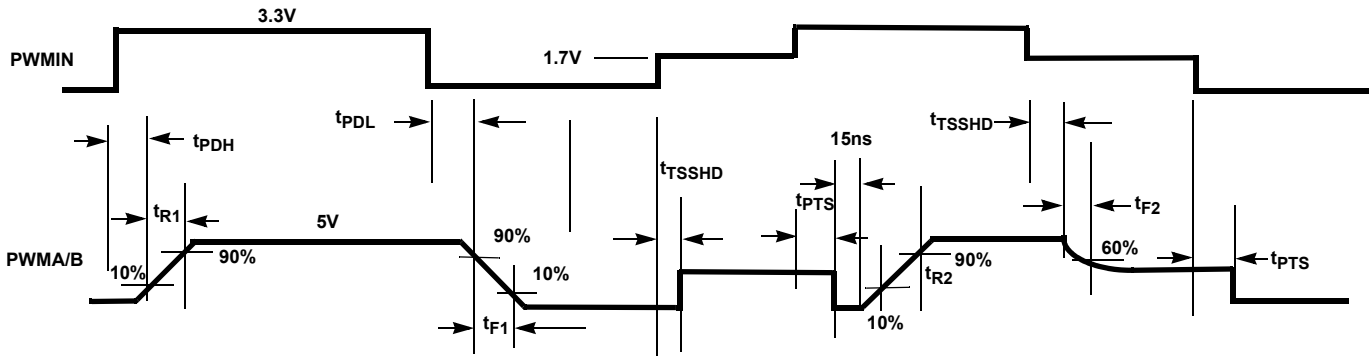


FIGURE 5. TIMING DIAGRAM

## Operation

Designed for high phase count and phase shedding applications, the ISL6617A driverless phase doubler is meant to double or quadruple (cascaded with two ISL6617s) the number of phases that 3.3V multiphase controllers can support.

A rising transition on PWMIN initiates the turn-on of the PWMA/B (see Figure 5). After a short propagation delay [t<sub>PDH</sub>], the PWMA/B begins to rise. Typical rise times [t<sub>R1</sub>] are provided in the “Electrical Specifications” table on page 8.

A falling transition on PWMIN indicates the turn-off of the PWMA/B. The PWMA/B begins to fall [t<sub>F1</sub>] after a propagation delay [t<sub>PDL</sub>], which is modulated by the current balance circuits.

When the PWMIN stays in the tri-state window for longer than [t<sub>TSSHD</sub>], both PWMA/B will pull to 40% of V<sub>CC</sub> so that the cascaded 5V PWM input MOSFET driver or integrated power stage can recognize tri-state.

## EN\_SYNC Operation

The EN\_SYNC pin features multiple functions. It is the enable input of the device and the input to select various operational modes.

### ENABLE OPERATION

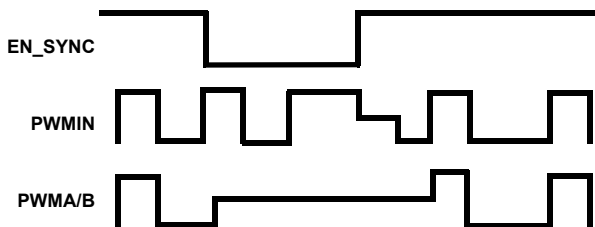


FIGURE 6. TYPICAL ENABLE OPERATION TIMING DIAGRAM

As shown in Figure 6, the ISL6617A disables the doubler operation when the EN\_SYNC pin is pulled to ground. When the EN\_SYNC returns high, the phase doubler will pull the PWM line into the tri-state window, and then will be enabled only at the leading edge of the PWM input. Prior to the first PWMIN rising edge, both the PWMA and PWMB output will remain in tri-state unless an overvoltage fault is detected. This fault is defined as when a phase is detected to have more than 60% of the

maximum I<sub>OUT</sub> current. This provides additional protection to the load if the upper MOSFET experiences a short while the doubler is enabled.

The EN\_SYNC pin should remain high if driving the PWM line high is prohibited for the associated controller. For proper system interface, please refer to the respective device datasheet.

### SYNCHRONOUS OPERATION

The ISL6617A can be set in Interleaving mode or Synchronous mode by pulling the EN\_SYNC pin to the respective level, as shown in Table 1. A synchronous pulse can be sent to the phase doubler during the load application to improve the voltage droop and current balance while still maintaining interleaving operation at DC load conditions. However, excessive ringback can occur; hence, the Synchronous mode operation should be carefully investigated. Figure 7 shows how to generate a synchronous pulse when a transient load is applied. The comparator should be a fast comparator with a minimum delay.

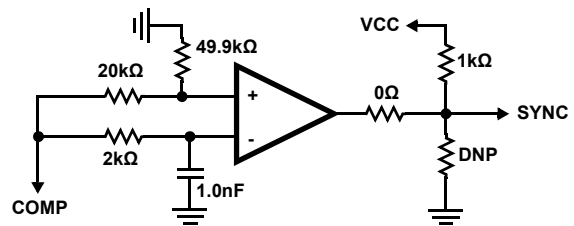


FIGURE 7. TYPICAL SYNC PULSE GENERATOR

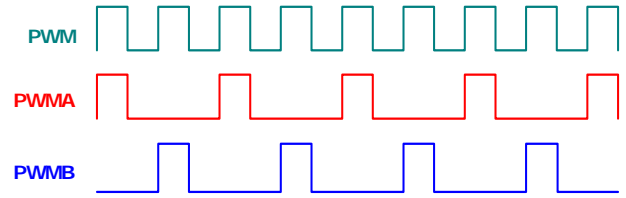
### VARIOUS OPERATIONAL MODES

The ISL6617A has three distinct operating modes depending upon the voltage level of the EN\_SYNC pin. To ensure that the ISL6617A is in operation, the pin must be above 2V. When the EN\_SYNC pin is set to above 97% of V<sub>CC</sub>, the ISL6617A will operate in Interleaving mode with a maximum extension of 70ns. When V<sub>CC</sub> is between 78% and 85% of V<sub>CC</sub>, the ISL6617A operates in Interleaving mode with a fixed extension of 120ns and a variable extension of up to 70ns. This results in a minimum extension of 120ns and a max of 190ns. To enter this 2nd Interleaving mode, the pin must remain in the 78% to 85% range for at least four cycles. Between 54% and 64% of V<sub>CC</sub>, the device operates in Synchronous mode. Figures 8 and 9 show simplified synchronous and Interleaving modes’ operational waveforms, respectively.

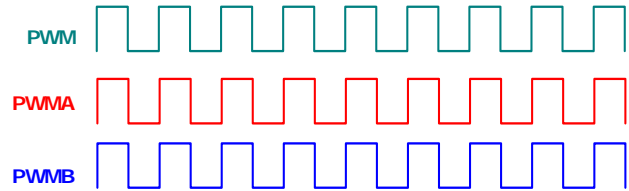
**TABLE 1. ISL6617A OPERATIONAL MODES**

| MODE            | MIN  | TYP                | MAX                | EXTENSION                        |
|-----------------|--|--------------------|--------------------|----------------------------------|
| Enable Low      |  |                    | 0.8V               |                                  |
| Enable High     | 2V   |                    |                    |                                  |
| Interleaving #1 | $97% \cdot V_{CC}$   |                    | $V_{CC}$           | 0ns to 70ns                      |
| Interleaving #2 | $78% \cdot V_{CC}$   | $81% \cdot V_{CC}$ | $85% \cdot V_{CC}$ | $120ns + (0ns \text{ to } 70ns)$ |
| Synchronous     | $54% \cdot V_{CC}$   | $60% \cdot V_{CC}$ | $64% \cdot V_{CC}$ | 0ns to 70ns                      |
| Not Used        | From 0.8V to 2V or 54% of $V_{CC}$ is not recommended region |                    |                    |                                  |

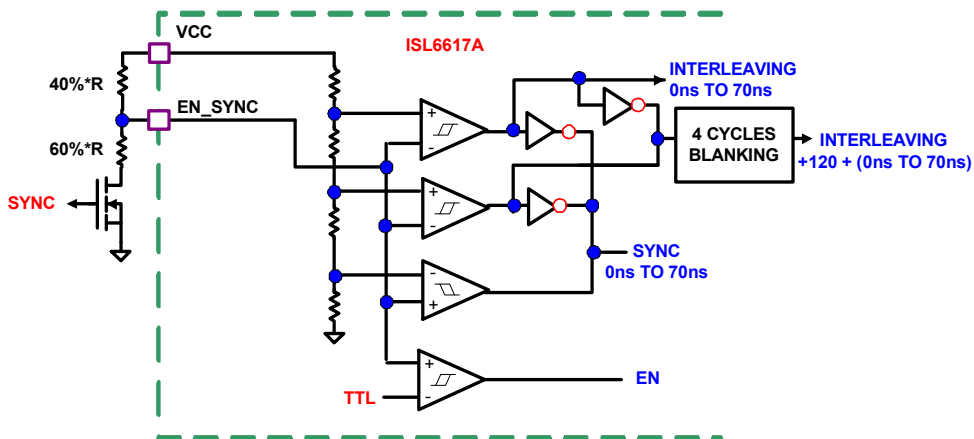
To transition between two different modes, the EN\_SYNC pin voltage level needs to be set accordingly. Figures 10 and 11 show an example of external circuits for mode transition between Synchronous mode and Interleaving #1 or #2 mode, respectively. The R should be less than 50kΩ to improve transition time.



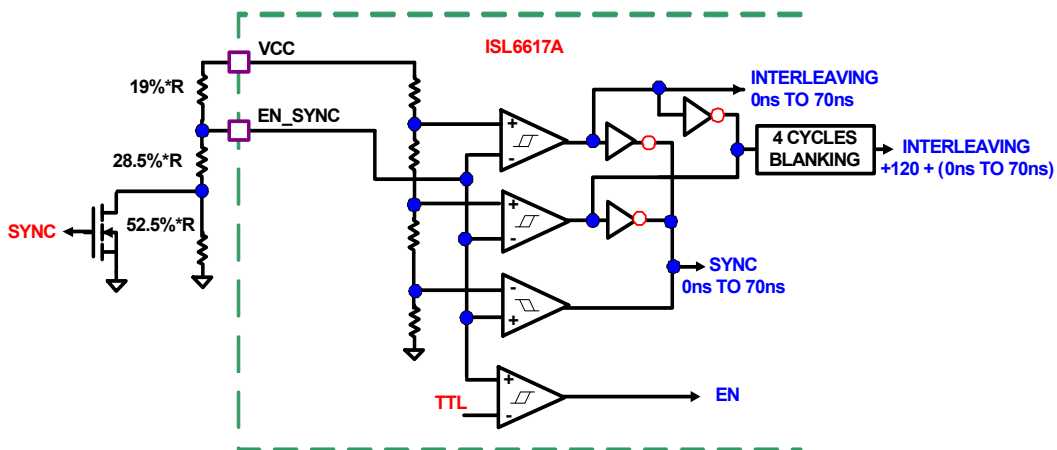
**FIGURE 8. INTERLEAVING MODE'S OPERATIONAL WAVEFORMS**  
( $EN_x = V_{CC}$ , OR  $81% \cdot V_{CC}$ )



**FIGURE 9. SYNCHRONOUS MODE'S OPERATIONAL WAVEFORMS**  
( $EN\_SYNC = 60% \cdot V_{CC}$ )



**FIGURE 10. CONFIGURATION FOR TRANSITION BETWEEN SYNCHRONOUS AND INTERLEAVING #1 MODES**



**FIGURE 11. CONFIGURATION FOR TRANSITION BETWEEN SYNCHRONOUS AND INTERLEAVING #2 MODES**

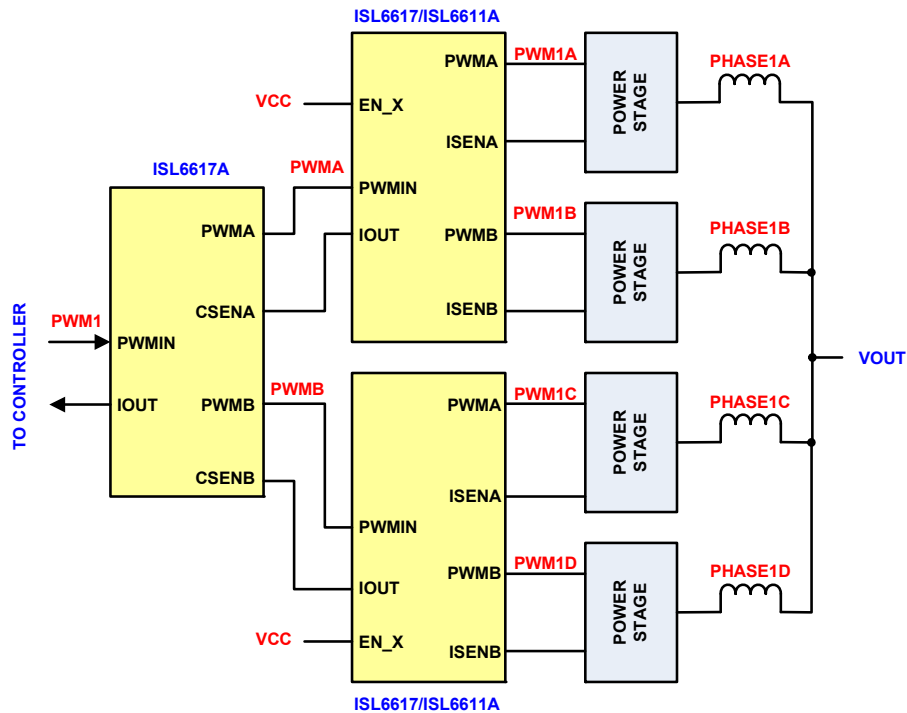


FIGURE 12. CASCADED PHASE DOUBLER SIMPLIFIED DIAGRAM

The ISL6617A can further be cascaded with ISL6617 or ISL6611A (phase doubler with integrated 5V drivers), as shown in Figure 12. This can quadruple the number of phases each PWM line can support. Figure 13 shows the operational waveforms of the cascaded doublers. The PWMIN pin of ISL6617 or ISL6611A will be pulled to VCC when it is disabled (EN\_x = Low). To avoid driving the PWM outputs of the 1st stage ISL6617A by the 2nd stage's PWMIN, the 2nd stage doubler's enable input should remain high, i.e., tied to VCC, as shown in Figure 12. Note that ISL6617A cannot cascade with itself and its PWMIN will not be pulled to VCC when EN\_x is disabled (Low).

To operate each phase at the switching frequency of  $f_{SW}$ , the operational frequency of the controller needs to be scaled accordingly for different modes, as shown in Table 2.

TABLE 2. CONTROLLER FREQUENCY AND MAXIMUM DUTY CYCLE

| OPERATIONAL MODES     | F <sub>CONTROLLER</sub> | ISL6617A MAXIMUM DUTY CYCLE PER PHASE |
|-----------------------|-------------------------|---------------------------------------|
| Interleaving          | 2 x $f_{SW}$            | 50%                                   |
| Synchronous           | $f_{SW}$                | 100%                                  |
| Cascaded Interleaving | 4 x $f_{SW}$            | 25%                                   |

When the doubler operates in Interleaving mode, the PWM controller frequency should be set at two times the desired phase frequency ( $f_{SW}$ ). Since the input PWM pulse is divided into half to feed into each phase of the doubler, the operational duty cycle of each phase should be less than 50%. In Synchronous mode, the PWM controller should be operated at the same frequency as the desired phase frequency. In this mode, the allowable duty cycle is up to 100%. For cascaded interleaving, the controller switching frequency needs to be set at four times the phase frequency. During cascaded operation, the maximum

allowable duty cycle will be less than 25%. All of the maximum allowable duty cycle numbers referenced assume that the PWM controller can send out a 100% duty cycle pulse. In many cases, this is not achievable because the controller needs time to reset its internal sawtooth ramp or internal max duty limit. However, the fixed 120ns extension of Interleaving mode #2 helps recover the typical 1% duty cycle loss associated with the ramp reset time.

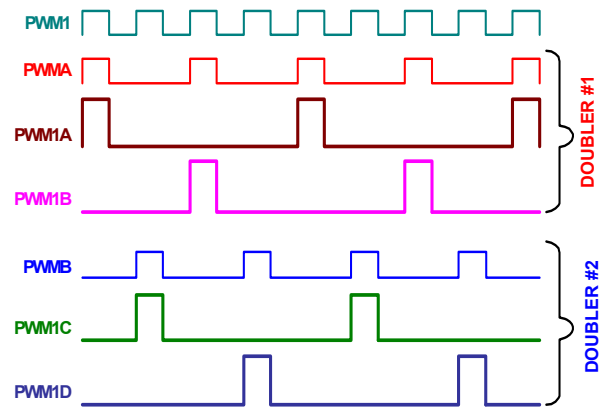


FIGURE 13. CASCADED DOUBLER OPERATIONAL WAVEFORMS

To properly compensate the system that uses phase doublers, the effective system sawtooth to calculate the modulator gain should factor in the duty cycle limitation ( $D_{MAX}$ ) as Equation 1. For instance, when using ISL6617A and ISL6617 in cascaded Interleaving mode, the effective sawtooth amplitude should be scaled as  $3V/22.5\% = 13.33V$ .

$$V_{RAMP\_EFFECTIVE} = \frac{V_{RAMP}}{D_{MAX}} \quad (EQ. 1)$$



## Current Balance and Current Monitoring

The sensed currents  $I_A$  and  $I_B$  from each respective channel are summed together and divided by 2. The resulting average current  $I_{AVG}$ , provides a measure of the total load current. Channel current balance is achieved by comparing the sensed current of each channel to the average current, to make an appropriate adjustment to the PWMA and PWMB duty cycle with Intersil's patented current-balance method.

Channel current balance is essential in achieving the thermal advantage of multiphase operation. With good current balance, the power loss is equally dissipated over multiple devices and a greater area.

The resulting average current  $I_{AVG}$ , also goes out from the IOOUT pin for current monitoring and can also be fed back to the controller's ISEN lines for current balance, load-line regulation, and overcurrent protection. For fast response to the current information, the IOOUT pin should have minimum decoupling; no more than 50ns filter is recommended. The full scale of IOOUT is 100 $\mu$ A; it typically should set resistor gain around 50 $\mu$ A to 80 $\mu$ A at the full load to ensure that it will not hit full scale prior to the overcurrent trip point. At the same time, the current signal accuracy is maximized.

## Benefits of a High Phase Count System

At heavy load condition, efficiency can be improved by spreading the load across many phases. This is primarily because the resistive loss becomes the dominant component of total loss budget at high current levels.

Since the load is carried by more phases, each power device handles less current. In addition, the devices are likely to be spread over a larger area on the Printed Circuit Board (PCB). Both these factors result in improved heat dissipation for higher phase count systems. By reducing the system's operating temperature, the reliability of the components is improved.

Furthermore, increasing the phase count also reduces the size of ripple on both the input and output currents. It reduces EMI and improves the efficiency. [Figures 16](#) and [17](#) show the ripple values for a 24-phase voltage regulator with the following parameters:

- Input voltage: 12V
- Output voltage: 1.6V
- Duty cycle: 13.3%
- Load current: 200A
- Output phase inductor: 500nH
- Phase switching frequency: 200kHz

In this example, the 24-phase Voltage Regulator (VR) can run in 6-phase, 8-phase, 12-phase, or 24-phase Interleaving mode. In 6-phase Interleaving mode, every four phases run synchronously, which yields 18.73A and 12.93A input and output ripple currents, respectively. The 24-phase interleaving regulator significantly drops these values to 4.05A and 0.78A, respectively. As shown in [Table 3](#), both input and output ripple currents are reduced when more phases are running in Interleaving mode. Note that the 8-phase VR has lower output ripple current than the 12-phase VR since the 8-phase VR has better output ripple cancellation factor close to the duty cycle of 1/8.

TABLE 3. RIPPLE CURRENT (UNIT: A)

| INTERLEAVED PHASES    | 6     | 8     | 12   | 24   |
|-----------------------|-------|-------|------|------|
| Input Ripple Current  | 18.73 | 11.64 | 8.79 | 4.05 |
| Output Ripple Current | 12.93 | 2.70  | 4.83 | 0.78 |

[Figure 18](#) shows the efficiency of a 12-phase VR design, which runs the doubler in Interleaving and Synchronous modes. For comparison, a 6-phase VR with the same number of MOSFETs and inductors is also plotted, clearly demonstrating the efficiency improvement of a high-phase count system and Interleaving mode over Synchronous mode resulting from the better ripple cancellation.

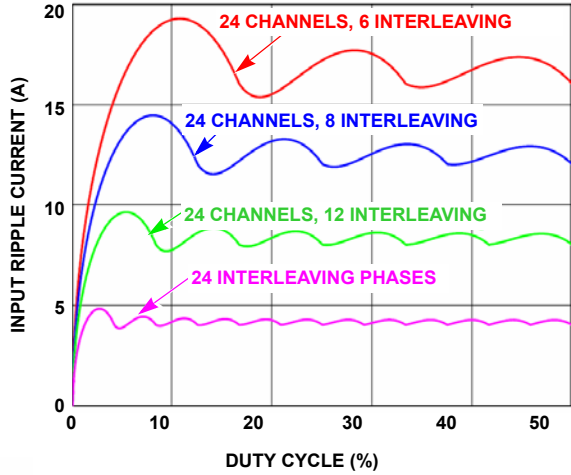


FIGURE 16. INPUT CURRENT RIPPLE vs DUTY CYCLE, PHASE COUNT



FIGURE 17. OUTPUT CURRENT RIPPLE vs DUTY CYCLE, PHASE COUNT

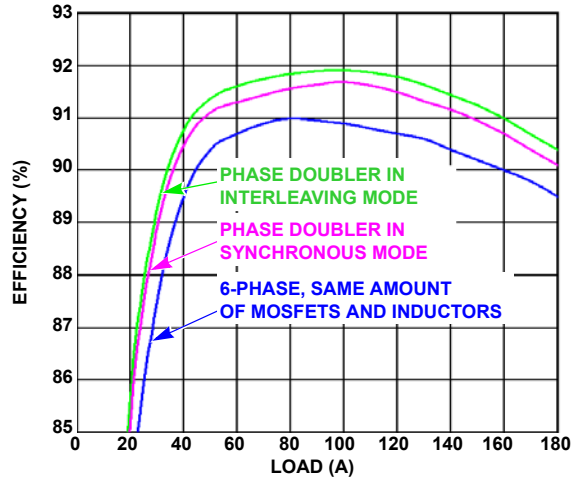


FIGURE 18. EFFICIENCY COMPARISON IN 12-PHASE DESIGN

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest Rev.

| DATE              | REVISION | CHANGE   |
|-------------------|----------|--|
| Jun 9, 2017       | FN7844.2 | Added Features bullet "Compatible with DCR Sensing or Smart Power Stage Sensing" on first page.<br>"Phase Doubler Selection Guide" table on page 1 - added "ISL691x7, ISL691x4, ISL691x8, ISL681x7, ISL681x4, and ISL6388/98 on ISL6617A row.<br>Added "Typical Application I with SPS sensing" on page 4.<br>Modified "Typical Applications II and III (on page 5 and page 6).<br>Updated About Intersil. |
| December 20, 2016 | FN7844.1 | Updated first page Table<br>Updated Notes 1 & 3 of Ordering Info table on page 2.<br>Updated POD from rev 10 to rev 11. Changes were:<br>Tiebar Note 4 updated<br>From: Tiebar shown (if present) is a non-functional feature.<br>To: Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).  |
| December 19, 2014 | FN7844.0 | Initial Release  |

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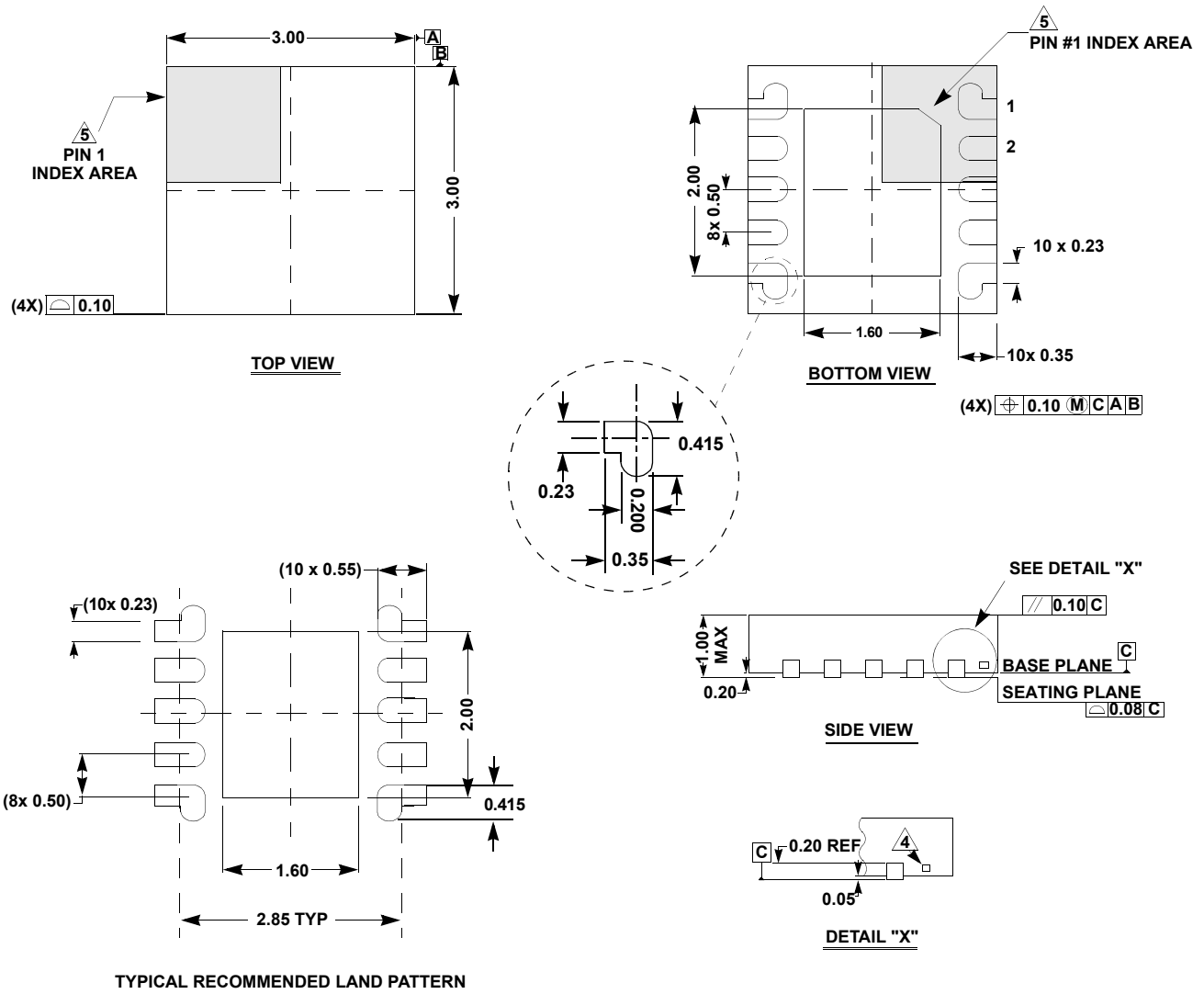
# Package Outline Drawing

For the most recent package outline drawing, see [L10.3x3](#).

## L10.3x3

10 LEAD DUAL FLAT PACKAGE (DFN)

Rev 11, 3/15



**NOTES:**

1. Dimensions are in millimeters.  
Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal  $\pm 0.05$
4. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.



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