MAX155/MAX156

8-/4-Channel ADCs with Simultaneous T/Hs and Reference

General Description

The MAX155/MAX156 are high-speed, 8-bit, multichannel analog-to-digital converters (ADCs) with simultaneous track/holds (T/Hs) to eliminate timing differences between input channel samples. The MAX155 has 8 analog input channels and the MAX156 has 4 analog input channels. Each channel has its own T/H, and all T/Hs sample at the same instant. The ADC converts a channel in 3.6µs and stores the result in an internal 8x8 RAM. The MAX155/MAX156 also feature a 2.5V internal reference and power-down capability, providing a complete, sampling data-acquisition system.

When operating from a single +5V supply, the MAX155/MAX156 perform either unipolar or bipolar, single-ended or differential conversions. For applications requiring wider dynamic range or bipolar conversions around ground, the V_{SS} supply pin may be connected to -5V.

Conversions are initiated with a pulse to the $\overline{WR}$ pin, and data is accessed from the ADC's RAM with a pulse to the $\overline{RD}$ pin. A bidirectional interface updates the channel configuration and provides output data. The ADC may also be wired for output-only operation.The MAX155 comes in 28-pin PDIP and wide SO packages, and the MAX156 comes in 24-pin narrow PDIP and 28-pin wide SO packages.

Features

- 8 Simultaneously Sampling Track/Hold Inputs
- 3.6µs Conversion Time Per Channel
- Unipolar or Bipolar Input Range
- Single-Ended or Differential Inputs
- Mixed Input Configurations Possible
- 2.5V Internal Reference
- Single +5V or Dual ±5V Supply Operation

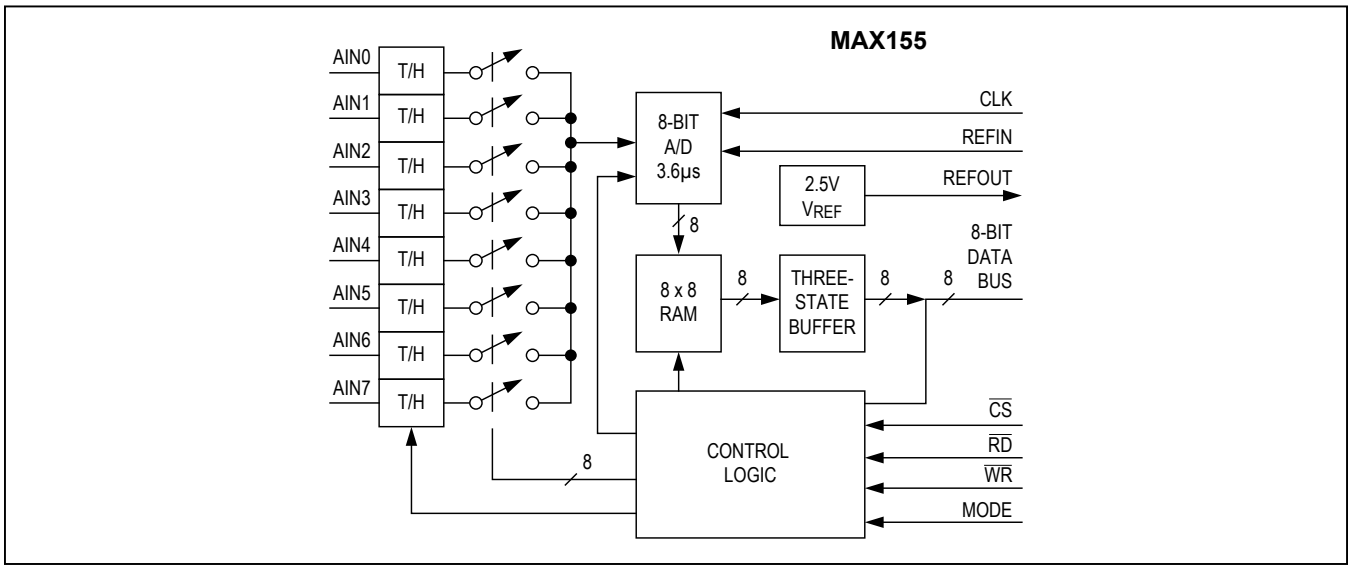
Applications

- Phase-Sensitive Data Acquisition
- Vibration and Waveform Analysis
- DSP Analog Input
- AC Power Meters
- Portable Data Loggers

***Ordering Information* appears at end of data sheet.**

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX155.related.

Functional Diagram



Absolute Maximum Ratings

V_{DD} to AGND ..... -0.3V, +6V
V_{DD} to DGND ..... -0.3V, +6V
AGND to DGND ..... -0.3V, (V_{DD} + 0.3V)
V_{SS} to AGND ..... +0.3V, -6V
V_{SS} to DGND ..... +0.3V, -6V
$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, CLK, MODE to DGND ..... -0.3V, (V_{DD} + 0 3V)
BUSY, D0–D7 to DGND ..... -0.3V, (V_{DD} + 0 3V)
REFOUT to AGND ..... -0.3V, (V_{DD} + 0 3V)
REFIN to AGND ..... -0.3V, (V_{DD} + 0 3V)
AIN to AGND ..... (V_{SS} - 0.3V), (V_{DD} + 0 3V)
Output Current (REFOUT) 30mA

Continuous Power Dissipation (T_A = +70°C)
24-Pin PDIP (derate 8.7mW/°C above +70°C) 696mW
28-Pin PDIP (derate 9.09mW/°C above +70°C) 727mW
28-Pin Wide SO (derate 12.5mW/°C above +70°C) .. 1000mW
Operating Temperature Ranges:
MAX155/MAX156_C_ _ ..... 0°C to +70°C
MAX155/MAX156_E_ _ ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{DD} = +5V, V_{REFIN} = +2.5V. External Reference, V_{AGND} = V_{DGND} = 0V, V_{SS} = 0V or -5V, f_{CLK} = 5MHz external, Unipolar range single-ended mode, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY (Note 1)							
Resolution				8			Bits
Integral Linearity Error		MAX15_A				±½	LSB
		MAX15_B				±1	
No Missing Codes Resolution		Guaranteed monotonic		8			Bits
Offset Error (Unipolar)		MAX15_A				±½	LSB
		MAX15_B				±1	
Offset Error (Bipolar)		MAX15_A				±1	LSB
		MAX15_B				±2	
Gain Error		Unipolar	MAX15_A			±1	LSB
			MAX15_B			±1	
		Bipolar	MAX15_A			±1	
			MAX15_B			±2	
Channel-to-Channel Matching		MAX15_A			±½		LSB
		MAX15_B			±1		
DYNAMIC PERFORMANCE (V_{IN} = 50kHz, 2.5V_{P-P} sine wave sampled at 220ksps)							
Signal-to-Noise and Distortion Ratio	SINAD	MAX15_A			48		dB
		MAX15_B			47		
Total Harmonic Distortion	THD				-60		dB
Spurious-Free Dynamic Range	SFDR				-62		dB
Small-Signal Bandwidth					4		MHz
Aperture Delay					20		ns
Aperture Delay Matching (Note 2)						4	ns

Electrical Characteristics (continued)

(V_{DD} = +5V, V_{REFIN} = +2.5V. External Reference, V_{AGND} = V_{DGND} = 0V, V_{SS} = 0V or -5V, f_{CLK} = 5MHz external, Unipolar range single-ended mode, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG INPUT							
Voltage Range, Unipolar, Single-Ended		AIN_(+) to AGND		0		V_{REF}	V
Unipolar Differential		AIN_(+) to AIN_(-)		0		V_{REF}	
Bipolar, Single-Ended		AIN_(+) to AGND		$-V_{REF}$		V_{REF}	
Bipolar, Differential		AIN_(+) to AIN_(-)		$-V_{REF}$		V_{REF}	
Common-Mode Range		Differential mode		V_{SS}		V_{DD}	
DC Input Impedance		AIN = V_{DD}		10			MΩ
REFERENCE INPUT							
REFIN Range (For Specified Performance) (Note 2)				2.375	2.500	2.625	V
I_{REF}		V_{REFIN} = 2.5V				1	mA
REFERENCE OUTPUT (C_L = 4.7µF)							
Output Voltage		I_L = 0mA	T_A = +25°C	2.44	2.50	2.56	V
			T_A = T_{MIN} to T_{MAX}	2.38	2.50	2.62	
Load Regulation		T_A = +25°C, I_{OUT} = 0 to 10mA				-10	mV
Power-Supply Sensitivity		T_A = +25°C, V_{DD} = 5V ±5%			±1	±3	mV
Temperature Drift					±100		ppm/°C
LOGIC INPUTS (Mode = Open Circuit)							
$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, CLK, D0–D7 (When Inputs) Input Low Voltage	V_{IL}					0.8	V
Input High Voltage	V_{IH}			2.4			V
Input Current	I_{IN}					±10	µA
Input Capacitance (Note 2)	C_{IN}					15	pF
MODE							
Input Low Voltage	V_{IL}					0.5	V
Input High Voltage	V_{IH}			V_{DD} - 0.5			V
Input Midlevel Voltage	V_{MID}			$V_{DD}/2$ - 0.5		$V_{DD}/2$ + 0.5	V
Input Floating Voltage	V_{FLT}				$V_{DD}/2$		V
Input Current	I_{IN}				±50	±100	µA

Electrical Characteristics (continued)

(V_{DD} = +5V, V_{REFIN} = +2.5V. External Reference, V_{AGND} = V_{DGND} = 0V, V_{SS} = 0V or -5V, f_{CLK} = 5MHz external, Unipolar range single-ended mode, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC OUTPUTS							
BUSY, D0–D7 Output Low Voltage	V_{OL}	I_{OUT} = 1.6mA				0.4	V
Output High Voltage	V_{OH}	I_{OUT} = -360µA		4			V
D0–D7 Floating State Leakage						±10	µA
Floating State Output Capacitance (Note 2)	C_{OUT}					15	pF
Conversion Time		f_{CLK} = 5MHz, single channel		3.6		3.8	µs
POWER REQUIREMENTS							
Positive Power-Supply Voltage	V_{DD}			4.75		5.25	V
Positive Power-Supply Current	I_{DD}	PD = 0	MAX155		18	24	mA
			MAX156		9	12	
		PD = 1	CLK, $\overline{CS}$, $\overline{WR}$, RD = 0V or V_{DD}; D_{OUT} = 0V or V_{DD}		25	100	µA
Negative Power-Supply Voltage	V_{SS}			0		-5	V
Negative Power-Supply Current	I_{SS}	PD = 0			2	50	µA
		PD = 1			2	50	
Power-Supply Rejection (Change in Full-Scale Error)		V_{DD} = 5V ±5%, V_{SS} = 0V			±0.1	±0.25	LSB
		V_{DD} = 5V, V_{SS} = -5V ±5%			±0.1		

TIMING CHARACTERISTICS (Note 3, Figures 1–7)

(V_{DD} = +5V, V_{REFIN} = +2.5V. External Reference, V_{AGND} = V_{DGND} = 0V, V_{SS} = 0V or -5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ to $\overline{WR}$ Setup Time	t_{CWS}		0			ns
$\overline{CS}$ to $\overline{WR}$ Hold Time	t_{CWH}		0			ns
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_{CRS}		0			ns
$\overline{CS}$ to $\overline{RD}$ Hold Time (Note 2)	t_{CRH}		0			ns
$\overline{WR}$ Low Pulse Width	t_{WR}	MAX15_C/E	100		2000	ns
$\overline{RD}$ Low Pulse Width	t_{RDL}	MAX15_C/E	100			ns
$\overline{RD}$ High Pulse Width (Note 2)	t_{RDH}	MAX15_C/E	180			ns
$\overline{WR}$ to $\overline{RD}$ Delay (Note 2)	t_{WRD}	MAX15_C/E	280			ns
$\overline{WR}$ to $\overline{BUSY}$ Low Delay	t_{WBD}	MAX15_C/E			220	ns

TIMING CHARACTERISTICS (Note 3, Figures 1-7) (continued)

(V_{DD} = +5V, V_{REFIN} = +2.5V. External Reference, V_{AGND} = V_{DGND} = 0V, V_{SS} = 0V or -5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{BUSY}$ High to $\overline{WR}$ Delay (to update configuration register) (Notes 2, 3)	t_{BWD}		50			ns
CLK to $\overline{WR}$ Delay (Acquisition Time) (Note 2)	t_{ACQ}		800			ns
$\overline{BUSY}$ High to $\overline{RD}$ Delay (Notes 2, 3)	t_{BRD}		50			ns
Address-Setup Time	t_{AS}		120			ns
Address-Hold Time	t_{AH}		0			ns
$\overline{RD}$ to Data Valid (Note 4)	t_{DV}	MAX15_C/E	100			ns
$\overline{RD}$ to Data Three-State Output (Note 5)	t_{TR}	MAX15_C/E	80			ns
CLK to $\overline{BUSY}$ Delay (Note 2)	t_{CB}			100	300	ns
CLK Frequency			0.5		5.0	MHz

Note 1: V_{DD} = +5V, V_{REFIN} = +2.5V, V_{SS} = 0V. Performance at ±5% power-supply tolerance is guaranteed by Power-Supply Rejection test.
Note 2: Guaranteed by design, not production tested.
Note 3: All input control signals are specified with t_r = t_f = 20ns (10% to 90% of +5V) and timed from a +1.6V voltage level. Output signals are timed from V_{OH} and V_{OL}.
Note 4: t_{DV} is the time required for an output to cross +0.8V or +2.4V measured with load circuit of Figure 1.
Note 5: t_{TR} is the time required for the data lines to change 0.5V, measured with load circuits of Figure 2.

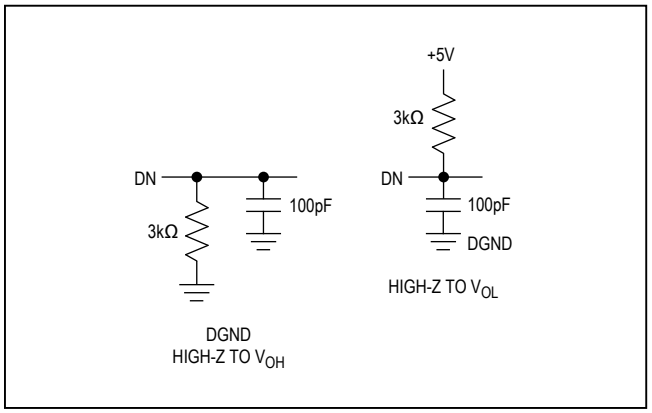


Figure 1. Load Circuits for Data-Access Timing

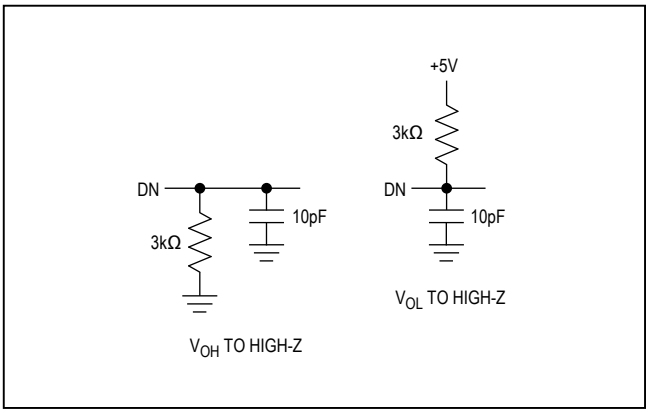


Figure 2. Load Circuits for Three-State Output Timing

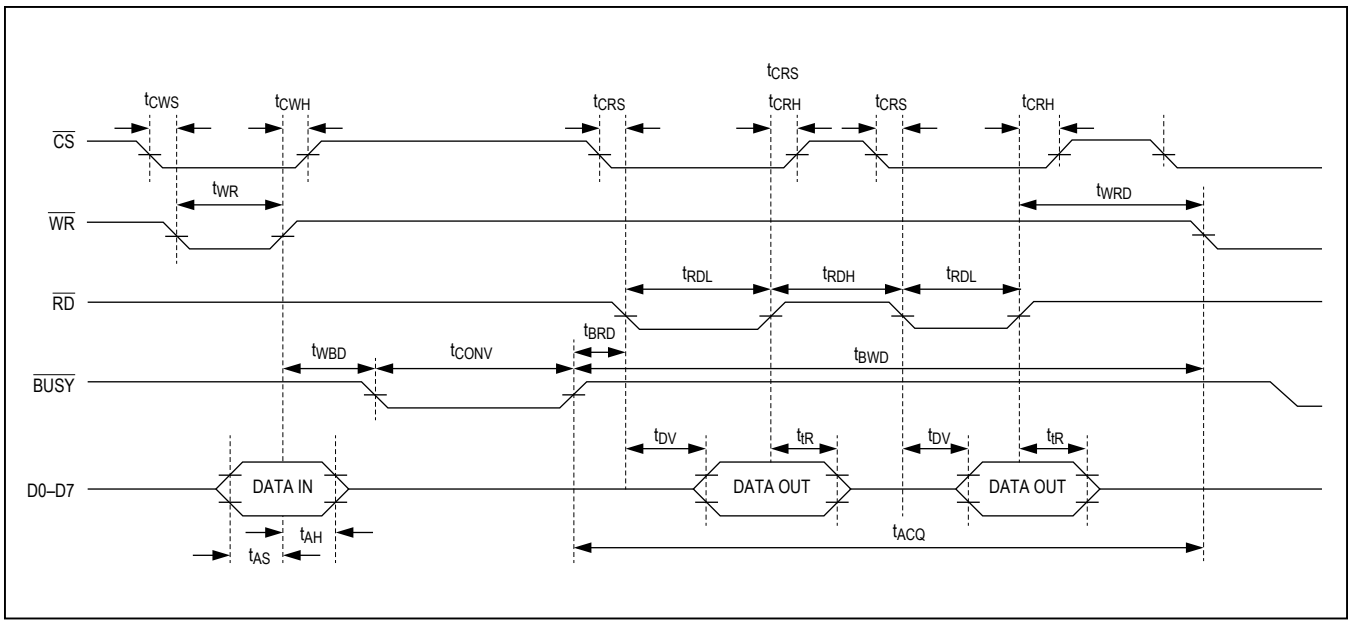
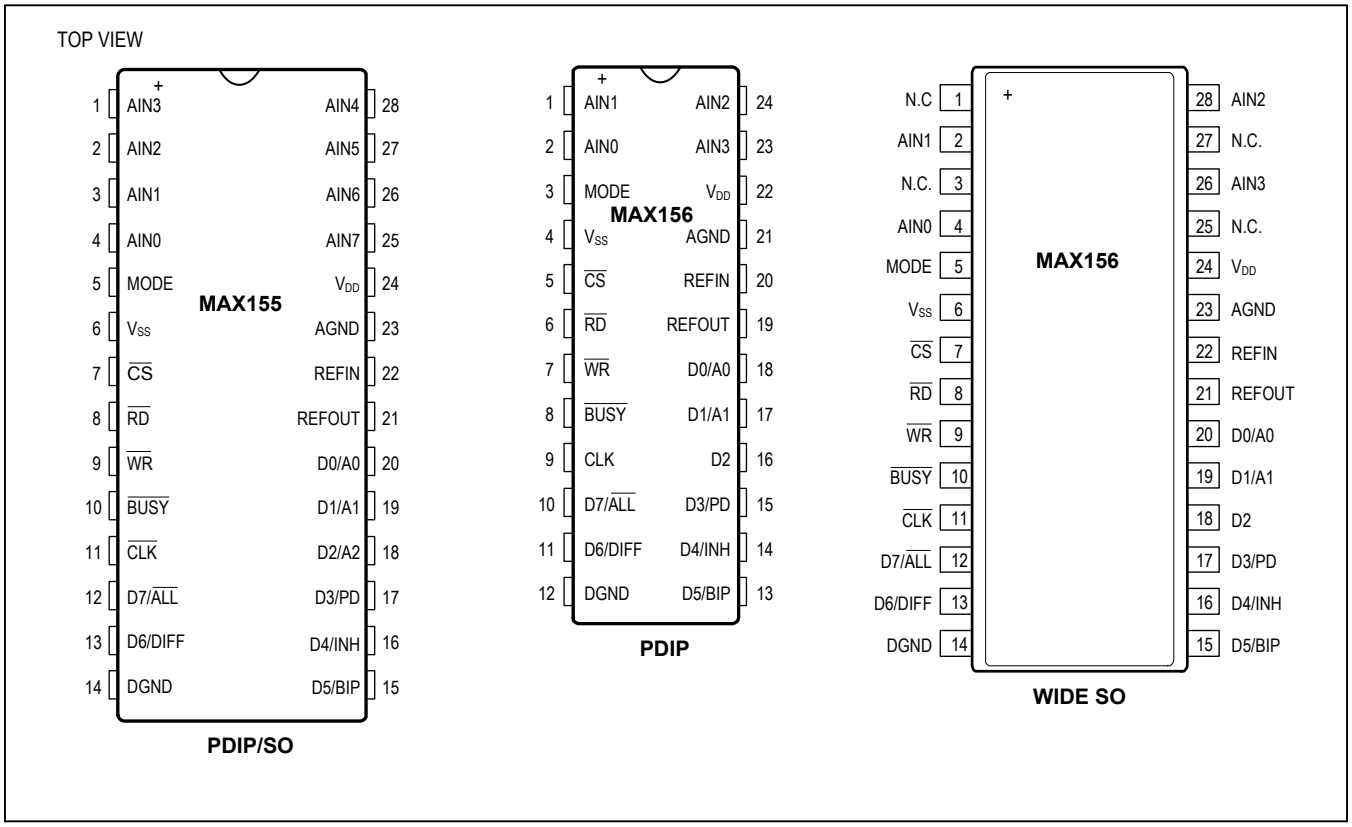


Figure 3. Write and Read Timing

Pin Configuration



Pin Description

PIN			NAME	FUNCTION
MAX155	MAX156			
PDIP/SO	PDIP	SO		
1	23	26	AIN3	Sampling Analog Input, Channel 3
2	24	28	AIN2	Sampling Analog Input, Channel 2
3	1	2	AIN1	Sampling Analog Input, Channel 1
4	2	4	AIN0	Sampling Analog Input, Channel 0
5	3	5	MODE	Mode configures multiplexer and converter. See Table 4.
6	4	6	V_{SS}	Negative Supply. Power V_{SS} with -5V for extended input range.
7	5	7	CS	$\overline{\text{CHIP SELECT}}$ Input must be low for the ADC to recognize $\overline{\text{RD}}$, or $\overline{\text{WR}}$
8	6	8	RD	$\overline{\text{READ}}$ Input reads data sequentially from RAM
9	7	9	WR	$\overline{\text{WRITE}}$ Input's rising edge initiates conversion and updates channel configuration register. Falling edge samples inputs.
10	8	10	BUSY	$\overline{\text{BUSY}}$ Output low when conversion is in progress
11	9	11	CLK	External Clock Input
12	10	12	D7/ALL	Three-State Data Output Bit 7 (MSB)/Sequential or Specific Conversion
13	11	13	D6/DIFF	Three-State Data Output Bit 6/Single-Ended/Differential Select
14	12	14	DGND	Digital Ground
15	13	15	D5/BIP	Three-State Data Output Bit 5/Unipolar/Bipolar Conversion
16	14	16	D4/INH	Three-State Data Output Bit 4/Inhibit Conversion Input
17	15	17	D3/PD	Three-State Data Output Bit 3/Power-Down Input
18	16	18	D2/A2	Three-State Data Output Bit 2/RAM Address Bit A2 (MAX155 Only)
19	17	19	D1/A1	Three-State Data Output Bit 1/RAM Address Bit A1
20	18	20	D0/A0	Three-State Data Output Bit 0/RAM Address Bit A0
21	19	21	REFOUT	Reference Output, +2.5V
22	20	22	REFIN	Reference Input, +2.5 Normally
23	21	23	AGND	Analog Ground
24	22	24	V_{DD}	Power-Supply Voltage, +5V Normally
25–28	—	—	AIN7–4	Sampling Analog Input, Channels 7–4
—	—	1, 3, 25, 27	N.C.	No Connection. No internal connection—pin unconnected.

Detailed Description

ADC Operation

The MAX155/MAX156 contain a 3.6µs successive approximation ADC and 8/4 track-and-hold (T/H) inputs. When a conversion is started, all AIN inputs are simultaneously sampled. All channels sample whether or not they are selected for the conversion. Either a single-channel or multichannel conversion may be requested and channel configurations may be mixed, ADC results are then stored in an internal RAM.

In hard-wired mode (see the *Multiplexer and AID Configurations* section) multichannel conversions are initiated with one write operation. In input/output (I/O) mode, multichannel configurations are set up prior to the conversion by loading channel selections into the configuration register. This register also selects single-ended/differential, unipolar/bipolar (Figure 9), power-down, and other functions. Each channel selection requires a separate write operation (i.e. 8 writes for 8 channels), but only after power-up. Once the desired channel arrangement is loaded, each subsequent write converts all selected channels without reconfiguring the multiplexer (mux). I/O mode requires more write operations, but provides more flexibility than hard-wired mode.

To access conversion results, successive $\overline{RD}$ pulses automatically sence through RAM, beginning with channel 0. Each $\overline{RD}$ pulse increments the RAM address counter, which resets to 0 when $\overline{WR}$ goes low in multi channel conversions. An arbitrary RAM location may also be read by writing a 1 to INH while loading the RAM address (A0–A2), and then performing a read operation.

Table 1. Multiplexer Configurations

PIN	NAME	FUNCTION
D0/A0 D1/A1 D2/A2	1 or 0	A0–A2 select a multiple channel for the configurations described below, or select a RAM address for reading with a subsequent $\overline{RD}$.
D3/PD	0	Normal ADC operation
	1	Power-down reduces the power-supply current. Configuration data may be loaded and is maintained during power-down.
D4/INH	0	A conversion starts when $\overline{WR}$ goes high
	1	Inhibits the conversion when $\overline{WR}$ goes high. Allows mux configuration to be loaded and RAM locations to be accessed without starting a conversion.
D5/BIP**	0	Unipolar conversion (Figure 9a) for the channel specified by A0–A2. Input range = 0V to V_{REF}.
	1	Bipolar conversion (Figure 9b) for the channel specified by A0–A2. Input range = ±V_{REF}.
D6/DIFF**	0	Single-ended configuration for the channel specified by A0–A2 as described in Table 2
	1	Differential contiguration for the channel specified by A0–A2 as described in Table 2
D7/$\overline{ALL}$	0	All previously configured channels are converted. Data is read with consecutive $\overline{RD}$ pulses, beginning with the lowest configured channel.
	1	Only the channel specified by A2–A0 is converted. A single $\overline{RD}$ pulse reads the result of that conversion.

•Configuration inputs are shared with data outputs D0-D7. The functions of D0-D7 are not described in this table.

••DIFF and BIP are not implemented on the current conversion, but go into effect on the.following conversion.

Multiplexer and A/D Configuration

A conversion is started with a $\overline{WR}$ pulse. All channels sample on $\overline{WR}$'s falling edge. Mux configuration data is loaded on $\overline{WR}$'s rising edge. In I/O mode (MODE = Open Circuit), selections for channel number, single or multi-channel conversion, unipolar or bipolar input, and single-ended or differential input are made with A0-A2, $\overline{ALL}$, BIP, and DIFF (Table 1). These input pins are also shared with the RAM data outputs D0–D7. An alternate, simpler interface is provided by the hard-wired mode, which selects some general mux configurations without requiring ADC programming. Hard-wired connections of MODE and V_{SS} select from 4 mux configurations as listed in Table 4 (see the *Hard-Wired Mode* section).

On the rising edge of $\overline{WR}$, the mux configuration register is updated; falling edge initiates sampling of all inputs. A channel selection can be implemented on the current conversion, but changes from unipolar to bipolar (with BIP) or from singleended to differential operation (with DIFF) do not go into effect until the following $\overline{WR}$. This can be overcome by writing to the configuration register while inhibiting the conversion (INH = 1), or by changing DIFF and BIP one conversion early, i.e. on the previous write.

Table 2. Single-Ended Channel Selection (MODE = Open Circuit)

MUX ADDRESS				SINGLE-ENDED CHANNEL SELECTION								
A0	**A1**	**A2**	**DIFF**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**AGND**
0	0	0	0	+								-
1	0	0	0		+							-
0	1	0	0			+						-
1	1	0	0				+					-
0	0	1	0					+				-
1	0	1	0						+			-
0	1	1	0							+		-
1	1	1	0								+	-

Note: *Shaded areas represent MAX156 operation.*

Table 3. Differential Channel Selection (MODE = Open Circuit)

MUX ADDRESS				DIFFERENTIAL CHANNEL SELECTION							
A0	**A1**	**A2**	**DIFF**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
0	0	0	1	+	-						
0	1	0	1			+	-				
0	0	1	1					+	-		
0	1	1	1							+	-
1	0	0	1	-	+						
1	1	0	1			-	+				
1	0	1	1					-	+		
1	1	1	1							-	+

Note: *Shaded areas represent MAX156 operation.*

Interface Timing

Input/Output Mode, Multichannel Conversion Timing

I/O mode is selected when the MODE input is open circuit. In I/O mode, the mux configuration register determines the conversion type. The register is updated on the rising edge of $\overline{WR}$.

Table 1 lists all conversion options. For example, at D6/DIFF, a logic 0 or 1 selects a single-ended or differential conversion. Data is loaded into addressed locations in the configuration register with a series of $\overline{WR}$ pulses. If INH is high while writing, no conversion takes place. A conversion is started by writing INH = 0 to the configuration register. When a change is made to the contents of the configuration register, a “dummy” conversion may be necessary. This is due to a built-in latency of one full conversion for unipolar/bipolar and single-ended/differential selections.

It is not necessary to update the configuration register before every conversion. A particular mux configuration must be loaded only once after power-up (but the configuration may require several writes to be loaded). A mux configuration is retained for successive conversions and during power-down (PD = 1) so that reconfiguring is unnecessary when the ADC returns to normal operation (PD = 0). Configuration and RAM data is lost only when power is removed from the ADC at V_{DD}.

When updating the configuration register, INH should be high for all except the last $\overline{WR}$ so the conversion is not started until the mux is set. On $\overline{WR}$’s falling edge, all input channels sample simultaneously. $\overline{BUSY}$ goes low at the beginning of the conversion, and channels are converted sequentially starting with the lowest selected channel. When $\overline{BUSY}$ goes high, conversion results are stored in RAM. At conversion end, a microprocessor (µP) can access the RAM contents with consecutive $\overline{RD}$ pulses. The first accessed data is the lowest channel’s result.

Subsequent $\overline{RD}$ pulses access conversion results for the remaining channels.

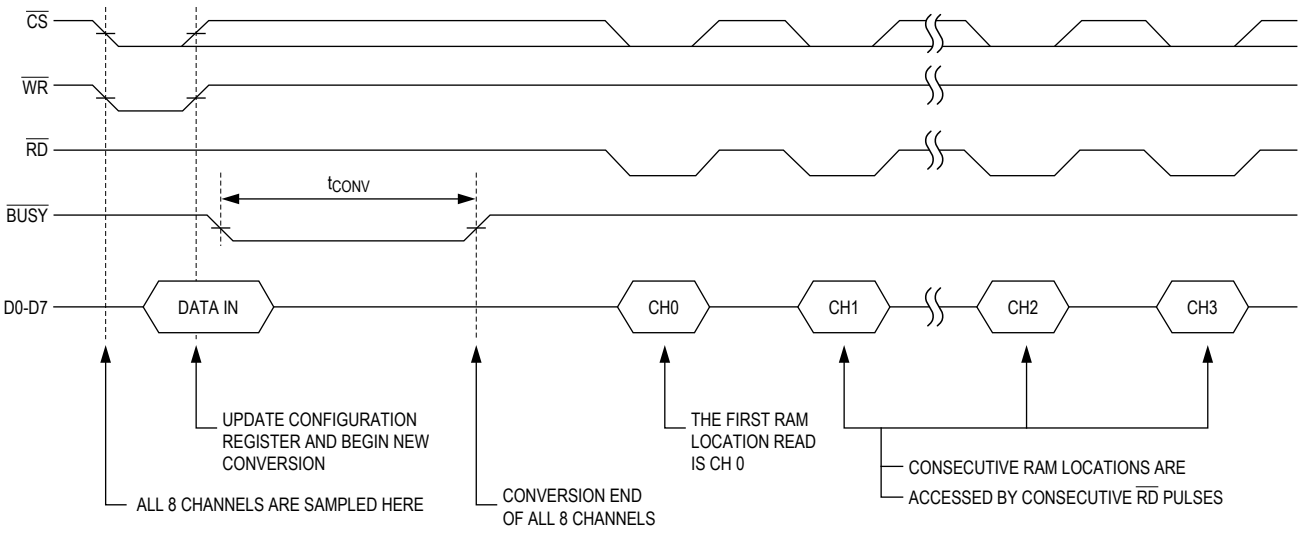
The configuration data determines which RAM locations are sequentially read by consecutive $\overline{RD}$ pulses, so new data should be placed in the configuration register only after a full $\overline{RD}$ operation. It is not necessary to update the configuration register for every conversion. A new conversion is initiated with a $\overline{WR}$ pulse (when INH = 0), regardless of the number of channe ls that have been read.

Figure 4a shows the MAX155 timing for an 8-channel unipolar configuration. 8 channels are configured and 8 consecutive $\overline{RD}$ pulses access data. Figure 4b illustrates 4-channel differential conversion timing involving 4 sampled channels and 4 $\overline{RD}$ pulses. In cases where conflicting differential configurations are loaded, the last channel selected with DIFF = 1 will be the positive input of the differential channel.

Input/Output Mode, Single-Channel Conversion Timing

Figure 5a shows timing for a single-channel ($\overline{ALL}$ = 1), single-ended conversion; Figure 5b shows a differential conversion. With MODE floating, the configuration register is updated on the rising edge of $\overline{WR}$. $\overline{BUSY}$ goes low at the beginning of the conversion and returns high when the channel designated by the configuration register has been converted. All channels are sampled on the falling edge of $\overline{WR}$ even if only a single channel has been requested. At conversion end, the µP can read the result for the selected channel with a single $\overline{RD}$ pulse. Subsequent $\overline{RD}$ pulses will access old conversion results remaining in other RAM locations. The next conversion is initiated with a $\overline{WR}$ pulse, regardless of the number of channels that have been read.

INH and A0–A2, in the configuration register, access locations in RAM. INH = 1 allows the RAM address pointer to be updated without starting a conversion. A $\overline{READ}$ pulse then reads the contents of the addressed location.



NOTE: After power-up, and prior to the above timing sequence, all single-ended channels must be set up by writing the following data into the configuration register. 8 WRs (see Figure 3) are needed for 8 channels:

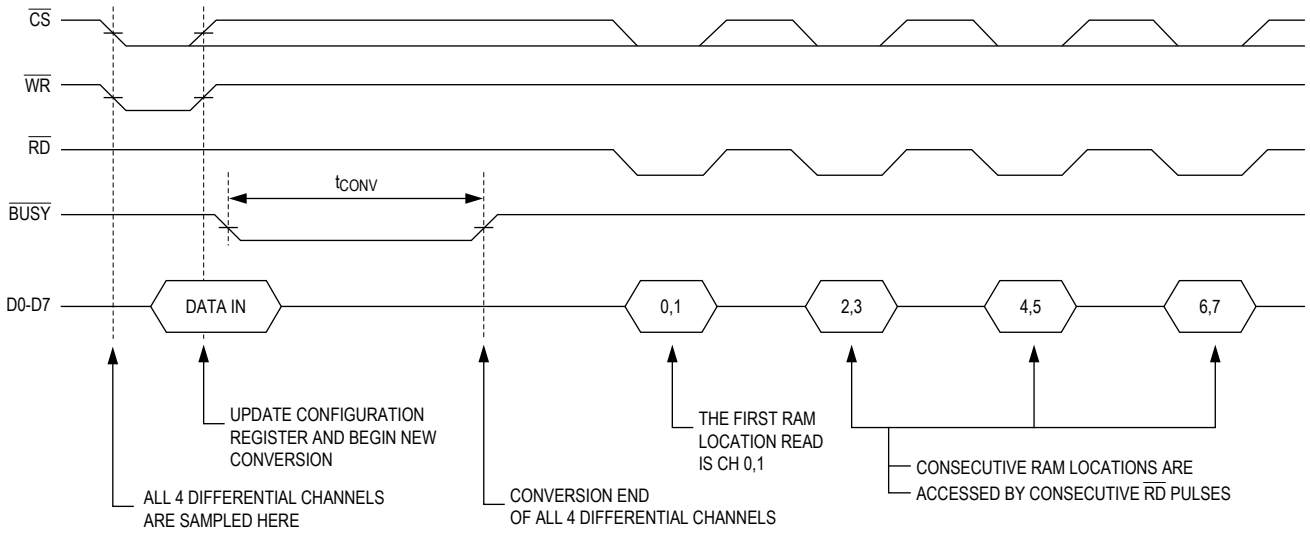
A0	A1	A2	PD	INH	BIP	DIFF	ALL
0	0	0	0	1	S	0	0
1	0	0	0	1	S	0	0
0	1	0	0	1	S	0	0
1	1	0	0	1	S	0	0
0	0	1	0	1	S	0	0
1	0	1	0	1	S	0	0
0	1	1	0	1	S	0	0
1	1	1	0	1	S	0	0

S = May be selected

Once the above data is loaded, all channels are converted with a single WR to any address (this is where the above timing diagram begins). With INH = 0, and ALL = 0:

A0	A1	A2	PD	INH	BIP	DIFF	ALL
0	0	0	0	0	S	0	0

Figure 4a. Input/Output Mode Timing–Eight Single-Ended Conversions



NOTE: After power-up, and prior to the above timing sequence, all differential channels must be set up by writing to the configuration register. (AIN0, 2, 4, 6 are +, and AIN1, 3, 5, 7 are - for this example). 4 $\overline{WR}$s (see Figure 3) are needed for 8 channels:

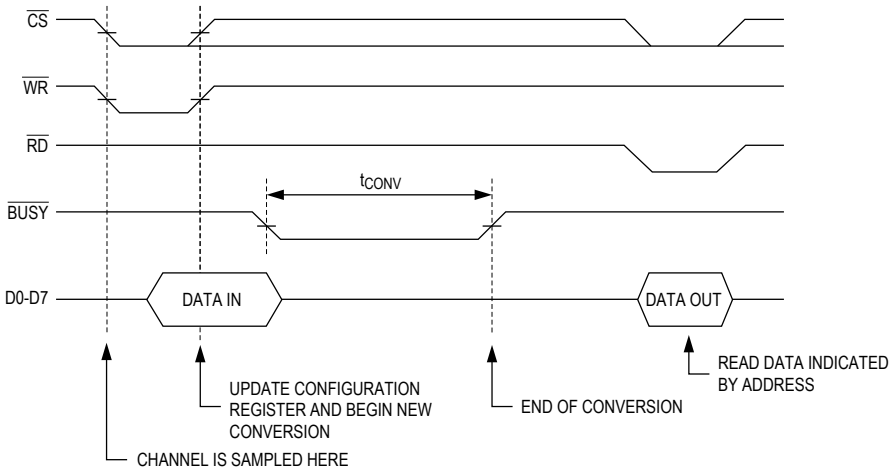
A0	A1	A2	PD	INH	BIP	DIFF	$\overline{ALL}$
0	0	0	0	1	S	0	0
1	1	0	0	1	S	0	0
0	0	1	0	1	S	0	0
1	1	1	0	1	S	0	0

S = May be selected

Once the above data is loaded, all channels are converted with a single $\overline{WR}$ to any address (this is where the above timing diagram begins). With INH = 0, and $\overline{ALL}$ = 0:

A0	A1	A2	PD	INH	BIP	DIFF	$\overline{ALL}$
0	0	0	0	0	S	0	0

Figure 4b. Input/Output Mode Timing–Four Differential Conversions

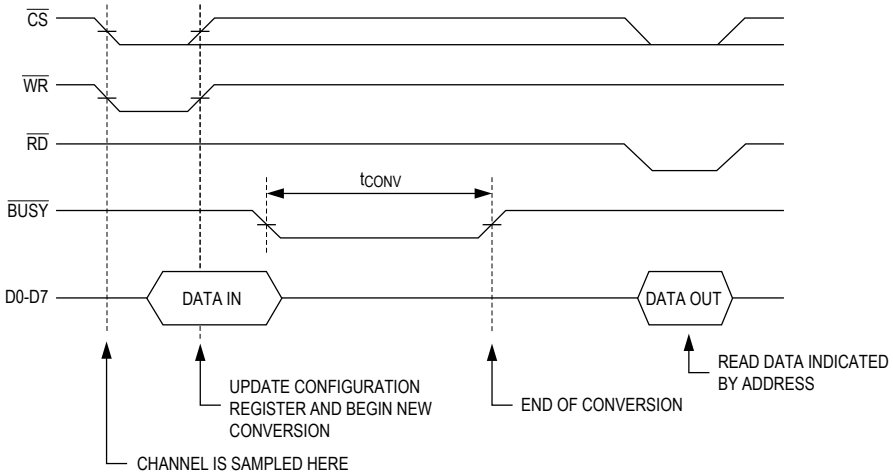


NOTE: A single-ended channel is converted by writing the following data into the configuration register (see Figure 3) The BIP and DIFF bits are not implemented until the next $\overline{WR}$

A0	A1	A2	PD	INH	BIP	DIFF	$\overline{ALL}$
S	S	S	0	0	S	0	1

S = May be selected

Figure 5a. Input/Output Mode Timing–Single-Channel, Single-Ended Conversion

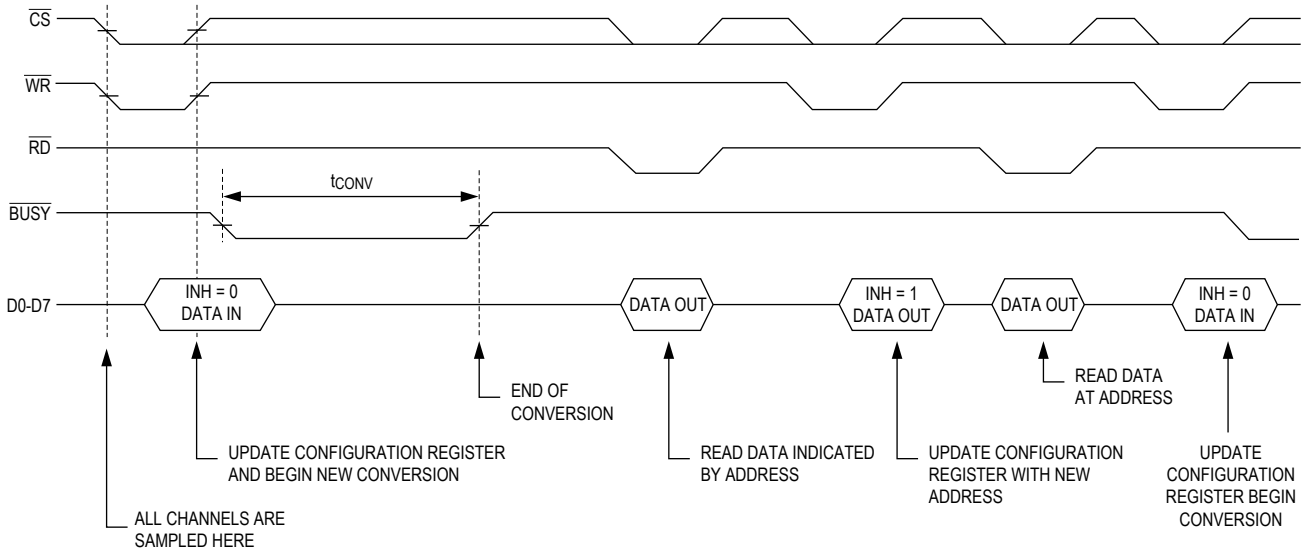


NOTE: A differential channel is converted by writing the following data into the configuration register (see Figure 3) The BIP and DIFF bits are not implemented until the next $\overline{WR}$

A0	A1	A2	PD	INH	BIP	DIFF	$\overline{ALL}$
S	S	S	0	0	S	1	1

S = May be selected

Figure 5b. Input/Output Mode Timing–Single-Channel, Differential Conversion



NOTE: A RAM location is read by writing the following data into the configuration register and when performing a $\overline{RD}$. If INH = 0, a conversion will begin.

A0	A1	A2	PD	INH	BIP	DIFF	$\overline{ALL}$
S	S	S	0	1	X	X	1

S = May be selected
X = Don't Care for this $\overline{WR}$ if INH = 0, but may effect next conversion.

Figure 6. Input/Output Mode Timing–Reading Arbitrary RAM Locations

Hard-Wired Mode

For simpler applications, the MODE and V_{SS} pins can be hard-wired to specify the type of conversion as outlined in Table 4. In this mode, the configuration register is not used, so input data on DO-D7 is ignored. For example, with MODE tied low, an 8-channel, single-ended conver sion begins with $\overline{WR}$ With MODE tied high, a 4-channel, differential conversion is init iated with $\overline{WR}$. Again, the configuration register is not affected by the data present on 00-07. These conversions are otherwise identical to those shown in Figure 4.

Analog Considerations

Intemal Reference

The internal 2.5V reference (REFOUT) must be bypassed to AGND (Figure 8a) with a 4.7µF electrolytic and a 0.1µF ceramic capacitor to ensure stability.

Table 4. Hard-Wired Mode—Multiplexer Selections

MODE	V_{SS}	CONVERSION TYPE
OPEN CIRCUIT	X	Multiplexer configuration register determines conversion type. Not hard-wired.
0	AGND	8-Channel, Single-Ended, Unipolar Conversion
1	AGND	4-Channel, Differential, Unipolar Conversion
0	-5V	8-Channel, Single-Ended, Bipolar Conversion
1	-5V	4-Channel, Differential, Bipolar Conversion

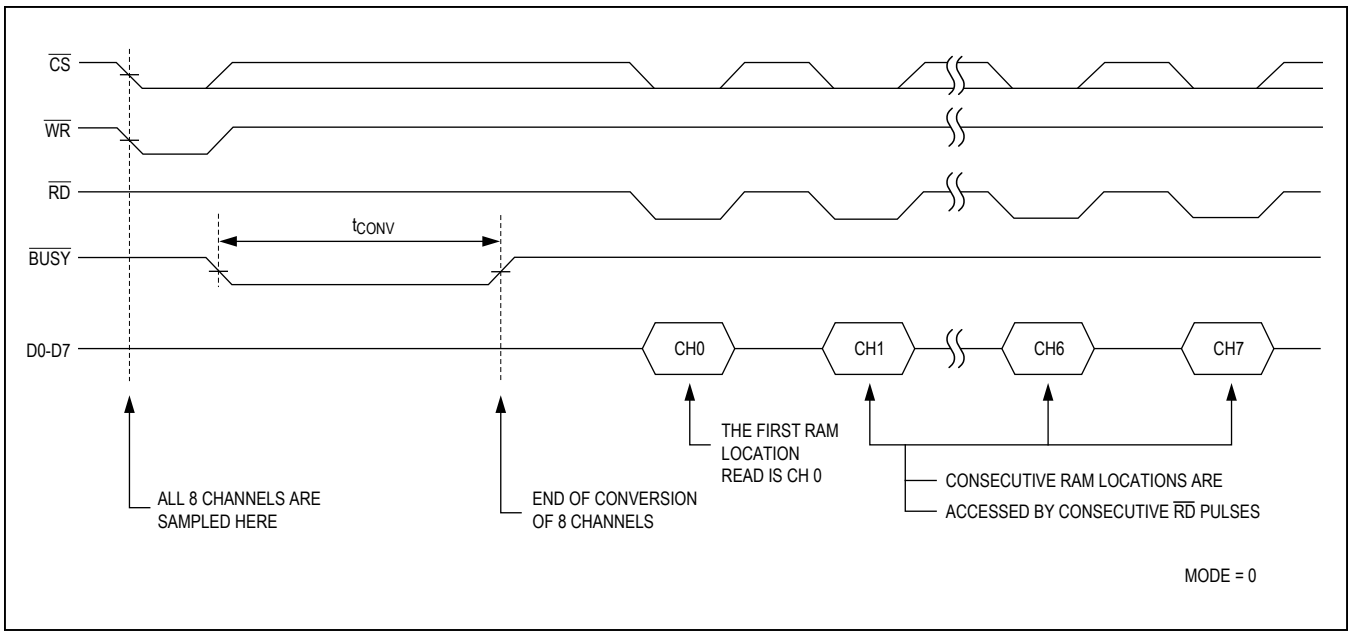


Figure 7a. Hard-Wired Mode Timing—Eight Single-Ended Conversions

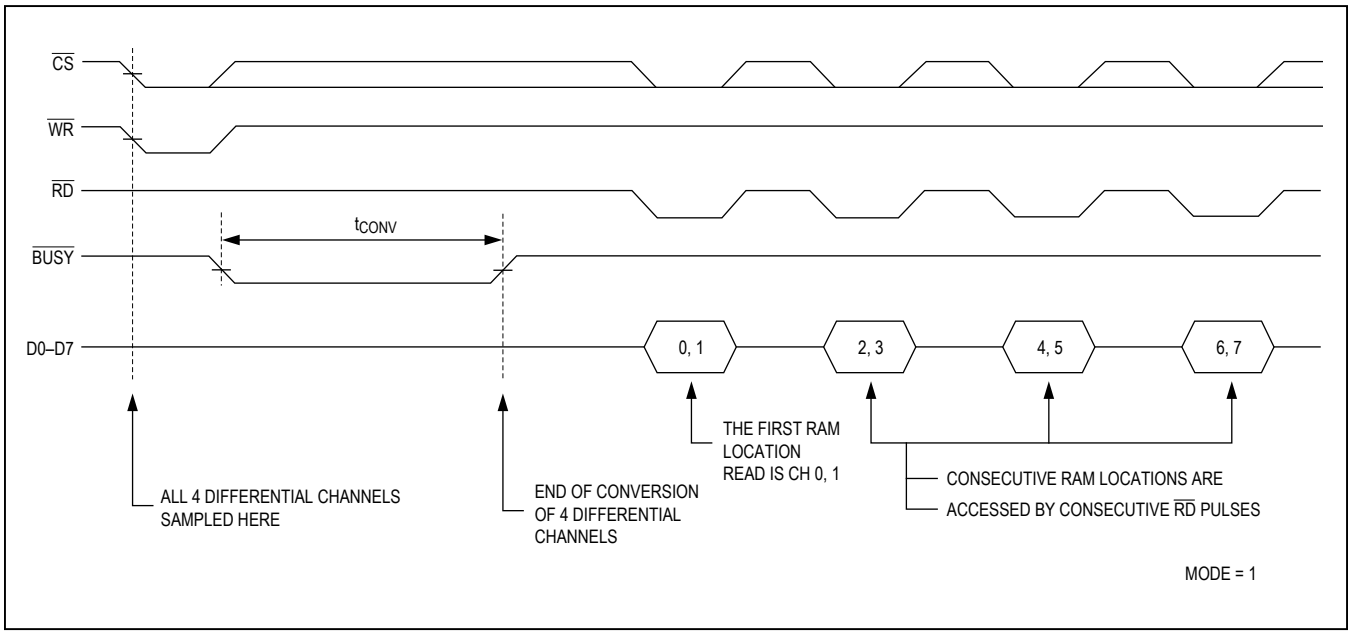


Figure 7b. Hard-Wired Mode Timing—Eight Single-Ended Conversions

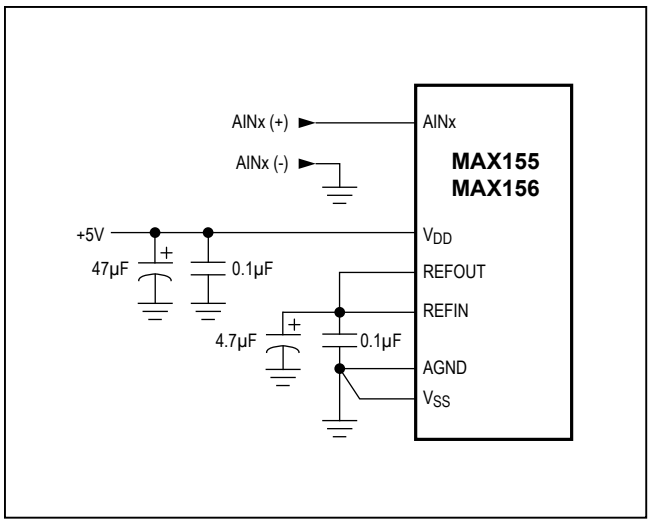


Figure 8a. Internal Reference

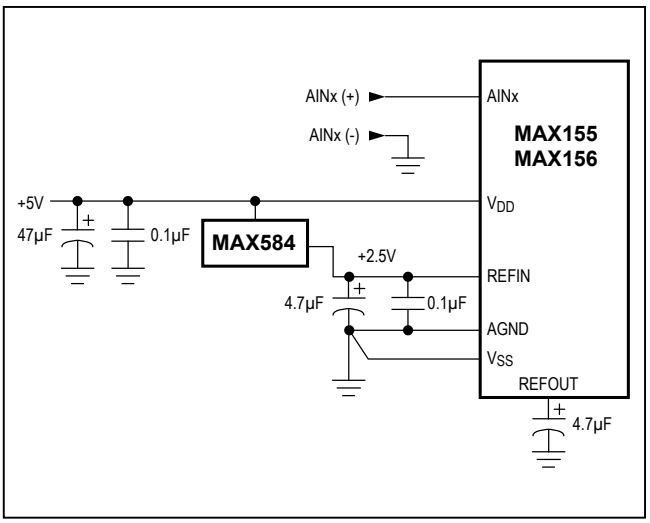


Figure 8b. External Reference, +2.5V Full Scale

Extemal Reference

If an external voltage reference is used at REFIN, REFOUT must either be bypassed (Figure 8b) or disabled to prevent its output from oscillating and generating unwanted conversion noise elsewhere in the ADC. If component count is critical when using an external reference, REFOUT may be disabled by connecting it to V_{DD}. In this case, the unused internal reference does not need a bypass cap. A disadvantage of tying REFOUT to V_{DD} is that power-down current will be increased by about 250µA above the specification limits.

Power-Down Mode

The MAX155/MAX156 may be placed in a powered-down state by writing a 1 to the PD location in the configuration register (Table 1). The register may be updated while in this state (to change mux configurations or exit power-down mode) and all register contents are retained; however no data can be read from RAM and no conversions can be started. The power-down command is implemented on $\overline{WR}$'s rising edge.

To minimize current drain, the MAX155/MAX156 internal reference is turned off during power-down. When returning to normal operation (PD = 0), up to 5ms may be needed to allow the reference to recharge its 4.7µF bypass capacitor before a conversion is performed. If an external reference is used, and remains on during power-down, a conversion can be started within 50µs after loading PD with a 0.

Bypassing

A 47µF electrolytic and a 0.1µF ceramic capacitor should bypass V_{DD} to AGND. If input signals below ground are expected, a negative supply is necessary. In that case, V_{SS} should be bypassed to AGND with a 4.7µF and 0.1µF combination.

The internal reference requires a 4.7µF and 0.1µF combination. If an external voltage reference is used, bypass REFIN to AGND with a 4.7µF capacitor close to the chip. When an external reference is used, REFOUT must still be either bypassed or connected to V_{DD}.

Track/Hold Amplifiers

The MAX155/MAX156 T/H amplifiers' high input impedance usually requires no input buffering. All T/Hs sample simultaneously. For best results, the analog inputs should not exceed the power-supply rails (V_{DD}, V_{SS}) by more than 50mV.

The time required for the T/H to acquire an input signal for one channel is a function of how quickly the channel input capacitance is charged. If the source impedance of the input signal is high, acquisition takes longer, and more time must be allowed between conversions. Acquisition time is calculated by:

$$t_{ACQ} = 8(R_S + R_{IN}) \times 4pF \text{ (but never less than 800ns)}$$

where R_{IN} = 15kΩ, and R_S = source impedance of the ADC's input signal.

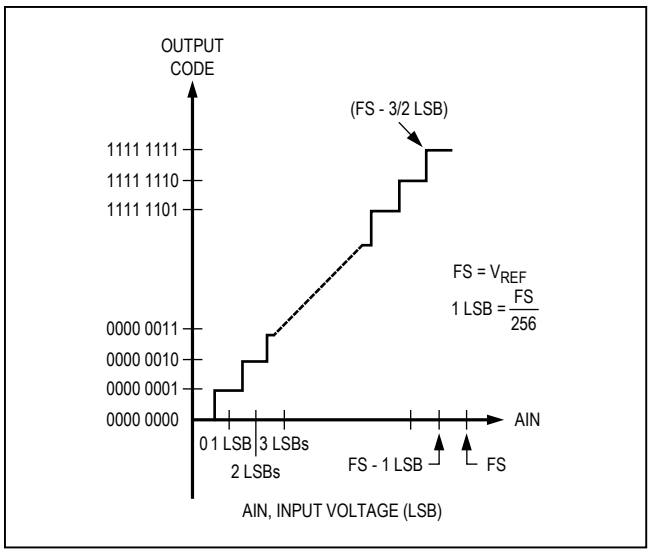


Figure 9a. Transfer Function—Unipolar Operation

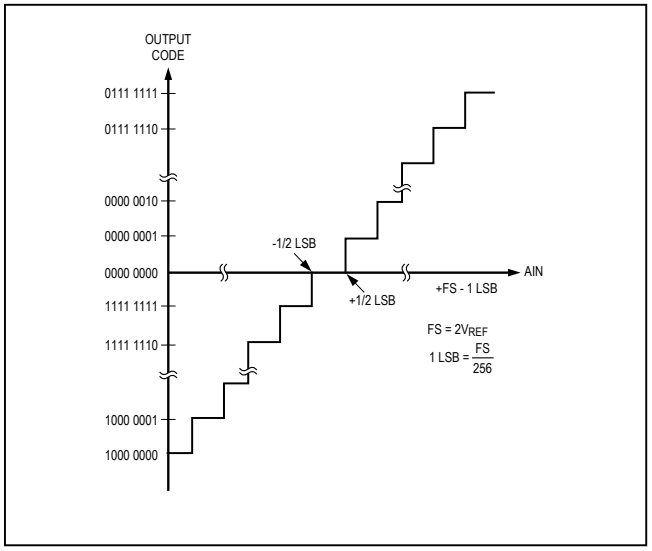


Figure 9b. Transfer Function—Bipolar Operation

Conversion Time

Conversion time is calculated by:

$$t_{CONV} = (9 \times N \times 2)/f_{CLK}$$

where N is the number of channels converted. This includes one clock cycle of uncertainty. For a single channel and 5MHz clock, the conversion time is (9 x 1 x 2)/5MHz = 3.6µs. For the MAX155, the maximum conversion time for 8 channels is (9 x 8 x 2)/5MHz = 28.8µs. In the application example (Figure 10), six conversions are configured, and the conversion time is (9 x 6 x 2}/5MHz = 21.6µs.

Applications Information

9-Bit A/D Conversion

In I/O mode, a 9th bit of resolution can be created by performing two unipolar differential conversions with opposite input polarities (i.e., first with AIN0[+] and AIN1[-], then with AINO[-] and AIN1[+]). Only the A0 bit must be changed to reverse input channel polarity (Table 3). The sign reversal also occurs on the current write without a one conversion delay. For a differential input signal, one of the two conversions will read 0 while the other will contain an 8-bit result. The input polarity that provides the 8-bit result indicates the 9th (sign) bit. 4 channels can be measured this way. A major drawback of this technique is that many of the sampling features of the MAX155/MAX156 are defeated since two separate samples are needed

If only two 9-bit channels are needed, then two separate differential channels with reversed input polarities can be connected so that both input pairs sample at the same time. This way the simultaneoussampling advantages of the MAX155/MAX156 are retained.

Typical I/O Mode Application

The MAX155/MAX156 address and configuration inputs for this example were determined by selecting the desired channel configurations in Tables 2 and 3. Figure 10 illustrates the configuration outlined in Table 5.

Table 5. Typical Multiplexer Configuration

A2	A1	A0	DIFF	BIP	FUNCTION
0	0	1	1	1	Channel (1, 0) Differential Bipolar
0	1	0	0	0	Channel 2 Single-Ended, Unipolar
0	1	1	0	1	Channel 3 Single-Ended, Bipolar
1	0	0	0	1	Channel 4 Single-Ended, Bipolar
1	0	1	0	0	Channel 5 Single-Ended, Unipolar
1	1	0	1	0	Channel (6. 7) Differential, Unipolar

An A/D conversion in I/O mode involves the following steps:

1) Configure the mux by loading data into the configuration register based on selections from Table 2 and/or 3 (with INH = 1 and MODE = open circuit).

For this example, 6 write operations (with each address and data setting in Table 5 above) load the mux after power-up.

2) Sample all selected channels with a $\overline{WR}$ pulse (and INH = 0), and update or rewrite any one location of the configuration register.

This write operation may be skipped by loading INH with a 0 on the last $\overline{WR}$ of the above step. The conversion then starts on the 6th $\overline{WR}$. DIFF and SIP cannot be changed on the 6th $\overline{WR}$ in the conversion is started at that time.

When the conversion starts, $\overline{BUSY}$ goes low while all selected channels are sequentially converted. Conversion results are stored in RAM and are ready to read when $\overline{BUSY}$ returns high.

3) Data is read from RAM with INH = L and consecutive $\overline{RD}$ strobes. Note that in the 6 channel configurations described in this example (Figure 10), 6 $\overline{RD}$ pulses access all available data, start with the differential channel (1, 0). Additional $\overline{RD}$ pulses loop around, accessing the lowest channel data again.

4) To start a new conversion cycle with the same mux configuration, repeat steps 2 and 3.

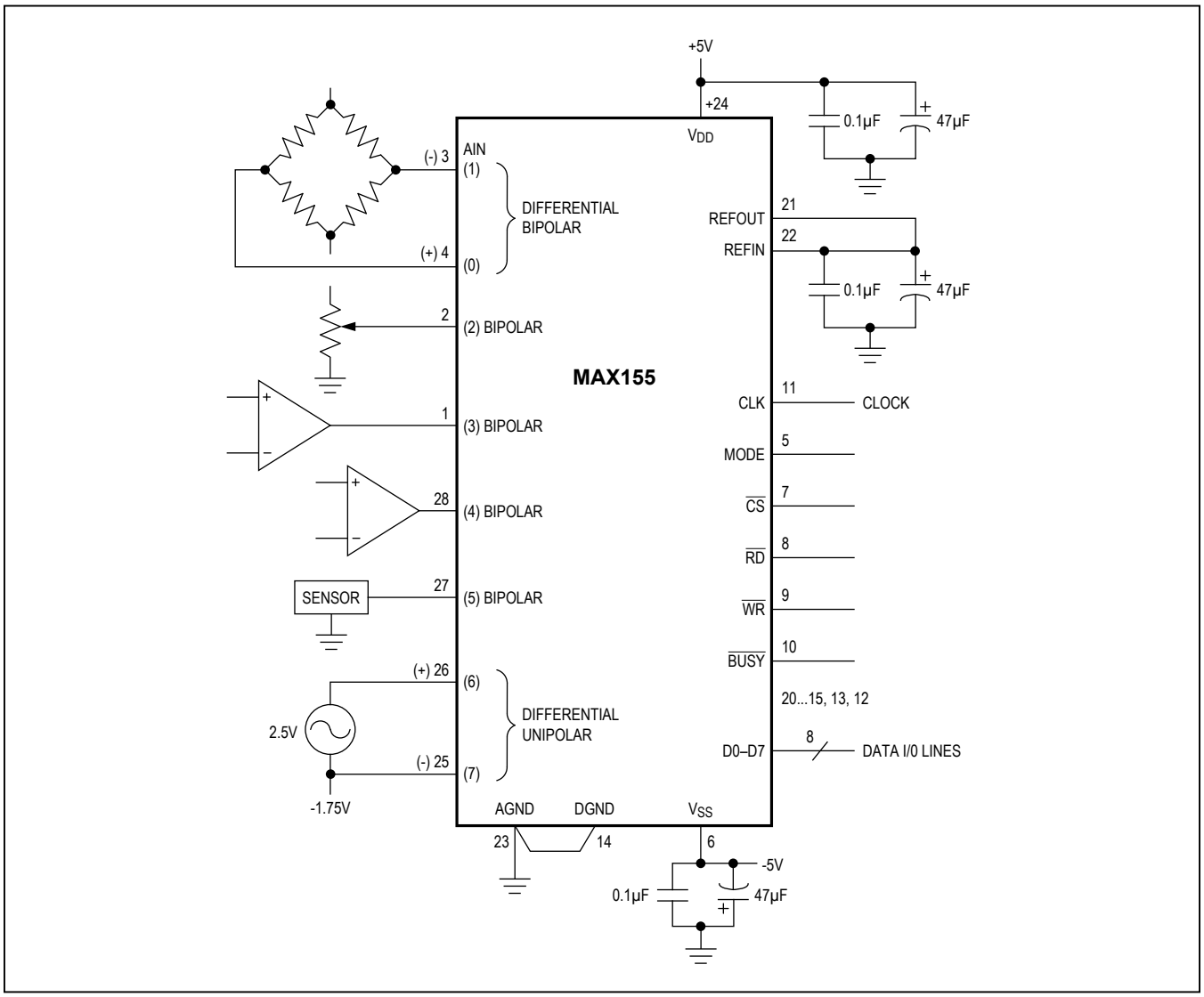


Figure 10. MAX155/MAX156 Typical Operating Circuit

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	ERROR (LSBs)
MAX155ACPI+	0°C to +70°C	28 PDIP	±½
MAX155BCPI+	0°C to +70°C	28 PDIP	±1
MAX155ACWI+	0°C to +70°C	28 Wide SO	±½
MAX155BCWI+	0°C to +70°C	28 Wide SO	±1
MAX155BC/D	0°C to +70°C	Dice*	±1
MAX155AEPI+	-40°C to +85°C	28 PDIP	±½
MAX155BEPI+	-40°C to +85°C	28 PDIP	±1
MAX155AEWI+	-40°C to +85°C	28 Wide SO	±½
MAX155BEWI+	-40°C to +85°C	28 Wide SO	±1
MAX156ACNG+	0°C to +70°C	24 PDIP	±½
MAX156BCNG+	0°C to +70°C	24 PDIP	±1
MAX156ACWI+	0°C to +70°C	28 Wide SO	±½
MAX156BCWI+	0°C to +70°C	28 Wide SO	±1
MAX156BC/D	0°C to +70°C	Dice*	±1
MAX156AENG+	-40°C to +85°C	24 PDIP	±½
MAX156BENG+	-40°C to +85°C	24 PDIP	±1
MAX156AEWI+	-40°C to +85°C	28 Wide SO	±½
MAX156BEWI+	-40°C to +85°C	28 Wide SO	±1

+Denotes a lead(Pb)-free/RoHS-compliant package.

**Contact factory for dice specifications.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 PDIP	N24+8	**21-0043**	—
28 PDIP	P28+7	**21-0044**	—
28 Wide SO	W28+3	**21-0042**	**90-0109**

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/91	Initial release	—
1	6/94	Revised Figure 9a	16
2	1/12	Removed military grade packages and updated stylistic changes	1–5, 18–20

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