# Dual N-Channel 2.5-V (G-S) Input Protected Load Switch

| PRODUCT SUMMARY | | | |
|---|---|---|---|
| $V_{DS}$ (V) | $R_{DS(on)}$ (Ω) | $I_D$ (A) | $Q_g$ (Typ.) |
| 20 | 0.030 at $V_{GS}$ = 4.5 V | 4.5 | 7.6 |
| | 0.033 at $V_{GS}$ = 3.0 V | 4.2 | |
| | 0.035 at $V_{GS}$ = 2.5 V | 3.9 | |

## FEATURES

- **Halogen-free**
- Low $R_{DS(on)}$
- $V_{GS}$ Max Rating: 14 V
- Exceeds 2 kV ESD Protection

Pb-free
RoHS COMPLIANT

## DESCRIPTION

The Si6926AEDQ is a dual N-Channel MOSFET with ESD protection and gate over-voltage protection circuitry incorporated into the MOSFET. The device is designed for use in Lithium Ion battery pack circuits. The 2-stage input protection circuit is a unique design, consisting of two stages of back-to-back zener diodes separated by a resistor. The first stage diode is designed to absorb most of the ESD energy. The second stage diode is designed to protect the gate from any remaining ESD energy and over-voltages above the gates inherent safe operating range. The series resistor used to limit the current through the second stage diode during over voltage conditions has a maximum value which limits the input current to ≤ 10 mA at 14 V and the maximum $t_{off}$ to 15 µs. The Si6926AEDQ has been optimized as a battery or load switch in Lithium Ion applications with the advantage of both a 2.5 V $R_{DS(on)}$ rating and a safe 14 V gate-to-source maximum rating.

## APPLICATION CIRCUITS

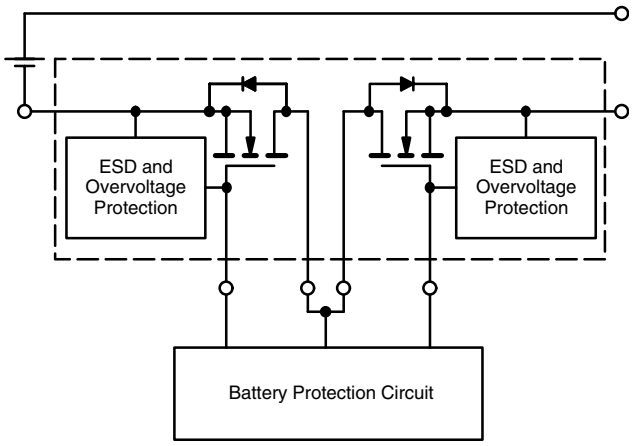
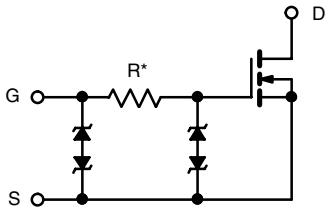



**Figure 1. Typical Use In a Lithium Ion Battery Pack**

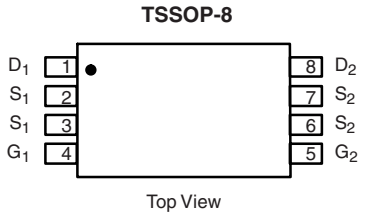



*R typical value is 1.9 kΩ by design.

See Typical Characteristics,
Gate-Current vs. Gate-Source Voltage, Page 3.

**Figure 2. Input ESD and Overvoltage Protection Circuit**

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION




**Ordering Information:** Si6926AEDQ-T1-GE3 (Lead (Pb)-free and Halogen-free)

**Figure 3.**

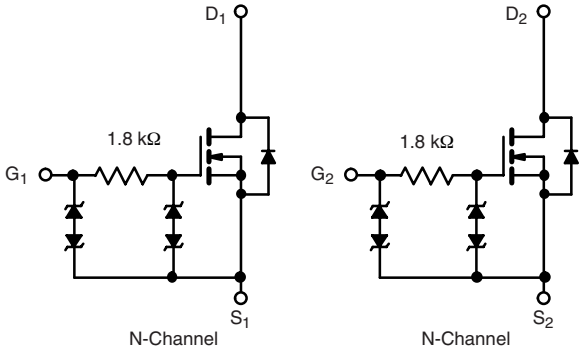



**Figure 4.**

| **ABSOLUTE MAXIMUM RATINGS** $T_A$ = 25 °C, unless otherwise noted | | | | | |
|---|---|---|---|---|---|
| **Parameter** | | **Symbol** | **10 s** | **Steady State** | **Unit** |
| Drain-Source Voltage, Source-Drain Voltage | | $V_{DS}$ | 20 | | V |
| Gate-Source Voltage | | $V_{GS}$ | ± 14 | | |
| Continuous Drain-to-Source Current ($T_J$ = 150 °C)[a] | $T_A$ = 25 °C | $I_D$ | 4.5 | 4.1 | A |
| | $T_A$ = 70 °C | | 3.6 | 3.3 | |
| Pulsed Drain-to-Source Current | | $I_{DM}$ | 20 | | |
| Pulsed Source Current (Diode Conduction)[a] | | $I_S$ | 0.83 | 0.69 | |
| Maximum Power Dissipation[a] | $T_A$ = 25 °C | $P_D$ | 1.0 | 0.83 | W |
| | $T_A$ = 70 °C | | 0.64 | 0.53 | |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | - 55 to 150 | | °C |

| **THERMAL RESISTANCE RATINGS** | | | | | |
|---|---|---|---|---|---|
| **Parameter** | | **Symbol** | **Typical** | **Maximum** | **Unit** |
| Maximum Junction-to-Ambient[a] | t ≤ 10 s | $R_{thJA}$ | 90 | 125 | °C/W |
| | Steady State | | 126 | 150 | |
| Maximum Junction-to-Foot (Drain) | Steady State | $R_{thJF}$ | 65 | 80 | |

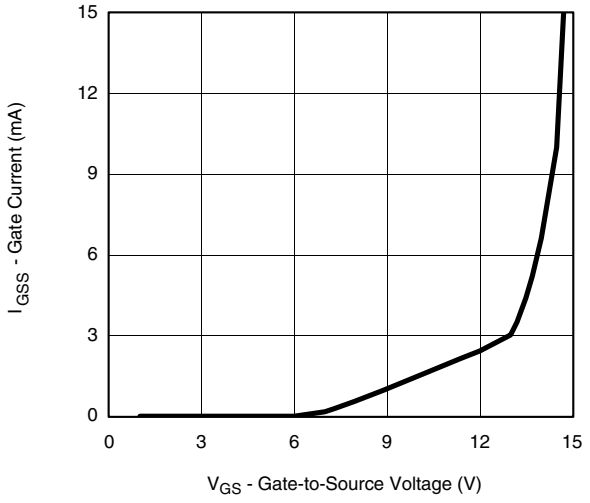
Notes:
a. Surface Mounted on FR4 board.

| **SPECIFICATIONS** $T_J$ = 25 °C, unless otherwise noted | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Test Conditions** | **Min.** | **Typ.** | **Max.** | **Unit** |
| **Static** | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D = 250\ \mu A$ | 0.4 | | 1.2 | V |
| Gate-Body Leakage | $I_{GSS}$ | $V_{DS} = 0$ V, $V_{GS} = \pm 4.5$ V | | | ± 1 | µA |
| | | $V_{DS} = 0$ V, $V_{GS} = \pm 12$ V | | | ± 10 | mA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS} = 20$ V, $V_{GS} = 0$ V | | | 1 | µA |
| | | $V_{DS} = 20$ V, $V_{GS} = 0$ V, $T_J = 55$ °C | | | 5 | |
| On-State Drain Current[b] | $I_{D(on)}$ | $V_{DS} \geq 5$ V, $V_{GS} = 5$ V | 10 | | | A |
| Drain-Source On-State Resistance[b] | $R_{DS(on)}$ | $V_{GS} = 4.5$ V, $I_D = 4.5$ A | | 0.023 | 0.030 | Ω |
| | | $V_{GS} = 3.0$ V, $I_D = 4.2$ A | | 0.025 | 0.033 | |
| | | $V_{GS} = 2.5$ V, $I_D = 3.9$ A | | 0.027 | 0.035 | |
| Forward Transconductance[b] | $g_{fs}$ | $V_{DS} = 10$ V, $I_D = 4.5$ A | | 26 | | S |
| Diode Forward Voltage[b] | $V_{SD}$ | $I_S = 0.83$ A, $V_{GS} = 0$ V | | 0.65 | 1.1 | V |
| **Dynamic[a]** | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{DS} = 10$ V, $V_{GS} = 4.5$ V, $I_D = 4.5$ A | | 7.6 | 12 | nC |
| Gate-Source Charge | $Q_{gs}$ | | | 1.5 | | |
| Gate-Drain Charge | $Q_{gd}$ | | | 1.5 | | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = 10$ V, $R_L = 10\ \Omega$<br>$I_D \cong 1$ A, $V_{GEN} = 4.5$ V, $R_g = 6\ \Omega$ | | 0.43 | 0.7 | µs |
| Rise Time | $t_r$ | | | 0.8 | 1.2 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 5.0 | 7.5 | |
| Fall Time | $t_f$ | | | 2.5 | 4.0 | |

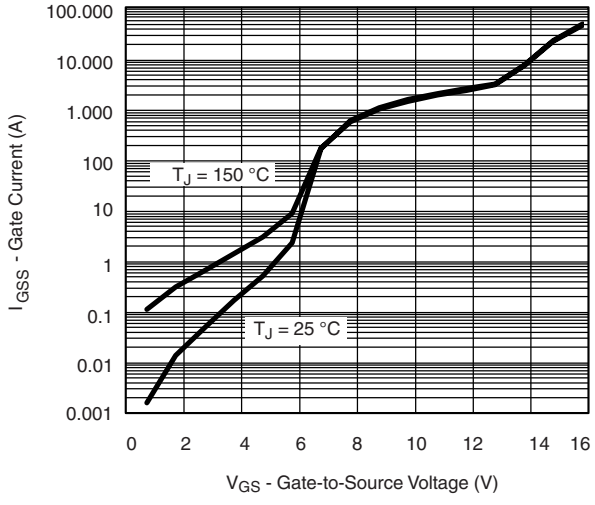
Notes:
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted




**Gate-Current vs. Gate-Source Voltage**




**Gate Current vs. Gate-Source Voltage**

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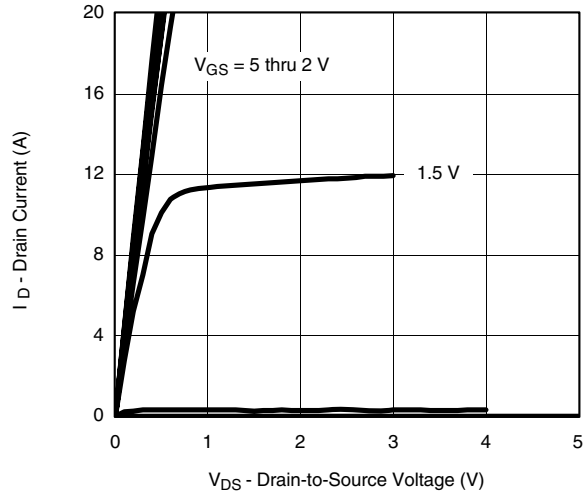
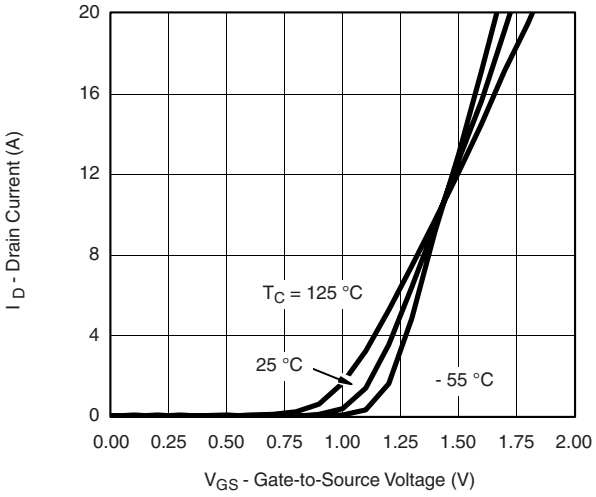
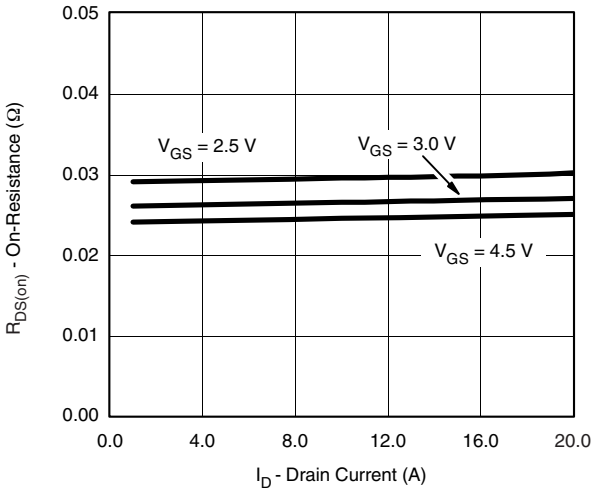


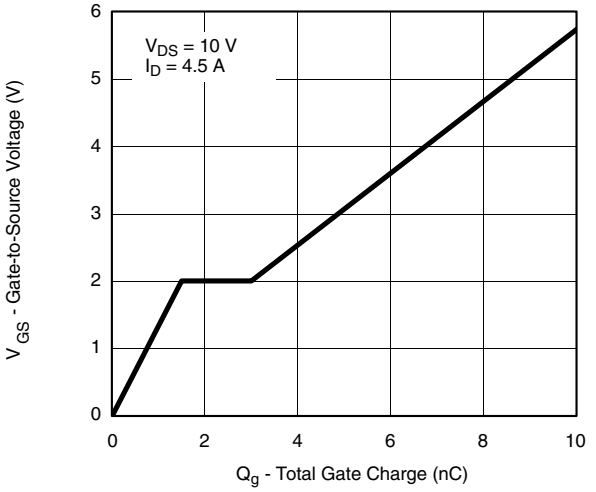

**Output Characteristics**



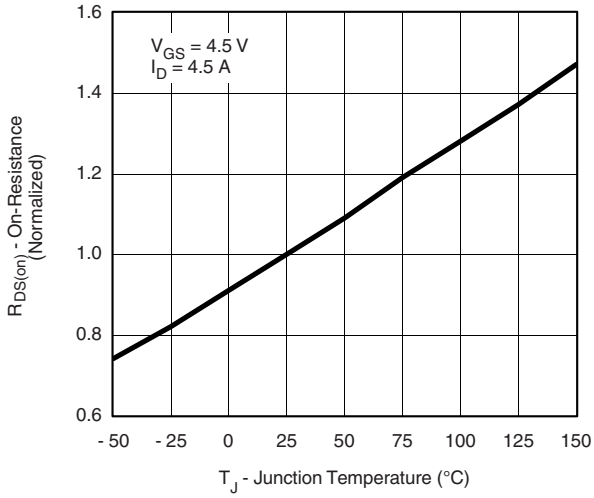

**Transfer Characteristics**



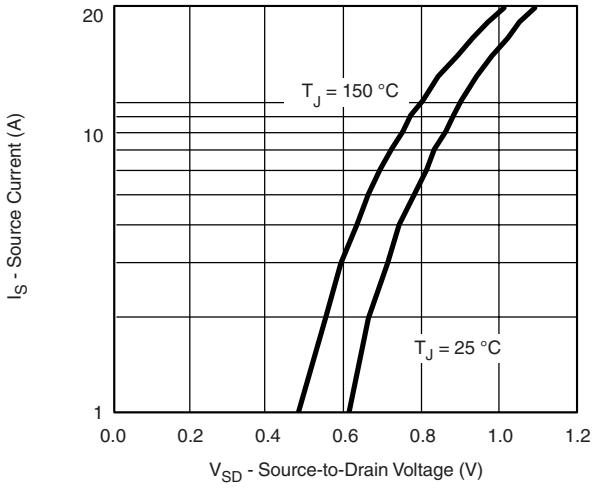

**On-Resistance vs. Drain Current**




**Gate Charge**

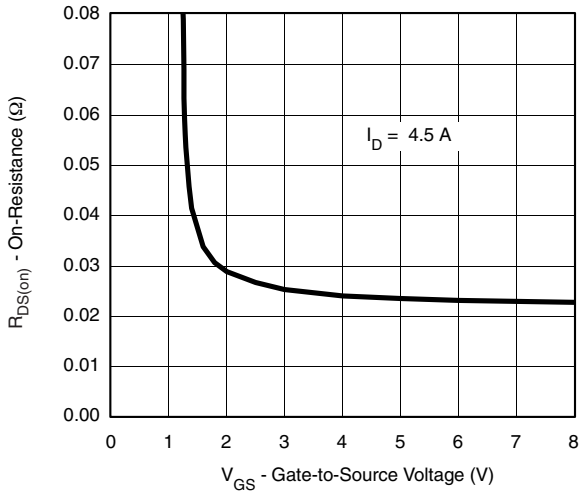



**On-Resistance vs. Junction Temperature**

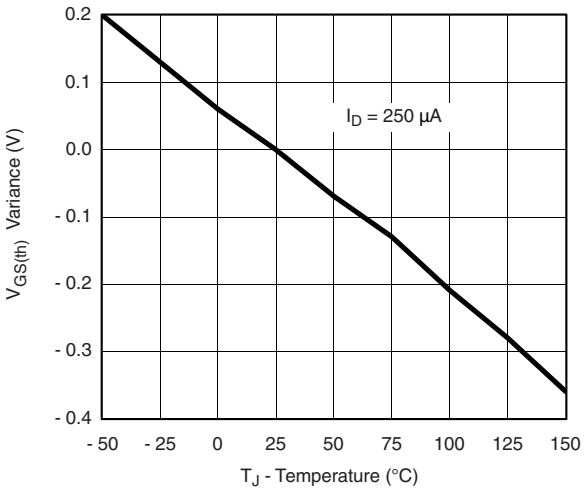



**Source-Drain Diode Forward Voltage**

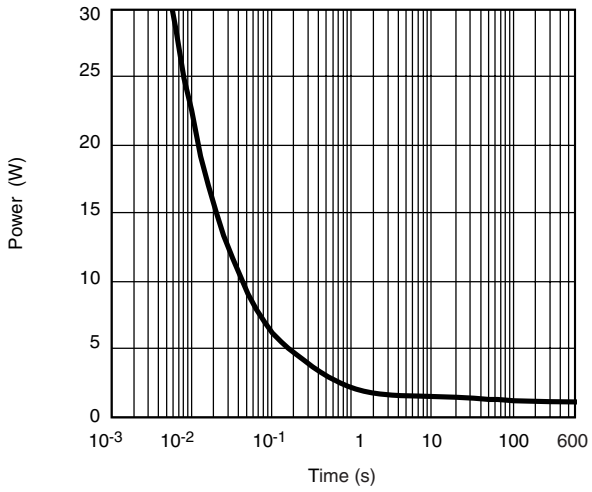
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



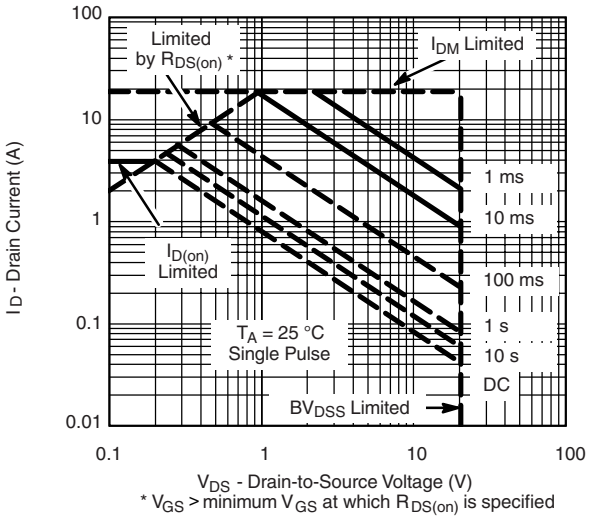

**On-Resistance vs. Gate-to-Source Voltage**



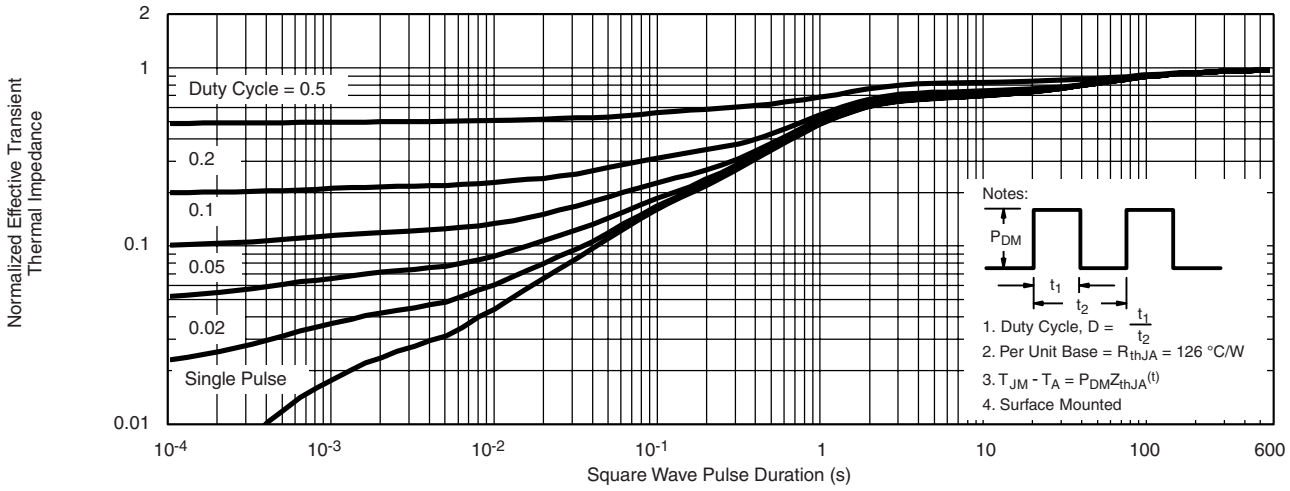

**Threshold Voltage**




**Single Pulse Power, Junction-to-Ambient**

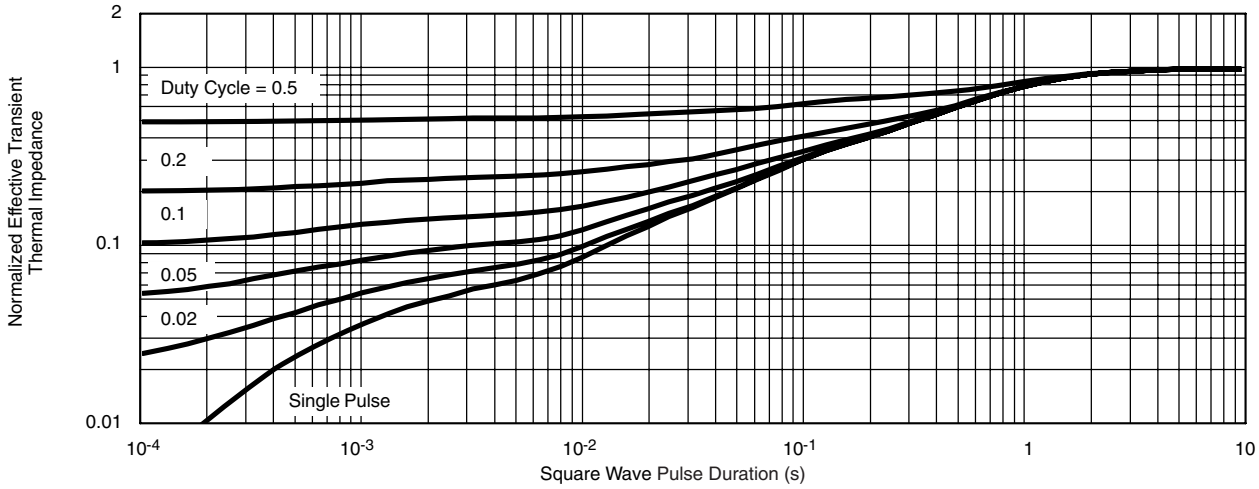



**Safe Operating Area, Junction-to-Case**




**Normalized Thermal Transient Impedance, Junction-to-Ambient**

## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted




**Normalized Thermal Transient Impedance, Junction-to-Foot**

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