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LS1088A

QorIQ LS1088A Data Sheet

Features

- LS1088A contains eight ARM® Cortex®-A53 (32/64 bit) cores with the following capabilities:
  - Speed up to 1.6 GHz
  - Arranged as two clusters of four cores
  - 32 KB L1 instruction cache (ECC protection) and 32 KB L1 data cache (ECC protection)
  - Two 1 MB unified I/D L2 cache (ECC protection), one per Cortex-A53 core cluster
  - NEON™ SIMD coprocessor
  - ARMv8 cryptography extensions
- Hierarchical interconnect fabric:
  - Hardware-managed data coherency
  - Up to 700 MHz operation
- One 32/64-bit DDR4 SDRAM memory controller:
  - ECC and interleaving support
  - Up to 2.1 GT/s
- Datapath acceleration architecture 2.0 (DPAA2) incorporates acceleration for the following functions:
  - Packet parsing, classification, and distribution (WRIOP)
  - Queue management for scheduling, packet sequencing, and congestion management (QMan)
  - Hardware buffer management for buffer allocation and de-allocation (BMan)
  - Cryptography acceleration (SEC)
  - IEEE 1588 support
  - Advanced I/O processor (AIOP)
- Parallel Ethernet interfaces:
  - Up to two RGMII interfaces
- Eight SerDes lanes for high-speed peripheral interfaces:
  - Three PCI Express 3.0 controllers (one supporting x4 operation)
  - One serial ATA (SATA 3.0) controller supporting 6 Gbps
  - Up to two SGMII supporting 2500 Mbps
  - Up to four SGMII supporting 1000 Mbps
  - Up to two XFI (10 GbE) interfaces
  - Up to two QSGMII
  - Supports 1000Base-KX
  - Supports 10GBase-KR
- Additional peripheral interfaces include:
  - One quad serial peripheral interface (QSPI) controller, one serial peripheral interface (SPI) controller
  - Integrated flash controller (IFC) supporting NAND and NOR flash with 28-bit addressing and 16-bit data
  - Two USB 3.0 controllers with integrated PHY
  - Enhanced secure digital host controller supporting SD 3.0, eMMC 4.4, and eMMC 4.5 modes
  - uQE supporting TDM/HDLC
  - Four I2C controllers
  - Two 16550-compliant DUARTs
  - General purpose IO (GPIO), four FlexTimers, and nine watchdog timers
  - Trust architecture
  - Debug support with run control, data acquisition, high-speed trace, and performance/event monitoring
- 780 FC-PBGA package, 23 mm x 23 mm, 0.8 mm pitch

NXP reserves the right to change the production detail specifications as may be required to permit improvements in the design of its products.

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1 Overview

A member of the Layerscape (LS1) series, the LS1088A is a cost-effective, power-efficient, and highly integrated system-on-chip (SoC) device featuring eight extremely power-efficient 64-bit ARM® Cortex®-A53 cores with ECC-protected L1 and L2 cache memories for high reliability, running up to 1.6 GHz.

The LS1088A family of devices can be used for enterprise and service provider routers, Virtual CPE, industrial communications, security appliance and military and aerospace applications.

This figure shows the LS1088A block diagram.

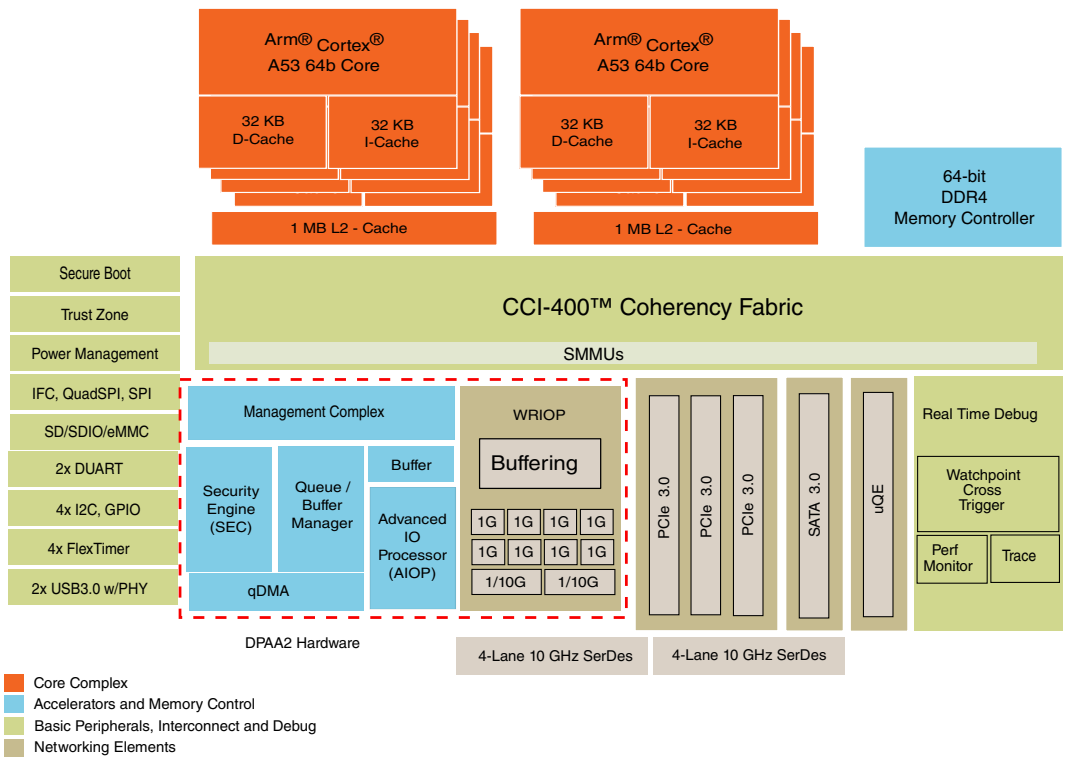

Figure 1. LS1088A block diagram

2 Pin assignments

NOTE: Information given in this section is preliminary and is subject to change.

2.1 780 BGA ball layout diagrams

This figure shows the complete view of the LS1088A BGA ball map diagram. Figure 3, Figure 4, Figure 5, and Figure 6 show quadrant views.

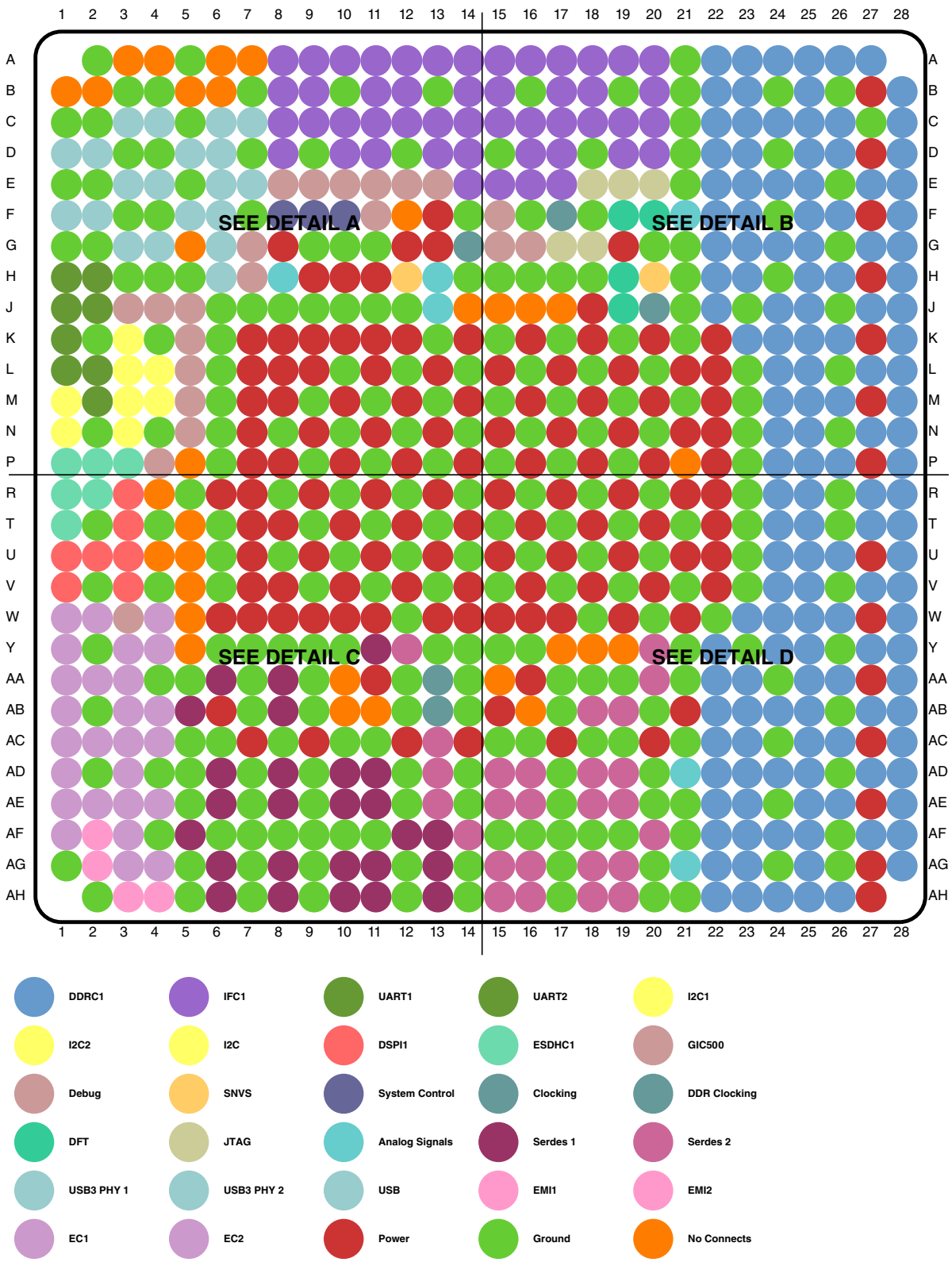

Figure 2. Complete BGA Map for the LS1088A

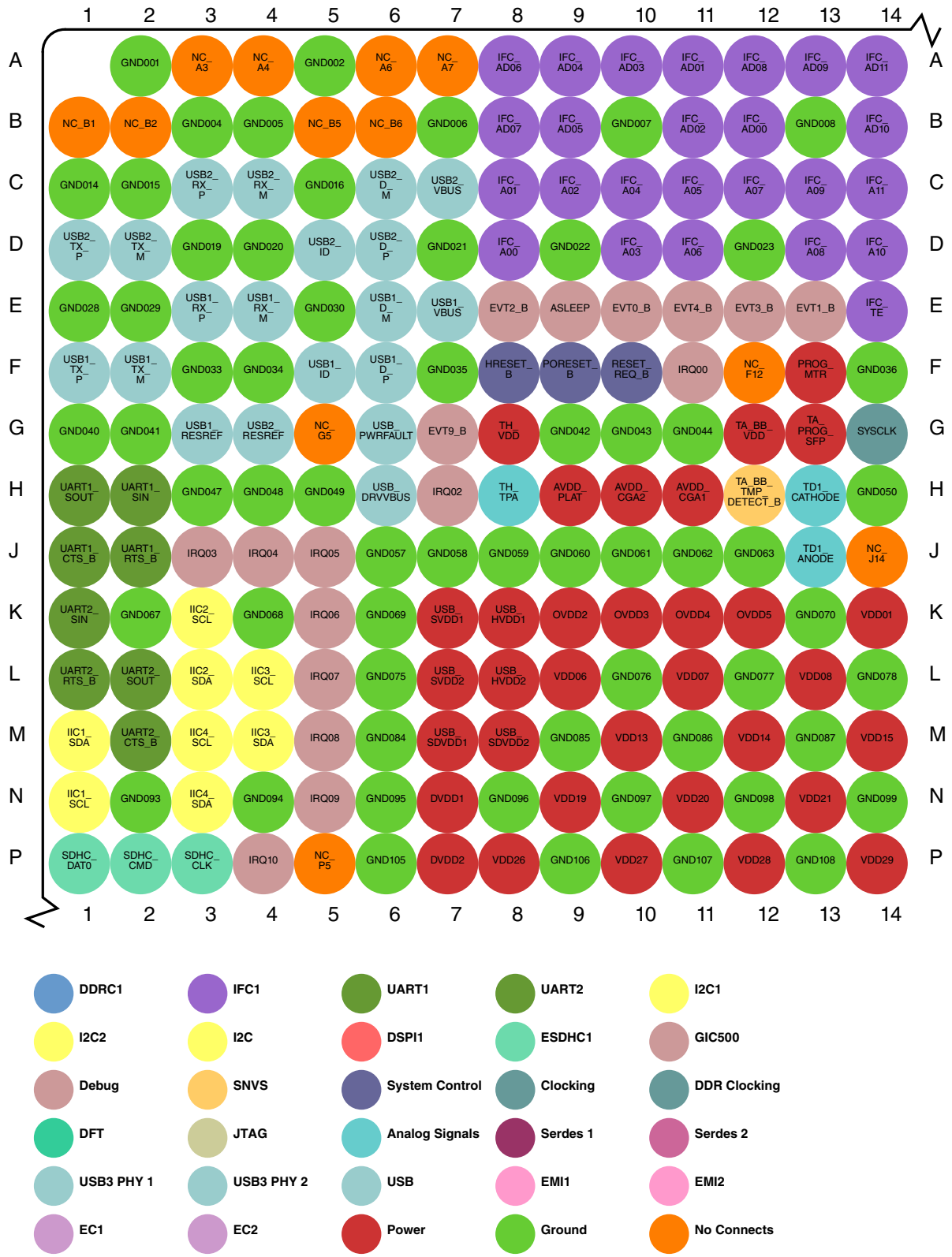

Figure 3. Detail A

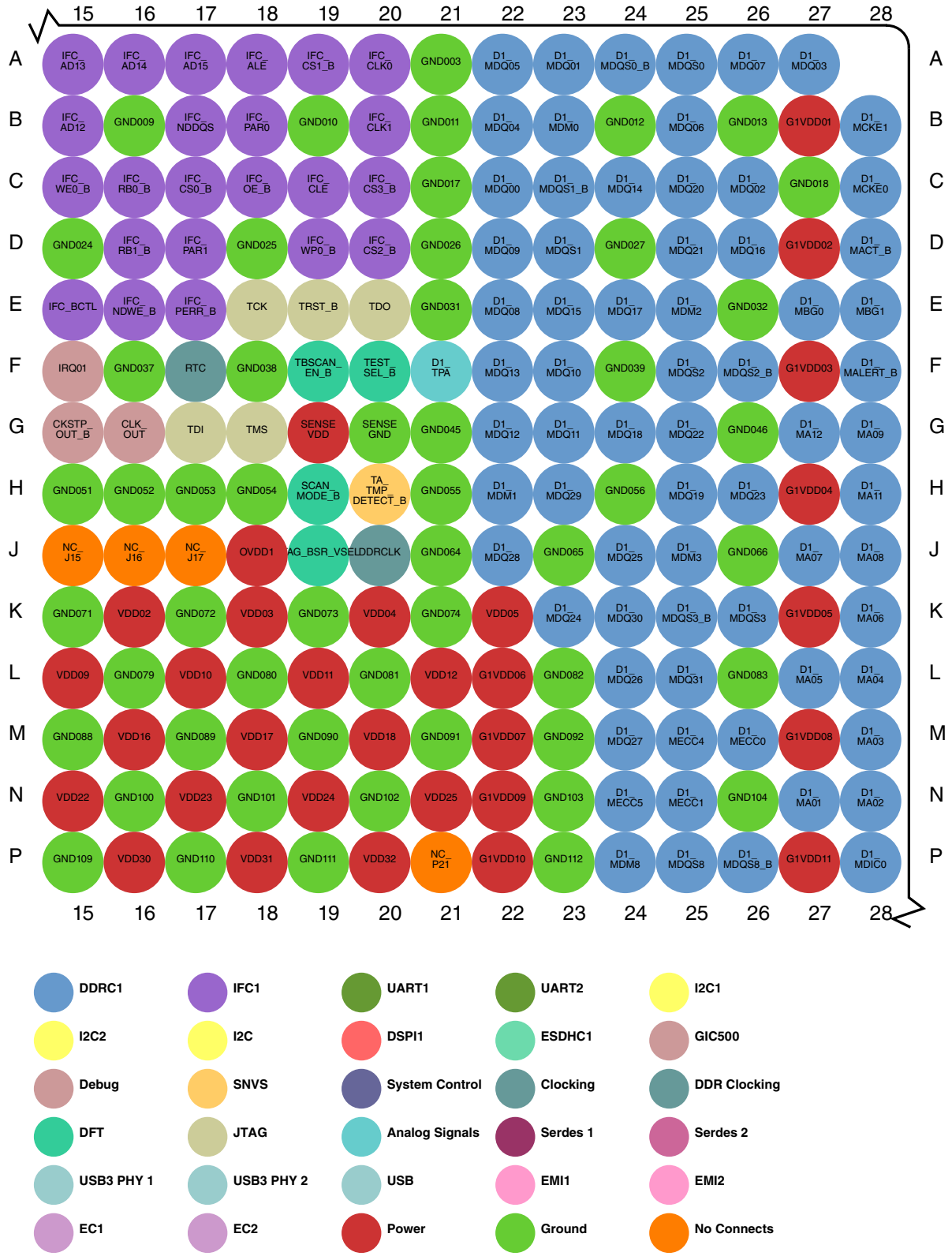

Figure 4. Detail B

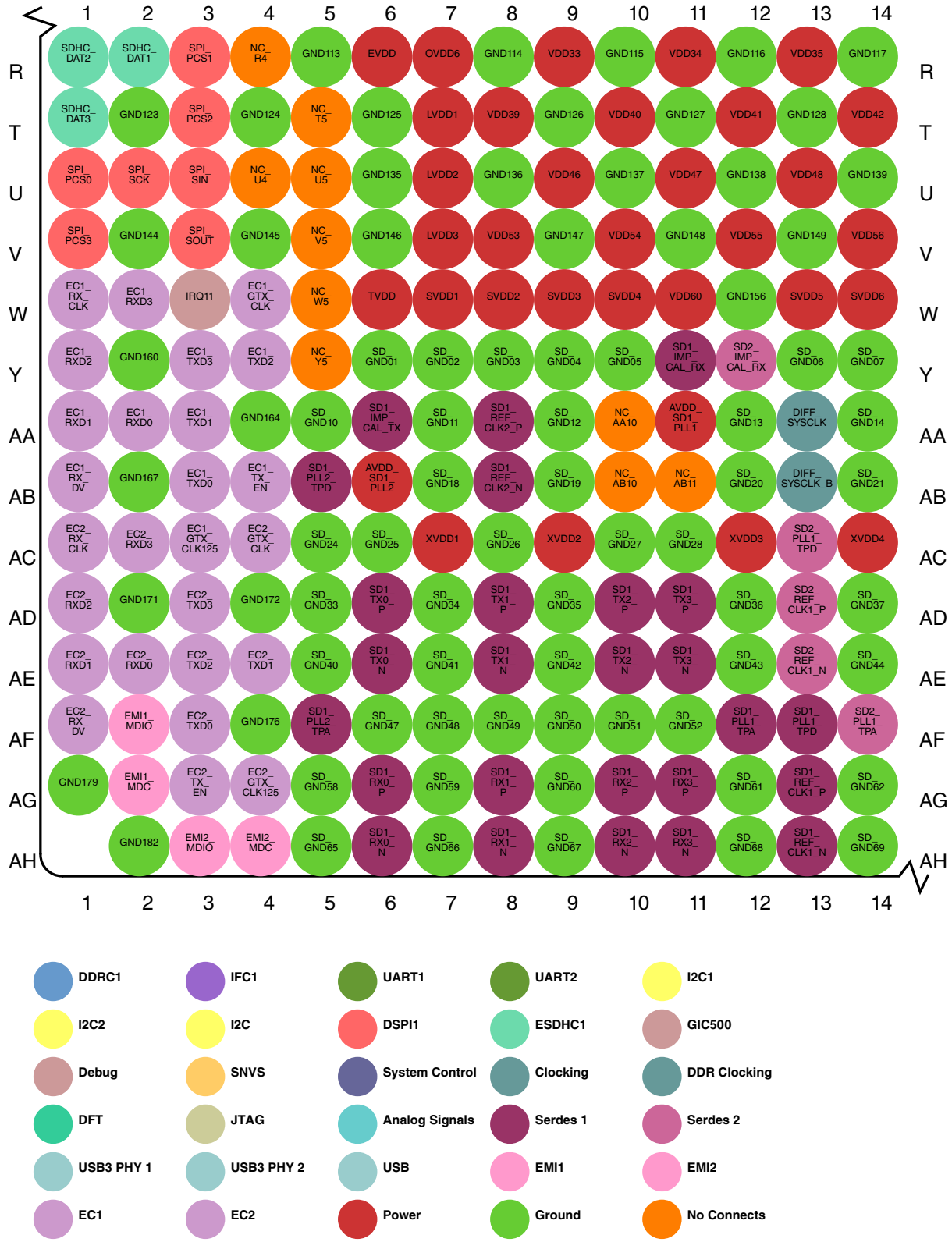

Figure 5. Detail C

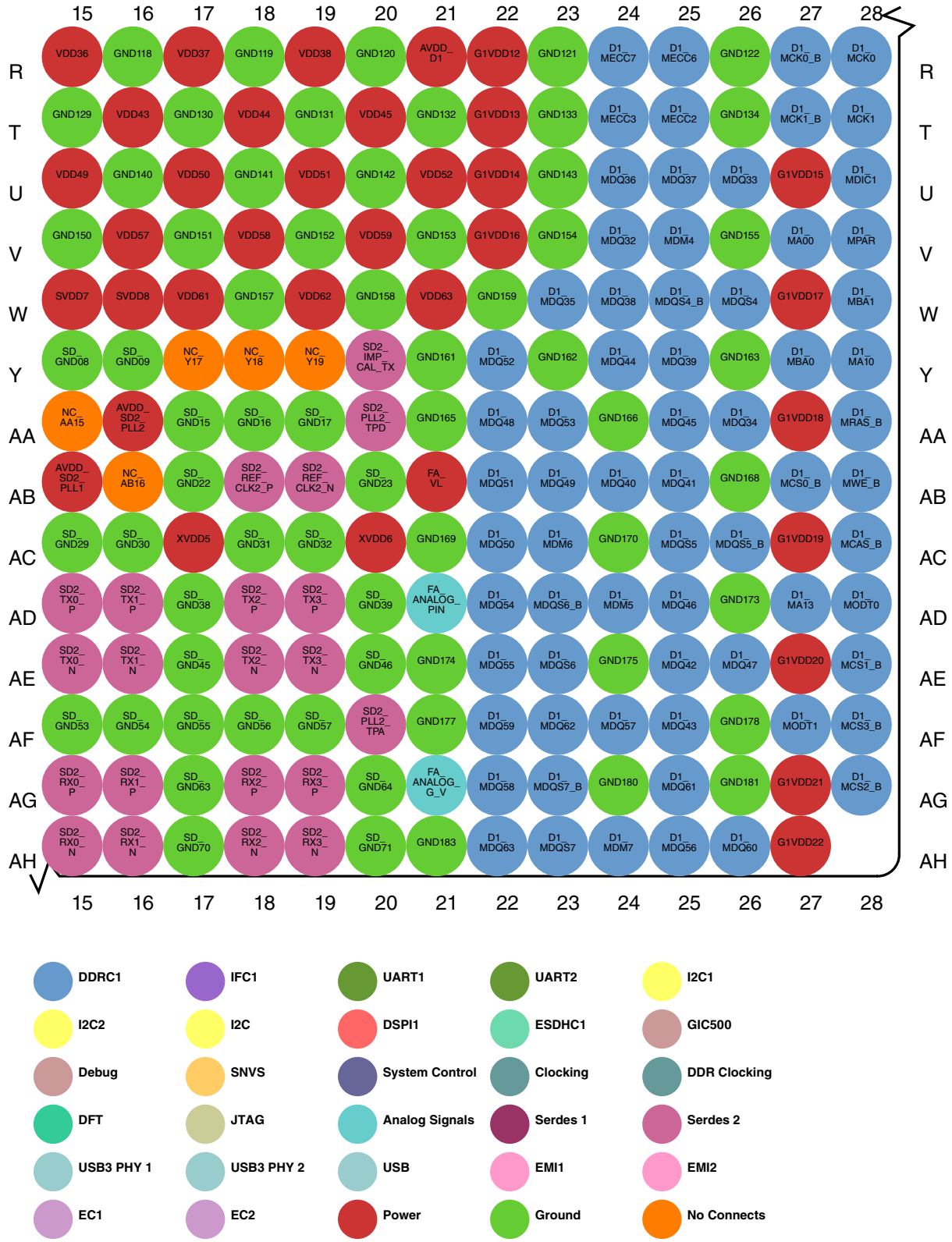

Figure 6. Detail D

2.2 Pinout list

This table provides the pinout listing for the LS1088A by bus. Primary functions are **bolded** in the table.

Table 1. Pinout list by bus

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
DDR SDRAM Memory Interface 1					
D1_MA00	Address	V27	O	$G1V_{DD}$	1
D1_MA01	Address	N27	O	$G1V_{DD}$	1
D1_MA02	Address	N28	O	$G1V_{DD}$	1
D1_MA03	Address	M28	O	$G1V_{DD}$	1
D1_MA04	Address	L28	O	$G1V_{DD}$	1
D1_MA05	Address	L27	O	$G1V_{DD}$	1
D1_MA06	Address	K28	O	$G1V_{DD}$	1
D1_MA07	Address	J27	O	$G1V_{DD}$	1
D1_MA08	Address	J28	O	$G1V_{DD}$	1
D1_MA09	Address	G28	O	$G1V_{DD}$	1
D1_MA10	Address	Y28	O	$G1V_{DD}$	1
D1_MA11	Address	H28	O	$G1V_{DD}$	1
D1_MA12	Address	G27	O	$G1V_{DD}$	1
D1_MA13	Address	AD27	O	$G1V_{DD}$	1
D1_MACT_B	Activate	D28	O	$G1V_{DD}$	1
D1_MALERT_B	Alert	F28	I	$G1V_{DD}$	1, 6
D1_MBA0	Bank Select	Y27	O	$G1V_{DD}$	1
D1_MBA1	Bank Select	W28	O	$G1V_{DD}$	1
D1_MBG0	Bank Group	E27	O	$G1V_{DD}$	1
D1_MBG1	Bank Group	E28	O	$G1V_{DD}$	1
D1_MCAS_B	Column Address Strobe / MA[15]	AC28	O	$G1V_{DD}$	1
D1_MCK0	Clock	R28	O	$G1V_{DD}$	---
D1_MCK0_B	Clock Complement	R27	O	$G1V_{DD}$	---
D1_MCK1	Clock	T28	O	$G1V_{DD}$	---
D1_MCK1_B	Clock Complement	T27	O	$G1V_{DD}$	---
D1_MCKE0	Clock Enable	C28	O	$G1V_{DD}$	1
D1_MCKE1	Clock Enable	B28	O	$G1V_{DD}$	1
D1_MCS0_B	Chip Select	AB27	O	$G1V_{DD}$	1
D1_MCS1_B	Chip Select	AE28	O	$G1V_{DD}$	1
D1_MCS2_B	Chip Select	AG28	O	$G1V_{DD}$	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MCS3_B	Chip Select	AF28	O	$G1V_{DD}$	1
D1_MDIC0	Driver Impedence Calibration	P28	IO	$G1V_{DD}$	3
D1_MDIC1	Driver Impedence Calibration	U28	IO	$G1V_{DD}$	3
D1_MDM0	Data Mask	B23	O	$G1V_{DD}$	---
D1_MDM1	Data Mask	H22	O	$G1V_{DD}$	---
D1_MDM2	Data Mask	E25	O	$G1V_{DD}$	---
D1_MDM3	Data Mask	J25	O	$G1V_{DD}$	---
D1_MDM4	Data Mask	V25	O	$G1V_{DD}$	---
D1_MDM5	Data Mask	AD24	O	$G1V_{DD}$	---
D1_MDM6	Data Mask	AC23	O	$G1V_{DD}$	---
D1_MDM7	Data Mask	AH24	O	$G1V_{DD}$	---
D1_MDM8	Data Mask	P24	O	$G1V_{DD}$	---
D1_MDQ00	Data	C22	IO	$G1V_{DD}$	---
D1_MDQ01	Data	A23	IO	$G1V_{DD}$	---
D1_MDQ02	Data	C26	IO	$G1V_{DD}$	---
D1_MDQ03	Data	A27	IO	$G1V_{DD}$	---
D1_MDQ04	Data	B22	IO	$G1V_{DD}$	---
D1_MDQ05	Data	A22	IO	$G1V_{DD}$	---
D1_MDQ06	Data	B25	IO	$G1V_{DD}$	---
D1_MDQ07	Data	A26	IO	$G1V_{DD}$	---
D1_MDQ08	Data	E22	IO	$G1V_{DD}$	---
D1_MDQ09	Data	D22	IO	$G1V_{DD}$	---
D1_MDQ10	Data	F23	IO	$G1V_{DD}$	---
D1_MDQ11	Data	G23	IO	$G1V_{DD}$	---
D1_MDQ12	Data	G22	IO	$G1V_{DD}$	---
D1_MDQ13	Data	F22	IO	$G1V_{DD}$	---
D1_MDQ14	Data	C24	IO	$G1V_{DD}$	---
D1_MDQ15	Data	E23	IO	$G1V_{DD}$	---
D1_MDQ16	Data	D26	IO	$G1V_{DD}$	---
D1_MDQ17	Data	E24	IO	$G1V_{DD}$	---
D1_MDQ18	Data	G24	IO	$G1V_{DD}$	---
D1_MDQ19	Data	H25	IO	$G1V_{DD}$	---
D1_MDQ20	Data	C25	IO	$G1V_{DD}$	---
D1_MDQ21	Data	D25	IO	$G1V_{DD}$	---
D1_MDQ22	Data	G25	IO	$G1V_{DD}$	---
D1_MDQ23	Data	H26	IO	$G1V_{DD}$	---
D1_MDQ24	Data	K23	IO	$G1V_{DD}$	---
D1_MDQ25	Data	J24	IO	$G1V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MDQ26	Data	L24	IO	$G1V_{DD}$	---
D1_MDQ27	Data	M24	IO	$G1V_{DD}$	---
D1_MDQ28	Data	J22	IO	$G1V_{DD}$	---
D1_MDQ29	Data	H23	IO	$G1V_{DD}$	---
D1_MDQ30	Data	K24	IO	$G1V_{DD}$	---
D1_MDQ31	Data	L25	IO	$G1V_{DD}$	---
D1_MDQ32	Data	V24	IO	$G1V_{DD}$	---
D1_MDQ33	Data	U26	IO	$G1V_{DD}$	---
D1_MDQ34	Data	AA26	IO	$G1V_{DD}$	---
D1_MDQ35	Data	W23	IO	$G1V_{DD}$	---
D1_MDQ36	Data	U24	IO	$G1V_{DD}$	---
D1_MDQ37	Data	U25	IO	$G1V_{DD}$	---
D1_MDQ38	Data	W24	IO	$G1V_{DD}$	---
D1_MDQ39	Data	Y25	IO	$G1V_{DD}$	---
D1_MDQ40	Data	AB24	IO	$G1V_{DD}$	---
D1_MDQ41	Data	AB25	IO	$G1V_{DD}$	---
D1_MDQ42	Data	AE25	IO	$G1V_{DD}$	---
D1_MDQ43	Data	AF25	IO	$G1V_{DD}$	---
D1_MDQ44	Data	Y24	IO	$G1V_{DD}$	---
D1_MDQ45	Data	AA25	IO	$G1V_{DD}$	---
D1_MDQ46	Data	AD25	IO	$G1V_{DD}$	---
D1_MDQ47	Data	AE26	IO	$G1V_{DD}$	---
D1_MDQ48	Data	AA22	IO	$G1V_{DD}$	---
D1_MDQ49	Data	AB23	IO	$G1V_{DD}$	---
D1_MDQ50	Data	AC22	IO	$G1V_{DD}$	---
D1_MDQ51	Data	AB22	IO	$G1V_{DD}$	---
D1_MDQ52	Data	Y22	IO	$G1V_{DD}$	---
D1_MDQ53	Data	AA23	IO	$G1V_{DD}$	---
D1_MDQ54	Data	AD22	IO	$G1V_{DD}$	---
D1_MDQ55	Data	AE22	IO	$G1V_{DD}$	---
D1_MDQ56	Data	AH25	IO	$G1V_{DD}$	---
D1_MDQ57	Data	AF24	IO	$G1V_{DD}$	---
D1_MDQ58	Data	AG22	IO	$G1V_{DD}$	---
D1_MDQ59	Data	AF22	IO	$G1V_{DD}$	---
D1_MDQ60	Data	AH26	IO	$G1V_{DD}$	---
D1_MDQ61	Data	AG25	IO	$G1V_{DD}$	---
D1_MDQ62	Data	AF23	IO	$G1V_{DD}$	---
D1_MDQ63	Data	AH22	IO	$G1V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MDQS0	Data Strobe	A25	IO	$G1V_{DD}$	---
D1_MDQS0_B	Data Strobe	A24	IO	$G1V_{DD}$	---
D1_MDQS1	Data Strobe	D23	IO	$G1V_{DD}$	---
D1_MDQS1_B	Data Strobe	C23	IO	$G1V_{DD}$	---
D1_MDQS2	Data Strobe	F25	IO	$G1V_{DD}$	---
D1_MDQS2_B	Data Strobe	F26	IO	$G1V_{DD}$	---
D1_MDQS3	Data Strobe	K26	IO	$G1V_{DD}$	---
D1_MDQS3_B	Data Strobe	K25	IO	$G1V_{DD}$	---
D1_MDQS4	Data Strobe	W26	IO	$G1V_{DD}$	---
D1_MDQS4_B	Data Strobe	W25	IO	$G1V_{DD}$	---
D1_MDQS5	Data Strobe	AC25	IO	$G1V_{DD}$	---
D1_MDQS5_B	Data Strobe	AC26	IO	$G1V_{DD}$	---
D1_MDQS6	Data Strobe	AE23	IO	$G1V_{DD}$	---
D1_MDQS6_B	Data Strobe	AD23	IO	$G1V_{DD}$	---
D1_MDQS7	Data Strobe	AH23	IO	$G1V_{DD}$	---
D1_MDQS7_B	Data Strobe	AG23	IO	$G1V_{DD}$	---
D1_MDQS8	Data Strobe	P25	IO	$G1V_{DD}$	---
D1_MDQS8_B	Data Strobe	P26	IO	$G1V_{DD}$	---
D1_MECC0	Error Correcting Code	M26	IO	$G1V_{DD}$	---
D1_MECC1	Error Correcting Code	N25	IO	$G1V_{DD}$	---
D1_MECC2	Error Correcting Code	T25	IO	$G1V_{DD}$	---
D1_MECC3	Error Correcting Code	T24	IO	$G1V_{DD}$	---
D1_MECC4	Error Correcting Code	M25	IO	$G1V_{DD}$	---
D1_MECC5	Error Correcting Code	N24	IO	$G1V_{DD}$	---
D1_MECC6	Error Correcting Code	R25	IO	$G1V_{DD}$	---
D1_MECC7	Error Correcting Code	R24	IO	$G1V_{DD}$	---
D1_MODT0	On Die Termination	AD28	O	$G1V_{DD}$	1
D1_MODT1	On Die Termination	AF27	O	$G1V_{DD}$	1
D1_MPAR	Address Parity Out	V28	O	$G1V_{DD}$	1
D1_MRAS_B	Row Address Strobe / MA[16]	AA28	O	$G1V_{DD}$	1
D1_MWE_B	Write Enable / MA[14]	AB28	O	$G1V_{DD}$	1
Integrated Flash Controller					
IFC_A00/GPIO1_16/ QSPI_A_CS0	IFC Address	D8	O	OV_{DD}	1, 5
IFC_A01/GPIO1_17/ QSPI_A_CS1	IFC Address	C8	O	OV_{DD}	1, 5
IFC_A02/GPIO1_18/ QSPI_A_SCK	IFC Address	C9	O	OV_{DD}	1, 5

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IFC_A03/GPIO1_19/ QSPI_B_CS0	IFC Address	D10	O	OV_{DD}	1, 5
IFC_A04/GPIO1_20/ QSPI_B_CS1	IFC Address	C10	O	OV_{DD}	1, 5
IFC_A05/GPIO1_21/ QSPI_B_SCK/cfg_dram_type	IFC Address	C11	O	OV_{DD}	1, 4
IFC_A06/GPIO2_00/ IFC_WP1_B/QSPI_A_DATA0	IFC Address	D11	O	OV_{DD}	1
IFC_A07/GPIO2_01/ IFC_WP2_B/QSPI_A_DATA1	IFC Address	C12	O	OV_{DD}	1
IFC_A08/GPIO2_02/ IFC_WP3_B/QSPI_A_DATA2	IFC Address	D13	O	OV_{DD}	1
IFC_A09/GPIO2_03/ IFC_RB2_B/IFC_CS_B4/ QSPI_A_DATA3	IFC Address	C13	O	OV_{DD}	1
IFC_A10/GPIO2_04/ IFC_RB3_B/IFC_CS_B5/ QSPI_A_DQS	IFC Address	D14	O	OV_{DD}	1
IFC_A11/GPIO2_05/ IFC_CS_B6/QSPI_B_DQS	IFC Address	C14	O	OV_{DD}	1
IFC_AD00/GPIO1_00/ cfg_gpinput0	IFC Address / Data	B12	IO	OV_{DD}	4, 9
IFC_AD01/GPIO1_01/ cfg_gpinput1	IFC Address / Data	A11	IO	OV_{DD}	4, 9
IFC_AD02/GPIO1_02/ cfg_gpinput2	IFC Address / Data	B11	IO	OV_{DD}	4, 9
IFC_AD03/GPIO1_03/ cfg_gpinput3	IFC Address / Data	A10	IO	OV_{DD}	4, 9
IFC_AD04/GPIO1_04/ cfg_gpinput4	IFC Address / Data	A9	IO	OV_{DD}	4, 9
IFC_AD05/GPIO1_05/ cfg_gpinput5	IFC Address / Data	B9	IO	OV_{DD}	4, 9
IFC_AD06/GPIO1_06/ cfg_gpinput6	IFC Address / Data	A8	IO	OV_{DD}	4, 9
IFC_AD07/GPIO1_07/ cfg_gpinput7	IFC Address / Data	B8	IO	OV_{DD}	4, 9
IFC_AD08/GPIO1_08/ cfg_rcw_src1	IFC Address / Data	A12	IO	OV_{DD}	4, 9
IFC_AD09/GPIO1_09/ cfg_rcw_src2	IFC Address / Data	A13	IO	OV_{DD}	4, 9
IFC_AD10/GPIO1_10/ cfg_rcw_src3	IFC Address / Data	B14	IO	OV_{DD}	4, 9
IFC_AD11/GPIO1_11/ cfg_rcw_src4	IFC Address / Data	A14	IO	OV_{DD}	4, 9

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IFC_AD12/GPIO1_12/ cfg_rcw_src5	IFC Address / Data	B15	IO	OV_{DD}	4, 9
IFC_AD13/GPIO1_13/ cfg_rcw_src6	IFC Address / Data	A15	IO	OV_{DD}	4, 9
IFC_AD14/GPIO1_14/ cfg_rcw_src7	IFC Address / Data	A16	IO	OV_{DD}	4, 9
IFC_AD15/GPIO1_15/ cfg_rcw_src8	IFC Address / Data	A17	IO	OV_{DD}	4, 9
IFC_ALE/GPIO1_24	IFC Address Latch Enable	A18	O	OV_{DD}	1, 5
IFC_BCTL/GPIO2_12	IFC Buffer control	E15	O	OV_{DD}	1
IFC_CLE/GPIO1_25/ cfg_rcw_src0	IFC NAND Command Latch Enable / Write Enable 1 / NOR Address active-low Valid	C19	O	OV_{DD}	1, 4
IFC_CLK0/GPIO2_17	IFC Clock	A20	O	OV_{DD}	1
IFC_CLK1/GPIO2_18	IFC Clock	B20	O	OV_{DD}	1
IFC_CS0_B/GPIO2_08	IFC Chip Select	C17	O	OV_{DD}	1, 6
IFC_CS1_B/GPIO2_09	IFC Chip Select	A19	O	OV_{DD}	1, 6
IFC_CS2_B/GPIO2_10	IFC Chip Select	D20	O	OV_{DD}	1, 6
IFC_CS3_B/GPIO2_11/ QSPI_B_DATA3/ QSPI_A_DATA7	IFC Chip Select	C20	O	OV_{DD}	1, 6
IFC_CS_B4/**IFC_A09**/ GPIO2_03/IFC_RB2_B/ QSPI_A_DATA3	IFC Chip Select	C13	O	OV_{DD}	1
IFC_CS_B5/**IFC_A10**/ GPIO2_04/IFC_RB3_B/ QSPI_A_DQS	IFC Chip Select	D14	O	OV_{DD}	1
IFC_CS_B6/**IFC_A11**/ GPIO2_05/QSPI_B_DQS	IFC Chip Select	C14	O	OV_{DD}	1
IFC_NDDQS/GPIO2_13	IFC DQS Strobe	B17	IO	OV_{DD}	9
IFC_NDWE_B/GPIO2_19	IFC NAND Write Enable / NAND DDR Clock	E16	O	OV_{DD}	1
IFC_OE_B/GPIO1_26/ cfg_eng_use1	IFC Output Enable	C18	O	OV_{DD}	1, 5
IFC_PAR0/GPIO2_06/ QSPI_B_DATA0/ QSPI_A_DATA4	IFC Address & Data Parity	B18	IO	OV_{DD}	9
IFC_PAR1/GPIO2_07/ QSPI_B_DATA1/ QSPI_A_DATA5	IFC Address & Data Parity	D17	IO	OV_{DD}	9
IFC_PERR_B/GPIO2_16/ QSPI_B_DATA2/ QSPI_A_DATA6	IFC Parity Error	E17	I	OV_{DD}	1
IFC_RB0_B/GPIO2_14	IFC Ready/Busy CS0	C16	I	OV_{DD}	1, 6

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IFC_RB1_B/GPIO2_15	IFC Ready/Busy CS1	D16	I	OV_{DD}	1, 6
IFC_RB2_B/**IFC_A09**/ GPIO2_03/IFC_CS_B4/ QSPI_A_DATA3	IFC Ready/Busy CS 2	C13	I	OV_{DD}	1
IFC_RB3_B/**IFC_A10**/ GPIO2_04/IFC_CS_B5/ QSPI_A_DQS	IFC Ready/Busy CS 3	D14	I	OV_{DD}	1
IFC_TE/GPIO1_23/cfg_ifc_te	IFC External Transceiver Enable	E14	O	OV_{DD}	1, 4
IFC_WE0_B/GPIO1_22/ cfg_eng_use0	IFC Write Enable 0 / Start of Frame	C15	O	OV_{DD}	1, 4, 19
IFC_WP0_B/GPIO1_27/ cfg_eng_use2	IFC Write Protect	D19	O	OV_{DD}	1, 5
IFC_WP1_B/**IFC_A06**/ GPIO2_00/QSPI_A_DATA0	IFC Write Protect	D11	O	OV_{DD}	1
IFC_WP2_B/**IFC_A07**/ GPIO2_01/QSPI_A_DATA1	IFC Write Protect	C12	O	OV_{DD}	1
IFC_WP3_B/**IFC_A08**/ GPIO2_02/QSPI_A_DATA2	IFC Write Protect	D13	O	OV_{DD}	1
DUART1					
UART1_CTS_B/GPIO3_10/ UART3_SIN	Clear To Send	J1	I	DV_{DD}	1
UART1_RTS_B/GPIO3_08/ UART3_SOUT	Ready to Send	J2	O	DV_{DD}	1
UART1_SIN	Receive Data	H2	I	DV_{DD}	1
UART1_SOUT	Transmit Data	H1	O	DV_{DD}	1
DUART2					
UART2_CTS_B/GPIO3_11/ UART4_SIN	Clear To Send	M2	I	DV_{DD}	1
UART2_RTS_B/GPIO3_09/ UART4_SOUT	Ready to Send	L1	O	DV_{DD}	1
UART2_SIN/GPIO3_07	Receive Data	K1	I	DV_{DD}	1
UART2_SOUT/GPIO3_06	Transmit Data	L2	O	DV_{DD}	1
DUART3 and 4					
UART3_SIN/**UART1_CTS_B**/ GPIO3_10	Receive Data	J1	I	DV_{DD}	1
UART3_SOUT/ **UART1_RTS_B**/GPIO3_08	Transmit Data	J2	O	DV_{DD}	1
UART4_SIN/**UART2_CTS_B**/ GPIO3_11	Receive Data	M2	I	DV_{DD}	1
UART4_SOUT/ **UART2_RTS_B**/GPIO3_09	Transmit Data	L1	O	DV_{DD}	1
I2C1					

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IIC1_SCL	Serial Clock	N1	IO	DV_{DD}	7, 8
IIC1_SDA	Serial Data	M1	IO	DV_{DD}	7, 8
I2C2					
IIC2_SCL/GPIO3_12/ SDHC_CD_B/CLK9/BRGO2	Serial Clock	K3	IO	DV_{DD}	7, 8
IIC2_SDA/GPIO3_13/ SDHC_WP/CLK10/BRGO3	Serial Data	L3	IO	DV_{DD}	7, 8
I2C3 and 4					
IIC3_SCL/GPIO4_28/EVT5_B/ USB2_DRVVBUS/BRGO4/ CLK11	Serial Clock	L4	IO	DV_{DD}	7, 8
IIC3_SDA/GPIO4_29/EVT6_B/ USB2_PWRFAULT/BRGO1/ CLK12_CLK8	Serial Data	M4	IO	DV_{DD}	7, 8
IIC4_SCL/GPIO4_30/EVT7_B/ TDMA_RQ/UC1_CDB_RXER	Serial Clock	M3	IO	DV_{DD}	7, 8
IIC4_SDA/GPIO4_31/EVT8_B/ TDMB_RQ/UC3_CDB_RXER	Serial Data	N3	IO	DV_{DD}	7, 8
SPI Interface					
SPI_PCS0/GPIO3_17/ SDHC_DAT4/SDHC_VS	SPI Chip Select	U1	IO	OV_{DD}	---
SPI_PCS1/GPIO3_18/ SDHC_DAT5/ SDHC_CMD_DIR	SPI Chip Select	R3	O	OV_{DD}	1
SPI_PCS2/GPIO3_19/ SDHC_DAT6/ SDHC_DAT0_DIR	SPI Chip Select	T3	O	OV_{DD}	1
SPI_PCS3/GPIO3_20/ SDHC_DAT7/ SDHC_DAT123_DIR	SPI Chip Select	V1	O	OV_{DD}	1
SPI_SCK/GPIO3_16/ SDHC_GATE_IN	SPI Clock	U2	IO	OV_{DD}	---
SPI_SIN/GPIO3_15/ SDHC_CLK_SYNC_IN	Master In Slave Out	U3	I	OV_{DD}	1
SPI_SOUT/GPIO3_14/ SDHC_CLK_SYNC_OUT	Master Out Slave In	V3	O	OV_{DD}	1
eSDHC					
SDHC_CD_B/**IIC2_SCL**/ GPIO3_12/CLK9/BRGO2	Command	K3	I	DV_{DD}	1
SDHC_CLK/GPIO3_26	Host to Card Clock	P3	O	EV_{DD}	1
SDHC_CLK_SYNC_IN/ **SPI_SIN**/GPIO3_15	IN	U3	I	OV_{DD}	1
SDHC_CLK_SYNC_OUT/ **SPI_SOUT**/GPIO3_14	OUT	V3	O	OV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SDHC_CMD/GPIO3_21	Command/Response	P2	IO	EV_{DD}	6
SDHC_CMD_DIR/**SPI_PCS1**/ GPIO3_18/SDHC_DAT5	DIR	R3	O	OV_{DD}	1
SDHC_DAT0/GPIO3_22	Data	P1	IO	EV_{DD}	6
SDHC_DAT0_DIR/**SPI_PCS2**/ GPIO3_19/SDHC_DAT6	DIR	T3	O	OV_{DD}	1
SDHC_DAT1/GPIO3_23	Data	R2	IO	EV_{DD}	6
SDHC_DAT123_DIR/ **SPI_PCS3**/GPIO3_20/ SDHC_DAT7	DIR	V1	O	OV_{DD}	1
SDHC_DAT2/GPIO3_24	Data	R1	IO	EV_{DD}	6
SDHC_DAT3/GPIO3_25	Data	T1	IO	EV_{DD}	6
SDHC_DAT4/**SPI_PCS0**/ GPIO3_17/SDHC_VS	Data	U1	IO	OV_{DD}	---
SDHC_DAT5/**SPI_PCS1**/ GPIO3_18/SDHC_CMD_DIR	Data	R3	IO	OV_{DD}	---
SDHC_DAT6/**SPI_PCS2**/ GPIO3_19/SDHC_DAT0_DIR	Data	T3	IO	OV_{DD}	---
SDHC_DAT7/**SPI_PCS3**/ GPIO3_20/ SDHC_DAT123_DIR	Data	V1	IO	OV_{DD}	---
SDHC_GATE_IN/**SPI_SCK**/ GPIO3_16	IN	U2	I	OV_{DD}	1
SDHC_VS/**SPI_PCS0**/ GPIO3_17/SDHC_DAT4	VS	U1	O	OV_{DD}	1
SDHC_WP/**IIC2_SDA**/ GPIO3_13/CLK10/BRGO3	Write Protect	L3	I	DV_{DD}	1
Interrupt Controller					
EVT9_B/GPIO4_10	Interrupt Output	G7	IO	OV_{DD}	7, 9
IRQ00	External Interrupt	F11	I	OV_{DD}	1
IRQ01	External Interrupt	F15	I	OV_{DD}	1
IRQ02	External Interrupt	H7	I	OV_{DD}	1
IRQ03/GPIO3_27/ TDMB_TSYNC/ UC3_RTSB_TXEN	External Interrupt	J3	I	DV_{DD}	1
IRQ04/GPIO3_28/ TDMA_RXD/UC1_RXD7/ TDMA_TXD	External Interrupt	J4	I	DV_{DD}	1
IRQ05/GPIO3_29/ TDMA_RSYNC/ UC1_CTSB_RXDV	External Interrupt	J5	I	DV_{DD}	1
IRQ06/GPIO4_04/ TDMA_RXD_EXC/ TDMA_TXD/UC1_TXD7	External Interrupt	K5	I	DV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IRQ07/GPIO4_05/ TDMA_TSYNC/ UC1_RTSB_TXEN	External Interrupt	L5	I	DV_{DD}	1
IRQ08/GPIO4_06/ TDMB_RXD/UC3_RXD7/ TDMB_TXD	External Interrupt	M5	I	DV_{DD}	1
IRQ09/GPIO4_07/ TDMB_RSYNC/ UC3_CTSB_RXDV	External Interrupt	N5	I	DV_{DD}	1
IRQ10/GPIO4_08/ TDMB_RXD_EXC/ TDMB_TXD/UC3_TXD7	External Interrupt	P4	I	DV_{DD}	1
IRQ11/GPIO4_09	External Interrupt	W3	I	LV_{DD}	1
Debug					
ASLEEP/GPIO1_28/ cfg_soc_use	Asleep	E9	O	OV_{DD}	1, 4
CKSTP_OUT_B	Checkstop Out	G15	O	OV_{DD}	1, 6, 7
CLK_OUT	Clock Out	G16	O	OV_{DD}	2
EVT0_B	Event 0	E10	IO	OV_{DD}	9
EVT1_B	Event 1	E13	IO	OV_{DD}	9
EVT2_B	Event 2	E8	IO	OV_{DD}	9
EVT3_B	Event 3	E12	IO	OV_{DD}	9
EVT4_B	Event 4	E11	IO	OV_{DD}	9
EVT5_B/**IIC3_SCL**/GPIO4_28/ USB2_DRVVBUS/BRGO4/ CLK11	Event 5	L4	IO	DV_{DD}	---
EVT6_B/**IIC3_SDA**/GPIO4_29/ USB2_PWRFAULT/BRGO1/ CLK12_CLK8	Event 6	M4	IO	DV_{DD}	---
EVT7_B/**IIC4_SCL**/GPIO4_30/ TDMA_RQ/UC1_CDB_RXER	Event 7	M3	IO	DV_{DD}	---
EVT8_B/**IIC4_SDA**/GPIO4_31/ TDMB_RQ/UC3_CDB_RXER	Event 8	N3	IO	DV_{DD}	---
Trust					
TA_BB_TMP_DETECT_B	Battery Backed Tamper Detect	H12	I	$TA_BB_V_{DD}$	---
TA_TMP_DETECT_B	Tamper Detect	H20	I	OV_{DD}	---
System Control					
HRESET_B	Hard Reset	F8	IO	OV_{DD}	6, 7
PORESET_B	Power On Reset	F9	I	OV_{DD}	---
RESET_REQ_B	Reset Request (POR or Hard)	F10	O	OV_{DD}	1, 5
Clocking					
DIFF_SYSCLK	Single Source System Clock Differential (positive)	AA13	I	SV_{DD}	20

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
DIFF_SYSCLK_B	Single Source System Clock Differential (negative)	AB13	I	SV_{DD}	20
RTC/GPIO3_30	Real Time Clock	F17	I	OV_{DD}	1
SYSCLK	System Clock	G14	I	OV_{DD}	---
DDR Clocking					
DDRCLK	DDR Controller Clock	J20	I	OV_{DD}	---
DFT					
JTAG_BSR_VSEL	Reserved	J19	I	OV_{DD}	15
SCAN_MODE_B	Reserved	H19	I	OV_{DD}	10
TBSCAN_EN_B	Test Boundary Scan Enable	F19	I	OV_{DD}	6
TEST_SEL_B	Reserved	F20	I	OV_{DD}	10
JTAG					
TCK	Test Clock	E18	I	OV_{DD}	---
TDI	Test Data In	G17	I	OV_{DD}	9
TDO	Test Data Out	E20	O	OV_{DD}	2
TMS	Test Mode Select	G18	I	OV_{DD}	9
TRST_B	Test Reset	E19	I	OV_{DD}	9
Analog Signals					
D1_TPA	Reserved	F21	IO		12
FA_ANALOG_G_V	Reserved	AG21	IO		15
FA_ANALOG_PIN	Reserved	AD21	IO		15
TD1_ANODE	Thermal diode anode	J13	IO		17
TD1_CATHODE	Thermal diode cathode	H13	IO		17
TH_TPA	Reserved	H8	-	-	12
SerDes 1					
SD1_IMP_CAL_RX	SerDes Receive Impedence Calibration	Y11	I	SV_{DD}	11
SD1_IMP_CAL_TX	SerDes Transmit Impedance Calibration	AA6	I	XV_{DD}	16
SD1_PLL1_TPA	SerDes PLL 1 Test Point Analog	AF12	O	AVDD_SD1_PLL1	12
SD1_PLL1_TPD	SerDes Test Point Digital	AF13	O	XV_{DD}	12
SD1_PLL2_TPA	SerDes PLL 2 Test Point Analog	AF5	O	AVDD_SD1_PLL2	12
SD1_PLL2_TPD	SerDes Test Point Digital	AB5	O	XV_{DD}	12
SD1_REF_CLK1_N	SerDes PLL 1 Reference Clock Complement	AH13	I	SV_{DD}	---
SD1_REF_CLK1_P	SerDes PLL 1 Reference Clock	AG13	I	SV_{DD}	---
SD1_REF_CLK2_N	SerDes PLL 2 Reference Clock Complement	AB8	I	SV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD1_REF_CLK2_P	SerDes PLL 2 Reference Clock	AA8	I	SV_{DD}	---
SD1_RX0_N	SerDes Receive Data (negative)	AH6	I	SV_{DD}	---
SD1_RX0_P	SerDes Receive Data (positive)	AG6	I	SV_{DD}	---
SD1_RX1_N	SerDes Receive Data (negative)	AH8	I	SV_{DD}	---
SD1_RX1_P	SerDes Receive Data (positive)	AG8	I	SV_{DD}	---
SD1_RX2_N	SerDes Receive Data (negative)	AH10	I	SV_{DD}	---
SD1_RX2_P	SerDes Receive Data (positive)	AG10	I	SV_{DD}	---
SD1_RX3_N	SerDes Receive Data (negative)	AH11	I	SV_{DD}	---
SD1_RX3_P	SerDes Receive Data (positive)	AG11	I	SV_{DD}	---
SD1_TX0_N	SerDes Transmit Data (negative)	AE6	O	XV_{DD}	---
SD1_TX0_P	SerDes Transmit Data (positive)	AD6	O	XV_{DD}	---
SD1_TX1_N	SerDes Transmit Data (negative)	AE8	O	XV_{DD}	---
SD1_TX1_P	SerDes Transmit Data (positive)	AD8	O	XV_{DD}	---
SD1_TX2_N	SerDes Transmit Data (negative)	AE10	O	XV_{DD}	---
SD1_TX2_P	SerDes Transmit Data (positive)	AD10	O	XV_{DD}	---
SD1_TX3_N	SerDes Transmit Data (negative)	AE11	O	XV_{DD}	---
SD1_TX3_P	SerDes Transmit Data (positive)	AD11	O	XV_{DD}	---
SerDes 2					
SD2_IMP_CAL_RX	SerDes Receive Impedence Calibration	Y12	I	SV_{DD}	11
SD2_IMP_CAL_TX	SerDes Transmit Impedance Calibration	Y20	I	XV_{DD}	16
SD2_PLL1_TPA	SerDes PLL 1 Test Point Analog	AF14	O	AVDD_SD2_PLL1	12
SD2_PLL1_TPD	SerDes Test Point Digital	AC13	O	XV_{DD}	12
SD2_PLL2_TPA	SerDes PLL 2 Test Point Analog	AF20	O	AVDD_SD2_PLL2	12
SD2_PLL2_TPD	SerDes Test Point Digital	AA20	O	XV_{DD}	12

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD2_REF_CLK1_N	SerDes PLL 1 Reference Clock Complement	AE13	I	SV_{DD}	---
SD2_REF_CLK1_P	SerDes PLL 1 Reference Clock	AD13	I	SV_{DD}	---
SD2_REF_CLK2_N	SerDes PLL 2 Reference Clock Complement	AB19	I	SV_{DD}	---
SD2_REF_CLK2_P	SerDes PLL 2 Reference Clock	AB18	I	SV_{DD}	---
SD2_RX0_N	SerDes Receive Data (negative)	AH15	I	SV_{DD}	---
SD2_RX0_P	SerDes Receive Data (positive)	AG15	I	SV_{DD}	---
SD2_RX1_N	SerDes Receive Data (negative)	AH16	I	SV_{DD}	---
SD2_RX1_P	SerDes Receive Data (positive)	AG16	I	SV_{DD}	---
SD2_RX2_N	SerDes Receive Data (negative)	AH18	I	SV_{DD}	---
SD2_RX2_P	SerDes Receive Data (positive)	AG18	I	SV_{DD}	---
SD2_RX3_N	SerDes Receive Data (negative)	AH19	I	SV_{DD}	---
SD2_RX3_P	SerDes Receive Data (positive)	AG19	I	SV_{DD}	---
SD2_TX0_N	SerDes Transmit Data (negative)	AE15	O	XV_{DD}	---
SD2_TX0_P	SerDes Transmit Data (positive)	AD15	O	XV_{DD}	---
SD2_TX1_N	SerDes Transmit Data (negative)	AE16	O	XV_{DD}	---
SD2_TX1_P	SerDes Transmit Data (positive)	AD16	O	XV_{DD}	---
SD2_TX2_N	SerDes Transmit Data (negative)	AE18	O	XV_{DD}	---
SD2_TX2_P	SerDes Transmit Data (positive)	AD18	O	XV_{DD}	---
SD2_TX3_N	SerDes Transmit Data (negative)	AE19	O	XV_{DD}	---
SD2_TX3_P	SerDes Transmit Data (positive)	AD19	O	XV_{DD}	---
USB PHY 1					
USB1_D_M	USB PHY HS Data (-)	E6	IO	-	---
USB1_D_P	USB PHY HS Data (+)	F6	IO	-	---
USB1_ID	USB PHY ID Detect	F5	I	-	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
USB1_RESREF	USB PHY Impedance Calibration	G3	IO	-	---
USB1_RX_M	USB PHY SS Receive Data (-)	E4	I	-	---
USB1_RX_P	USB PHY SS Receive Data (+)	E3	I	-	---
USB1_TX_M	USB PHY SS Transmit Data (-)	F2	O	-	---
USB1_TX_P	USB PHY SS Transmit Data (+)	F1	O	-	---
USB1_VBUS	USB PHY VBUS	E7	I	-	---
USB PHY 2					
USB2_D_M	USB PHY HS Data (-)	C6	IO	-	---
USB2_D_P	USB PHY HS Data (+)	D6	IO	-	---
USB2_ID	USB PHY ID Detect	D5	I	-	---
USB2_RESREF	USB PHY Impedance Calibration	G4	IO	-	---
USB2_RX_M	USB PHY SS Receive Data (-)	C4	I	-	---
USB2_RX_P	USB PHY SS Receive Data (+)	C3	I	-	---
USB2_TX_M	USB PHY SS Transmit Data (-)	D2	O	-	---
USB2_TX_P	USB PHY SS Transmit Data (+)	D1	O	-	---
USB2_VBUS	USB PHY VBUS	C7	I	-	---
USB1 and 2					
USB2_DRVVBUS/**IIC3_SCL**/ GPIO4_28/EVT5_B/BRGO4/ CLK11	DRV VBus	L4	O	DV_{DD}	1
USB2_PWRFAULT/**IIC3_SDA**/ GPIO4_29/EVT6_B/BRGO1/ CLK12_CLK8	PWR Fault	M4	I	DV_{DD}	1
USB_DRVVBUS/GPIO4_02	USB_DRVVBUS	H6	O	DV_{DD}	1
USB_PWRFAULT/GPIO4_03	USB_PWRFAULT	G6	I	DV_{DD}	1
Ethernet Management Interface 1					
EMI1_MDC/GPIO4_00	Management Data Clock	AG2	O	LV_{DD}	1, 13
EMI1_MDIO/GPIO4_01	Management Data In/Out	AF2	IO	LV_{DD}	13
Ethernet Management Interface 2					
EMI2_MDC/GPIO2_20	Management Data Clock	AH4	O	TV_{DD}	1
EMI2_MDIO/GPIO2_21	Management Data In/Out	AH3	IO	TV_{DD}	---
Ethernet Controller 1					
EC1_GTX_CLK/GPIO2_27	Transmit Clock Out	W4	O	LV_{DD}	1
EC1_GTX_CLK125/GPIO2_28	Reference Clock	AC3	I	LV_{DD}	1
EC1_RXD0/GPIO4_12	Receive Data	AA2	I	LV_{DD}	1
EC1_RXD1/GPIO4_11	Receive Data	AA1	I	LV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
EC1_RXD2/GPIO2_30	Receive Data	Y1	I	LV_{DD}	1
EC1_RXD3/GPIO2_29	Receive Data	W2	I	LV_{DD}	1
EC1_RX_CLK/GPIO4_13	Receive Clock	W1	I	LV_{DD}	1
EC1_RX_DV/GPIO4_14	Receive Data Valid	AB1	I	LV_{DD}	1
EC1_TXD0/GPIO2_25	Transmit Data	AB3	O	LV_{DD}	1
EC1_TXD1/GPIO2_24	Transmit Data	AA3	O	LV_{DD}	1
EC1_TXD2/GPIO2_23	Transmit Data	Y4	O	LV_{DD}	1
EC1_TXD3/GPIO2_22	Transmit Data	Y3	O	LV_{DD}	1
EC1_TX_EN/GPIO2_26	Transmit Enable	AB4	O	LV_{DD}	1, 14
Ethernet Controller 2					
EC2_GTX_CLK/GPIO4_20	Transmit Clock Out	AC4	O	LV_{DD}	1
EC2_GTX_CLK125/GPIO4_21	Reference Clock	AG4	I	LV_{DD}	1
EC2_RXD0/GPIO4_25/ TSEC_1588_TRIG_IN2	Receive Data	AE2	I	LV_{DD}	1
EC2_RXD1/GPIO4_24/ TSEC_1588_PULSE_OUT1	Receive Data	AE1	I	LV_{DD}	1
EC2_RXD2/GPIO4_23	Receive Data	AD1	I	LV_{DD}	1
EC2_RXD3/GPIO4_22	Receive Data	AC2	I	LV_{DD}	1
EC2_RX_CLK/GPIO4_26/ TSEC_1588_CLK_IN	Receive Clock	AC1	I	LV_{DD}	1
EC2_RX_DV/GPIO4_27/ TSEC_1588_TRIG_IN1	Receive Data Valid	AF1	I	LV_{DD}	1
EC2_TXD0/GPIO4_18/ TSEC_1588_PULSE_OUT2	Transmit Data	AF3	O	LV_{DD}	1
EC2_TXD1/GPIO4_17/ TSEC_1588_CLK_OUT	Transmit Data	AE4	O	LV_{DD}	1
EC2_TXD2/GPIO4_16/ TSEC_1588_ALARM_OUT1	Transmit Data	AE3	O	LV_{DD}	1
EC2_TXD3/GPIO4_15/ TSEC_1588_ALARM_OUT2	Transmit Data	AD3	O	LV_{DD}	1
EC2_TX_EN/GPIO4_19	Transmit Enable	AG3	O	LV_{DD}	1, 14
General Purpose Input/Output					
GPIO1_00/**IFC_AD00**/ cfg_gpinput0	General Purpose Input/Output	B12	O	OV_{DD}	1, 4
GPIO1_01/**IFC_AD01**/ cfg_gpinput1	General Purpose Input/Output	A11	O	OV_{DD}	1, 4
GPIO1_02/**IFC_AD02**/ cfg_gpinput2	General Purpose Input/Output	B11	O	OV_{DD}	1, 4
GPIO1_03/**IFC_AD03**/ cfg_gpinput3	General Purpose Input/Output	A10	O	OV_{DD}	1, 4
GPIO1_04/**IFC_AD04**/ cfg_gpinput4	General Purpose Input/Output	A9	O	OV_{DD}	1, 4

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO1_05/**IFC_AD05**/ cfg_gpinput5	General Purpose Input/Output	B9	O	OV_{DD}	1, 4
GPIO1_06/**IFC_AD06**/ cfg_gpinput6	General Purpose Input/Output	A8	O	OV_{DD}	1, 4
GPIO1_07/**IFC_AD07**/ cfg_gpinput7	General Purpose Input/Output	B8	O	OV_{DD}	1, 4
GPIO1_08/**IFC_AD08**/ cfg_rcw_src1	General Purpose Input/Output	A12	O	OV_{DD}	1, 4
GPIO1_09/**IFC_AD09**/ cfg_rcw_src2	General Purpose Input/Output	A13	O	OV_{DD}	1, 4
GPIO1_10/**IFC_AD10**/ cfg_rcw_src3	General Purpose Input/Output	B14	O	OV_{DD}	1, 4
GPIO1_11/**IFC_AD11**/ cfg_rcw_src4	General Purpose Input/Output	A14	O	OV_{DD}	1, 4
GPIO1_12/**IFC_AD12**/ cfg_rcw_src5	General Purpose Input/Output	B15	O	OV_{DD}	1, 4
GPIO1_13/**IFC_AD13**/ cfg_rcw_src6	General Purpose Input/Output	A15	O	OV_{DD}	1, 4
GPIO1_14/**IFC_AD14**/ cfg_rcw_src7	General Purpose Input/Output	A16	O	OV_{DD}	1, 4
GPIO1_15/**IFC_AD15**/ cfg_rcw_src8	General Purpose Input/Output	A17	O	OV_{DD}	1, 4
GPIO1_16/**IFC_A00**/ QSPI_A_CS0	General Purpose Input/Output	D8	O	OV_{DD}	1, 5
GPIO1_17/**IFC_A01**/ QSPI_A_CS1	General Purpose Input/Output	C8	O	OV_{DD}	1, 5
GPIO1_18/**IFC_A02**/ QSPI_A_SCK	General Purpose Input/Output	C9	O	OV_{DD}	1, 5
GPIO1_19/**IFC_A03**/ QSPI_B_CS0	General Purpose Input/Output	D10	O	OV_{DD}	1, 5
GPIO1_20/**IFC_A04**/ QSPI_B_CS1	General Purpose Input/Output	C10	O	OV_{DD}	1, 5
GPIO1_21/**IFC_A05**/ QSPI_B_SCK/cfg_dram_type	General Purpose Input/Output	C11	O	OV_{DD}	1, 4
GPIO1_22/**IFC_WE0_B**/ cfg_eng_use0	General Purpose Input/Output	C15	O	OV_{DD}	1, 4, 19
GPIO1_23/**IFC_TE**/cfg_ifc_te	General Purpose Input/Output	E14	O	OV_{DD}	1, 4
GPIO1_24/**IFC_ALE**	General Purpose Input/Output	A18	O	OV_{DD}	1, 5
GPIO1_25/**IFC_CLE**/ cfg_rcw_src0	General Purpose Input/Output	C19	O	OV_{DD}	1, 4
GPIO1_26/**IFC_OE_B**/ cfg_eng_use1	General Purpose Input/Output	C18	O	OV_{DD}	1, 5
GPIO1_27/**IFC_WP0_B**/ cfg_eng_use2	General Purpose Input/Output	D19	O	OV_{DD}	1, 5

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO1_28/**ASLEEP**/ cfg_soc_use	General Purpose Input/Output	E9	O	OV_{DD}	1, 4
GPIO2_00/**IFC_A06**/ IFC_WP1_B/QSPI_A_DATA0	General Purpose Input/Output	D11	IO	OV_{DD}	---
GPIO2_01/**IFC_A07**/ IFC_WP2_B/QSPI_A_DATA1	General Purpose Input/Output	C12	IO	OV_{DD}	---
GPIO2_02/**IFC_A08**/ IFC_WP3_B/QSPI_A_DATA2	General Purpose Input/Output	D13	IO	OV_{DD}	---
GPIO2_03/**IFC_A09**/ IFC_RB2_B/IFC_CS_B4/ QSPI_A_DATA3	General Purpose Input/Output	C13	IO	OV_{DD}	---
GPIO2_04/**IFC_A10**/ IFC_RB3_B/IFC_CS_B5/ QSPI_A_DQS	General Purpose Input/Output	D14	IO	OV_{DD}	---
GPIO2_05/**IFC_A11**/ IFC_CS_B6/QSPI_B_DQS	General Purpose Input/Output	C14	IO	OV_{DD}	---
GPIO2_06/**IFC_PAR0**/ QSPI_B_DATA0/ QSPI_A_DATA4	General Purpose Input/Output	B18	IO	OV_{DD}	---
GPIO2_07/**IFC_PAR1**/ QSPI_B_DATA1/ QSPI_A_DATA5	General Purpose Input/Output	D17	IO	OV_{DD}	---
GPIO2_08/**IFC_CS0_B**	General Purpose Input/Output	C17	IO	OV_{DD}	---
GPIO2_09/**IFC_CS1_B**	General Purpose Input/Output	A19	IO	OV_{DD}	---
GPIO2_10/**IFC_CS2_B**	General Purpose Input/Output	D20	IO	OV_{DD}	---
GPIO2_11/**IFC_CS3_B**/ QSPI_B_DATA3/ QSPI_A_DATA7	General Purpose Input/Output	C20	IO	OV_{DD}	---
GPIO2_12/**IFC_BCTL**	General Purpose Input/Output	E15	IO	OV_{DD}	---
GPIO2_13/**IFC_NDDQS**	General Purpose Input/Output	B17	IO	OV_{DD}	---
GPIO2_14/**IFC_RB0_B**	General Purpose Input/Output	C16	IO	OV_{DD}	---
GPIO2_15/**IFC_RB1_B**	General Purpose Input/Output	D16	IO	OV_{DD}	---
GPIO2_16/**IFC_PERR_B**/ QSPI_B_DATA2/ QSPI_A_DATA6	General Purpose Input/Output	E17	IO	OV_{DD}	---
GPIO2_17/**IFC_CLK0**	General Purpose Input/Output	A20	IO	OV_{DD}	---
GPIO2_18/**IFC_CLK1**	General Purpose Input/Output	B20	IO	OV_{DD}	---
GPIO2_19/**IFC_NDWE_B**	General Purpose Input/Output	E16	IO	OV_{DD}	---
GPIO2_20/**EMI2_MDC**	General Purpose Input/Output	AH4	IO	TV_{DD}	---
GPIO2_21/**EMI2_MDIO**	General Purpose Input/Output	AH3	IO	TV_{DD}	---
GPIO2_22/**EC1_TXD3**	General Purpose Input/Output	Y3	IO	LV_{DD}	---
GPIO2_23/**EC1_TXD2**	General Purpose Input/Output	Y4	IO	LV_{DD}	---
GPIO2_24/**EC1_TXD1**	General Purpose Input/Output	AA3	IO	LV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO2_25/**EC1_TXD0**	General Purpose Input/Output	AB3	IO	LV_{DD}	---
GPIO2_26/**EC1_TX_EN**	General Purpose Input/Output	AB4	IO	LV_{DD}	---
GPIO2_27/**EC1_GTX_CLK**	General Purpose Input/Output	W4	IO	LV_{DD}	---
GPIO2_28/**EC1_GTX_CLK125**	General Purpose Input/Output	AC3	IO	LV_{DD}	---
GPIO2_29/**EC1_RXD3**	General Purpose Input/Output	W2	IO	LV_{DD}	---
GPIO2_30/**EC1_RXD2**	General Purpose Input/Output	Y1	IO	LV_{DD}	---
GPIO3_06/**UART2_SOUT**	General Purpose Input/Output	L2	IO	DV_{DD}	---
GPIO3_07/**UART2_SIN**	General Purpose Input/Output	K1	IO	DV_{DD}	---
GPIO3_08/**UART1_RTS_B**/ UART3_SOUT	General Purpose Input/Output	J2	IO	DV_{DD}	---
GPIO3_09/**UART2_RTS_B**/ UART4_SOUT	General Purpose Input/Output	L1	IO	DV_{DD}	---
GPIO3_10/**UART1_CTS_B**/ UART3_SIN	General Purpose Input/Output	J1	IO	DV_{DD}	---
GPIO3_11/**UART2_CTS_B**/ UART4_SIN	General Purpose Input/Output	M2	IO	DV_{DD}	---
GPIO3_12/**IIC2_SCL**/ SDHC_CD_B/CLK9/BRGO2	General Purpose Input/Output	K3	IO	DV_{DD}	---
GPIO3_13/**IIC2_SDA**/ SDHC_WP/CLK10/BRGO3	General Purpose Input/Output	L3	IO	DV_{DD}	---
GPIO3_14/**SPI_SOUT**/ SDHC_CLK_SYNC_OUT	General Purpose Input/Output	V3	IO	OV_{DD}	---
GPIO3_15/**SPI_SIN**/ SDHC_CLK_SYNC_IN	General Purpose Input/Output	U3	IO	OV_{DD}	---
GPIO3_16/**SPI_SCK**/ SDHC_GATE_IN	General Purpose Input/Output	U2	IO	OV_{DD}	---
GPIO3_17/**SPI_PCS0**/ SDHC_DAT4/SDHC_VS	General Purpose Input/Output	U1	IO	OV_{DD}	---
GPIO3_18/**SPI_PCS1**/ SDHC_DAT5/ SDHC_CMD_DIR	General Purpose Input/Output	R3	IO	OV_{DD}	---
GPIO3_19/**SPI_PCS2**/ SDHC_DAT6/ SDHC_DAT0_DIR	General Purpose Input/Output	T3	IO	OV_{DD}	---
GPIO3_20/**SPI_PCS3**/ SDHC_DAT7/ SDHC_DAT123_DIR	General Purpose Input/Output	V1	IO	OV_{DD}	---
GPIO3_21/**SDHC_CMD**	General Purpose Input/Output	P2	IO	EV_{DD}	---
GPIO3_22/**SDHC_DAT0**	General Purpose Input/Output	P1	IO	EV_{DD}	---
GPIO3_23/**SDHC_DAT1**	General Purpose Input/Output	R2	IO	EV_{DD}	---
GPIO3_24/**SDHC_DAT2**	General Purpose Input/Output	R1	IO	EV_{DD}	---
GPIO3_25/**SDHC_DAT3**	General Purpose Input/Output	T1	IO	EV_{DD}	---
GPIO3_26/**SDHC_CLK**	General Purpose Input/Output	P3	IO	EV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO3_27/**IRQ03**/ TDMB_TSYNC/ UC3_RTSB_TXEN	General Purpose Input/Output	J3	IO	DV_{DD}	---
GPIO3_28/**IRQ04**/ TDMA_RXD/UC1_RXD7/ TDMA_TXD	General Purpose Input/Output	J4	IO	DV_{DD}	---
GPIO3_29/**IRQ05**/ TDMA_RSYNC/ UC1_CTSB_RXDV	General Purpose Input/Output	J5	IO	DV_{DD}	---
GPIO3_30/**RTC**	General Purpose Input/Output	F17	IO	OV_{DD}	---
GPIO4_00/**EMI1_MDC**	General Purpose Input/Output	AG2	IO	LV_{DD}	---
GPIO4_01/**EMI1_MDIO**	General Purpose Input/Output	AF2	IO	LV_{DD}	---
GPIO4_02/**USB_DRVVBUS**	General Purpose Input/Output	H6	IO	DV_{DD}	---
GPIO4_03/**USB_PWRFAULT**	General Purpose Input/Output	G6	IO	DV_{DD}	---
GPIO4_04/**IRQ06**/ TDMA_RXD_EXC/ TDMA_TXD/UC1_TXD7	General Purpose Input/Output	K5	IO	DV_{DD}	---
GPIO4_05/**IRQ07**/ TDMA_TSYNC/ UC1_RTSB_TXEN	General Purpose Input/Output	L5	IO	DV_{DD}	---
GPIO4_06/**IRQ08**/ TDMB_RXD/UC3_RXD7/ TDMB_TXD	General Purpose Input/Output	M5	IO	DV_{DD}	---
GPIO4_07/**IRQ09**/ TDMB_RSYNC/ UC3_CTSB_RXDV	General Purpose Input/Output	N5	IO	DV_{DD}	---
GPIO4_08/**IRQ10**/ TDMB_RXD_EXC/ TDMB_TXD/UC3_TXD7	General Purpose Input/Output	P4	IO	DV_{DD}	---
GPIO4_09/**IRQ11**	General Purpose Input/Output	W3	IO	LV_{DD}	---
GPIO4_10/**EVT9_B**	General Purpose Input/Output	G7	IO	OV_{DD}	---
GPIO4_11/**EC1_RXD1**	General Purpose Input/Output	AA1	IO	LV_{DD}	---
GPIO4_12/**EC1_RXD0**	General Purpose Input/Output	AA2	IO	LV_{DD}	---
GPIO4_13/**EC1_RX_CLK**	General Purpose Input/Output	W1	IO	LV_{DD}	---
GPIO4_14/**EC1_RX_DV**	General Purpose Input/Output	AB1	IO	LV_{DD}	---
GPIO4_15/**EC2_TXD3**/ TSEC_1588_ALARM_OUT2	General Purpose Input/Output	AD3	IO	LV_{DD}	---
GPIO4_16/**EC2_TXD2**/ TSEC_1588_ALARM_OUT1	General Purpose Input/Output	AE3	IO	LV_{DD}	---
GPIO4_17/**EC2_TXD1**/ TSEC_1588_CLK_OUT	General Purpose Input/Output	AE4	IO	LV_{DD}	---
GPIO4_18/**EC2_TXD0**/ TSEC_1588_PULSE_OUT2	General Purpose Input/Output	AF3	IO	LV_{DD}	---
GPIO4_19/**EC2_TX_EN**	General Purpose Input/Output	AG3	IO	LV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO4_20/**EC2_GTX_CLK**	General Purpose Input/Output	AC4	IO	LV_{DD}	---
GPIO4_21/**EC2_GTX_CLK125**	General Purpose Input/Output	AG4	IO	LV_{DD}	---
GPIO4_22/**EC2_RXD3**	General Purpose Input/Output	AC2	IO	LV_{DD}	---
GPIO4_23/**EC2_RXD2**	General Purpose Input/Output	AD1	IO	LV_{DD}	---
GPIO4_24/**EC2_RXD1**/ TSEC_1588_PULSE_OUT1	General Purpose Input/Output	AE1	IO	LV_{DD}	---
GPIO4_25/**EC2_RXD0**/ TSEC_1588_TRIG_IN2	General Purpose Input/Output	AE2	IO	LV_{DD}	---
GPIO4_26/**EC2_RX_CLK**/ TSEC_1588_CLK_IN	General Purpose Input/Output	AC1	IO	LV_{DD}	---
GPIO4_27/**EC2_RX_DV**/ TSEC_1588_TRIG_IN1	General Purpose Input/Output	AF1	IO	LV_{DD}	---
GPIO4_28/**IIC3_SCL**/EVT5_B/ USB2_DRVVBUS/BRGO4/ CLK11	General Purpose Input/Output	L4	IO	DV_{DD}	---
GPIO4_29/**IIC3_SDA**/EVT6_B/ USB2_PWRFAULT/BRGO1/ CLK12_CLK8	General Purpose Input/Output	M4	IO	DV_{DD}	---
GPIO4_30/**IIC4_SCL**/EVT7_B/ TDMA_RQ/UC1_CDB_RXER	General Purpose Input/Output	M3	IO	DV_{DD}	---
GPIO4_31/**IIC4_SDA**/EVT8_B/ TDMB_RQ/UC3_CDB_RXER	General Purpose Input/Output	N3	IO	DV_{DD}	---
Power-On-Reset Configuration					
cfg_eng_use0/**IFC_WE0_B**/ GPIO1_22	Power-on-Reset Configuration	C15	I	OV_{DD}	1, 4, 19
cfg_eng_use1/**IFC_OE_B**/ GPIO1_26	Power-on-Reset Configuration	C18	I	OV_{DD}	1, 5
cfg_eng_use2/**IFC_WP0_B**/ GPIO1_27	Power-on-Reset Configuration	D19	I	OV_{DD}	1, 5
cfg_gpinput0/**IFC_AD00**/ GPIO1_00	Power-on-Reset Configuration	B12	I	OV_{DD}	1, 4
cfg_gpinput1/**IFC_AD01**/ GPIO1_01	Power-on-Reset Configuration	A11	I	OV_{DD}	1, 4
cfg_gpinput2/**IFC_AD02**/ GPIO1_02	Power-on-Reset Configuration	B11	I	OV_{DD}	1, 4
cfg_gpinput3/**IFC_AD03**/ GPIO1_03	Power-on-Reset Configuration	A10	I	OV_{DD}	1, 4
cfg_gpinput4/**IFC_AD04**/ GPIO1_04	Power-on-Reset Configuration	A9	I	OV_{DD}	1, 4
cfg_gpinput5/**IFC_AD05**/ GPIO1_05	Power-on-Reset Configuration	B9	I	OV_{DD}	1, 4
cfg_gpinput6/**IFC_AD06**/ GPIO1_06	Power-on-Reset Configuration	A8	I	OV_{DD}	1, 4

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Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
cfg_gpinput7/**IFC_AD07**/ GPIO1_07	Power-on-Reset Configuration	B8	I	OV_{DD}	1, 4
cfg_ifc_te/**IFC_TE**/GPIO1_23	Power-on-Reset Configuration	E14	I	OV_{DD}	1, 4
cfg_rcw_src0/**IFC_CLE**/ GPIO1_25	Power-on-Reset Configuration	C19	I	OV_{DD}	1, 4
cfg_rcw_src1/**IFC_AD08**/ GPIO1_08	Power-on-Reset Configuration	A12	I	OV_{DD}	1, 4
cfg_rcw_src2/**IFC_AD09**/ GPIO1_09	Power-on-Reset Configuration	A13	I	OV_{DD}	1, 4
cfg_rcw_src3/**IFC_AD10**/ GPIO1_10	Power-on-Reset Configuration	B14	I	OV_{DD}	1, 4
cfg_rcw_src4/**IFC_AD11**/ GPIO1_11	Power-on-Reset Configuration	A14	I	OV_{DD}	1, 4
cfg_rcw_src5/**IFC_AD12**/ GPIO1_12	Power-on-Reset Configuration	B15	I	OV_{DD}	1, 4
cfg_rcw_src6/**IFC_AD13**/ GPIO1_13	Power-on-Reset Configuration	A15	I	OV_{DD}	1, 4
cfg_rcw_src7/**IFC_AD14**/ GPIO1_14	Power-on-Reset Configuration	A16	I	OV_{DD}	1, 4
cfg_rcw_src8/**IFC_AD15**/ GPIO1_15	Power-on-Reset Configuration	A17	I	OV_{DD}	1, 4
Quad SPI					
QSPI_A_CS0/**IFC_A00**/ GPIO1_16	Chip Select	D8	O	OV_{DD}	1, 5
QSPI_A_CS1/**IFC_A01**/ GPIO1_17	CS1	C8	O	OV_{DD}	1, 5
QSPI_A_DATA0/**IFC_A06**/ GPIO2_00/IFC_WP1_B	DATA0	D11	IO	OV_{DD}	---
QSPI_A_DATA1/**IFC_A07**/ GPIO2_01/IFC_WP2_B	DATA1	C12	IO	OV_{DD}	---
QSPI_A_DATA2/**IFC_A08**/ GPIO2_02/IFC_WP3_B	DATA2	D13	IO	OV_{DD}	---
QSPI_A_DATA3/**IFC_A09**/ GPIO2_03/IFC_RB2_B/ IFC_CS_B4	DATA3	C13	IO	OV_{DD}	---
QSPI_A_DATA4/**IFC_PAR0**/ GPIO2_06/QSPI_B_DATA0	DATA4	B18	IO	OV_{DD}	---
QSPI_A_DATA5/**IFC_PAR1**/ GPIO2_07/QSPI_B_DATA1	DATA5	D17	IO	OV_{DD}	---
QSPI_A_DATA6/ **IFC_PERR_B**/GPIO2_16/ QSPI_B_DATA2	DATA6	E17	IO	OV_{DD}	---
QSPI_A_DATA7/**IFC_CS3_B**/ GPIO2_11/QSPI_B_DATA3	DATA7	C20	IO	OV_{DD}	---

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Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
QSPI_A_DQS/**IFC_A10**/ GPIO2_04/IFC_RB3_B/ IFC_CS_B5	DQS	D14	I	OV_{DD}	1
QSPI_A_SCK/**IFC_A02**/ GPIO1_18	SCK	C9	O	OV_{DD}	1, 5
QSPI_B_CS0/**IFC_A03**/ GPIO1_19	Chip Select	D10	O	OV_{DD}	1, 5
QSPI_B_CS1/**IFC_A04**/ GPIO1_20	CS1	C10	O	OV_{DD}	1, 5
QSPI_B_DATA0/**IFC_PAR0**/ GPIO2_06/QSPI_A_DATA4	DATA0	B18	IO	OV_{DD}	---
QSPI_B_DATA1/**IFC_PAR1**/ GPIO2_07/QSPI_A_DATA5	DATA1	D17	IO	OV_{DD}	---
QSPI_B_DATA2/ **IFC_PERR_B**/GPIO2_16/ QSPI_A_DATA6	DATA2	E17	IO	OV_{DD}	---
QSPI_B_DATA3/**IFC_CS3_B**/ GPIO2_11/QSPI_A_DATA7	DATA3	C20	IO	OV_{DD}	---
QSPI_B_DQS/**IFC_A11**/ GPIO2_05/IFC_CS_B6	DQS	C14	I	OV_{DD}	1
QSPI_B_SCK/**IFC_A05**/ GPIO1_21/cfg_dram_type	SCK	C11	O	OV_{DD}	1, 4
QUICC Engine					
BRGO1/**IIC3_SDA**/GPIO4_29/ EVT6_B/USB2_PWRFAULT/ CLK12_CLK8	Baud Rate Generator Output	M4	O	DV_{DD}	1
BRGO2/**IIC2_SCL**/GPIO3_12/ SDHC_CD_B/CLK9	Baud Rate Generator Output	K3	O	DV_{DD}	1
BRGO3/**IIC2_SDA**/GPIO3_13/ SDHC_WP/CLK10	Baud Rate Generator Output	L3	O	DV_{DD}	1
BRGO4/**IIC3_SCL**/GPIO4_28/ EVT5_B/USB2_DRVVBUS/ CLK11	Baud Rate Generator Output	L4	O	DV_{DD}	1
CLK10/**IIC2_SDA**/GPIO3_13/ SDHC_WP/BRGO3	Clock	L3	I	DV_{DD}	1
CLK9/**IIC2_SCL**/GPIO3_12/ SDHC_CD_B/BRGO2	Clock	K3	I	DV_{DD}	1
TDMA_RQ/**IIC4_SCL**/ GPIO4_30/EVT7_B/ UC1_CDB_RXER	RQ	M3	O	DV_{DD}	1
TDMB_RQ/**IIC4_SDA**/ GPIO4_31/EVT8_B/ UC3_CDB_RXER	RQ	N3	O	DV_{DD}	1
UC1_CDB_RXER/**IIC4_SCL**/ GPIO4_30/EVT7_B/TDMA_RQ	Receive Error	M3	I	DV_{DD}	1

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Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
UC1_CTSB_RXDV/**IRQ05**/ GPIO3_29/TDMA_RSYNC	Receive Data	J5	I	DV_{DD}	1
UC1_RTSB_TXEN/**IRQ07**/ GPIO4_05/TDMA_TSYNC	Transmit Enable	L5	O	DV_{DD}	1
UC1_RXD7/**IRQ04**/GPIO3_28/ TDMA_RXD/TDMA_TXD	Receive Data	J4	I	DV_{DD}	1
UC1_TXD7/**IRQ06**/GPIO4_04/ TDMA_RXD_EXC/TDMA_TXD	Transmit Data	K5	O	DV_{DD}	1
UC3_CDB_RXER/**IIC4_SDA**/ GPIO4_31/EVT8_B/TDMB_RQ	Receive Error	N3	I	DV_{DD}	1
UC3_CTSB_RXDV/**IRQ09**/ GPIO4_07/TDMB_RSYNC	Receive Data	N5	I	DV_{DD}	1
UC3_RTSB_TXEN/**IRQ03**/ GPIO3_27/TDMB_TSYNC	Transmit Enable	J3	O	DV_{DD}	1
UC3_RXD7/**IRQ08**/GPIO4_06/ TDMB_RXD/TDMB_TXD	Receive Data	M5	I	DV_{DD}	1
UC3_TXD7/**IRQ10**/GPIO4_08/ TDMB_RXD_EXC/TDMB_TXD	Transmit Data	P4	O	DV_{DD}	1
Time Division Multiplexing					
TDMA_RSYNC/**IRQ05**/ GPIO3_29/UC1_CTSB_RXDV	RSYNC	J5	I	DV_{DD}	1
TDMA_RXD/**IRQ04**/ GPIO3_28/UC1_RXD7/ TDMA_TXD	RXD	J4	I	DV_{DD}	1
TDMA_RXD_EXC/**IRQ06**/ GPIO4_04/TDMA_TXD/ UC1_TXD7	Recieve Data	K5	I	DV_{DD}	1
TDMA_TSYNC/**IRQ07**/ GPIO4_05/UC1_RTSB_TXEN	TSYNC	L5	I	DV_{DD}	1
TDMA_TXD/**IRQ04**/GPIO3_28/ TDMA_RXD/UC1_RXD7	Transmit Data	J4	O	DV_{DD}	1
TDMA_TXD/**IRQ06**/GPIO4_04/ TDMA_RXD_EXC/UC1_TXD7	Transmit Data	K5	O	DV_{DD}	1
TDMB_RSYNC/**IRQ09**/ GPIO4_07/UC3_CTSB_RXDV	RSYNC	N5	I	DV_{DD}	1
TDMB_RXD/**IRQ08**/ GPIO4_06/UC3_RXD7/ TDMB_TXD	RXD	M5	I	DV_{DD}	1
TDMB_RXD_EXC/**IRQ10**/ GPIO4_08/TDMB_TXD/ UC3_TXD7	Recieve Data	P4	I	DV_{DD}	1
TDMB_TSYNC/**IRQ03**/ GPIO3_27/UC3_RTSB_TXEN	TSYNC	J3	I	DV_{DD}	1
TDMB_TXD/**IRQ08**/GPIO4_06/ TDMB_RXD/UC3_RXD7	Transmit Data	M5	O	DV_{DD}	1

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Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
TDMB_TXD/**IRQ10**/GPIO4_08/ TDMB_RXD_EXC/UC3_TXD7	Transmit Data	P4	O	DV_{DD}	1
IEEE 1588					
TSEC_1588_ALARM_OUT1/ **EC2_TXD2**/GPIO4_16	Alarm Out	AE3	O	LV_{DD}	1
TSEC_1588_ALARM_OUT2/ **EC2_TXD3**/GPIO4_15	Alarm Out	AD3	O	LV_{DD}	1
TSEC_1588_CLK_IN/ **EC2_RX_CLK**/GPIO4_26	Clock In	AC1	I	LV_{DD}	1
TSEC_1588_CLK_OUT/ **EC2_TXD1**/GPIO4_17	Clock Out	AE4	O	LV_{DD}	1
TSEC_1588_PULSE_OUT1/ **EC2_RXD1**/GPIO4_24	Pulse Out	AE1	O	LV_{DD}	1
TSEC_1588_PULSE_OUT2/ **EC2_TXD0**/GPIO4_18	Pulse Out	AF3	O	LV_{DD}	1
TSEC_1588_TRIG_IN1/ **EC2_RX_DV**/GPIO4_27	Trigger In	AF1	I	LV_{DD}	1
TSEC_1588_TRIG_IN2/ **EC2_RXD0**/GPIO4_25	Trigger In	AE2	I	LV_{DD}	1
TMR					
CLK11/**IIC3_SCL**/GPIO4_28/ EVT5_B/USB2_DRVVBUS/ BRGO4	Clock #11	L4	I	DV_{DD}	1
CLK12_CLK8/**IIC3_SDA**/ GPIO4_29/EVT6_B/ USB2_PWRFAULT/BRGO1	CLK8	M4	I	DV_{DD}	1
Power and Ground Signals					
GND001	Core, Platform and PLL Ground	A2	---	---	---
GND002	Core, Platform and PLL Ground	A5	---	---	---
GND003	Core, Platform and PLL Ground	A21	---	---	---
GND004	Core, Platform and PLL Ground	B3	---	---	---
GND005	Core, Platform and PLL Ground	B4	---	---	---
GND006	Core, Platform and PLL Ground	B7	---	---	---
GND007	Core, Platform and PLL Ground	B10	---	---	---
GND008	Core, Platform and PLL Ground	B13	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND009	Core, Platform and PLL Ground	B16	---	---	---
GND010	Core, Platform and PLL Ground	B19	---	---	---
GND011	Core, Platform and PLL Ground	B21	---	---	---
GND012	Core, Platform and PLL Ground	B24	---	---	---
GND013	Core, Platform and PLL Ground	B26	---	---	---
GND014	Core, Platform and PLL Ground	C1	---	---	---
GND015	Core, Platform and PLL Ground	C2	---	---	---
GND016	Core, Platform and PLL Ground	C5	---	---	---
GND017	Core, Platform and PLL Ground	C21	---	---	---
GND018	Core, Platform and PLL Ground	C27	---	---	---
GND019	Core, Platform and PLL Ground	D3	---	---	---
GND020	Core, Platform and PLL Ground	D4	---	---	---
GND021	Core, Platform and PLL Ground	D7	---	---	---
GND022	Core, Platform and PLL Ground	D9	---	---	---
GND023	Core, Platform and PLL Ground	D12	---	---	---
GND024	Core, Platform and PLL Ground	D15	---	---	---
GND025	Core, Platform and PLL Ground	D18	---	---	---
GND026	Core, Platform and PLL Ground	D21	---	---	---
GND027	Core, Platform and PLL Ground	D24	---	---	---
GND028	Core, Platform and PLL Ground	E1	---	---	---
GND029	Core, Platform and PLL Ground	E2	---	---	---
GND030	Core, Platform and PLL Ground	E5	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND031	Core, Platform and PLL Ground	E21	---	---	---
GND032	Core, Platform and PLL Ground	E26	---	---	---
GND033	Core, Platform and PLL Ground	F3	---	---	---
GND034	Core, Platform and PLL Ground	F4	---	---	---
GND035	Core, Platform and PLL Ground	F7	---	---	---
GND036	Core, Platform and PLL Ground	F14	---	---	---
GND037	Core, Platform and PLL Ground	F16	---	---	---
GND038	Core, Platform and PLL Ground	F18	---	---	---
GND039	Core, Platform and PLL Ground	F24	---	---	---
GND040	Core, Platform and PLL Ground	G1	---	---	---
GND041	Core, Platform and PLL Ground	G2	---	---	---
GND042	Core, Platform and PLL Ground	G9	---	---	---
GND043	Core, Platform and PLL Ground	G10	---	---	---
GND044	Core, Platform and PLL Ground	G11	---	---	---
GND045	Core, Platform and PLL Ground	G21	---	---	---
GND046	Core, Platform and PLL Ground	G26	---	---	---
GND047	Core, Platform and PLL Ground	H3	---	---	---
GND048	Core, Platform and PLL Ground	H4	---	---	---
GND049	Core, Platform and PLL Ground	H5	---	---	---
GND050	Core, Platform and PLL Ground	H14	---	---	---
GND051	Core, Platform and PLL Ground	H15	---	---	---
GND052	Core, Platform and PLL Ground	H16	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND053	Core, Platform and PLL Ground	H17	---	---	---
GND054	Core, Platform and PLL Ground	H18	---	---	---
GND055	Core, Platform and PLL Ground	H21	---	---	---
GND056	Core, Platform and PLL Ground	H24	---	---	---
GND057	Core, Platform and PLL Ground	J6	---	---	---
GND058	Core, Platform and PLL Ground	J7	---	---	---
GND059	Core, Platform and PLL Ground	J8	---	---	---
GND060	Core, Platform and PLL Ground	J9	---	---	---
GND061	Core, Platform and PLL Ground	J10	---	---	---
GND062	Core, Platform and PLL Ground	J11	---	---	---
GND063	Core, Platform and PLL Ground	J12	---	---	---
GND064	Core, Platform and PLL Ground	J21	---	---	---
GND065	Core, Platform and PLL Ground	J23	---	---	---
GND066	Core, Platform and PLL Ground	J26	---	---	---
GND067	Core, Platform and PLL Ground	K2	---	---	---
GND068	Core, Platform and PLL Ground	K4	---	---	---
GND069	Core, Platform and PLL Ground	K6	---	---	---
GND070	Core, Platform and PLL Ground	K13	---	---	---
GND071	Core, Platform and PLL Ground	K15	---	---	---
GND072	Core, Platform and PLL Ground	K17	---	---	---
GND073	Core, Platform and PLL Ground	K19	---	---	---
GND074	Core, Platform and PLL Ground	K21	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND075	Core, Platform and PLL Ground	L6	---	---	---
GND076	Core, Platform and PLL Ground	L10	---	---	---
GND077	Core, Platform and PLL Ground	L12	---	---	---
GND078	Core, Platform and PLL Ground	L14	---	---	---
GND079	Core, Platform and PLL Ground	L16	---	---	---
GND080	Core, Platform and PLL Ground	L18	---	---	---
GND081	Core, Platform and PLL Ground	L20	---	---	---
GND082	Core, Platform and PLL Ground	L23	---	---	---
GND083	Core, Platform and PLL Ground	L26	---	---	---
GND084	Core, Platform and PLL Ground	M6	---	---	---
GND085	Core, Platform and PLL Ground	M9	---	---	---
GND086	Core, Platform and PLL Ground	M11	---	---	---
GND087	Core, Platform and PLL Ground	M13	---	---	---
GND088	Core, Platform and PLL Ground	M15	---	---	---
GND089	Core, Platform and PLL Ground	M17	---	---	---
GND090	Core, Platform and PLL Ground	M19	---	---	---
GND091	Core, Platform and PLL Ground	M21	---	---	---
GND092	Core, Platform and PLL Ground	M23	---	---	---
GND093	Core, Platform and PLL Ground	N2	---	---	---
GND094	Core, Platform and PLL Ground	N4	---	---	---
GND095	Core, Platform and PLL Ground	N6	---	---	---
GND096	Core, Platform and PLL Ground	N8	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND097	Core, Platform and PLL Ground	N10	---	---	---
GND098	Core, Platform and PLL Ground	N12	---	---	---
GND099	Core, Platform and PLL Ground	N14	---	---	---
GND100	Core, Platform and PLL Ground	N16	---	---	---
GND101	Core, Platform and PLL Ground	N18	---	---	---
GND102	Core, Platform and PLL Ground	N20	---	---	---
GND103	Core, Platform and PLL Ground	N23	---	---	---
GND104	Core, Platform and PLL Ground	N26	---	---	---
GND105	Core, Platform and PLL Ground	P6	---	---	---
GND106	Core, Platform and PLL Ground	P9	---	---	---
GND107	Core, Platform and PLL Ground	P11	---	---	---
GND108	Core, Platform and PLL Ground	P13	---	---	---
GND109	Core, Platform and PLL Ground	P15	---	---	---
GND110	Core, Platform and PLL Ground	P17	---	---	---
GND111	Core, Platform and PLL Ground	P19	---	---	---
GND112	Core, Platform and PLL Ground	P23	---	---	---
GND113	Core, Platform and PLL Ground	R5	---	---	---
GND114	Core, Platform and PLL Ground	R8	---	---	---
GND115	Core, Platform and PLL Ground	R10	---	---	---
GND116	Core, Platform and PLL Ground	R12	---	---	---
GND117	Core, Platform and PLL Ground	R14	---	---	---
GND118	Core, Platform and PLL Ground	R16	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND119	Core, Platform and PLL Ground	R18	---	---	---
GND120	Core, Platform and PLL Ground	R20	---	---	---
GND121	Core, Platform and PLL Ground	R23	---	---	---
GND122	Core, Platform and PLL Ground	R26	---	---	---
GND123	Core, Platform and PLL Ground	T2	---	---	---
GND124	Core, Platform and PLL Ground	T4	---	---	---
GND125	Core, Platform and PLL Ground	T6	---	---	---
GND126	Core, Platform and PLL Ground	T9	---	---	---
GND127	Core, Platform and PLL Ground	T11	---	---	---
GND128	Core, Platform and PLL Ground	T13	---	---	---
GND129	Core, Platform and PLL Ground	T15	---	---	---
GND130	Core, Platform and PLL Ground	T17	---	---	---
GND131	Core, Platform and PLL Ground	T19	---	---	---
GND132	Core, Platform and PLL Ground	T21	---	---	---
GND133	Core, Platform and PLL Ground	T23	---	---	---
GND134	Core, Platform and PLL Ground	T26	---	---	---
GND135	Core, Platform and PLL Ground	U6	---	---	---
GND136	Core, Platform and PLL Ground	U8	---	---	---
GND137	Core, Platform and PLL Ground	U10	---	---	---
GND138	Core, Platform and PLL Ground	U12	---	---	---
GND139	Core, Platform and PLL Ground	U14	---	---	---
GND140	Core, Platform and PLL Ground	U16	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND141	Core, Platform and PLL Ground	U18	---	---	---
GND142	Core, Platform and PLL Ground	U20	---	---	---
GND143	Core, Platform and PLL Ground	U23	---	---	---
GND144	Core, Platform and PLL Ground	V2	---	---	---
GND145	Core, Platform and PLL Ground	V4	---	---	---
GND146	Core, Platform and PLL Ground	V6	---	---	---
GND147	Core, Platform and PLL Ground	V9	---	---	---
GND148	Core, Platform and PLL Ground	V11	---	---	---
GND149	Core, Platform and PLL Ground	V13	---	---	---
GND150	Core, Platform and PLL Ground	V15	---	---	---
GND151	Core, Platform and PLL Ground	V17	---	---	---
GND152	Core, Platform and PLL Ground	V19	---	---	---
GND153	Core, Platform and PLL Ground	V21	---	---	---
GND154	Core, Platform and PLL Ground	V23	---	---	---
GND155	Core, Platform and PLL Ground	V26	---	---	---
GND156	Core, Platform and PLL Ground	W12	---	---	---
GND157	Core, Platform and PLL Ground	W18	---	---	---
GND158	Core, Platform and PLL Ground	W20	---	---	---
GND159	Core, Platform and PLL Ground	W22	---	---	---
GND160	Core, Platform and PLL Ground	Y2	---	---	---
GND161	Core, Platform and PLL Ground	Y21	---	---	---
GND162	Core, Platform and PLL Ground	Y23	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND163	Core, Platform and PLL Ground	Y26	---	---	---
GND164	Core, Platform and PLL Ground	AA4	---	---	---
GND165	Core, Platform and PLL Ground	AA21	---	---	---
GND166	Core, Platform and PLL Ground	AA24	---	---	---
GND167	Core, Platform and PLL Ground	AB2	---	---	---
GND168	Core, Platform and PLL Ground	AB26	---	---	---
GND169	Core, Platform and PLL Ground	AC21	---	---	---
GND170	Core, Platform and PLL Ground	AC24	---	---	---
GND171	Core, Platform and PLL Ground	AD2	---	---	---
GND172	Core, Platform and PLL Ground	AD4	---	---	---
GND173	Core, Platform and PLL Ground	AD26	---	---	---
GND174	Core, Platform and PLL Ground	AE21	---	---	---
GND175	Core, Platform and PLL Ground	AE24	---	---	---
GND176	Core, Platform and PLL Ground	AF4	---	---	---
GND177	Core, Platform and PLL Ground	AF21	---	---	---
GND178	Core, Platform and PLL Ground	AF26	---	---	---
GND179	Core, Platform and PLL Ground	AG1	---	---	---
GND180	Core, Platform and PLL Ground	AG24	---	---	---
GND181	Core, Platform and PLL Ground	AG26	---	---	---
GND182	Core, Platform and PLL Ground	AH2	---	---	---
GND183	Core, Platform and PLL Ground	AH21	---	---	---
SD_GND01	SerDes core logic, transceiver, and PLL ground	Y6	---	---	18

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Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD_GND02	SerDes core logic, transceiver, and PLL ground	Y7	---	---	18
SD_GND03	SerDes core logic, transceiver, and PLL ground	Y8	---	---	18
SD_GND04	SerDes core logic, transceiver, and PLL ground	Y9	---	---	18
SD_GND05	SerDes core logic, transceiver, and PLL ground	Y10	---	---	18
SD_GND06	SerDes core logic, transceiver, and PLL ground	Y13	---	---	18
SD_GND07	SerDes core logic, transceiver, and PLL ground	Y14	---	---	18
SD_GND08	SerDes core logic, transceiver, and PLL ground	Y15	---	---	18
SD_GND09	SerDes core logic, transceiver, and PLL ground	Y16	---	---	18
SD_GND10	SerDes core logic, transceiver, and PLL ground	AA5	---	---	18
SD_GND11	SerDes core logic, transceiver, and PLL ground	AA7	---	---	18
SD_GND12	SerDes core logic, transceiver, and PLL ground	AA9	---	---	18
SD_GND13	SerDes core logic, transceiver, and PLL ground	AA12	---	---	18
SD_GND14	SerDes core logic, transceiver, and PLL ground	AA14	---	---	18
SD_GND15	SerDes core logic, transceiver, and PLL ground	AA17	---	---	18
SD_GND16	SerDes core logic, transceiver, and PLL ground	AA18	---	---	18
SD_GND17	SerDes core logic, transceiver, and PLL ground	AA19	---	---	18
SD_GND18	SerDes core logic, transceiver, and PLL ground	AB7	---	---	18
SD_GND19	SerDes core logic, transceiver, and PLL ground	AB9	---	---	18
SD_GND20	SerDes core logic, transceiver, and PLL ground	AB12	---	---	18
SD_GND21	SerDes core logic, transceiver, and PLL ground	AB14	---	---	18
SD_GND22	SerDes core logic, transceiver, and PLL ground	AB17	---	---	18
SD_GND23	SerDes core logic, transceiver, and PLL ground	AB20	---	---	18

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Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD_GND24	SerDes core logic, transceiver, and PLL ground	AC5	---	---	18
SD_GND25	SerDes core logic, transceiver, and PLL ground	AC6	---	---	18
SD_GND26	SerDes core logic, transceiver, and PLL ground	AC8	---	---	18
SD_GND27	SerDes core logic, transceiver, and PLL ground	AC10	---	---	18
SD_GND28	SerDes core logic, transceiver, and PLL ground	AC11	---	---	18
SD_GND29	SerDes core logic, transceiver, and PLL ground	AC15	---	---	18
SD_GND30	SerDes core logic, transceiver, and PLL ground	AC16	---	---	18
SD_GND31	SerDes core logic, transceiver, and PLL ground	AC18	---	---	18
SD_GND32	SerDes core logic, transceiver, and PLL ground	AC19	---	---	18
SD_GND33	SerDes core logic, transceiver, and PLL ground	AD5	---	---	18
SD_GND34	SerDes core logic, transceiver, and PLL ground	AD7	---	---	18
SD_GND35	SerDes core logic, transceiver, and PLL ground	AD9	---	---	18
SD_GND36	SerDes core logic, transceiver, and PLL ground	AD12	---	---	18
SD_GND37	SerDes core logic, transceiver, and PLL ground	AD14	---	---	18
SD_GND38	SerDes core logic, transceiver, and PLL ground	AD17	---	---	18
SD_GND39	SerDes core logic, transceiver, and PLL ground	AD20	---	---	18
SD_GND40	SerDes core logic, transceiver, and PLL ground	AE5	---	---	18
SD_GND41	SerDes core logic, transceiver, and PLL ground	AE7	---	---	18
SD_GND42	SerDes core logic, transceiver, and PLL ground	AE9	---	---	18
SD_GND43	SerDes core logic, transceiver, and PLL ground	AE12	---	---	18
SD_GND44	SerDes core logic, transceiver, and PLL ground	AE14	---	---	18
SD_GND45	SerDes core logic, transceiver, and PLL ground	AE17	---	---	18

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Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD_GND46	SerDes core logic, transceiver, and PLL ground	AE20	---	---	18
SD_GND47	SerDes core logic, transceiver, and PLL ground	AF6	---	---	18
SD_GND48	SerDes core logic, transceiver, and PLL ground	AF7	---	---	18
SD_GND49	SerDes core logic, transceiver, and PLL ground	AF8	---	---	18
SD_GND50	SerDes core logic, transceiver, and PLL ground	AF9	---	---	18
SD_GND51	SerDes core logic, transceiver, and PLL ground	AF10	---	---	18
SD_GND52	SerDes core logic, transceiver, and PLL ground	AF11	---	---	18
SD_GND53	SerDes core logic, transceiver, and PLL ground	AF15	---	---	18
SD_GND54	SerDes core logic, transceiver, and PLL ground	AF16	---	---	18
SD_GND55	SerDes core logic, transceiver, and PLL ground	AF17	---	---	18
SD_GND56	SerDes core logic, transceiver, and PLL ground	AF18	---	---	18
SD_GND57	SerDes core logic, transceiver, and PLL ground	AF19	---	---	18
SD_GND58	SerDes core logic, transceiver, and PLL ground	AG5	---	---	18
SD_GND59	SerDes core logic, transceiver, and PLL ground	AG7	---	---	18
SD_GND60	SerDes core logic, transceiver, and PLL ground	AG9	---	---	18
SD_GND61	SerDes core logic, transceiver, and PLL ground	AG12	---	---	18
SD_GND62	SerDes core logic, transceiver, and PLL ground	AG14	---	---	18
SD_GND63	SerDes core logic, transceiver, and PLL ground	AG17	---	---	18
SD_GND64	SerDes core logic, transceiver, and PLL ground	AG20	---	---	18
SD_GND65	SerDes core logic, transceiver, and PLL ground	AH5	---	---	18
SD_GND66	SerDes core logic, transceiver, and PLL ground	AH7	---	---	18
SD_GND67	SerDes core logic, transceiver, and PLL ground	AH9	---	---	18

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Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD_GND68	SerDes core logic, transceiver, and PLL ground	AH12	---	---	18
SD_GND69	SerDes core logic, transceiver, and PLL ground	AH14	---	---	18
SD_GND70	SerDes core logic, transceiver, and PLL ground	AH17	---	---	18
SD_GND71	SerDes core logic, transceiver, and PLL ground	AH20	---	---	18
SENSEGND	Ground Sense pin	G20	---	---	---
OVDD1	General I/O supply	J18	---	OV_{DD}	---
OVDD2	General I/O supply	K9	---	OV_{DD}	---
OVDD3	General I/O supply	K10	---	OV_{DD}	---
OVDD4	General I/O supply	K11	---	OV_{DD}	---
OVDD5	General I/O supply	K12	---	OV_{DD}	---
OVDD6	General I/O supply	R7	---	OV_{DD}	---
DVDD1	UART/I2C/QE supply	N7	---	DV_{DD}	---
DVDD2	UART/I2C/QE supply	P7	---	DV_{DD}	---
EVDD	eSDHC supply - switchable	R6	---	EV_{DD}	---
LVDD1	RGMII supply	T7	---	LV_{DD}	---
LVDD2	RGMII supply	U7	---	LV_{DD}	---
LVDD3	RGMII supply	V7	---	LV_{DD}	---
TVDD	10G MDIO supply	W6	---	TV_{DD}	---
G1VDD01	DDR supply	B27	---	$G1V_{DD}$	---
G1VDD02	DDR supply	D27	---	$G1V_{DD}$	---
G1VDD03	DDR supply	F27	---	$G1V_{DD}$	---
G1VDD04	DDR supply	H27	---	$G1V_{DD}$	---
G1VDD05	DDR supply	K27	---	$G1V_{DD}$	---
G1VDD06	DDR supply	L22	---	$G1V_{DD}$	---
G1VDD07	DDR supply	M22	---	$G1V_{DD}$	---
G1VDD08	DDR supply	M27	---	$G1V_{DD}$	---
G1VDD09	DDR supply	N22	---	$G1V_{DD}$	---
G1VDD10	DDR supply	P22	---	$G1V_{DD}$	---
G1VDD11	DDR supply	P27	---	$G1V_{DD}$	---
G1VDD12	DDR supply	R22	---	$G1V_{DD}$	---
G1VDD13	DDR supply	T22	---	$G1V_{DD}$	---
G1VDD14	DDR supply	U22	---	$G1V_{DD}$	---
G1VDD15	DDR supply	U27	---	$G1V_{DD}$	---
G1VDD16	DDR supply	V22	---	$G1V_{DD}$	---
G1VDD17	DDR supply	W27	---	$G1V_{DD}$	---

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Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
G1VDD18	DDR supply	AA27	---	$G1V_{DD}$	---
G1VDD19	DDR supply	AC27	---	$G1V_{DD}$	---
G1VDD20	DDR supply	AE27	---	$G1V_{DD}$	---
G1VDD21	DDR supply	AG27	---	$G1V_{DD}$	---
G1VDD22	DDR supply	AH27	---	$G1V_{DD}$	---
SVDD1	SerDes transceiver supply	W7	---	SV_{DD}	---
SVDD2	SerDes transceiver supply	W8	---	SV_{DD}	---
SVDD3	SerDes transceiver supply	W9	---	SV_{DD}	---
SVDD4	SerDes transceiver supply	W10	---	SV_{DD}	---
SVDD5	SerDes transceiver supply	W13	---	SV_{DD}	---
SVDD6	SerDes transceiver supply	W14	---	SV_{DD}	---
SVDD7	SerDes transceiver supply	W15	---	SV_{DD}	---
SVDD8	SerDes transceiver supply	W16	---	SV_{DD}	---
XVDD1	SerDes transceiver supply	AC7	---	XV_{DD}	---
XVDD2	SerDes transceiver supply	AC9	---	XV_{DD}	---
XVDD3	SerDes transceiver supply	AC12	---	XV_{DD}	---
XVDD4	SerDes transceiver supply	AC14	---	XV_{DD}	---
XVDD5	SerDes transceiver supply	AC17	---	XV_{DD}	---
XVDD6	SerDes transceiver supply	AC20	---	XV_{DD}	---
FA_VL	Reserved	AB21	---	FA_VL	---
PROG_MTR	Reserved	F13	---	PROG_MTR	---
TA_PROG_SFP	SFP Fuse Programming Override supply	G13	---	TA_PROG_SFP	---
TH_VDD	Thermal Monitor Unit supply	G8	---	TH_V_{DD}	---
VDD01	Supply for cores and platform	K14	---	V_{DD}	---
VDD02	Supply for cores and platform	K16	---	V_{DD}	---
VDD03	Supply for cores and platform	K18	---	V_{DD}	---
VDD04	Supply for cores and platform	K20	---	V_{DD}	---
VDD05	Supply for cores and platform	K22	---	V_{DD}	---
VDD06	Supply for cores and platform	L9	---	V_{DD}	---
VDD07	Supply for cores and platform	L11	---	V_{DD}	---
VDD08	Supply for cores and platform	L13	---	V_{DD}	---
VDD09	Supply for cores and platform	L15	---	V_{DD}	---
VDD10	Supply for cores and platform	L17	---	V_{DD}	---
VDD11	Supply for cores and platform	L19	---	V_{DD}	---
VDD12	Supply for cores and platform	L21	---	V_{DD}	---
VDD13	Supply for cores and platform	M10	---	V_{DD}	---
VDD14	Supply for cores and platform	M12	---	V_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
VDD15	Supply for cores and platform	M14	---	V_{DD}	---
VDD16	Supply for cores and platform	M16	---	V_{DD}	---
VDD17	Supply for cores and platform	M18	---	V_{DD}	---
VDD18	Supply for cores and platform	M20	---	V_{DD}	---
VDD19	Supply for cores and platform	N9	---	V_{DD}	---
VDD20	Supply for cores and platform	N11	---	V_{DD}	---
VDD21	Supply for cores and platform	N13	---	V_{DD}	---
VDD22	Supply for cores and platform	N15	---	V_{DD}	---
VDD23	Supply for cores and platform	N17	---	V_{DD}	---
VDD24	Supply for cores and platform	N19	---	V_{DD}	---
VDD25	Supply for cores and platform	N21	---	V_{DD}	---
VDD26	Supply for cores and platform	P8	---	V_{DD}	---
VDD27	Supply for cores and platform	P10	---	V_{DD}	---
VDD28	Supply for cores and platform	P12	---	V_{DD}	---
VDD29	Supply for cores and platform	P14	---	V_{DD}	---
VDD30	Supply for cores and platform	P16	---	V_{DD}	---
VDD31	Supply for cores and platform	P18	---	V_{DD}	---
VDD32	Supply for cores and platform	P20	---	V_{DD}	---
VDD33	Supply for cores and platform	R9	---	V_{DD}	---
VDD34	Supply for cores and platform	R11	---	V_{DD}	---
VDD35	Supply for cores and platform	R13	---	V_{DD}	---
VDD36	Supply for cores and platform	R15	---	V_{DD}	---
VDD37	Supply for cores and platform	R17	---	V_{DD}	---
VDD38	Supply for cores and platform	R19	---	V_{DD}	---
VDD39	Supply for cores and platform	T8	---	V_{DD}	---
VDD40	Supply for cores and platform	T10	---	V_{DD}	---
VDD41	Supply for cores and platform	T12	---	V_{DD}	---
VDD42	Supply for cores and platform	T14	---	V_{DD}	---
VDD43	Supply for cores and platform	T16	---	V_{DD}	---
VDD44	Supply for cores and platform	T18	---	V_{DD}	---
VDD45	Supply for cores and platform	T20	---	V_{DD}	---
VDD46	Supply for cores and platform	U9	---	V_{DD}	---
VDD47	Supply for cores and platform	U11	---	V_{DD}	---
VDD48	Supply for cores and platform	U13	---	V_{DD}	---
VDD49	Supply for cores and platform	U15	---	V_{DD}	---
VDD50	Supply for cores and platform	U17	---	V_{DD}	---
VDD51	Supply for cores and platform	U19	---	V_{DD}	---
VDD52	Supply for cores and platform	U21	---	V_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
VDD53	Supply for cores and platform	V8	---	V_{DD}	---
VDD54	Supply for cores and platform	V10	---	V_{DD}	---
VDD55	Supply for cores and platform	V12	---	V_{DD}	---
VDD56	Supply for cores and platform	V14	---	V_{DD}	---
VDD57	Supply for cores and platform	V16	---	V_{DD}	---
VDD58	Supply for cores and platform	V18	---	V_{DD}	---
VDD59	Supply for cores and platform	V20	---	V_{DD}	---
VDD60	Supply for cores and platform	W11	---	V_{DD}	---
VDD61	Supply for cores and platform	W17	---	V_{DD}	---
VDD62	Supply for cores and platform	W19	---	V_{DD}	---
VDD63	Supply for cores and platform	W21	---	V_{DD}	---
TA_BB_VDD	Battery Backed Security Monitor supply	G12	---	TA_BB_V_{DD}	---
AVDD_CGA1	CPU Cluster Group A PLL1 supply	H11	---	AVDD_CGA1	---
AVDD_CGA2	CPU Cluster Group A PLL1 supply	H10	---	AVDD_CGA2	---
AVDD_PLAT	Platform PLL supply	H9	---	AVDD_PLAT	---
AVDD_D1	DDR1 PLL supply	R21	---	AVDD_D1	---
AVDD_SD1_PLL1	SerDes1 PLL 1 supply	AA11	---	AVDD_SD1_PLL1	---
AVDD_SD1_PLL2	SerDes1 PLL 2 supply	AB6	---	AVDD_SD1_PLL2	---
AVDD_SD2_PLL1	SerDes2 PLL 1 supply	AB15	---	AVDD_SD2_PLL1	---
AVDD_SD2_PLL2	SerDes2 PLL 2 supply	AA16	---	AVDD_SD2_PLL2	---
SENSEVDD	Vdd Sense pin	G19	---	SENSEVDD	---
USB_HVDD1	USB PHY 3.3V High Supply	K8	---	USB_HV_{DD}	---
USB_HVDD2	USB PHY 3.3V High Supply	L8	---	USB_HV_{DD}	---
USB_SDVDD1	USB PHY 1.0 V Analog and digital SS supply	M7	---	USB_SDV_{DD}	---
USB_SDVDD2	USB PHY 1.0 V Analog and digital SS supply	M8	---	USB_SDV_{DD}	---
USB_SVDD1	USB PHY 1.0 V Analog and digital HS supply	K7	---	USB_SV_{DD}	---
USB_SVDD2	USB PHY 1.0 V Analog and digital HS supply	L7	---	USB_SV_{DD}	---
No Connection Pins					
NC_A3	No Connection	A3	---	---	12
NC_A4	No Connection	A4	---	---	12
NC_A6	No Connection	A6	---	---	12
NC_A7	No Connection	A7	---	---	12
NC_AA10	No Connection	AA10	---	---	12

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
NC_AA15	No Connection	AA15	---	---	12
NC_AB10	No Connection	AB10	---	---	12
NC_AB11	No Connection	AB11	---	---	12
NC_AB16	No Connection	AB16	---	---	12
NC_B1	No Connection	B1	---	---	12
NC_B2	No Connection	B2	---	---	12
NC_B5	No Connection	B5	---	---	12
NC_B6	No Connection	B6	---	---	12
NC_G5	No Connection	G5	---	---	12
NC_J14	No Connection	J14	---	---	12
NC_J15	No Connection	J15	---	---	12
NC_J16	No Connection	J16	---	---	12
NC_J17	No Connection	J17	---	---	12
NC_P21	No Connection	P21	---	---	12
NC_P5	No Connection	P5	---	---	12
NC_R4	No Connection	R4	---	---	12
NC_T5	No Connection	T5	---	---	12
NC_U4	No Connection	U4	---	---	12
NC_U5	No Connection	U5	---	---	12
NC_V5	No Connection	V5	---	---	12
NC_W5	No Connection	W5	---	---	12
NC_Y17	No Connection	Y17	---	---	12
NC_Y18	No Connection	Y18	---	---	12
NC_Y19	No Connection	Y19	---	---	12
NC_Y5	No Connection	Y5	---	---	12
NC_F12	No Connection	F12	---	---	12

1. Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. Therefore, this pin is described as an I/O for boundary scan.

2. This output is actively driven during reset rather than being tri-stated during reset.

3. MDIC[0] is grounded through a 162 Ω precision 1% resistor and MDIC[1] is connected to GV_{DD} through a 162 Ω precision 1% resistor. For either full or half driver strength calibration of DDR I/Os, use the same MDIC resistor value of 162 Ω. The memory controller register setting can be used to determine automatic calibration is done to full or half drive strength. These pins are used for automatic calibration of the DDR4 I/Os.

4. This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. This pull-up is designed such that it can be overpowered by an external 4.7 kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.

5. Pin must **NOT** be pulled down during power-on reset. This pin may be pulled up, driven high, or, if there are any externally connected devices, left in tristate. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.

6. Recommend that a weak pull-up resistor (2-10 kΩ) be placed on this pin to the respective power supply.

7. This pin is an open-drain signal.

8. Recommend that a pull-up resistor (1 kΩ) be placed on this pin to the respective power supply.

9. This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled.

10. These are test signals for factory use only and must be pulled up (100 Ω to 1 kΩ) to the respective power supply for normal operation.

11. This pin requires a 200 Ω pull-up to the respective power supply.

12. Do not connect. These pins should be left floating.

13. These pins must be pulled up to TV_{DD} through a 180 Ω ± 1% resistor for MDC and a 330 Ω ± 1% resistor for MDIO.

14. This pin requires an external 1 kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.

15. These pins must be pulled to ground (GND).

16. This pin requires a 698 Ω pull-up to the respective power supply.

17. These pins should be tied to ground if the diode is not utilized for temperature monitoring.

18. SD_GND must be directly connected to GND.

19. For proper clock selection, terminate cfg_eng_use0 with a pull up or pull down of 4.7 kΩ to ensure that the signal will have a valid state as soon as the IO voltage reaches its operating condition.

20. DIFF_SYSCLK and DIFF_SYSCLK_B is tied to cfg_eng_use0, the configuration is described in section "Reset Configuration Word (RCW)" of *QorIQ LS1088A Reference Manual*.

Warning

See **"Connection Recommendations"** for additional details on properly connecting these pins for specific applications.

3 Electrical characteristics

This section describes the DC and AC electrical specifications for the chip. The chip is currently targeted to these specifications, some of which are independent of the I/O cell but are included for a more complete reference. These are not purely I/O buffer design specifications.

3.1 Overall DC electrical characteristics

This section describes the ratings, conditions, and other characteristics.

3.1.1 Absolute maximum ratings

This table provides the absolute maximum ratings.

Table 2. Absolute maximum ratings[1]

Characteristic	Symbol	Min	Max	Unit	Notes
Core and platform supply voltage	V_{DD}	-0.3	1.1	V	8
PLL supply voltage (core PLL, platform, DDR)	AV_{DD}_CGA1, AV_{DD}_CGA2, AV_{DD}_PLAT, AV_{DD}_D1	-0.3	1.98	V	—
PLL supply voltage (SerDes, filtered from XV_{DD})	AVDD_SD*n*_PLL1 AVDD_SD*n*_PLL2	-0.3	1.48	V	—
SFP Fuse Programming	TA_PROG_SFP	-0.3	1.98	V	—
Thermal Unit Monitor supply	TH_V_{DD}	-0.3	1.98	V	—
IFC, SPI, GIC (IRQ 0/1/2), Tamper_Detect, System control and power management, SYSCLK, DDR_CLK, GPIO1, GPIO2, GPIO3, eSDHC[4-7]/VS/DAT123_DIR/DAT0_DIR/ CMD_DIR/SYNC), Debug, JTAG, RTC, POR signals	OV_{DD}	-0.3	1.98	V	—

Table continues on the next page...

Table 2. Absolute maximum ratings[1] (continued)

Characteristic		Symbol	Min	Max	Unit	Notes
DUART1/2, I^2C, DMA, QE, GPIO3, GPIO4, GIC (IRQ 3/4/5/6/7/8/9/10), USB control (DRVVBUS, PWRFAULT)		DV_{DD}	-0.3	3.63; 1.98	V	9
eSDHC[0-3]/CLK/CMD, GPIO3		EV_{DD}	-0.3	3.63; 1.98	V	—
DDR4 DRAM I/O voltage		$G1V_{DD}$	-0.3	1.32	V	—
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receivers and DIFF_SYSCLK		SV_{DD}	-0.3	1.1	V	—
Pad power supply for SerDes transmitter		XV_{DD}	-0.3	1.48	V	—
Ethernet interface 1/2, Ethernet management interface 1 (EMI1), TSEC_1588, GPIO2, GPIO4, GIC (IRQ11)		LV_{DD}	-0.3	2.75; 1.98	V	—
Ethernet management interface 2 (EMI2), GPIO2		TV_{DD}	-0.3	2.75; 1.98; 1.32	V	—
USB PHY Transceiver supply voltage		USB_HV_{DD}	-0.3	3.63	V	10
		USB_SDV_{DD}	-0.3	1.1	V	11
		USB_SV_{DD}	-0.3	1.1	V	12
Battery Backed Security Monitor supply		$TA_BB_V_{DD}$	-0.3	1.1	V	—
Input voltage	DDR4 DRAM signals	MV_{IN}	-0.3	$G1V_{DD}$ + 0.3	V	2
	SerDes interface and DIFF_SYSCLK	SV_{IN}	-0.3	-0.3 to (SV_{DD} + 0.3)	V	5
	Ethernet interface 1/2, Ethernet management interface 1 (EMI1), TSEC_1588, GPIO2, GPIO4, GIC (IRQ11)	LV_{IN}	-0.3	LV_{DD} + 0.3	V	4, 5
	IFC, SPI, GIC (IRQ 0/1/2), Tamper_Detect, System control and power management, SYSCLK, DDR_CLK, GPIO3, GPIO2, GPIO1, eSDHC[4-7]/VS/ DAT123_DIR/ DAT0_DIR/CMD_DIR/ SYNC), Debug, JTAG, RTC, POR signals	OV_{IN}	-0.3	OV_{DD} + 0.3	V	3, 5
	eSDHC[0-3]/CLK/ CMD, GPIO3	EV_{IN}	-0.3	EV_{DD} + 0.3	V	5, 6, 7
	DUART1/2, I^2C, DMA, QE, GPIO3, GPIO4, GIC (IRQ	DV_{IN}	-0.3	DV_{DD} + 0.3	V	5, 6, 9

Table continues on the next page...

Table 2. Absolute maximum ratings[1] (continued)

Characteristic		Symbol	Min	Max	Unit	Notes
	3/4/5/6/7/8/9/10), USB control (DRVVBUS, PWRFAULT)					
	Ethernet management interface 2 (EMI2), GPIO2	TV_{IN}	-0.3	TV_{DD} + 0.3	V	13
USB PHY transceiver supply voltage	Transceiver supply for USB PHY	USB_HV_{IN}	-0.3	USB_HV_{DD} + 0.3	V	10
	Analog and Digital HS supply for USB PHY	USB_SDV_{DD}	-0.3	USB_SDV_{DD} + 0.3	V	11
	Analog and Digital SS supply for USB PHY	USB_SV_{DD}	-0.3	USB_SV_{DD} + 0.3	V	12
Storage temperature range		T_{STG}	-55	150	°C	--

Notes:

1. Functional operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

4. **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

5. (D, G1, L, O, X, S, T, E)V_{IN} and $USBn_HV_{IN}$ may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 7.

6. **Caution:** DV_{IN} must not exceed DV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

7. **Caution:** EV_{IN} must not exceed EV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

8. Supply voltage specified at the voltage sense pin. Voltage input pins should be regulated to provide specified voltage at the sense pin.

9. See the power supply column to determine which power supply rail is used for each interface.

10. Transceiver supply for USB PHY.

11. Analog and Digital SS supply for USB PHY.

12. Analog and Digital HS supply for USB PHY.

13. **Caution:** TV_{IN} must not exceed TV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

3.1.2 Recommended operating conditions

This table provides the recommended operating conditions for this chip.

NOTE

The values shown are the recommended operating conditions and proper device operation outside these conditions is not guaranteed.

Table 3. Recommended operating conditions

Characteristic	Symbol	Recommended value	Unit	Notes
VID core and platform supply voltage at initial start up	V_{DD}	1.025 V ± 30 mV	V	3, 4, 5, 9
VID core and platform supply voltage during normal operation		VID ± 30 mV	V	3, 4, 5, 9
0.9V core and platform supply voltage		0.9 V ± 30 mV	V	4, 5, 9
0.9V core and platform supply voltage at initial start up		1.025 V ± 30 mV or 0.9 V ± 30 mV	V	4, 5, 9
Battery backed security monitor supply (TA_BB_TMP_DETECT_B)	TA_BB_V_{DD}	1.0 V + 50 mV / - 30 mV	V	9
		0.9 V + 50 mV / - 30 mV	V	9
PLL supply voltage (core PLL, platform, DDR)	AV_{DD}_CGA1, AV_{DD}_CGA2, AV_{DD}_PLAT, AV_{DD}_D1	1.8 V ± 90 mV	V	—
PLL supply voltage (SerDes, filtered from XV_{DD})	AV_{DD}_SD*n*_PLL1 AV_{DD}_SD*n*_PLL2	1.35 V ± 67 mV	V	—
SFP fuse programming	TA_PROG_SFP	1.8 V ± 90 mV	V	2
Thermal monitor unit supply	TH_V_{DD}	1.8 V ± 90 mV	V	—
IFC, SPI, GIC (IRQ 0/1/2), Tamper_Detect, System control and power management, SYSCLK, DDR_CLK, GPIO3, GPIO2, GPIO1, eSDHC[4-7]/VS/DAT123_DIR/ DAT0_DIR/CMD_DIR/SYNC), Debug, JTAG, RTC, POR signals	OV_{DD}	1.8 V ± 90 mV	V	—
DUART1/2, I^2C, DMA, QE, GPIO3, GPIO4, GIC (IRQ 3/4/5/6/7/8/9/10), USB control (DRVVBUS, PWRFAULT)	DV_{DD}	3.3 V ± 165 mV 1.8 V ± 90 mV	V	6
eSDHC[0-3]/CLK/CMD, GPIO3	EV_{DD}	3.3 V ±165 mV 1.8 V ± 90 mV	V	—
DDR4 DRAM I/O voltage	$G1V_{DD}$	1.2V ± 60 mV	V	—
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receivers and DIFF_SYSCLK	SV_{DD}	1.0 V + 50 mV / - 30 mV	V	9
		0.9V +50 mV / -30 mV	V	9
Pad power supply for SerDes transmitters	XV_{DD}	1.35 V ± 67 mV	V	—
Ethernet interface 1/2, Ethernet management interface 1 (EMI1), TSEC_1588, GPIO2, GPIO4, GIC (IRQ11)	LV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	1
Ethernet management interface 2 (EMI2), GPIO2	TV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV 1.2V ± 60 mV	V	—
USB PHY 3.3 V high supply voltage	USB_HV_{DD}	3.3 V ± 165 mV	V	6

Table continues on the next page...

Table 3. Recommended operating conditions (continued)

Characteristic		Symbol	Recommended value	Unit	Notes
USB PHY analog and digital HS supply		USB_SDV_{DD}	1.0 + 50 mV / - 30 mV	V	7, 9
			0.9 V + 50 mV / - 30 mV	V	7, 9
USB PHY analog and digital SS supply		USB_SV_{DD}	1.0 + 50 mV / - 30 mV	V	8, 9
			0.9 V + 50 mV / - 30 mV	V	8, 9
Input voltage	DDR4 DRAM signals	MV_{IN}	GND to $G1V_{DD}$	V	—
	Ethernet interface 1/2, Ethernet management interface 1 (EMI1), TSEC_1588, GPIO2, GPIO4, GIC (IRQ11)	LV_{IN}	GND to LV_{DD}	V	—
	IFC, SPI, GIC (IRQ 0/1/2), Tamper_Detect, System control and power management, SYSCLK, DDR_CLK, GPIO3, GPIO2, GPIO1, eSDHC[4-7]/VS/ DAT123_DIR/DAT0_DIR/ CMD_DIR/SYNC), Debug, JTAG, RTC, POR signals	OV_{IN}	GND to OV_{DD}	V	—
	DUART1/2, I^2C, DMA, QE, GPIO3, GPIO4, GIC (IRQ 3/4/5/6/7/8/9/10), USB Control (DRVVBUS, PWRFAULT)	DV_{IN}	GND to DV_{DD}	V	—
	eSDHC[0-3]/CLK/CMD, GPIO3	EV_{IN}	GND to EV_{DD}	V	—
	Main power supply for internal circuitry of SerDes and DIFF_SYSCLK	SV_{IN}	GND to SV_{DD}	V	—
	Ethernet management interface 2 (EMI2), GPIO2	TV_{IN}	GND to TV_{DD}	V	—
PHY transceiver signals	USB transceiver supply for USB PHY	USB_HV_{IN}	GND to USB_HV_{DD}	V	6
	Analog and digital SS supply for USB PHY	USB_SDV_{DD}	GND to USB_SDV_{DD}	V	7
	Analog and digital HS supply for USB PHY	USB_SV_{DD}	0.3 to USB_SV_{DD}	V	8
Operating temperature range	Normal operation	T_A, T_J	T_A = 0 (min) to T_J = 105 (max)	°C	—
	Extended temperature	T_A, T_J	T_A = -40 (min) to T_J = 105 (max)	°C	—
	Secure boot fuse programming	T_A, T_J	T_A = 0 (min) to T_J = 105 (max)	°C	2

Notes:

1. RGMII is supported at 2.5 V or 1.8 V.

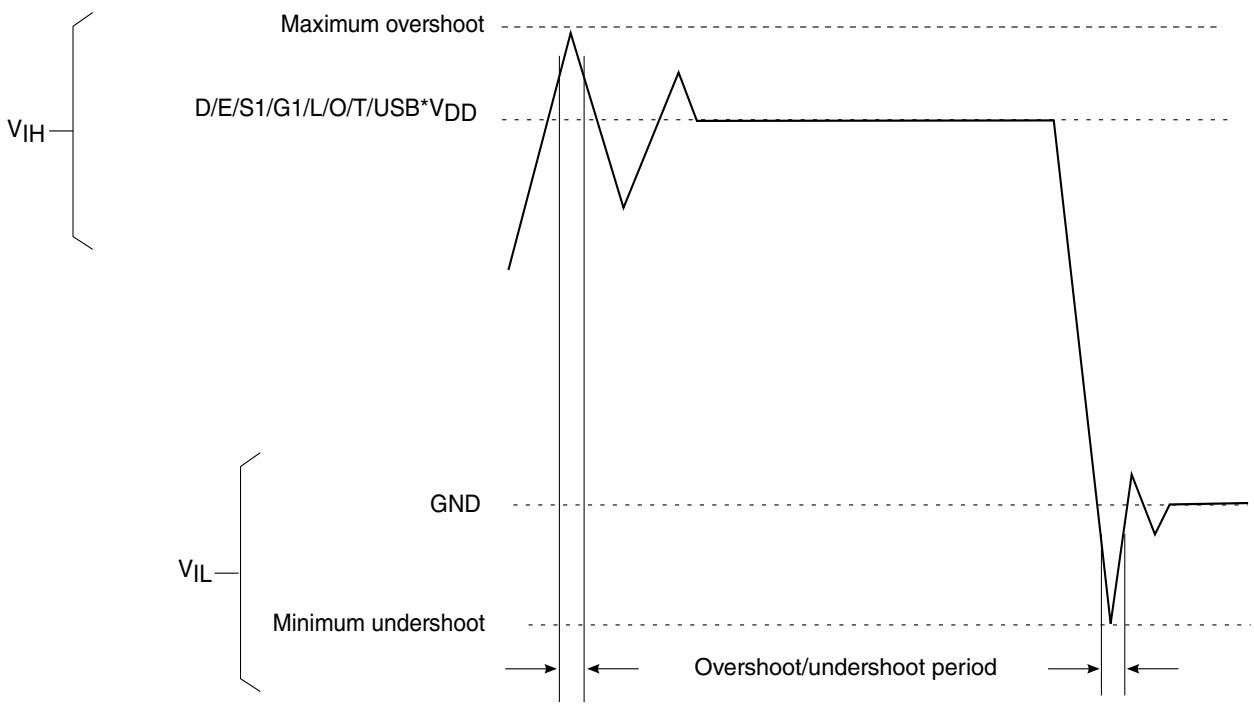
2. TA_PROG_SFP must be supplied 1.8 V and the chip must operate in the specified fuse programming temperature range only during secure boot fuse programming, subject to the power sequencing constraints shown in Power sequencing. For all other operating conditions, TA_PROG_SFP must be tied to GND.

3. For additional information, see the Core and platform supply voltage filtering section in the chip design checklist.

Table 3. Recommended operating conditions

Characteristic	Symbol	Recommended value	Unit	Notes
4. Supply voltage specified at the voltage sense pin. Voltage input pins should be regulated to provide specified voltage at the sense pin.				
5. Operation at 1.1 V is allowable for up to 25 ms at initial power on.				
6. Transceiver supply for USB PHY.				
7. Analog and Digital SS supply for USB PHY.				
8. Analog and Digital HS supply for USB PHY.				
9. For supported voltage requirement for a given part number, contact your NXP sales representative.				

This figure shows the undershoot and overshoot voltages at the interfaces of the chip.



Notes:
The overshoot/undershoot period should be less than 10% of shortest possible toggling period of the input signal or per input signal specific protocol requirement. For GPIO input signal overshoot/undershoot period, it should be less than 10% of the SYSCLK period.

Figure 7. Overshoot/Undershoot voltage for $G1V_{DD}$/OV_{DD}/$S1V_{DD}$/DV_{DD}/TV_{DD}/ LV_{DD}/EV_{DD}/ USB*V_{DD}

See Table 3 for actual recommended core voltage. Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. DVDD-, OVDD-, and LVDD-based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM

interface uses differential receivers referenced by the internally generated MVREF signal. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

3.1.3 Output driver characteristics

This chip provides information on the characteristics of the output driver strengths.

NOTE

These values are preliminary estimates.

Table 4. Output drive capability

Driver type	Output impedance (Ω)			Supply Voltage	Notes
	Minimum[2]	Typical	Maximum[3]		
DDR4 signal	-	18 (full-strength mode) 27 (half-strength mode)	-	$G1V_{DD}$ = 1.2 V	1
Ethernet interface 1/2, Ethernet management interface 1 (EMI1), TSEC_1588, GPIO2, GPIO4, GIC (IRQ11)	30	50	70	LV_{DD} = 2.5 V	-
	30	45	60	LV_{DD} = 1.8 V	-
MDC of Ethernet management interface 2 (EMI 2)	45	65	100	TV_{DD} = 1.2 V	-
	40	55	75	TV_{DD} = 1.8 V	-
	40	60	90	TV_{DD} = 2.5 V	-
MDIO of Ethernet management interface 2 (EMI 2)	30	40	60	TV_{DD} = 1.2 V	-
	25	33	44	TV_{DD} = 1.8 V	-
	25	40	57	TV_{DD} = 2.5 V	-
IFC, SPI, GIC (IRQ 0/1/2), Tamper_Detect, System control and power management, DDR_CLK, GPIO1, GPIO2, GPIO3, eSDHC[4-7]/VS/DAT123_DIR/DAT0_DIR/ CMD_DIR/SYNC), Debug, JTAG, RTC, POR signals	30	45	60	OV_{DD} = 1.8 V	-
DUART1/2, I^2C, DMA, QE, GPIO3, GPIO4, GIC (IRQ 3/4/5/6/7/8/9/10), USB control (DRVVBUS, PWRFAULT)	45	65	90	DV_{DD} = 3.3 V	-
	40	55	75	DV_{DD} = 1.8 V	
eSDHC[0-3]/CLK/CMD, GPIO3	45	65	90	EV_{DD} = 3.3 V	-
	40	55	75	EV_{DD} = 1.8 V	

1. The drive strength of the DDR4 interface in half-strength mode is at T_j = 105°C and at $G1V_{DD}$ (min).

2. Estimated number based on best case processed device.

3. Estimated number based on worst case processed device.

3.2 General AC timing specifications

This table provides AC timing specifications for the sections not covered under the specific interface sections.

Table 5. AC Timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
Input signal rise and fall times	t_R/t_F	-	5	ns	1
1. Rise time refers to signal transitions from 10% to 90% of Supply; fall time refers to transitions from 90% to 10% of supply					

3.3 Power sequencing

The chip requires that its power rails be applied in a specific sequence in order to ensure proper device operation. For power up, these requirements are as follows:

1. AV_{DD}_SDn_PLL1, AV_{DD}_SDn_PLL2, EV_{DD}, DV_{DD}, LV_{DD}, OV_{DD}, SV_{DD}, TV_{DD}, XV_{DD}, USB_HV_{DD}, USB_SDV_{DD}, USB_SV_{DD}. Drive TA_PROG_SFP = GND.
   - PORESET_B input must be driven asserted and held during this step.
2. V_{DD}.
3. $G1V_{DD}$.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of their value. XV_{DD}, AV_{DD}_SD*n*_PLL1, and AV_{DD}_SD*n*_PLL2 have no ordering requirement to any other supplies, and they can ramp up in any step. SV_{DD} should ramp up before VDD. Alternatively, V_{DD} may ramp up together with SV_{DD} provided that the relative timing between SV_{DD} and V_{DD} ramp up conforms to Figure 8 below.

All supplies must be at their stable values within 400 ms.

Negate PORESET_B input when the required assertion/hold time has been met per RESET initialization timing specifications.

NOTE

- While V_{DD} is ramping up, leakage current might occur from V_{DD} through LS1088A to $G1V_{DD}$.
- Ensure that SYSCLK is available as soon as power ramps up.
- Ramp rate requirements should be met per Table 11.

NOTE

If using Trust Architecture Security Monity battery backed features, prior to V_{DD} or SV_{DD} ramping up to 0.5 V level, ensure that OV_{DD} is properly ramped to at least 90% and SYSCLK or DIFF_SYSCLK / DIFF_SYSCLK_B is running. The clock should have a minimum frequency of 800 Hz and a maximum frequency no greater that the supported system clock frequency for the device.

Warning

Only 300,000 POR cycles are permitted per lifetime of a device. Note that this value is based on design estimates and is preliminary.

This figure shows the SV_{DD} and V_{DD} ramp-up diagram.

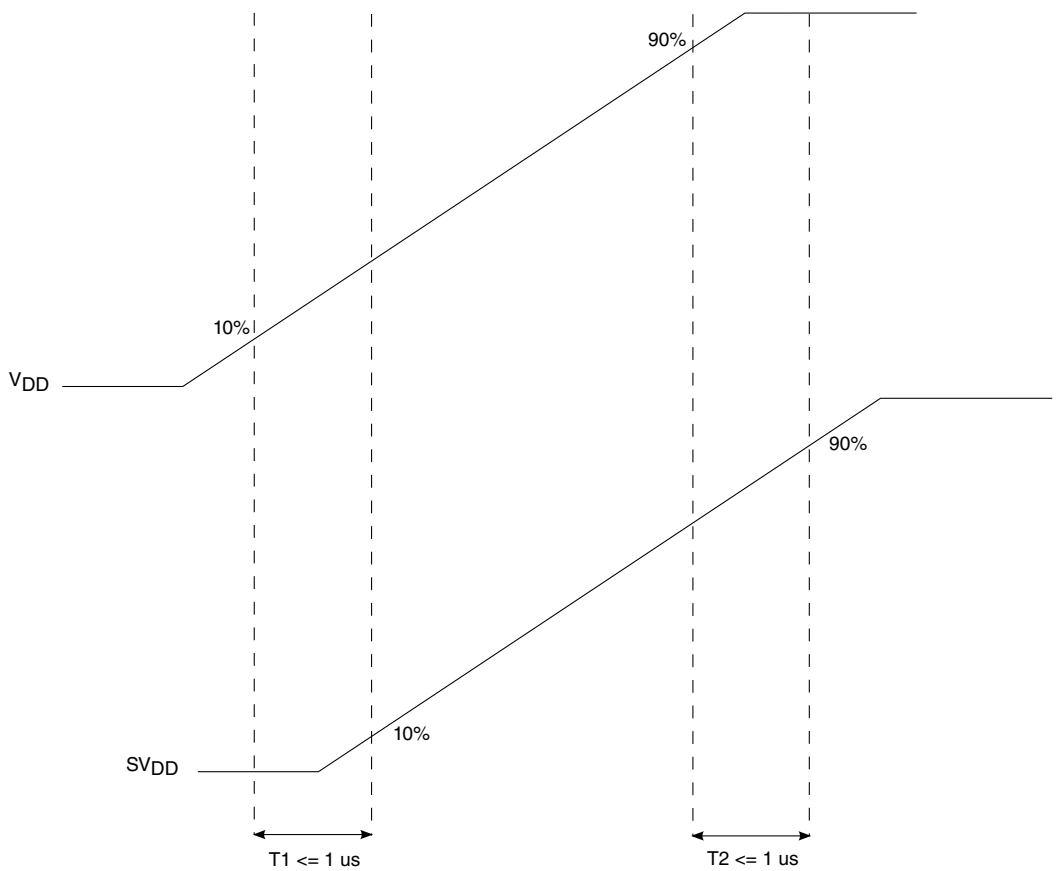


Figure 8. SV_{DD} and V_{DD} ramp-up diagram

For secure boot fuse programming, use the following steps:

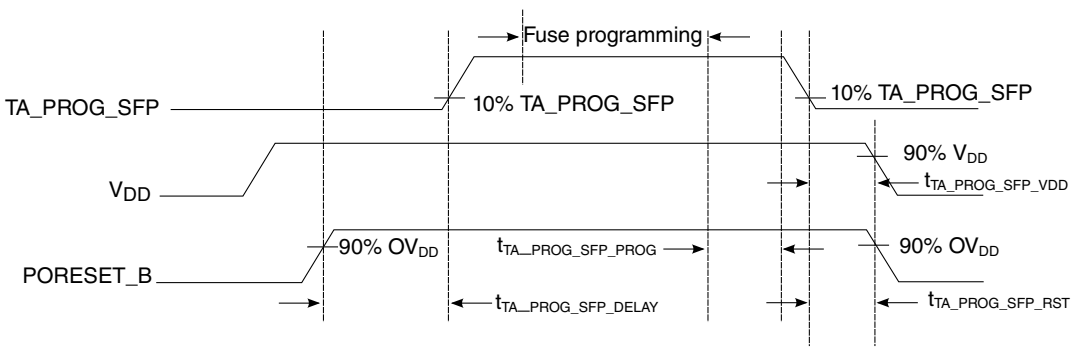
1. After negation of PORESET_B, drive TA_PROG_SFP = 1.80 V after a required minimum delay per Table 6.

2. After fuse programming is completed, it is required to return TA_PROG_SFP = GND before the system is power cycled (PORESET_B assertion) or powered down (V_{DD} ramp down) per the required timing specified in Table 6. See Security fuse processor for additional details.

Warning

No activity other than that required for secure boot fuse programming is permitted while TA_PROG_SFP is driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while TA_PROG_SFP = GND.

This figure shows the TA_PROG_SFP timing diagram.



NOTE: TA_PROG_SFP must be stable at 1.8 V prior to initiating fuse programming.

Figure 9. TA_PROG_SFP timing diagram

This table provides information on the power-down and power-up sequence parameters for TA_PROG_SFP.

Table 6. TA_PROG_SFP timing [5]

Driver type	Min	Max	Unit	Notes
$t_{TA_PROG_SFP_DELAY}$	100	—	SYSCLKs	1
$t_{TA_PROG_SFP_PROG}$	0	—	us	2
$t_{TA_PROG_SFP_VDD}$	0	—	us	3
$t_{TA_PROG_SFP_RST}$	0	—	us	4

Notes:

1. Delay required from the deassertion of PORESET_B to driving TA_PROG_SFP ramp up. Delay measured from PORESET_B deassertion at 90% OV_{DD} to 10% TA_PROG_SFP ramp up.

2. Delay required from fuse programming completion to TA_PROG_SFP ramp down start. Fuse programming must complete while TA_PROG_SFP is stable at 1.8 V. No activity other than that required for secure boot fuse programming is permitted while TA_PROG_SFP is driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while TA_PROG_SFP = GND. After fuse programming is complete, it is required to return TA_PROG_SFP = GND.

Table 6. TA_PROG_SFP timing [5]

Driver type	Min	Max	Unit	Notes
3. Delay required from TA_PROG_SFP ramp-down complete to V_{DD} ramp-down start. TA_PROG_SFP must be grounded to minimum 10% TA_PROG_SFP before V_{DD} reaches 90% V_{DD}. 4. Delay required from TA_PROG_SFP ramp-down complete to PORESET_B assertion. TA_PROG_SFP must be grounded to minimum 10% TA_PROG_SFP before PORESET_B assertion reaches 90% OV_{DD}. 5. Only two secure boot fuse programming events are permitted per lifetime of a device.				

3.4 Power-down requirements

The power-down cycle must complete such that power supply values are below 0.4 V before a new power-up cycle can be started.

If performing secure boot fuse programming per the requirements in Power sequencing, it is required that TA_PROG_SFP = GND before the system is power cycled (PORESET_B assertion) or powered down (V_{DD} ramp down) per the required timing specified in Power sequencing.

3.5 Power characteristics

This table shows the thermal power dissipation of the V_{DD} power supply for A53 core/ platform/DDR frequency combinations.

Table 7. LS1088A VDD power dissipation for the thermal design

A53 frequency (MHz)	Platform frequency(MHz)	Main DDR data rate (MT/s)	V_{DD} (V)	Power (W)	Notes
1600	700	2100	VID	9.6	1, 2, 3, 4
1400	600	1800	VID	7.6	1, 2, 3, 4
1200	500	1600	0.9	5.3	1, 2, 3, 4

Notes:

1. VDD must run at VID voltage level, which is defined in FUSESR register
2. Thermal power assumes Dhrystone running with activity factor of 60% (on all cores) and executing DMA on the platform at 100% activity factor. AIOP is powered but idle.
3. Thermal power are based on worst-case processed device. The above powers are measured at the junction temperature of 85C.
4. Refer to AN5144 "QorIQ LS1088A Design Checklist":

Section "Maximum VDD Power and IO Power" for the power supply design and regulator sizing

Section "Thermal Power" for the thermal power and thermal solution design

Table 8. LS1048A VDD power dissipation for the thermal design

A53 frequency (MHz)	Platform frequency(MHz)	Main DDR data rate (MT/s)	V_{DD} (V)	Power (W)	Notes
1600	700	2100	VID	8.0	1, 2, 3, 4
1400	600	1800	VID	6.4	1, 2, 3, 4
1200	500	1600	0.9	4.5	1, 2, 3, 4

Notes:

1. VDD must run at VID voltage level, which is defined in FUSESR register
2. Thermal power assumes Dhrystone running with activity factor of 70% (on all cores) and executing DMA on the platform at 100% activity factor. AIOP is powered but idle
3. Thermal power are based on worst-case processed device. The above powers are measured at the junction temperature of 85C.
4. Refer to AN5144 "QorIQ LS1088A Design Checklist":

Section "Maximum VDD Power and IO Power" for the power supply design and regulator sizing

Section "Thermal Power" for the thermal power and thermal solution design

Table 9. LS1084A VDD power dissipation for the thermal design

A53 frequency (MHz)	Platform frequency(MHz)	Main DDR data rate (MT/s)	V_{DD} (V)	Power (W)	Notes
1600	700	2100	VID	9.3	1, 2, 3, 4
1400	600	1800	VID	7.4	1, 2, 3, 4
1200	500	1600	0.9	5.2	1, 2, 3, 4

Notes:

1. VDD must run at VID voltage level, which is defined in FUSESR register
2. Thermal power assumes Dhrystone running with activity factor of 60% (on all cores) and executing DMA on the platform at 100% activity factor.
3. Thermal power are based on worst-case processed device. The above powers are measured at the junction temperature of 85C.
4. Refer to AN5144 "QorIQ LS1088A Design Checklist":

Section "Maximum VDD Power and IO Power" for the power supply design and regulator sizing

Section "Thermal Power" for the thermal power and thermal solution design

Table 10. LS1044A VDD power dissipation for the thermal design

A53 frequency (MHz)	Platform frequency(MHz)	Main DDR data rate (MT/s)	V_{DD} (V)	Power (W)	Notes
1600	700	2100	VID	7.7	1, 2, 3, 4
1400	600	1800	VID	6.1	1, 2, 3, 4
1200	500	1600	0.9	4.3	1, 2, 3, 4

Notes:

1. VDD must run at VID voltage level, which is defined in FUSESR register

Table 10. LS1044A VDD power dissipation for the thermal design

A53 frequency (MHz)	Platform frequency(MHz)	Main DDR data rate (MT/s)	V_{DD} (V)	Power (W)	Notes
2. Thermal power assumes Dhrystone running with activity factor of 70% (on all cores) and executing DMA on the platform at 100% activity factor.					
3. Thermal power are based on worst-case processed device. The above powers are measured at the junction temperature of 85C.					
4. Refer to AN5144 "QorIQ LS1088A Design Checklist":					
Section "Maximum VDD Power and IO Power" for the power supply design and regulator sizing					
Section "Thermal Power" for the thermal power and thermal solution design					

3.6 Power-on ramp rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid excess in-rush current.

This table provides the power supply ramp rate specifications.

Table 11. Power supply ramp rate

Parameter	Min	Max	Unit	Notes
Required ramp rate for all voltage supplies (including OV_{DD}/DV_{DD}/$G1V_{DD}$/ SV_{DD}/XV_{DD}/LV_{DD}/EV_{DD}/TV_{DD} all core and platform V_{DD} supplies, TA_PROG_SFP, and all AV_{DD} supplies.)	—	25	V/ms	1, 2
Required ramp rate for PROG_SFP	---	25	V/ms	1,2
Required ramp rate for USB_HVDD	---	26.7	V/ms	1,2
Notes:				
1. Ramp rate is specified as a linear ramp from 10% to 90%. If non-linear (for example, exponential), the maximum rate of change from 200 mV to 500 mV is the most critical as this range might falsely trigger the ESD circuitry.				
2. Over full recommended operating temperature range. See Table 3.				

3.7 Input clocks

3.7.1 System clock (SYSCLK)

This section describes the system clock DC electrical characteristics and AC timing specifications.

3.7.1.1 SYSCLK DC electrical characteristics

This table provides the SYSCLK DC characteristics.

Table 12. SYSCLK DC electrical characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 X OV_{DD}	—	—	V	1
Input low voltage	V_{IL}	—	—	0.3 X OV_{DD}	V	1
Input capacitance	C_{IN}	—	7	12	pF	—
Input current (V_{IN}= 0 V or V_{IN} = OV_{DD})	I_{IN}	—	—	± 50	μA	2

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. At recommended operating conditions with OV_{DD}= 1.8 V. See Table 3.

3.7.1.2 SYSCLK AC timing specifications

This table provides the SYSCLK AC timing specifications.

Table 13. SYSCLK AC timing specifications[1, 5]

Parameter/condition	Symbol	Min	Typ	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	100.0	—	125/133.3	MHz	2, 6
SYSCLK cycle time	t_{SYSCLK}	7.5	—	10.0	ns	1, 2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	2
SYSCLK slew rate	—	1	—	4	V/ns	3
SYSCLK peak period jitter	—	—	—	± 150	ps	—
SYSCLK jitter phase noise at -56 dBc	—	—	—	500	kHz	4
AC Input Swing Limits at 1.8 V OV_{DD}	ΔV_{AC}	1.08	—	1.8	V	—

Notes:

1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting SYSCLK frequencies do not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at OV_{DD}/2.
3. Slew rate as measured from 0.35 x OV_{DD} to 0.65 x OV_{DD}.
4. Phase noise is calculated as FFT of TIE jitter.
5. At recommended operating conditions with OV_{DD} = 1.8 V. See Table 3.
6. The 125 MHz max frequency is limited to parts with 1200 MHz CPU frequency. The 133 MHz max frequency can be used for parts with 1600 MHz and 1400 MHz CPU frequency.

3.7.2 Spread-spectrum sources

Spread-spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter to diffuse the EMI spectral content.

The jitter specification given in this table considers short-term (cycle-to-cycle) jitter only. The clock generator's cycle-to-cycle output jitter should meet the chip's input cycle-to-cycle jitter requirement.

Frequency modulation and spread are separate concerns; the chip is compatible with spread-spectrum sources if the recommendations listed in this table are observed.

Table 14. Spread-spectrum clock source recommendations[3]

Parameter	Min	Max	Unit	Notes
Frequency modulation	—	60	kHz	—
Frequency spread	—	1.0	%	1, 2

Notes:

1. SYSCLK frequencies that result from frequency spreading and the resulting core frequency must meet the minimum and maximum specifications given in Table 13.

2. Maximum spread-spectrum frequency may not result in exceeding any maximum operating frequency of the device.

3. At recommended operating conditions with OVDD = 1.8 V. See Table 3.

CAUTION

The processor's minimum and maximum SYSCLK and core/platform/DDR frequencies must not be exceeded, regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core/platform/DDR frequency should use only down-spreading to avoid violating the stated limits.

3.7.3 USB 3.0 reference clock requirements

There are two options for the reference clock of USB PHY: SYSCLK or DIFF_SYSCLK/DIFF_SYSCLK_B. This table provides the additional requirements when SYSCLK or DIFF_SYSCLK/DIFF_SYSCLK_B is used as USB REFCLK. The 100 MHz reference clock is also required with the following requirements.

Table 15. USB AC timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
Reference clock frequency-offset	F_{REF_OFFSET}	-300.0	300.0	ppm	-
Reference clock random jitter (RMS)	$JRMS_{REF_CLK}$	-	3.0	ps	1, 2
Reference clock deterministic jitter	DJ_{REF_CLK}	-	150.0	ps	3
Duty cycle	DC_{REF_CLK}	40.0	60.0	%	-
1. 1.5 MHz to Nyquist frequency. For example, for 100 MHz reference clock, the Nyquist frequency is 50 MHz.					
2. The peak-to-peak Rj specification is calculated at 14.069 times the RJ_{RMS} for 10^{-12} BER.					
3. DJ across all frequencies.					

3.7.4 Real-time clock timing

The real-time clock timing (RTC) input is sampled by the platform clock. The output of the sampling latch is then used as an input to the time base unit of the core; there is no need for jitter specification. The minimum period of the RTC signal should be greater than or equal to 16x the period of the platform clock with a 50% duty cycle. There is no minimum RTC frequency; RTC pin may be grounded if not needed.

3.7.5 Gigabit Ethernet reference clock timing

This table provides the Ethernet gigabit reference clock DC electrical characteristics with LV_{DD} = 1.8 V.

Table 16. EC*n*_GTX_CLK125 DC electrical characteristics (LV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	—	—	V	2
Input low voltage	V_{IL}	—	—	0.3 x OV_{DD}	V	2
Input capacitance	C_{IN}	—	—	6	pF	—
Input current (V_{IN} = 0 V or V_{IN} = LV_{DD})	I_{IN}	—	—	± 50	μA	3
Notes:						
1. For recommended operating conditions, see Table 3.						
2. The min V_{IL} and max V_{IH} values are based on the respective min and max V_{IN} values found in Table 3.						
3. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 3.						

This table provides the Ethernet gigabit reference clock DC electrical characteristics with LV_{DD} = 2.5 V.

Table 17. EC*n*_GTX_CLK125 DC electrical characteristics (LV_{DD} = 2.5 V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 X LV_{DD}	—	—	V	2
Input low voltage	V_{IL}	—	—	0.2 x LV_{DD}	V	2
Input capacitance	C_{IN}	—	—	6	pF	—
Input current (V_{IN} = 0 V or V_{IN} = LV_{DD})	I_{IN}	—	—	± 50	μA	3

Notes:

1. For recommended operating conditions, see Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max V_{IN} values found in Table 3.
3. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 3.

This table provides the Ethernet gigabit reference clock AC timing specifications.

Table 18. EC*n*_GTX_CLK125 AC timing specifications [1]

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC*n*_GTX_CLK125 frequency	f_{G125}	125 - 100 ppm	125	125 + 100 ppm	MHz	—
EC*n*_GTX_CLK125 cycle time	t_{G125}	7.5	8	8.5	ns	—
EC*n*_GTX_CLK125 rise and fall time LV_{DD} = 1.8 V LV_{DD} = 2.5 V	t_{G125R}/t_{G125F}	—	—	 0.54 0.75	ns	2
EC*n*_GTX_CLK125 duty cycle 1000Base-T for RGMII	t_{G125H}/t_{G125}	40	—	60	%	3
EC*n*_GTX_CLK125 jitter	—	—	—	± 150	ps	3

Notes:

1. At recommended operating conditions with LV_{DD} = 1.8 V ± 90mV / 2.5 V ± 125 mV. See Table 3.
2. Rise times are measured from 20% of LVDD to 80% of LV_{DD}. Fall times are measured from 80% of LV_{DD} to 20% of LV_{DD}.
3. ECn_GTX_CLK125 is used to generate the GTX clock for the Ethernet transmitter. See RGMII AC timing specifications for duty cycle for the 10Base-T and 100Base-T reference clocks.

3.7.6 DDR clock (DDRCLK)

This section provides the DDRCLK DC electrical characteristics and AC timing specifications.

3.7.6.1 DDRCLK DC electrical characteristics

This table provides the DDRCLK DC electrical characteristics.

Table 19. DDRCLK DC electrical characteristics[3]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	—	—	V	1
Input low voltage	V_{IL}	—	—	0.3 x OV_{DD}	V	1
Input capacitance	C_{IN}	—	7	12	pF	—
Input current (V_{IN}= 0V or V_{IN} = OV_{DD})	I_{IN}	—	—	± 50	μA	2

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.
3. At recommended operating conditions with OV_{DD} = 1.8 V. See Table 3.

3.7.6.2 DDRCLK AC timing specifications

This table provides the DDRCLK AC timing specifications.

Table 20. DDRCLK AC timing specifications[5]

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
DDRCLK frequency	f_{DDRCLK}	100.0	—	133.3	MHz	1, 2
DDRCLK cycle time	t_{DDRCLK}	7.5	—	10	ns	1, 2
DDRCLK duty cycle	t_{KHK}/t_{DDRCLK}	40	—	60	%	2
DDRCLK slew rate	—	1	—	4	V/ns	3
DDRCLK peak period jitter	—	—	—	± 150	ps	—
DDRCLK jitter phase noise at -56 dBc	—	—	—	500	kHz	4
AC Input Swing Limits at 1.8 V OV_{DD}	ΔV_{AC}	1.08	—	1.8	V	—

Notes:

1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting DDRCLK frequencies do not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at OV_{DD}/2.
3. Slew rate as measured from 0.35 x OV_{DD} to 0.65 x OV_{DD}.
4. Phase noise is calculated as FFT of TIE jitter.
5. At recommended operating conditions with OV_{DD} = 1.8 V. See Table 3.
6. DDRCLK pin does not provide the reference clock to DDR when chip is operated in Single Source Clocking mode.

3.7.7 Differential system clock (DIFF_SYSCLK/DIFF_SYSCLK_B) timing specifications

The single source clocking mode requires a single on-board oscillator to provide reference clock input to the differential system clock pair (DIFF_SYSCLK/ DIFF_SYSCLK_B).

This differential clock pair input can provide the clock to core, platform, DDR, and SerDes1, SerDes2 PLLs, and USB PLLs.

This figure shows a receiver reference diagram of the differential system clock.

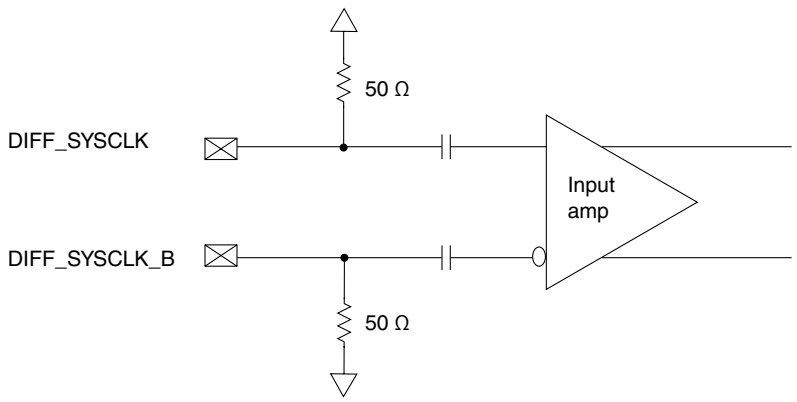


Figure 10. LVDS receiver

This section provides the differential system clock DC and AC timing specifications.

3.7.7.1 Differential system clock DC electrical characteristics

For DC electrical characteristics, see DC-level requirements for SerDes reference clocks.

The differential system clock receiver's core power supply voltage requirements (SV_{DD}) are specified in Table 3.

The Differential system clock can also be single-ended. For this DIFF_SYSCLK_B should be connected to $SV_{DD}/2$.

3.7.7.2 Differential system clock AC timing specifications

The DIFF_SYSCLK/DIFF_SYSCLK_B input pair supports an input clock frequency of 100 MHz.

For AC timing specifications, see AC requirements for SerDes reference clocks.

Spread-spectrum clocking is not supported on differential system clock pair input.

3.7.8 Other input clocks

A description of the overall clocking of this device is available in the chip reference manual in the form of a clock subsystem block diagram. For information about the input clock requirements of functional modules sourced external of the chip, such as SerDes, Ethernet management, eSDHC, and IFC, see the specific interface section.

3.8 RESET initialization timing specifications

This table provides the AC timing specifications for the RESET initialization timing.

Table 21. RESET Initialization timing specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of PORESET_B after V_{DD} is stable	1	—	ms	1
Required input assertion time of HRESET_B	32	—	SYSCLKs	2, 3
Maximum rise/fall time of HRESET_B	—	10	SYSCLK	4
Maximum rise/fall time of PORESET_B	—	1	SYSCLK	4
Input setup time for POR configs (other than cfg_eng_use0) with respect to negation of PORESET_B	4	—	SYSCLKs	2, 5
Input hold time for all POR configs with respect to negation of PORESET_B	2	—	SYSCLKs	2
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of PORESET_B	—	5	SYSCLKs	2

Notes:

1. PORESET_B must be driven asserted before the core and platform power supplies are powered up.
2. SYSCLK is the primary clock input for the chip.
3. The device asserts HRESET_B as an output when PORESET_B is asserted to initiate the power-on reset process. The device releases HRESET_B sometime after PORESET_B is deasserted. The exact sequencing of HRESET_B deassertion is documented in the reference manual's "Power-on Reset Sequence" section.
4. The system/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.
5. For proper clock selection, terminate cfg_eng_use0 with a pull up or pull down of 4.7 kΩ to ensure that the signal will have a valid state as soon as the IO voltage reach its operating condition.

This table provides the phase-locked loop (PLL) lock times.

Table 22. PLL lock times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times (Core, platform, DDR only)	—	100	µs	—

3.9 Battery-backed security monitor interface

This section describes the DC and AC electrical characteristics for the battery-backed security monitor interface, which includes TA_BB_TMP_DETECT_B.

3.9.1 Battery-backed security monitor interface DC electrical characteristics

This table provides the DC electrical characteristics for the battery-backed security monitor interface operating at 1.0 V ($TA_BB_V_{DD}$).

Table 23. Battery-backed security monitor interface DC electrical characteristics ($TA_BB_V_{DD}$ = 1.0 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x $TA_BB_V_{DD}$	—	V	1
Input low voltage	V_{IL}	—	0.3 x $TA_BB_V_{DD}$	V	1
Input current (V_{IN} = 0 V or V_{IN} = $TA_BB_V_{DD}$)	I_{IN}	—	±50	μA	2
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max $TA_BB_V_{DD}$ values found in Table 3.					
2. The symbol V_{IN}, in this case, represents the $TA_BB_V_{DD}$ symbol referenced in Table 3.					
3. For recommended operating conditions, see Table 3.					

This table provides the DC electrical characteristics for the battery-backed security monitor interface operating at 0.9 V ($TA_BB_V_{DD}$).

Table 24. Battery-backed security monitor interface DC electrical characteristics ($TA_BB_V_{DD}$ = 0.9 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x $TA_BB_V_{DD}$	—	V	1
Input low voltage	V_{IL}	—	0.3 x $TA_BB_V_{DD}$	V	1
Input current (V_{IN} = 0 V or V_{IN} = $TA_BB_V_{DD}$)	I_{IN}	—	±50	μA	2
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max $TA_BB_V_{DD}$ values found in Table 3.					
2. The symbol V_{IN}, in this case, represents the $TA_BB_V_{DD}$ symbol referenced in Table 3.					
3. For recommended operating conditions, see Table 3.					

3.9.2 Battery-backed security monitor interface AC timing specifications

This table provides the AC timing specifications for the battery-backed security monitor interface.

Table 25. Battery-backed security monitor interface AC timing specifications[2]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
TA_BB_TMP_DETECT_B	t_{TMP}	100			ns	1

Notes:

1. TA_BB_TMP_DETECT_B is asynchronous to any clock.
2. For recommended operating conditions, see Table 3.

3.10 DDR4 SDRAM controller

This section describes the DC and AC electrical specifications for the DDR4 SDRAM controller interface. Note that the required GV_{DD}(typ) voltage is 1.2 V when interfacing to DDR4 SDRAM.

3.10.1 DDR4 SDRAM interface DC electrical characteristics

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR4 SDRAM.

Table 26. DDR4 SDRAM interface DC electrical characteristics (GV_{DD} = 1.2 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input low	V_{IL}	—	0.7 x GV_{DD} - 0.175	V	3, 6
Input high	V_{IH}	0.7 x GV_{DD} + 0.175	—	V	3, 6
I/O leakage current	I_{OZ}	-165	165	µA	5

Notes:

1. GV_{DD} is expected to be within 60 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. V_{TT} and VREFCA are applied directly to the DRAM device. Both V_{TT} and VREFCA voltages must track GV_{DD}/2.
3. Input capacitance load for DQ, DQS, and DQS_B are available in the IBIS models.
4. See the IBIS model for the complete output IV curve characteristics.
5. Output leakage is measured with all outputs disabled, 0V ≤ V_{OUT} ≤ GV_{DD}.Made internal per Mazyar's updates in DDR4 spec v2.

Table 26. DDR4 SDRAM interface DC electrical characteristics (GV_{DD} = 1.2 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
6. Internal Vref for data bus must be set to 0.7 x GV_{DD}.					
7. For recommended operating conditions, see Table 3.					

3.10.2 DDR4 SDRAM interface AC timing specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports DDR4 memories. Note that the required GV_{DD}(typ) voltage is 1.2 V when interfacing to DDR4 SDRAM.

3.10.2.1 DDR4 SDRAM interface input AC timing specifications

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR4 SDRAM.

Table 27. DDR4 SDRAM interface input AC timing specifications (GV_{DD} = 1.2 V ± 5%)$_1$

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage ≤ 2133 MT/s data rate	V_{ILAC}	—	0.7 x GV_{DD} - 0.175	V	—
AC input high voltage ≤ 2133 MT/s data rate	V_{IHAC}	0.7 x GV_{DD} + 0.175	—	V	—
Note: 1. For recommended operating conditions, see Table 3.					

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR4 SDRAM.

Table 28. DDR4 SDRAM interface input AC timing specifications (GV_{DD} = 1.2 V ± 5% for DDR4)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Controller skew for MDQS-MDQ/MECC	t_{CISKEW}	—	—	ps	1
2100 MT/s data rate		-80	80		
1800 MT/s data rate		-93	93		
1600 MT/s data rate		-112	112		
1333 MT/s data rate		-125	125		
Tolerated Skew for MDQS-MDQ/MECC	t_{DISKEW}	—	—	ps	2
2100 MT/s data rate		-154	154		
1800 MT/s data rate		-175	175		

Table continues on the next page...

Table 28. DDR4 SDRAM interface input AC timing specifications (GV_{DD} = 1.2 V ± 5% for DDR4)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
1600 MT/s data rate		-200	200		
1333 MT/s data rate		-250	250		

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This must be subtracted from the total timing budget.

2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - abs(t_{CISKEW}))$ where T is the clock period and abs(t_{CISKEW}) is the absolute value of t_{CISKEW}.

3. For recommended operating conditions, see Table 3.

This figure shows the DDR4 SDRAM interface input timing diagram.

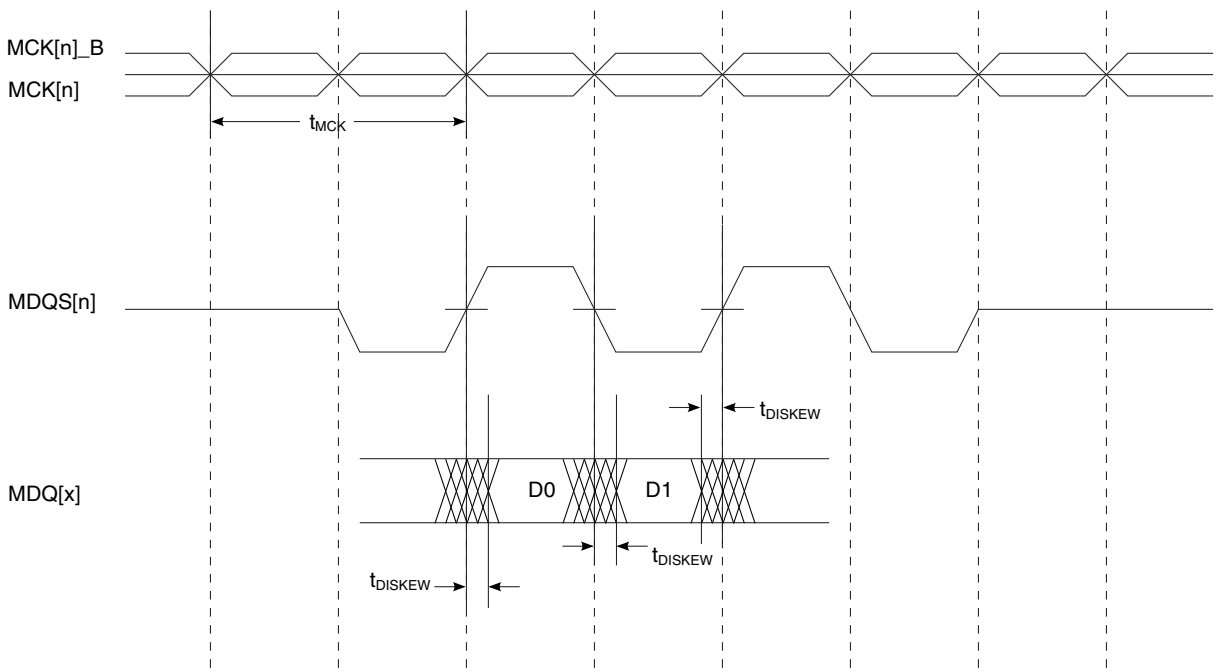


Figure 11. DDR4 SDRAM interface input timing diagram

3.10.2.2 DDR4 SDRAM interface output AC timing specifications

This table contains the output AC timing targets for the DDR4 SDRAM interface.

Table 29. DDR4 SDRAM interface output AC timing specifications (GV_{DD} = 1.2 V)[7]

Parameter	Symbol[1]	Min	Max	Unit	Notes
MCK[n] cycle time	t_{MCK}	938	1500	ps	2

Table continues on the next page...

Table 29. DDR4 SDRAM interface output AC timing specifications (GV_{DD} = 1.2 V)[7] (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
ADDR/CMD/CNTL output setup with respect to MCK	t_{DDKHAS}	—	—	ps	3
2100 MT/s data rate		350	—		
1800 MT/s data rate		410	—		
1600 MT/s data rate		495	—		
1333 MT/s data rate		606	—		
ADDR/CMD/CNTL output hold with respect to MCK	t_{DDKHAX}	—	—	ps	3
2100 MT/s data rate		350	—		
1800 MT/s data rate		390	—		
1600 MT/s data rate		495	—		
1333 MT/s data rate		606	—		
MCK to MDQS Skew	t_{DDKHMH}	-150	150	ps	4,7
MDQ/MECC/MDM output data eye	$t_{DDKXDEYE}$	—	—	ps	5
2100 MT/s data rate		320	—		
1800 MT/s data rate		350	—		
1600 MT/s data rate		400	—		
1333 MT/s data rate		500	—		
MDQS preamble	t_{DDKHMP}	900 x t_{MCK}	—	ps	—
MDQS postamble	t_{DDKHME}	400 x t_{MCK}	600 x t_{MCK}	ps	—

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.

2. All MCK/MCK_B and MDQS/MDQS_B referenced measurements are made from the crossing of the two signals.

3. ADDR/CMD/CNTL includes all DDR SDRAM output signals except MCK/MCK_B, MCS_B, and MDQ/MECC/MDM/MDQS.

4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This is typically set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the chip reference manual for a description and explanation of the timing modifications enabled by the use of these bits.

5. Available eye for data (MDQ), ECC (MECC), and data mask (MDM) outputs at the pin of the processor. Memory controller will center the strobe (MDQS) in the available data eye at the DRAM (end point) during the initialization.

6. Note that this is required to program the start value of the DQS adjust for write leveling.

7. For recommended operating conditions, see Table 3.

NOTE

For the ADDR/CMD/CNTL setup and hold specifications in Table 3, it is assumed that the clock control register is set to

adjust the memory clocks by ½ applied cycle for data rates of 1866 MT/s or less and 9/16 applied cycle for data rates greater than 1866 MT/s. It is recommended that, during system validation, memory clocks are adjusted to best fit the particular system design.

This figure shows the DDR4 SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

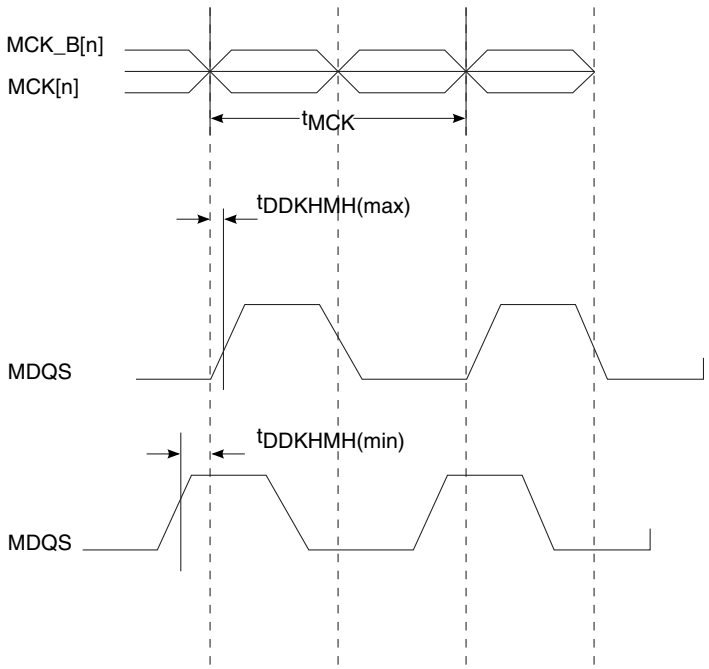


Figure 12. t_{DDKHMH} timing diagram

This figure shows the DDR4 SDRAM output timing diagram.

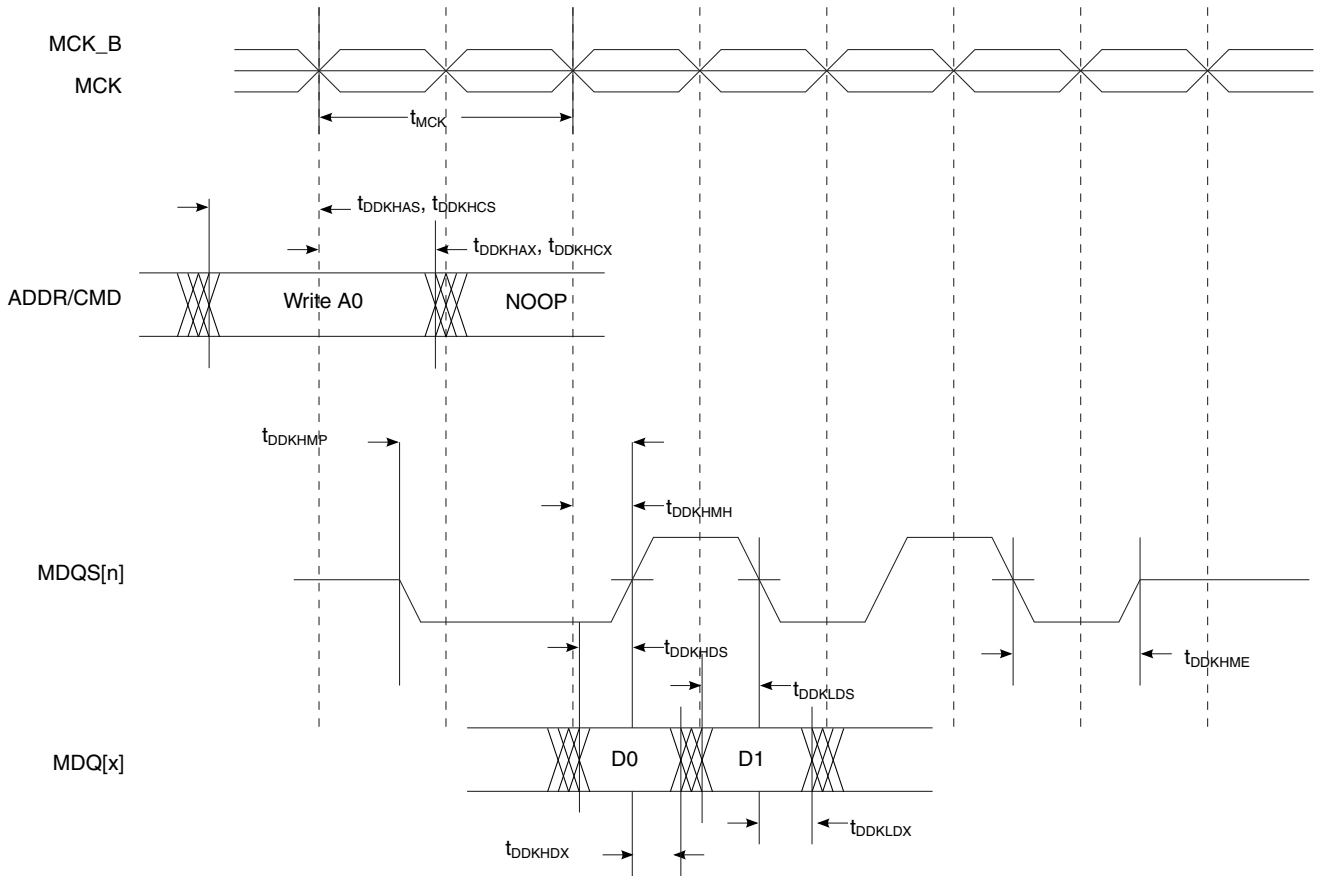


Figure 13. DDR4 output timing diagram

3.11 Dual universal asynchronous receiver/transmitter (DUART) interface

This section describes the DC and AC electrical characteristics for the DUART interface.

3.11.1 DUART DC electrical characteristics

This table provides the DC electrical characteristics for the DUART interface when operating at DV_{DD} = 3.3 V.

Table 30. DUART DC electrical characteristics (DV_{DD} = 3.3 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DVDD	-	V	2
Input low voltage	V_{IL}	-	0.2 x DVDD	V	2

Table continues on the next page...

Table 30. DUART DC electrical characteristics (DV_{DD} = 3.3 V)[1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input current (V_{IN} = 0V or V_{IN} = DV_{DD})	I_{IN}	-50	50	µA	3
Output high voltage (I_{OH} = -2.0 mA)	V_{OH}	2.4	-	V	-
Output low voltage (I_{OL} = 2.0 mA)	V_{OL}	-	0.4	V	-

1. For recommended operating conditions, see Table 3.

2. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in the Recommended Operating Conditions table.

3. Note that the symbol DV_{IN} represents the input voltage of the supply referenced in the Recommended Operating Conditions table.

This table provides the DC electrical characteristics for the DUART interface when operating at DV_{DD} = 1.8 V.

Table 31. DUART DC electrical characteristics (DV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x DV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN} = DV_{DD})	I_{IN}	-50	50	µA	3
Output high voltage (I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

1. For recommended operating conditions, see Table 3.

2. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in the Recommended Operating Conditions table.

3. Note that the symbol DV_{IN} represents the input voltage of the supply referenced in the Recommended Operating Conditions table.

3.11.2 DUART AC timing specifications

This table provides the AC timing specifications for the DUART interface.

Table 32. DUART AC timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
Minimum baud rate	baud	f_{PLAT}/(2 x 1,048,576)	-	baud	1, 2
Maximum baud rate	baud	-	f_{PLAT}/(2 x 16)	baud	1, 3

1. f_{PLAT} refers to the internal platform clock.

2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

3. The actual attainable baud rate is limited by the latency of interrupt processing.

3.12 Enhanced secure digital host controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface.

3.12.1 eSDHC DC electrical characteristics

This table provides the DC electrical characteristics for the eSDHC interface.

Table 33. eSDHC interface DC electrical characteristics (E/DV_{DD}=3.3 V)[3]

Characteristic	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x E/DV_{DD}	-	V	1
Input low voltage	V_{IL}	-	0.25 x E/DV_{DD}	V	1
Output high voltage (I_{OH} = -100 µA at E/DV_{DD} min)	V_{OH}	0.75 x E/DV_{DD}	-	V	-
Output low voltage (I_{OL} = 100 µA at E/DV_{DD} min)	V_{OL}	-	0.125 x E/DV_{DD}	V	-
Output high voltage (I_{OH} = -100 µA)	V_{OH}	E/DV_{DD} - 0.2	-	V	2
Output low voltage (I_{OL} = 2 mA)	V_{OL}	-	0.3	V	2
Input/output leakage current	(I_{IN}/I_{OZ})	-10	10	µA	2

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max EV_{IN} values found in the Table 3.
2. Open-drain mode is for MMC cards only.
3. At recommended operating conditions with E/DV_{DD} = 3.3 V.

Table 34. eSDHC interface DC electrical characteristics ($E/D/OV_{DD}$=1.8 V)[3]

Characteristic	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x $E/D/OV_{DD}$	-	V	1
Input low voltage	V_{IL}	-	0.3 x $E/D/OV_{DD}$	V	1
Output high voltage (I_{OH} = -2 mA at $E/D/OV_{DD}$ min)	V_{OH}	$E/D/OV_{DD}$ - 0.45	-	V	-
Output low voltage (I_{OL} = 2 mA at EV_{DD} min)	V_{OL}	-	0.45	V	-
Output high voltage (I_{OH} = -100 µA)	V_{OH}	$E/D/OV_{DD}$ - 0.2	-	V	2
Output low voltage (I_{OL} = 2 mA)	V_{OL}	-	0.3	V	2

Table continues on the next page...

Table 34. eSDHC interface DC electrical characteristics (E/D/OV_{DD}=1.8 V)[3] (continued)

Characteristic	Symbol	Min	Max	Unit	Notes
Input/output leakage current	(I_{IN}/I_{OZ})	-10	10	μA	2

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max E/D/OV_{IN} values found in the Table 3.
2. Open-drain mode is for MMC cards only.
3. At recommended operating conditions with E/D/OV_{DD} = 1.8 V.

3.12.2 eSDHC AC timing specifications

This section provides the AC timing specifications.

This table provides the eSDHC AC timing specifications as defined in Figure 14, Figure 15, and Figure 16.

Table 35. eSDHC AC timing specifications (full-speed/high-speed mode)[6]

Parameter	Symbol[1]	Min	Max	Unit	Notes
SDHC_CLK clock frequency: • SD/SDIO (full-speed/high-speed mode) • MMC (full-speed/high-speed mode)	f_{SHSCK}	0	25/50 20/52	MHz	2, 4
SDHC_CLK clock low time (full-speed/high-speed mode)	t_{SHSCKL}	10/7	-	ns	4
SDHC_CLK clock high time (full-speed/high-speed mode)	t_{SHSCKH}	10/7	-	ns	4
SDHC_CLK clock rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	-	3	ns	4
Input setup times: SDHC_CMD, SDHC_DATx, SDHC_CD to SDHC_CLK	$t_{SHSIVKH}$	2.5	-	ns	3, 4, 5
Input hold times: SDHC_CMD, SDHC_DATx, SDHC_CD to SDHC_CLK	$t_{SHSIXKH}$	2.5	-	ns	4, 5
Output hold time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid	$t_{SHSKHOX}$	-3	-	ns	4, 5
Output delay time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid	$t_{SHSKHOV}$	-	3	ns	4, 5

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SHKHOX} symbolizes eSDHC high-speed mode device timing (SH) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In full-speed mode, the clock frequency value can be 0-25MHz for an SD/SDIO card and 0-20MHz for an MMC card. In high-speed mode, the clock frequency value can be 0-50MHz for an SD/SDIO card and 0-52MHz for an MMC card.

Table 35. eSDHC AC timing specifications (full-speed/high-speed mode)[6]

Parameter	Symbol[1]	Min	Max	Unit	Notes
3. SDHC_SYNC_OUT/IN loop back is recommended to compensate the clock delay. In case the SDHC_SYNC_OUT/IN loopback is not used, to satisfy setup timing, one-way board-routing delay between host and card, on SDHC_CLK, SDHC_CMD, and SDHC_DATx should not exceed 1ns for any high-speed MMC card. For any high-speed or default speed mode SD card, the one-way board-routing delay between host and card, on SDHC_CLK, SDHC_CMD, and SDHC_DATx should not exceed 1.5ns.					
4. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF.					
5. The parameter values apply to both full-speed and high-speed modes.					
6. For recommended operating conditions, see Table 3.					

This figure provides the eSDHC clock input timing diagram.

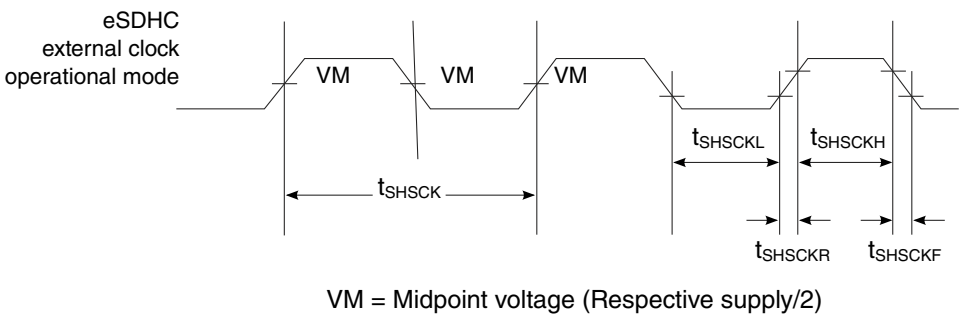


Figure 14. eSDHC clock input timing diagram

This figure provides the input AC timing diagram for high-speed mode.

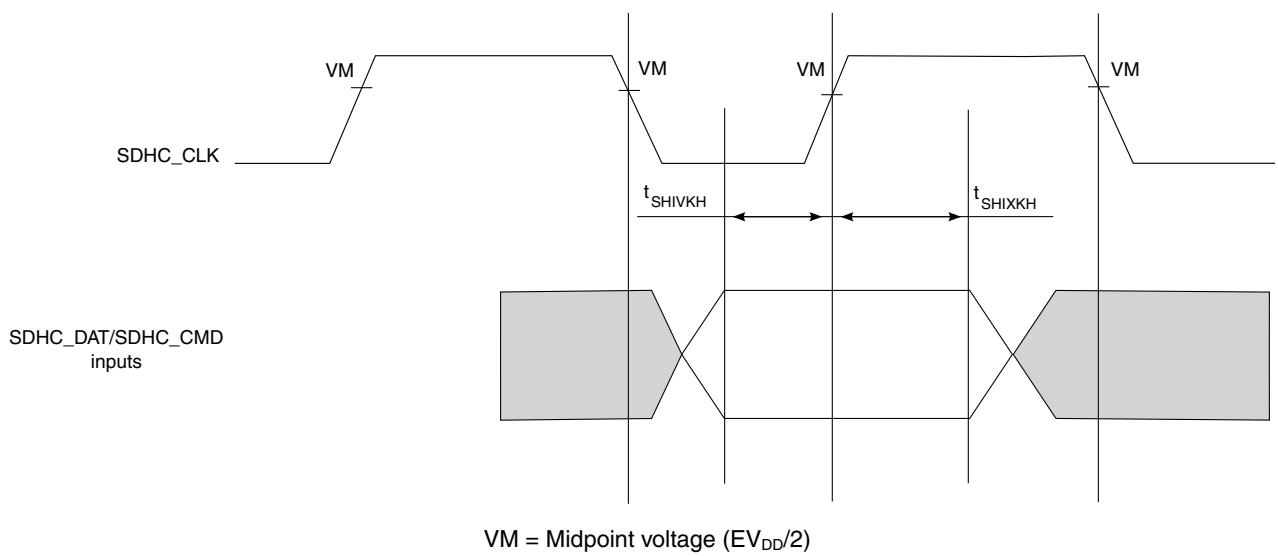


Figure 15. eSDHC high-speed mode input AC timing diagram

This figure provides the output AC timing diagram for high-speed mode.

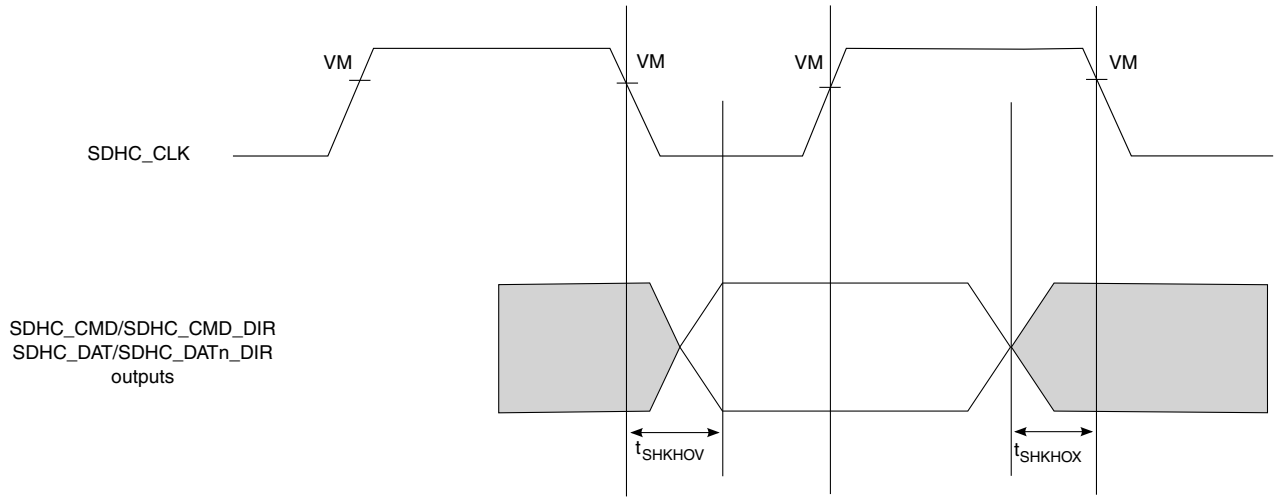


Figure 16. eSDHC high-speed mode output AC timing diagram

This table provides the eSDHC AC timing specifications for SDR50 mode.

Table 36. eSDHC AC timing specifications (SDR50)[2]

Parameter	Symbol	Min	Max	Unit	Notes
SDHC_CLK clock frequency	f_{SHSCK}	0	100	MHz	-
SDHC_CLK clock rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	-	2	ns	1
Skew between SDHC_CLK_SYNC_OUT and SDHC_CLK	t_{SHSCSK}	-0.1	0.1	ns	1
Input setup times: SDHC_CMD, SDHC_DATx to SDHC_CLK_SYNC_IN	$t_{SHSIVKH}$	2.1	-	ns	1
Input hold times: SDHC_CMD, SDHC_DATx to SDHC_CLK_SYNC_IN	$t_{SHSIXKH}$	1.1	-	ns	1
Output hold time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid, SDHC_DATx_DIR, SDHC_CMD_DIR	$t_{SHSKHOX}$	1.7	-	ns	1
Output delay time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid, SDHC_DATx_DIR, SDHC_CMD_DIR	$t_{SHSKHOV}$	-	6.1	ns	1

Notes:

1. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 30$ pF.
2. For recommended operating conditions, see Table 3.

This figure provides the eSDHC clock input timing diagram for SDR50 mode.

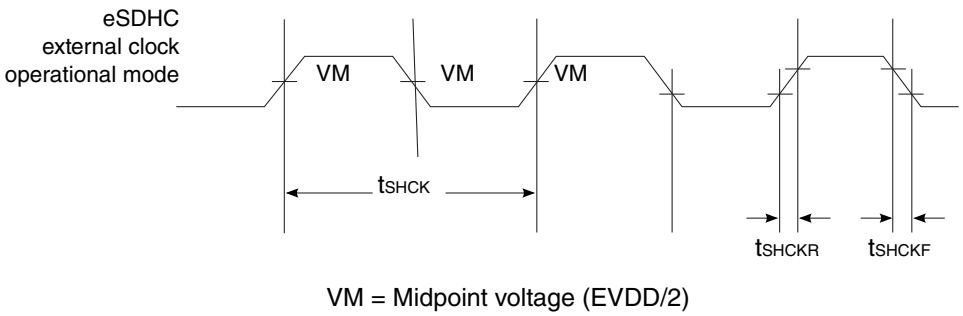


Figure 17. eSDHC SDR50 mode clock input timing diagram

This figure provides the eSDHC input AC timing diagram for SDR50 mode.

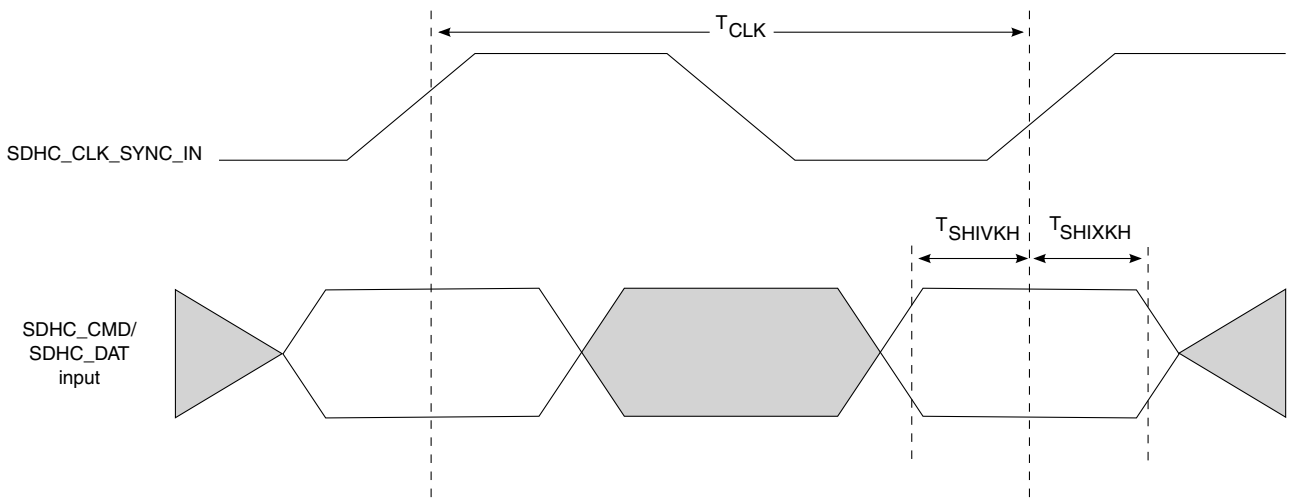


Figure 18. eSDHC SDR50 mode input AC timing diagram

This figure provides the eSDHC output timing diagram for SDR50 mode.

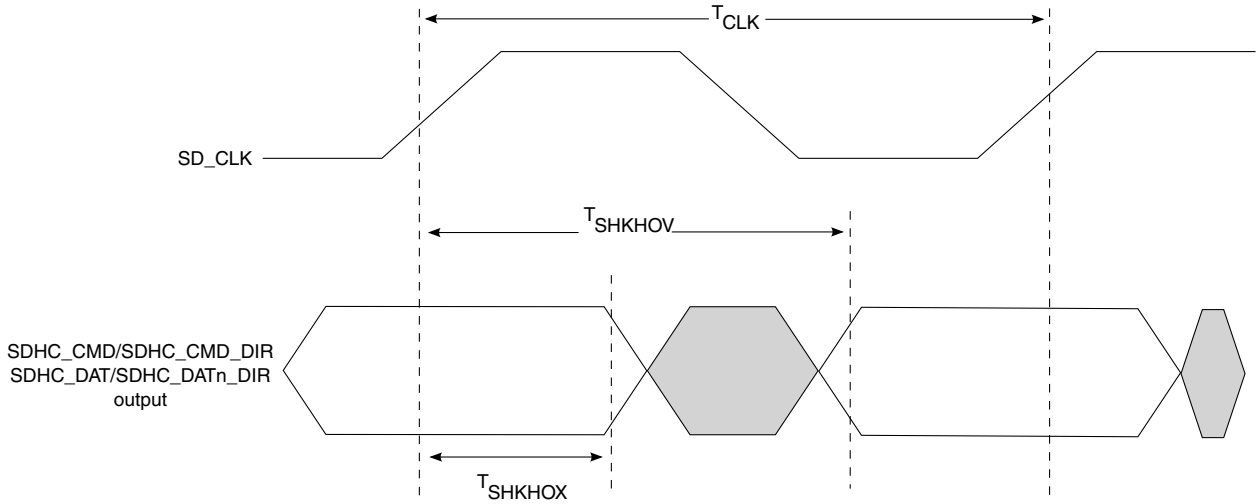


Figure 19. eSDHC SDR50 mode output timing diagram

This table provides the eSDHC AC timing specifications for DDR50/DDR mode.

Table 37. eSDHC AC timing specifications (DDR50/DDR)[3]

Parameter		Symbol	Min	Max	Units	Notes
SDHC_CLK clock frequency	SD/SDIO DDR50 mode	f_{SHCK}	—	50	MHz	—
	eMMC DDR mode			52		
Skew between SDHC_CLK_SYNC_OUT and SDHC_CLK		t_{SHSCSK}	-0.1	0.1	ns	—
SDHC_CLK clock rise and fall times	SD/SDIO DDR50 mode	t_{SHCKR}/	—	4	ns	1, 2
	eMMC DDR mode	t_{SHCKF}		2		1, 2
Input setup times: SDHC_DATx to SDHC_CLK_SYNC_IN	SD/SDIO DDR50 mode	$t_{SHDIVKH}$	2.0	—	ns	1
	eMMC DDR mode		1.6			2
Input hold times: SDHC_DATx to SDHC_CLK_SYNC_IN	SD/SDIO DDR50 mode	$t_{SHDIXKH}$	1.3	—	ns	1
	eMMC DDR mode		1.3			2, 4
Output hold time: SDHC_CLK to SDHC_DATx valid, SDHC_DATx_DIR	SD/SDIO DDR50 mode	$t_{SHDKHOX}$	1.7	—	ns	1
	eMMC DDR mode		3.4			2
Output delay time: SDHC_CLK to SDHC_DATx valid, SDHC_DATx_DIR	SD/SDIO DDR50 mode	$t_{SHDKHOV}$	—	6.1	ns	1
	eMMC DDR mode			6.2		2
Input setup times: SDHC_CMD to SDHC_CLK_SYNC_IN	SD/SDIO DDR50 mode	$t_{SHCIVKH}$	5.3	—	ns	1
	eMMC DDR mode		5			2
Input hold times: SDHC_CMD to SDHC_CLK_SYNC_IN	SD/SDIO DDR50 mode	$t_{SHCIXKH}$	1.2	—	ns	1
	eMMC DDR mode		1.2			2, 5
Output hold time: SDHC_CLK to SDHC_CMD valid, SDHC_CMD_DIR	SD/SDIO DDR50 mode	$t_{SHCKHOX}$	1.7	—	ns	1
	eMMC DDR mode		3.9			2
Output delay time: SDHC_CLK to SDHC_CMD valid, SDHC_CMD_DIR	SD/SDIO DDR50 mode	$t_{SHCKHOV}$	—	15.3	ns	1
	eMMC DDR mode			15.3		2

Table continues on the next page...

Table 37. eSDHC AC timing specifications (DDR50/DDR)[3] (continued)

Parameter	Symbol	Min	Max	Units	Notes
Notes:					
1. C_{CARD} ≤ 10 pF, (1 card).					
2. $C_L = C_{BUS} + C_{HOST} + C_{CARD}$ ≤ 20 pF for MMC, ≤ 25pF for Input Data of DDR50, ≤ 30pF for Input CMD of DDR50.					
3. For recommended operating conditions, see Table 3.					
4. Total clock duty cycle and data and clock skew on the board should be limited to 0.2ns.					
5. Total clock duty cycle and command and clock skew on the board should be limited to 0.3ns.					

This figure provides the eSDHC DDR50/DDR mode input AC timing diagram.

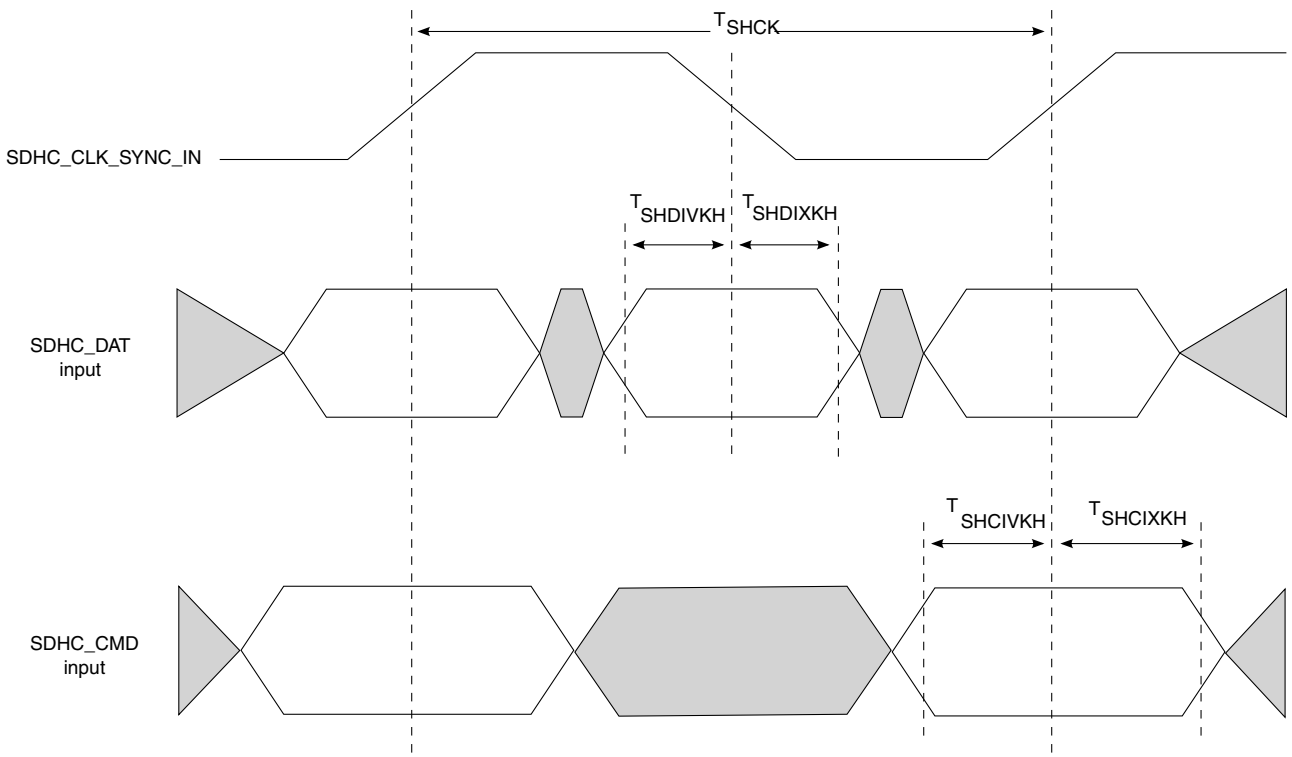


Figure 20. eSDHC DDR50/DDR mode input AC timing diagram

This figure provides the eSDHC DDR50/DDR mode output AC timing diagram.

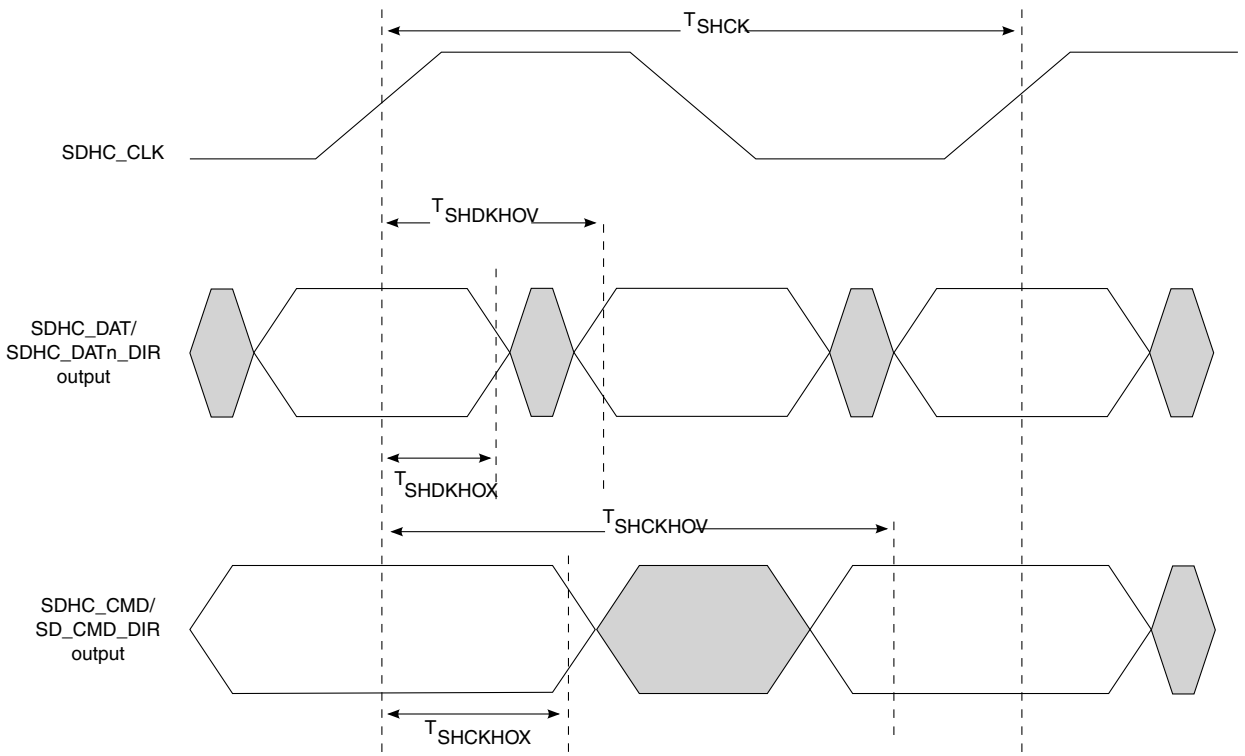


Figure 21. eSDHC DDR50/DDR mode output AC timing diagram

This table provides the eSDHC AC timing specifications for SDR104/eMMC HS200 mode.

Table 38. eSDHC AC timing specifications (SDR104/eMMC HS200)

Parameter		Symbol[1]	Min	Max	Unit	Notes
SDHC_CLK clock frequency	SD/SDIO SDR104 mode	f_{SHCK}	-	167	MHz	-
	eMMC HS200 mode			167		-
SDHC_CLK clock rise and fall times		t_{SHCKR}/t_{SHCKF}	-	1	ns	1
Output hold time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid, SDHC_CMD_DIR, SDHC_DATx_DIR	SD/SDIO SDR104 mode	T_{SHKHOX}	1.58	-	ns	1
	eMMC HS200 mode		1.6			
Output delay time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid, SDHC_CMD_DIR, SDHC_DATx_DIR	SD/SDIO SDR104 mode	T_{SHKHOV}	-	3.94	ns	1
	eMMC HS200 mode			3.92		
Input data window (UI)	SD/SDIO SDR104 mode	t_{SHIDV}	0.5	-	Unit Interval	1
	eMMC HS200 mode		0.475			

Notes:

1. $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 15pF$.
2. For recommended operating conditions, see Table 3.

This figure provides the eSDHC SDR104/HS200 mode timing diagram.

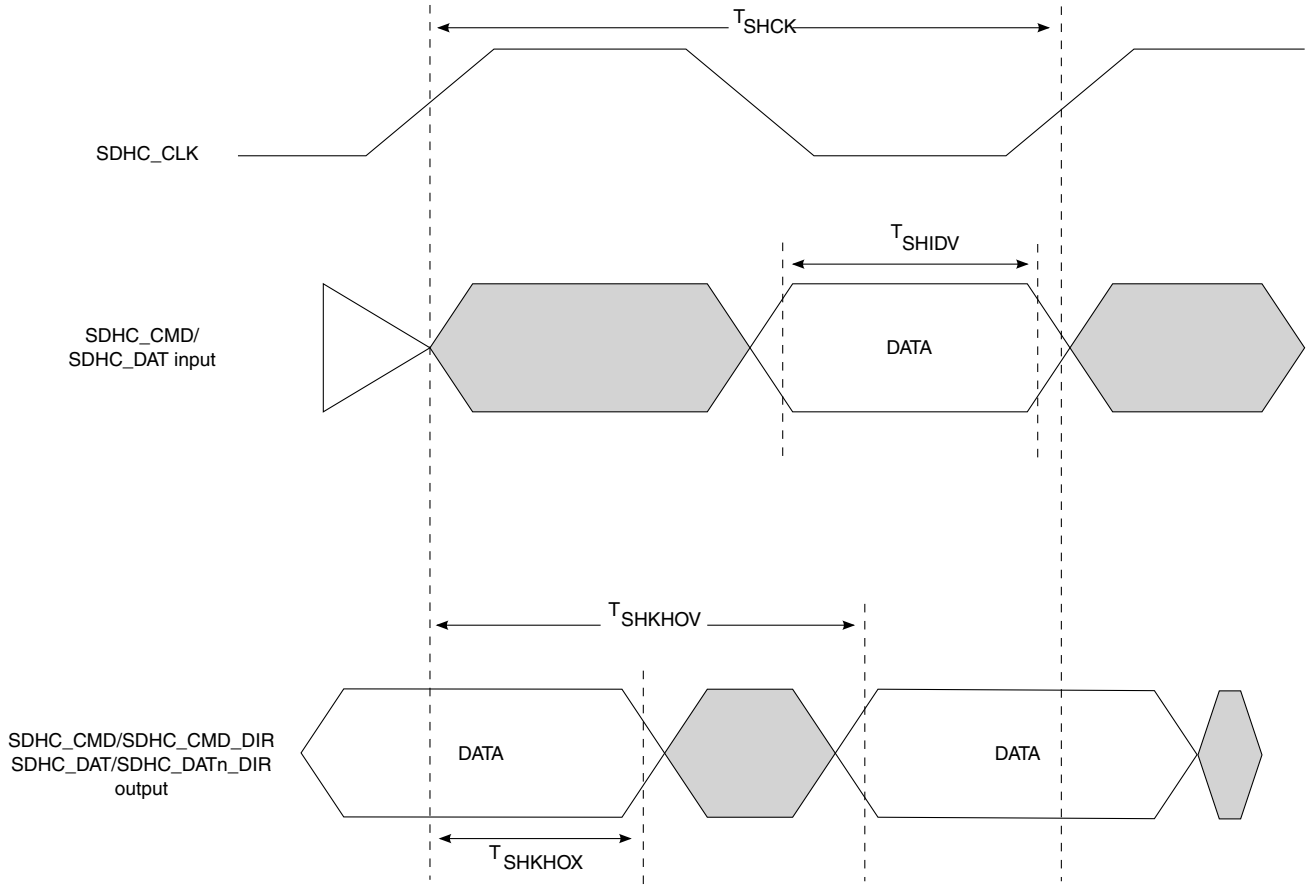


Figure 22. eSDHC SDR104/HS200 mode timing diagram

3.13 Ethernet interface (EMI, RGMII, and IEEE Std 1588™)

This section describes the DC and AC electrical characteristics for the Ethernet controller, Ethernet management, RGMII, and IEEE Std 1588 interfaces.

3.13.1 Ethernet management interface (EMI)

This section describes the electrical characteristics for the Ethernet management interface (EMI).

The EMI1 and EMI2 interface timings are compatible with IEEE Std 802.3™ clauses 22 and 45, respectively.

3.13.1.1 Ethernet management interface 1 (EMI1)

This section describes the electrical characteristics for the EMI1 interface.

The EMI1 interface timing is compatible with IEEE Std 802.3™ clause 22.

3.13.1.1.1 EMI1 DC electrical characteristics

This section describes the DC electrical characteristics for EMI1_MDIO and EMI1_MDC. The pins are available on LV_{DD}. For operating voltages, see the Recommended operating conditions table.

This table provides the EMI1 DC electrical characteristics when operating at LV_{DD} = 2.5 V.

Table 39. EMI1 DC electrical characteristics (LV_{DD} = 2.5 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LVDD	-	V	2
Input low voltage	V_{IL}	-	0.2 x LVDD	V	2
Input current (V_{IN} = 0 or V_{IN} = LV_{DD})	I_{IN}	-50.0	50.0	μA	3, 4
Output high voltage (LV_{DD} = min, I_{OH} = -1.0 mA)	V_{OH}	2.0	-	V	4
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	-	0.4	V	4

1. For recommended operating conditions, see Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
3. The symbol LV_{IN} represents the input voltage of the supply referenced in Table 3.
4. The symbol LV_{DD} represents the input voltage of the supply referenced in Table 3.

This table provides the EMI1 DC electrical characteristics when operating at LV_{DD} = 1.8 V.

Table 40. EMI1 DC electrical characteristics (LV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LVDD	-	-	2
Input low voltage	V_{IL}	-	0.3 x LVDD	-	2
Input current (V_{IN} = 0 or V_{IN} = LV_{DD})	I_{IN}	-50.0	50.0	-	3, 4
Output high voltage (LV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	-	4
Output low voltage (LV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	-	4

1. For recommended operating conditions, see Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.

Table 40. EMI1 DC electrical characteristics (LV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
3. The symbol LV_{IN} represents the input voltage of the supply referenced in Table 3.					
4. The symbol LV_{DD} represents the input voltage of the supply referenced in Table 3.					

3.13.1.1.2 EMI1 AC timing specifications

This table provides the AC timing specifications for the EMI1 interface.

Table 41. EMI1 AC timing specifications[4]

Parameter	Symbol	Min	Max	Unit	Notes
MDC frequency	f_{MDC}	-	2.5	MHz	1
MDC clock pulse width high	t_{MDCH}	160.0	-	ns	-
MDC to MDIO delay	t_{MDKHDX}	(5 x t_{enet_clk}) - 3	(5 x t_{enet_clk}) + 3	ns	2, 3
MDIO to MDC setup time	t_{MDDVKH}	8.0	-	ns	-
MDIO to MDC hold time	t_{MDDXKH}	2	-	ns	-
1. This parameter is dependent on the Ethernet clock frequency. The MDIO_CFG [MDIO_CLK_DIV] field determines the clock frequency of the MgmtClk Clock EC_MDC.					
2. This parameter is dependent on the Ethernet clock frequency. The delay is equal to 5 Ethernet clock periods ± 3 ns. For example, with an Ethernet clock of 400 MHz, the min/max delay is 12.5 ns ± 3 ns.					
3. t_{enet_clk} is the Ethernet clock period (Frame Manager clock period x 2).					
4. The symbols used for timing specifications follow these patterns: $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time.					

This figure shows the Ethernet management interface 1 timing diagram.

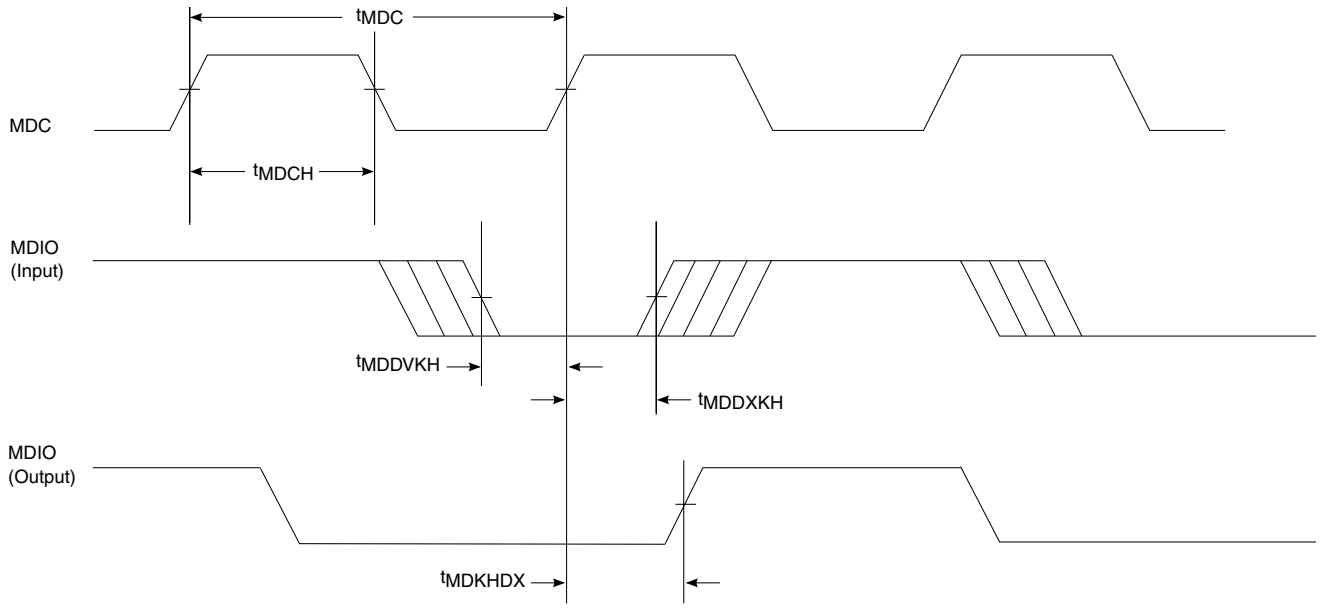


Figure 23. Ethernet management interface 1 timing diagram

3.13.1.2 Ethernet management interface 2 (EMI2)

This section describes the electrical characteristics for the EMI2 interface.

The EMI2 interface timing is compatible with IEEE Std 802.3™ clause 45.

3.13.1.2.1 EMI2 DC electrical characteristics

This section describes the DC electrical characteristics for EMI2_MDIO and EMI2_MDC. The pins are available on TV_{DD}. For operating voltages, see Table 3.

This table provides the EMI2 DC electrical characteristics when operating at TV_{DD} = 2.5 V.

Table 42. EMI2 DC electrical characteristics (TV_{DD} = 2.5 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x TVDD	-	-	2
Input low voltage	V_{IL}	-	0.2 x TVDD	-	2
Input current (V_{IN} = 0 or V_{IN} = TV_{DD})	I_{IN}	-50.0	50.0	-	3, 4
Output high voltage (TV_{DD} = min, I_{OH} = -1.0 mA)	V_{OH}	2.0	-	-	4
Output low voltage (TV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	-	0.4	-	4

1. For recommended operating conditions, see Table 3.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max TV_{IN} values found in Table 3.

Table 42. EMI2 DC electrical characteristics (TV_{DD} = 2.5 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
3. The symbol TV_{IN} represents the input voltage of the supply referenced in Table 3.					
4. The symbol TV_{DD} represents the input voltage of the supply referenced in Table 3.					

This table provides the EMI2 DC electrical characteristics when operating at TV_{DD} = 1.8 V.

Table 43. EMI2 DC electrical characteristics (TV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x TVDD	-	-	2
Input low voltage	V_{IL}	-	0.3 x TVDD	-	2
Input current (V_{IN} = 0 or V_{IN} = TV_{DD})	I_{IN}	-50.0	50.0	-	3, 4
Output high voltage (TV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	-	4
Output low voltage (TV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	-	4
1. For recommended operating conditions, see Table 3.					
2. The min V_{IL} and max V_{IH} values are based on the respective min and max TV_{IN} values found in Table 3.					
3. The symbol TV_{IN} represents the input voltage of the supply referenced in Table 3.					
4. The symbol TV_{DD} represents the input voltage of the supply referenced in Table 3.					

This table provides the EMI2 DC electrical characteristics when operating at TV_{DD} = 1.2 V.

Table 44. EMI2 DC electrical characteristics (TV_{DD} = 1.2 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x TVDD	-	-	2
Input low voltage	V_{IL}	-	0.2 x TVDD	-	2
Output low current (V_{OL} = 0.2 V)	I_{OL}	4.0	-	mA	-
Output high voltage (TV_{DD} = min, I_{OH} = -100 µA)	V_{OH}	1.0	-	V	3
Output low voltage (TV_{DD} = min, I_{OL} = 100 µA)	V_{OL}	-	0.2	V	3
Input capacitance	C_{IN}	-	10.0	pF	-
1. For recommended operating conditions, see Table 3.					
2. The min V_{IL} and max V_{IH} values are based on the respective min and max TV_{IN} values found in Table 3.					
3. The symbol TV_{DD} represents the input voltage of the supply referenced in Table 3.					

3.13.1.2.2 EMI2 AC timing specifications

This table provides the AC timing specifications for the EMI2 interface.

Table 45. EMI2 AC timing specifications[4]

Parameter	Symbol	Min	Max	Unit	Notes
MDC frequency	f_{MDC}	-	2.5	MHz	1
MDC clock pulse width high	t_{MDCH}	160.0	-	ns	-
MDC to MDIO delay	t_{MDKHDX}	(5 x t_{enet_clk}) - 3	(5 x t_{enet_clk}) + 3	ns	2, 3
MDIO to MDC setup time	t_{MDDVKH}	8.0	-	ns	-
MDIO to MDC hold time	t_{MDDXKH}	2	-	ns	5

1. This parameter is dependent on the Ethernet clock frequency. The MDIO_CFG [MDIO_CLK_DIV] field determines the clock frequency of the MgmtClk Clock EC_MDC.

2. This parameter is dependent on the Ethernet clock frequency. The delay is equal to 5 Ethernet clock periods ± 3 ns. For example, with an Ethernet clock of 400 MHz, the min/max delay is 12.5 ns ± 3 ns.

3. t_{enet_clk} is the Ethernet clock period (Frame Manager clock period x 2).

4. The symbols used for timing specifications follow these patterns: $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time.

5. See "AN5144, LS1088A Design Checklist" for more details.

This figure shows the Ethernet management interface 2 timing diagram.

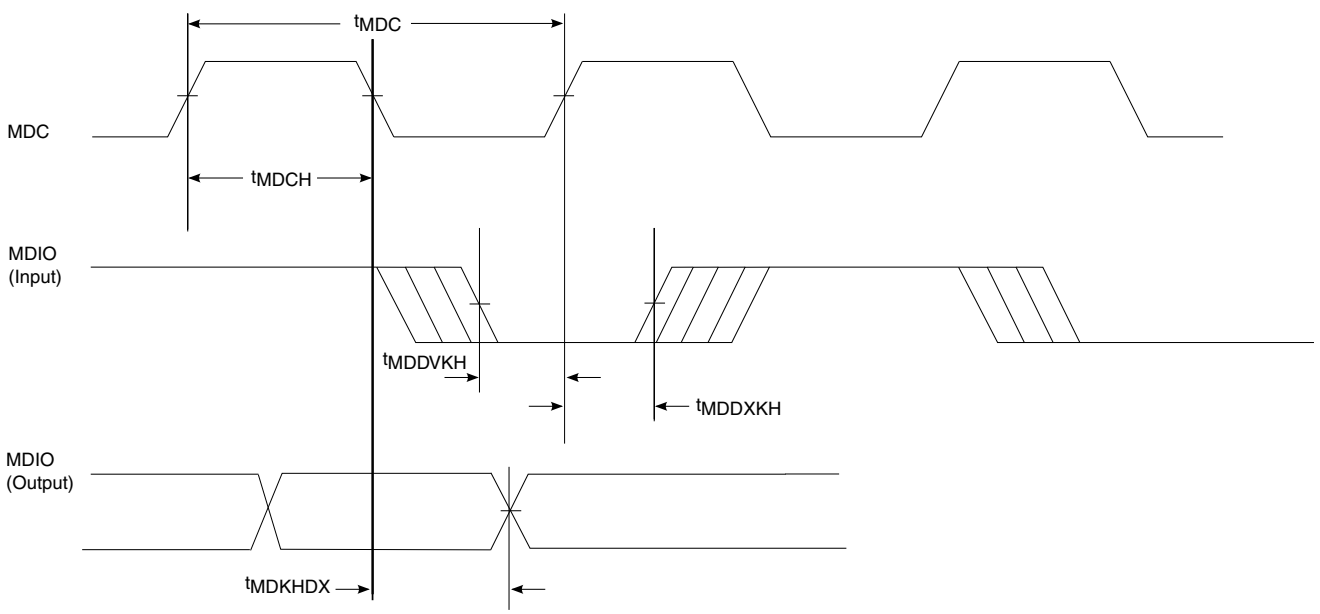


Figure 24. Ethernet management interface 2 timing diagram

3.13.2 IEEE 1588 interface

This section describes the DC and AC electrical characteristics for the IEEE 1588 interface.

3.13.2.1 IEEE 1588 DC electrical characteristics

This table provides the IEEE 1588 DC electrical characteristics when operating at LV_{DD} = 2.5 V supply.

Table 46. IEEE 1588 DC electrical characteristics (LV_{DD} = 2.5 V)[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LVDD	-	-	V	2
Input low voltage	V_{IL}	-	-	0.2 x LVDD	V	2
Input current (V_{IN} = 0 or V_{IN} = LV_{DD})	I_{IN}	-50.0	-	50.0	μA	3
Output high voltage (LV_{DD} = min, I_{OH} = -1.0 mA)	V_{OH}	2.0	-	-	V	-
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	-	-	0.4	V	-

1. For recommended operating conditions, see Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
3. The symbol LV_{IN} represents the input voltage of the supply referenced in Table 3.

This table provides the IEEE 1588 DC electrical characteristics when operating at LV_{DD} = 1.8 V supply.

Table 47. IEEE 1588 DC electrical characteristics (LV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LVDD	-	-	V	2
Input low voltage	V_{IL}	-	-	0.3 x LVDD	V	2
Input current (V_{IN} = 0 or V_{IN} = LV_{DD})	I_{IN}	-50.0	-	50.0	μA	3
Output high voltage (LV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	-	V	-
Output low voltage (LV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	-	0.4	V	-

1. For recommended operating conditions, see Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
3. The symbol LV_{IN} represents the input voltage of the supply referenced in Table 3.

3.13.2.2 IEEE 1588 AC timing specifications

This table provides the AC timing specifications for the IEEE 1588 interface.

Table 48. IEEE 1588 AC timing specifications

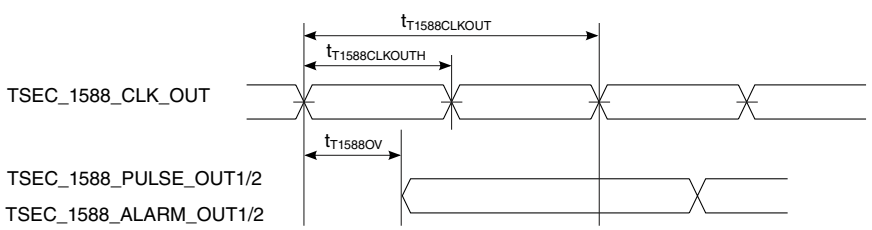
Parameter	Symbol	Min	Typ	Max	Unit	Notes
TSEC_1588_CLK_IN clock period	$t_{1588CLK}$	6.0	-	-	ns	-
TSEC_1588_CLK_IN duty cycle	$t_{T1588CLKH}$/ $t_{T1588CLK}$	40.0	50.0	60.0	%	1
TSEC_1588_CLK_IN peak-to-peak jitter	$t_{T1588CLKINJ}$	-	-	250.0	ps	-
Rise time TSEC_1588_CLK_IN (20% to 80%)	$t_{T1588CLKINR}$	1.0	-	2.0	ns	-
Fall time TSEC_1588_CLK_IN (80% to 20%)	$t_{T1588CLKINF}$	1.0	-	2.0	ns	-
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	2 x $t_{T1588CLK}$	-	-	ns	2
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}$/ $t_{T1588CLKOUT}$	30.0	50.0	70.0	%	-
TSEC_1588_PULSE_OUT1/2, TSEC_1588_ALARM_OUT1/2	$t_{T1588OV}$	0.5	-	4.0	ns	-
TSEC_1588_TRIG_IN1/2 pulse width	$t_{T1588TRIGH}$	2 x $t_{T1588CLK}$	-	-	ns	1, 3

1. This needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the chip reference manual for a description of TMR_CTRL registers.

2. There are three input clock sources for 1588: TSEC_1588_CLK_IN, RTC, and MAC clock / platform clock. When using TSEC_1588_CLK_IN, the minimum clock period is 2 x $t_{T1588CLK}$.

3. The maximum value of $t_{T1588CLK}$ is not only defined by the value of TRX_CLK, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ will be 2800, 280, and 56 ns, respectively.

This figure shows the data and command output AC timing diagram.



Note: The output delay is counted starting at the rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is counted starting at the falling edge.

Figure 25. IEEE 1588 output AC timing

This figure shows the data and command input AC timing diagram.

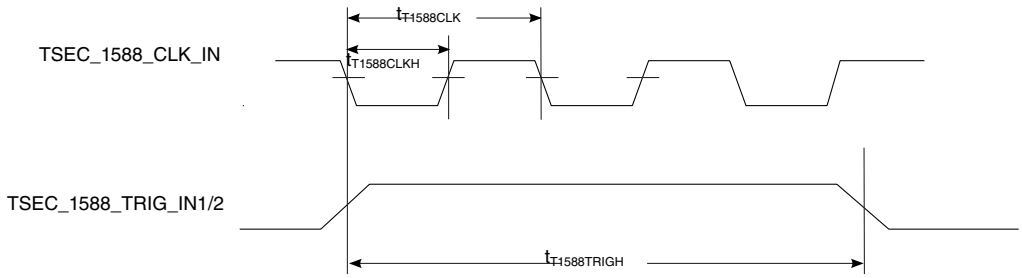


Figure 26. IEEE 1588 input AC timing

3.13.3 RGMII interface

This section describes the DC and AC electrical characteristics for the RGMII interface.

3.13.3.1 RGMII DC electrical characteristics

This table provides the DC electrical characteristics for the RGMII interfaces operating at $LV_{DD}/L1V_{DD}$ = 2.5 V.

Table 49. RGMII DC electrical characteristics (LV_{DD} = 2.5 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LVDD	-	V	2
Input low voltage	V_{IL}	-	0.2 x LVDD	V	2
Input current (V_{IN}=0V or V_{IN}=LV_{DD})	I_{IN}	-50.0	50.0	µA	3, 4
Output high voltage (LV_{DD} = min, I_{OH} = -1.0 mA)	V_{OH}	2.0	-	V	3
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	-	0.4	V	3
1. For recommended operating conditions, see Table 3.					
2. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.					
3. The symbol LV_{DD} represents the input voltage of the supply referenced in Table 3.					
4. The symbol LV_{IN} represents the input voltage of the supply referenced in Table 3.					

This table provides the DC electrical characteristics for the RGMII interface operating at LV_{DD} = 1.8 V.

Table 50. RGMII DC electrical characteristics (LV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LVDD	-	V	2
Input low voltage	V_{IL}	-	0.3 x LVDD	V	2

Table continues on the next page...

Table 50. RGMII DC electrical characteristics (LV_{DD} = 1.8 V)[1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input current (V_{IN}=0V or V_{IN}=LV_{DD})	I_{IN}	-50.0	50.0	µA	3, 4
Output high voltage (LV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	3
Output low voltage (LV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	3

1. For recommended operating conditions, see Table 3.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.

3. The symbol LV_{DD} represents the input voltage of the supply referenced in Table 3.

4. The symbol LV_{IN} represents the input voltage of the supply referenced in Table 3.

3.13.3.2 RGMII AC timing specifications

This table provides the AC timing specifications for the RGMII interface.

Table 51. RGMII AC timing specifications[7]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	-400	0.0	600	ps	1
Data to clock input skew (at receiver)	t_{SKRGT_RX}	1.0	-	2.6	ns	2
Clock period duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40.0	50.0	60.0	%	3, 4
Duty cycle for Gigabit	t_{RGTH}/t_{RGT}	45.0	50.0	55.0	%	-
Rise time (20%-80%) L1/ LV_{DD}=2.5V	t_{RGTR}	-	-	0.75	ns	5, 6
Rise time (20%-80%) L1/ LV_{DD}=1.8V	t_{RGTR}	-	-	0.54	ns	5, 6
Fall time (20%-80%) L1/LV_{DD}=2.5V	t_{RGTF}	-	-	0.75	ns	5, 6
Fall time (20%-80%) L1/LV_{DD}=1.8V	t_{RGTF}	-	-	0.54	ns	5, 6

1. The frequency of ECn_RX_CLK (input) should not exceed the frequency of ECn_GTX_CLK (output) by more than 300 ppm.

2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their device. If so, additional PCB delay is probably not needed.

3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.

4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three tRGT of the lowest speed transitioned between.

5. Applies to inputs and outputs.

6. The system/board must be designed to ensure this input requirement to the chip is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

Table 51. RGMII AC timing specifications[7]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
7. In general, the clock reference symbol representation is based on the symbol RGT, which represents RGMII timing. Note that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).						

This figure shows the RGMII AC timing and multiplexing diagrams.

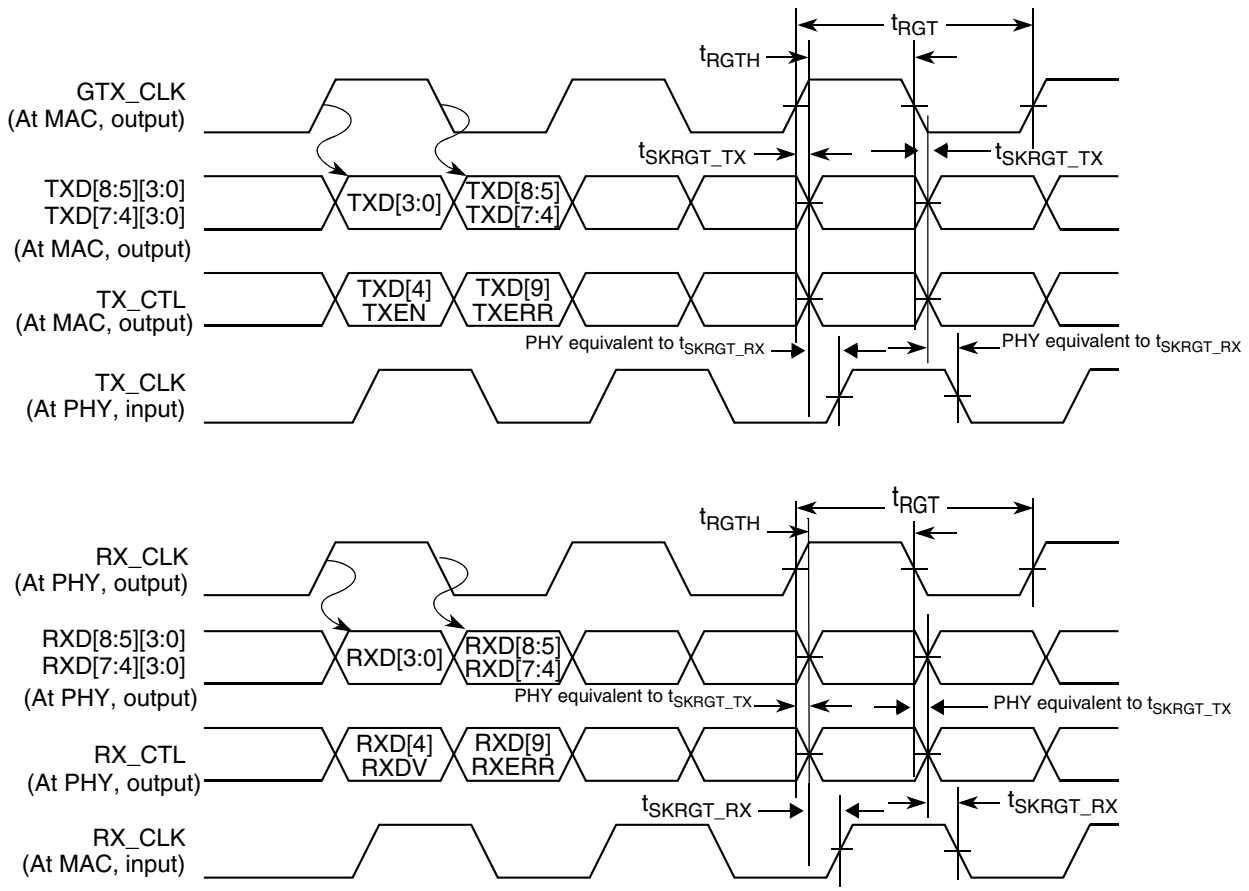


Figure 27. RGMII AC timing and multiplexing diagrams

NOTE

NXP guarantees timings generated from the MAC. Board designers must ensure delays needed at the PHY or the MAC.

3.14 General purpose input/output (GPIO) interface

This section describes the DC and AC electrical characteristics for the GPIO interface.

3.14.1 GPIO DC electrical characteristics

This table provides the DC electrical characteristics for the GPIO interface operating at D/EV_{DD} = 3.3 V.

Table 52. GPIO DC electrical characteristics (D/EV_{DD} = 3.3 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x D/EV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.2 x D/EV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN}= LV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (D/EV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.4	-	V	-
Output low voltage (D/EV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	-	0.4	V	-
1. For recommended operating conditions, see Table 3. 2. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN}/EV_{IN} values found in Table 3. 3. The symbol DV_{IN}/EV_{IN} represents the input voltage of the supply referenced in Table 3.					

This table provides the DC electrical characteristics for the GPIO interface operating at TV_{DD} = 2.5 V.

Table 53. GPIO DC electrical characteristics (TV_{DD} = 2.5 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x TV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.2 x TV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN}= LV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (TV_{DD} = min, I_{OH} = -1 mA)	V_{OH}	2.0	-	V	-
Output low voltage (TV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	-	0.4	V	-
1. For recommended operating conditions, see Table 3. 2. The min V_{IL} and max V_{IH} values are based on the respective min and max TV_{IN} values found in Table 3. 3. The symbol TV_{IN} represents the input voltage of the supply referenced in Table 3.					

This table provides the DC electrical characteristics for the GPIO interface operating at $D/E/TV_{DD}$ = 1.8 V.

Table 54. GPIO DC electrical characteristics ($D/E/TV_{DD}$ = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x $D/E/TV_{DD}$	-	V	2

Table continues on the next page...

Table 54. GPIO DC electrical characteristics (D/E/TV_{DD} = 1.8 V)[1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input low voltage	V_{IL}	-	0.3 x D/E/TV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN}= LV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (D/E/TV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (D/E/TV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-
1. For recommended operating conditions, see Table 3.					
2. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN}/EV_{IN}/TV_{IN} values found in Table 3.					
3. The symbol DV_{IN}/EV_{IN}/TV_{IN} represents the input voltage of the supply referenced in Table 3.					

This table provides the DC electrical characteristics for the GPIO interface operating at LV_{DD} = 2.5 V.

Table 55. GPIO DC electrical characteristics (LV_{DD} = 2.5 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LVDD	-	V	2
Input low voltage	V_{IL}	-	0.2 x LVDD	V	2
Input current (V_{IN} = 0V or V_{IN}= LV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (LV_{DD} = min, I_{OH} = -1 mA)	V_{OH}	2.0	-	V	-
Output low voltage (LV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	-	0.4	V	-
1. For recommended operating conditions, see Table 3.					
2. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.					
3. The symbol LV_{IN} represents the input voltage of the supply referenced in Table 3.					

This table provides the DC electrical characteristics for the GPIO interface operating at O/LV_{DD} = 1.8 V.

Table 56. GPIO DC electrical characteristics (O/LV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x O/LVDD	-	V	2
Input low voltage	V_{IL}	-	0.3 x O/LVDD	V	2
Input current (V_{IN} = 0V or V_{IN}= O/LV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (O/LV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (O/LV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-
1. For recommended operating conditions, see Table 3.					

Table 56. GPIO DC electrical characteristics (O/LV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN}/LV_{IN} values found in Table 3.					
3. The symbol OV_{IN}/LV_{IN} represents the input voltage of the supply referenced in Table 3.					

This table provides the DC electrical characteristics for the GPIO interface operating at O/LV_{DD} = 1.8 V.

Table 57. GPIO DC electrical characteristics (TV_{DD} = 1.2 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x TVDD	-	-	2
Input low voltage	V_{IL}	-	0.2 x TVDD	-	2
Output low current (V_{OL} = 0.2 V)	I_{OL}	4.0	-	mA	-
Output high voltage (TV_{DD} = min, I_{OH} = -100 µA)	V_{OH}	1.0	-	V	3
Output low voltage (TV_{DD} = min, I_{OL} = 100 µA)	V_{OL}	-	0.2	V	3
Input capacitance	C_{IN}	-	10.0	pF	-
1. For recommended operating conditions, see Table 3.					
2. The min V_{IL} and max V_{IH} values are based on the respective min and max TV_{IN} values found in Table 3.					
3. The symbol TV_{DD} represents the input voltage of the supply referenced in Table 3.					

3.14.2 GPIO AC timing specifications

This table provides the AC timing specifications for the GPIO interface.

Table 58. GPIO AC timing specifications

Parameter	Symbol	Min	Unit	Notes
GPIO inputs-minimum pulse width	t_{PIWID}	20.0	ns	GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs must be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

This figure shows the AC test load for the GPIO interface.

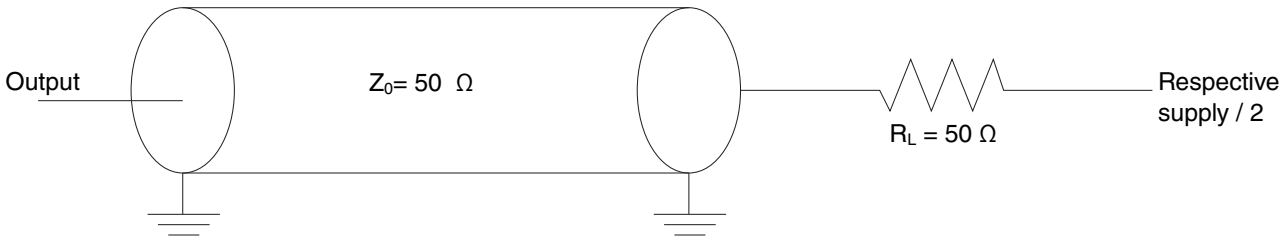


Figure 28. GPIO AC test load

3.15 Generic interrupt controller (GIC) interface

This section describes the DC and AC electrical characteristics for the GIC interface.

3.15.1 GIC DC electrical characteristics

This table provides the DC electrical characteristics for the GIC interface operating at DV_{DD} = 3.3 V.

Table 59. GIC DC electrical characteristics (DV_{DD} = 3.3 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.2 x DV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN}= DV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (DV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.4	-	V	-
Output low voltage (DV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	-	0.4	V	-

1. For recommended operating conditions, see Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 3.
3. The symbol DV_{IN} represents the input voltage of the supply referenced in Table 3.

This table provides the DC electrical characteristics for the GIC interface operating at DV_{DD} = 1.8 V.

Table 60. GIC DC electrical characteristics (DV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x DV_{DD}	V	2

Table continues on the next page...

Table 60. GIC DC electrical characteristics (DV_{DD} = 1.8 V)[1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input current (V_{IN} = 0V or V_{IN}= DV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (DV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (DV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-
1. For recommended operating conditions, see Table 3. 2. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 3. 3. The symbol DV_{IN} represents the input voltage of the supply referenced in Table 3.					

This table provides the DC electrical characteristics for the GIC interface operating at LV_{DD} = 2.5 V.

Table 61. GIC DC electrical characteristics (LV_{DD} = 2.5 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.2 x LV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN}= LV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (LV_{DD} = min, I_{OH} = -1 mA)	V_{OH}	2.0	-	V	-
Output low voltage (LV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	-	0.4	V	-
1. For recommended operating conditions, see Table 3. 2. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3. 3. The symbol LV_{IN} represents the input voltage of the supply referenced in Table 3.					

This table provides the DC electrical characteristics for the GIC interface operating at O/LV_{DD} = 1.8 V.

Table 62. GIC DC electrical characteristics (O/LV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x O/LV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x O/LV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN}= O/LV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (O/LV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (O/LV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-
1. For recommended operating conditions, see Table 3. 2. The min V_{IL} and max V_{IH} values are based on the respective min and max O/LV_{IN} values found in Table 3. 3. The symbol O/LV_{IN} represents the input voltage of the supply referenced in Table 3.					

3.15.2 GIC AC timing specifications

This table provides the AC timing specifications for the GIC interface.

Table 63. GIC AC timing specifications

Parameter	Symbol	Min	Unit	Notes
GIC inputs-minimum pulse width	t_{PIWID}	3.0	SYSCLKs	1, 2
1. Entry and exit from deep sleep respectively require a minimum pulse width t_{PIWID} of 25 SYSCLK. See the applicable device reference manual for details on entry and exit from deep sleep.				
2. GIC inputs and outputs are asynchronous to any visible clock. GIC outputs must be synchronized before use by any external synchronous logic. GIC inputs are required to be valid for at least tPIWID ns to ensure proper operation when working in edge triggered mode.				

3.16 High-speed serial interfaces (HSSI)

The chip features a Serializer/Deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express, SGMII, and serial ATA (SATA) data transfers.

This section describes the most common portion of the SerDes DC electrical specifications: the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter (Tx) and receiver (Rx) reference circuits are also described.

3.16.1 Signal terms definitions

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines the terms that are used in the description and specification of differential signals.

This figure shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. This figure shows the waveform for either a transmitter output (SD_TX*n*_P and SD_TX*n*_N) or a receiver input (SD_RX*n*_P and SD_RX*n*_N). Each signal swings between A volts and B volts where A > B.

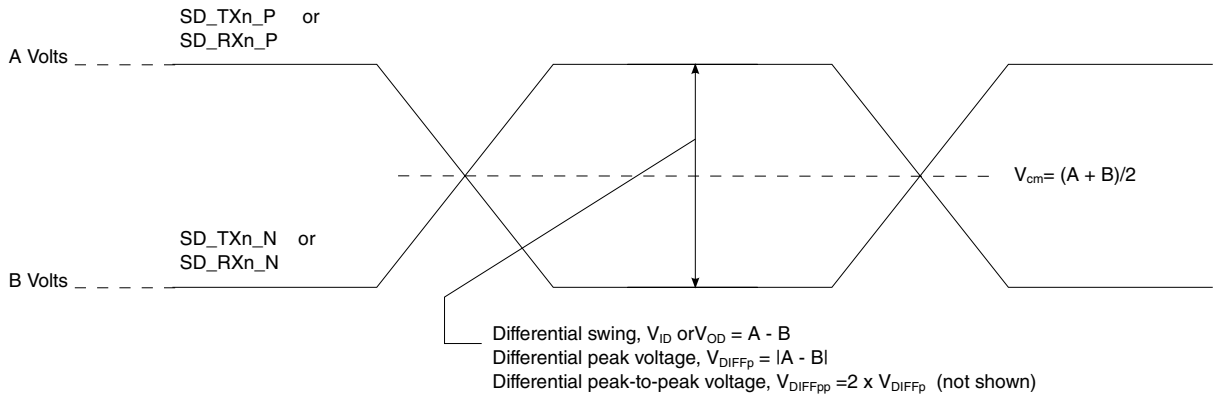


Figure 29. Differential voltage definitions for transmitter or receiver

Using this waveform, the definitions are as described in the following list. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment:

Single-Ended Swing

The transmitter output signals and the receiver input signals SD_TX*n*_P, SD_TX*n*_N, SD_RX*n*_P and SD_RX*n*_N each have a peak-to-peak swing of A - B volts. This is also referred to as each signal wire's single-ended swing.

Differential Output Voltage, V_{OD} (or Differential Output Swing)

The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complementary output voltages: $V_{SD_TXn_P}$ - $V_{SD_TXn_N}$. The V_{OD} value can be either positive or negative.

Differential Input Voltage, V_{ID} (or Differential Input Swing)

The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complementary input voltages: $V_{SD_RXn_P}$- $V_{SD_RXn_N}$. The V_{ID} value can be either positive or negative.

Differential Peak Voltage, V_{DIFFp}

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, V_{DIFFp} = |A - B| volts.

Differential Peak-to-Peak, $V_{DIFFp-p}$

Because the differential output signal of the transmitter and the differential input signal of the receiver each range from A - B to -(A - B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p}$ = 2 x V_{DIFFp} = 2 x |(A - B)| volts, which is twice the differential swing in amplitude, or twice the differential peak. For example, the output differential peak-to-peak voltage can also be calculated as $V_{TX-DIFFp-p}$ = 2 x |V_{OD}|.

Differential Waveform

The differential waveform is constructed by subtracting the inverting signal (SD_TX*n*_N, for example) from the non-inverting signal (SD_TX*n*_P, for example)

within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. See Figure 34 as an example for differential waveform.

Common Mode Voltage, V_{cm}

The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = (V_{SD_TXn_P} + V_{SD_TXn_N}) \div 2 = (A + B) \div 2$, which is the arithmetic mean of the two complementary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and TD_B. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or TD_B) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and -500 mV. In other words, V_{OD} is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

3.16.2 SerDes reference clocks

The SerDes reference clock inputs are applied to an internal phase-locked loop (PLL) whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD*n*_REF_CLK[1:2]_P and SD*n*_REF_CLK[1:2]_N.

SerDes may be used for various combinations of the following IP block based on the RCW Configuration field SRDS_PRTCLn:

- SGMII (1.25 Gbaud or 3.125 Gbaud), QSGMII (5 Gbps)
- XFI (10.3125 Gb/s)
- PCIe (2.5, 5, and 8 GT/s)
- SATA (1.5, 3.0, and 6.0 Gbps)

The following sections describe the SerDes reference clock requirements and provide application information.

3.16.2.1 SerDes spread-spectrum clock source recommendations

SD*n*_REF_CLK*n*_P and SD*n*_REF_CLK*n*_N are designed to work with spread-spectrum clocking for the PCI Express protocol only with the spreading specification defined in Table 64. When using spread-spectrum clocking for PCI Express, both ends of the link partners should use the same reference clock. For best results, a source without significant unintended modulation must be used.

The SerDes transmitter does not support spread-spectrum clocking for the SATA protocol. The SerDes receiver does support spread-spectrum clocking on receive, which means the SerDes receiver can receive data correctly from a SATA serial link partner using spread-spectrum clocking.

Spread-spectrum clocking cannot be used if the same SerDes reference clock is shared with other non-spread-spectrum-supported protocols. For example, if spread-spectrum clocking is desired on a SerDes reference clock for the PCI Express protocol and the same reference clock is used for any other protocol, such as SATA or SGMII because of the SerDes lane usage mapping option, spread-spectrum clocking cannot be used at all.

This table provides the source recommendations for SerDes spread-spectrum clocking.

Table 64. SerDes spread-spectrum clock source recommendations [1]

Parameter	Min	Max	Unit	Notes
Frequency modulation	30	33	kHz	—
Frequency spread	+0	-0.5	%	2

Notes:

1. At recommended operating conditions. See Table 3.
2. Only down-spreading is allowed.

3.16.2.2 SerDes reference clock receiver characteristics

This figure shows a receiver reference diagram of the SerDes reference clocks.

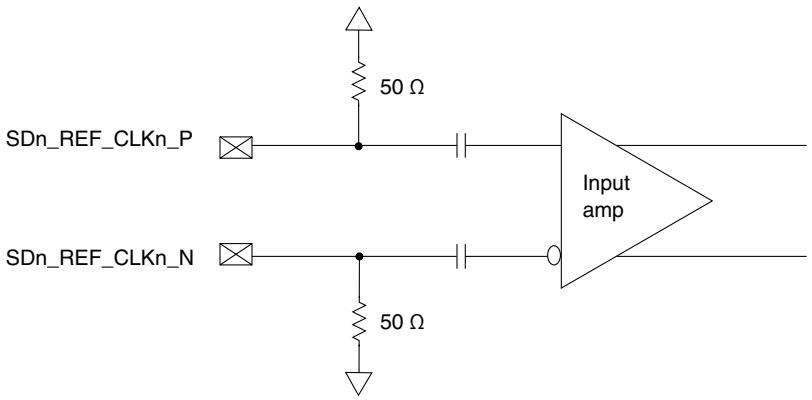


Figure 30. Receiver of SerDes reference clocks

The characteristics of the clock signals are as follows:

- The SerDes transceiver's core power supply voltage requirements (SV_{DD}) are as specified in Table 3.
- The SerDes reference clock receiver reference circuit structure is as follows:
  - The SD*n*_REF_CLK*n*_P and SD*n*_REF_CLK*n*_N are internally AC-coupled differential inputs as shown in Figure 30. Each differential clock input (SD*n*_REF_CLK*n*_P or SD*n*_REF_CLK*n*_N) has on-chip 50-Ω termination to SGND*n* followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. See the differential mode and single-ended mode descriptions in Signal terms definitions for detailed requirements.
- The maximum average current requirement also determines the common mode voltage range.
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V ÷ 50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND*n*. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0-0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SD*n*_REF_CLK*n*_P and SD*n*_REF_CLK*n*_N inputs cannot drive 50 Ω to SGND*n* DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled off-chip.
- The input amplitude requirement is described in detail in the following sections.

3.16.2.3 DC-level requirements for SerDes reference clocks

The DC-level requirements for the SerDes reference clock inputs are different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below:

- Differential Mode
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-to-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For an external DC-coupled connection, as described in Figure 30, the maximum average current requirements set the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV.
  - This figure shows the SerDes reference clock input requirement for a DC-coupled connection scheme.

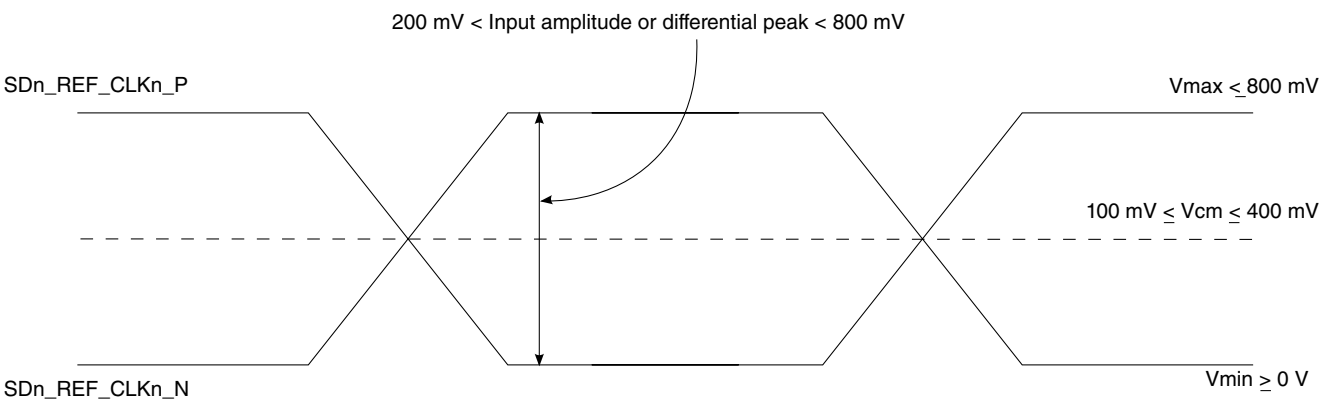


Figure 31. Differential reference clock input DC requirements (external DC-coupled)

  - For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different common mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND*n*. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (SGND*n*).
  - This figure shows the SerDes reference clock input requirement for an AC-coupled connection scheme.

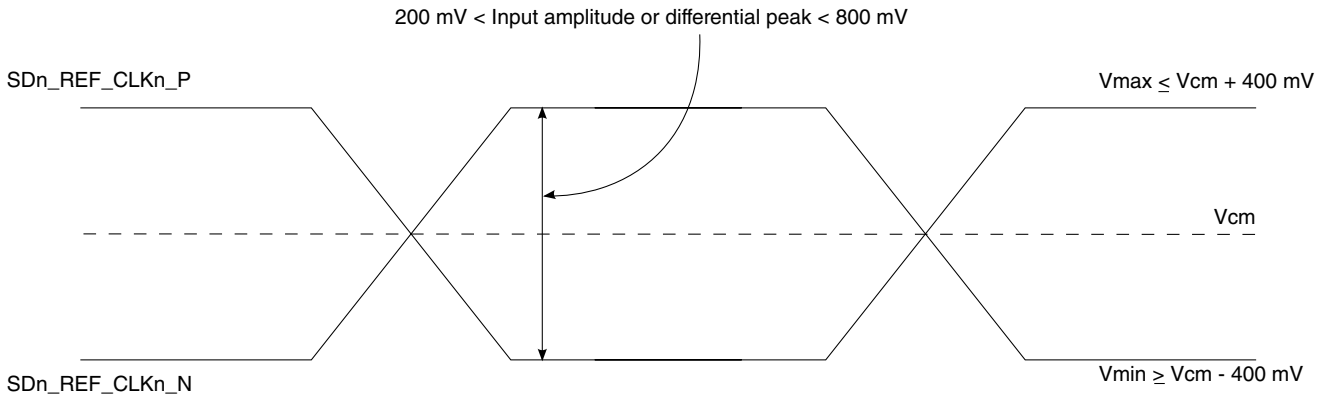


Figure 32. Differential reference clock input DC requirements (external AC-coupled)

- Single-ended mode
  - The reference clock can also be single-ended. The SD*n*_REF_CLK*n*_P input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-to-peak (from V_{MIN} to V_{MAX}) with SD*n*_REF_CLK*n*_N either left unconnected or tied to ground.
  - To meet the input amplitude requirement, the reference clock inputs may need to be externally DC- or AC-coupled. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase (SD*n*_REF_CLK*n*_N) through the same source impedance as the clock input (SD*n*_REF_CLK*n*_P) in use.
  - The SD*n*_REF_CLK*n*_P input average voltage must be between 200 and 400 mV.
  - This figure shows the SerDes reference clock input requirement for single-ended signaling mode.

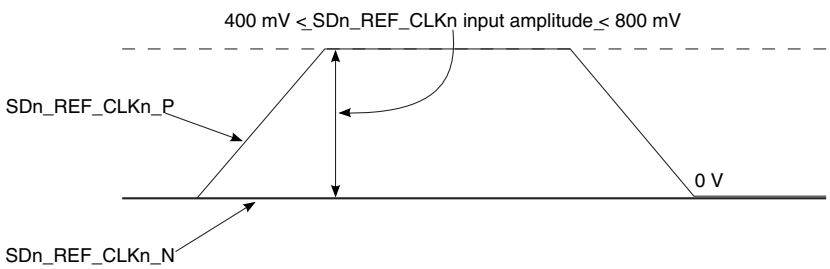


Figure 33. Single-ended reference clock input DC requirements

3.16.2.4 AC requirements for SerDes reference clocks

This table provides the AC requirements for SerDes reference clocks for PCI Express protocols running at data rates up to 8 GT/s.

This includes PCI Express (2.5, 5, and 8 GT/s), SGMII (1.25 Gbaud), 2.5 x SGMII (3.125 Gbaud), QSGMII (5 Gbps), and SATA (1.5, 3.0, and 6.0 Gbps). SerDes reference clocks need to be verified by the customer's application design.

Table 65. SD*n*_REF_CLK*n*_P and SD*n*_REF_CLK*n*_N input clock requirements (SV_{DD} = 0.9V/ 1.0 V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N frequency range	t_{CLK_REF}	—	100/125/156.25	—	MHz	2
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N clock frequency tolerance	t_{CLK_TOL}	-300	—	300	ppm	3
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N clock frequency tolerance	t_{CLK_TOL}	-100	—	100	ppm	4
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	5
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N max deterministic peak-to-peak jitter at 10^{-6} BER	t_{CLK_DJ}	—	—	42	ps	—
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N total reference clock jitter at 10^{-6} BER (peak-to-peak jitter at refClk input)	t_{CLK_TJ}	—	—	86	ps	6
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N 10 kHz to 1.5 MHz RMS jitter	$t_{REFCLK\text{-}LF\text{-}RMS}$	—	—	3	ps RMS	7
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N > 1.5 MHz to Nyquist RMS jitter	$t_{REFCLK\text{-}HF\text{-}RMS}$	—	—	3.1	ps RMS	7
RMS reference clock jitter	$t_{REFCLK\text{-}RMS\text{-}DC}$	—	—	1	ps RMS	8
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N rising/ falling edge rate	t_{CLKRR}/t_{CLKFR}	1	—	4	V/ns	9
Differential input high voltage	V_{IH}	200	—	—	mV	5
Differential input low voltage	V_{IL}	—	—	-200	mV	5
Rising edge rate (SD*n*_REF_CLK*n*_P) to falling edge rate (SD*n*_REF_CLK*n*_N) matching	Rise-Fall Matching	—	—	20	%	10, 11

Notes:

1. For recommended operating conditions, see Table 3.
2. **Caution:** Only 100, 125, and 156.25 have been tested. In-between values do not work correctly with the rest of the system.
3. For PCI Express (2.5, 5 and 8 GT/s).
4. For SGMII, 2.5 x SGMII and QSGMII.
5. Measurement taken from differential waveform.
6. Limits from PCI Express CEM Rev 2.0.
7. For PCI Express 5 GT/s, per PCI Express base specification Rev 3.0.
8. For PCI Express 8 GT/s, per PCI Express base specification Rev. 3.0.
9. Measured from -200 mV to +200 mV on the differential waveform (derived from SD*n*_REF_CLK*n*_P minus SD*n*_REF_CLK*n*_N). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 34.
10. Measurement taken from single-ended waveform.

Table 65. SD*n*_REF_CLK*n*_P and SD*n*_REF_CLK*n*_N input clock requirements (SV_{DD} = 0.9V/ 1.0 V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
11. Matching applies to rising edge for SD*n*_REF_CLK*n*_P and falling edge rate for SD*n*_REF_CLK*n*_N. It is measured using a 200 mV window centered on the median cross point where SD*n*_REF_CLK*n*_P rising meets SD*n*_REF_CLK*n*_N falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD*n*_REF_CLK*n*_P must be compared to the fall edge rate of SD*n*_REF_CLK*n*_N, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 35.						

This table lists the AC requirements for SerDes reference clocks for protocols running at data rates greater than 8 Gb/s.

This includes XFI (10.3125 Gb/s) SerDes reference clocks to be guaranteed by the customer's application design.

Table 66. Input clock requirements for XFI (10.3125)[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Frequency range	t_{CLK_REF}	—	156.25	—	MHz	2
Clock frequency tolerance	t_{CLK_TOL}	-100	—	100	ppm	—
Reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	3
Single side band noise	@1 kHz	—	—	-85	dBC/Hz	4
Single side band noise	@10 kHz	—	—	-108	dBC/Hz	4
Single side band noise	@100 kHz	—	—	-128	dBC/Hz	4
Single side band noise	@1 MHz	—	—	-138	dBC/Hz	4
Single side band noise	@10MHz	—	—	-138	dBC/Hz	4
Random jitter (1.2 MHz to 15 MHz)	t_{CLK_RJ}	—	—	0.8	ps	—
Total reference clock jitter at 10^{-12} BER (1.2 MHz to 15 MHz)	t_{CLK_TJ}	—	—	11	ps	—
Spurious noise (1.2 MHz to 15 MHz)	—	—	—	-75	dBC	—

Notes:

1. For recommended operating conditions, see Table 3.
2. **Caution:** Only 156.25 have been tested. Inbetween values do not work correctly with the rest of the system.
3. Measurement taken from differential waveform.
4. Per XFP Spec. Rev 4.5, the Module Jitter Generation spec at XFI Optical Output is 10mUI (RMS) and 100 mUI (p-p). In the CDR mode the host is contributing 7 mUI (RMS) and 50 mUI (p-p) jitter.

This figure shows the differential measurement points for rise and fall time.

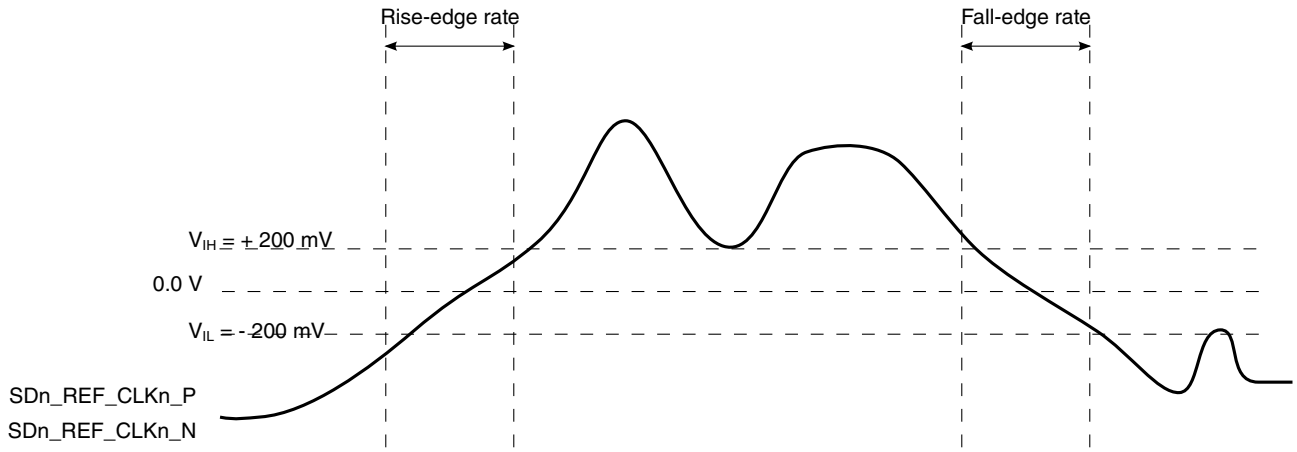


Figure 34. Differential measurement points for rise and fall time

This figure shows the single-ended measurement points for rise and fall time matching.

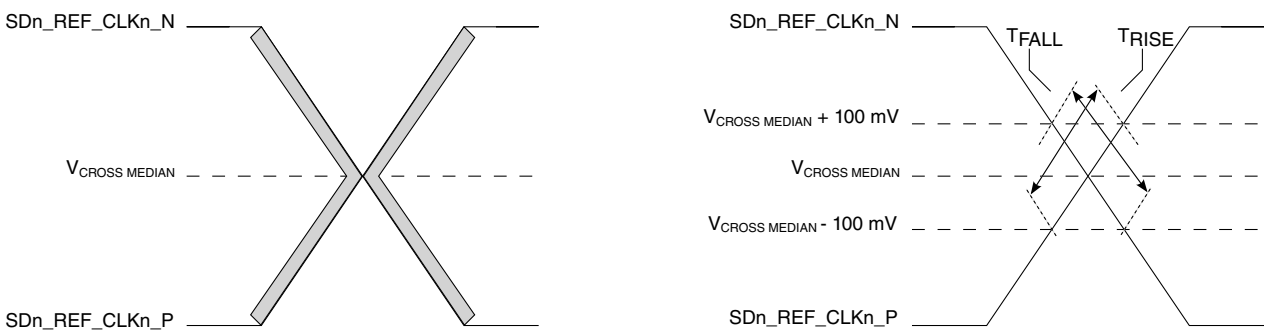


Figure 35. Single-ended measurement points for rise and fall time matching

3.16.3 SerDes transmitter and receiver reference circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

Figure 36. SerDes transmitter and receiver reference circuits

The DC and AC specifications of the SerDes data lanes are defined in each interface protocol section below based on the application usage:

- PCI Express
- Serial ATA (SATA) interface
- SGMII interface
- QSGMII interface
- XFI interface

Note that an external AC-coupling capacitor is required for the above serial transmission protocols with the capacitor value defined in the specification of each protocol section.

3.16.4 PCI Express

This section describes the clocking dependencies, as well as the DC and AC electrical specifications for the PCI Express bus.

3.16.4.1 Clocking dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 ppm of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

3.16.4.2 PCI Express clocking requirements for SD2_REF_CLK*n*_P and SD2_REF_CLK*n*_N

SerDes 2 (SD2_REF_CLK[1:2]_P and SD2_REF_CLK[1:2]_N) may be used for various SerDes PCI Express configurations based on the RCW configuration field SRDS_PRTCL. PCI Express is supported on SerDes 2.

For more information on these specifications, see SerDes reference clocks.

3.16.4.3 PCI Express DC physical layer specifications

This section contains the DC specifications for the physical layer of PCI Express on this chip.

3.16.4.3.1 PCI Express DC physical layer transmitter specifications

This section discusses the PCI Express DC physical layer transmitter specifications for 2.5 GT/s, 5 GT/s, and 8 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 67. PCI Express 2.0 (2.5 GT/s) differential transmitter output DC specifications (XV_{DD} = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	1000	1200	mV	$V_{TX-DIFFp-p}$ = 2 x | V_{TX-D+} - V_{TX-D-} |
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Transmitter DC differential mode low Impedance
Transmitter DC impedance	Z_{TX-DC}	40	50	60	Ω	Required transmitter D+ as well as D- DC Impedance during all states

Notes:

1. For recommended operating conditions, see Table 3.

This table defines the PCI Express 2.0 (5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 68. PCI Express 2.0 (5 GT/s) differential transmitter output DC specifications (XV_{DD} = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	1000	1200	mV	$V_{TX-DIFFp-p}$ = 2 x | V_{TX-D+} - V_{TX-D-} |
Low power differential peak-to-peak output voltage	$V_{TX-DIFFp-p_low}$	400	500	1200	mV	$V_{TX-DIFFp-p}$ = 2 x | V_{TX-D+} - V_{TX-D-} |
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Transmitter DC differential mode low impedance
Transmitter DC Impedance	Z_{TX-DC}	40	50	60	Ω	Required transmitter D+ as well as D- DC impedance during all states

Notes:

1. For recommended operating conditions, see Table 3.

This table defines the PCI Express 3.0 (8 GT/s) DC characteristics for the differential output at all transmitters. The parameters are specified at the component pins.

Table 69. PCI Express 3.0 (8 GT/s) differential transmitter output DC characteristics (XV_{DD} = 1.35 V)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Full swing transmitter voltage with no TX Eq	$V_{TX-FS-NO-EQ}$	800	—	1300	mVp-p	See Note 1.
Reduced swing transmitter voltage with no TX Eq	$V_{TX-RS-NO-EQ}$	400	—	1300	mV	See Note 1.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	—
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	—
Minimum swing during EIEOS for full swing	$V_{TX-EIEOS-FS}$	250	—	—	mVp-p	See Note 2
Minimum swing during EIEOS for reduced swing	$V_{TX-EIEOS-RS}$	232	—	—	mVp-p	See Note 2
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Transmitter DC differential mode low impedance
Transmitter DC Impedance	Z_{TX-DC}	40	50	60	Ω	Required transmitter D+ as well as D- DC impedance during all states

Notes:

1. Voltage measurements for $V_{TX-FS-NO-EQ}$ and $V_{TX-RS-NO-EQ}$ are made using the 64-zeroes/64-ones pattern in the compliance pattern.

2. Voltage limits comprehend both full swing and reduced swing modes. The transmitter must reject any changes that would violate this specification. The maximum level is covered in the $V_{TX-FS-NO-EQ}$ measurement which represents the maximum peak voltage the transmitter can drive. The $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ voltage limits are imposed to guarantee the EIEOS threshold of 175 mV_{P-P} at the receiver pin. This parameter is measured using the actual EIEOS pattern that is part of the compliance pattern and then removing the ISI contribution of the breakout channel.

3. For recommended operating conditions, see Table 3.

3.16.4.3.2 PCI Express DC physical layer receiver specifications

This section discusses the PCI Express DC physical layer receiver specifications for 2.5 GT/s, 5 GT/s, and 8 GT/s.

This table defines the DC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 70. PCI Express 2.0 (2.5 GT/s) differential receiver input DC specifications (SV_{DD} = 0.9V/1.0 V)[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	175	1000	1200	mV	$V_{RX-DIFFp-p}$ = 2 x $\lvert V_{RX-D+} - V_{RX-D-} \rvert$ See Note 1.

Table continues on the next page...

Table 70. PCI Express 2.0 (2.5 GT/s) differential receiver input DC specifications (SV_{DD} = 0.9V/1.0 V)[4] (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required receiver D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	-	-	kΩ	Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	-	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the package pins of the receiver

Notes:

1. Measured at the package pins with a test load of 50Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.
4. For recommended operating conditions, see Table 3.

This table defines the DC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 71. PCI Express 2.0 (5 GT/s) differential receiver input DC specifications (SV_{DD} = 0.9V/1.0 V)[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	120	1000	1200	mV	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ See Note 1.
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required receiver D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	-	-	kΩ	Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	-	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the package pins of the receiver

Table continues on the next page...

Table 71. PCI Express 2.0 (5 GT/s) differential receiver input DC specifications (SV_{DD} = 0.9V/1.0 V)[4] (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Notes: 1. Measured at the package pins with a test load of 50 Ω to GND on each pin. 2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port. 3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground. 4. For recommended operating conditions, see Table 3.						

This table defines the DC characteristics for the PCI Express 3.0 (8 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 72. PCI Express 3.0 (8 GT/s) differential receiver input DC characteristics (SV_{DD} = 0.9V/1.0 V)[6]

Characteristic	Symbol	Min	Typ	Max	Units	Notes
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required receiver D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	—	—	kΩ	Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3.
Generator launch voltage	$V_{RX-LAUNCH-8G}$	—	800	—	mV	Measured at TP1 per PCI Express base spec. rev 3.0
Eye height (-20dB Channel)	$V_{RX-SV-8G}$	25	—	—	mV	Measured at TP2P per PCI Express base spec. rev 3.0. See Notes 4, 5
Eye height (-12dB Channel)	$V_{RX-SV-8G}$	50	—	—	mV	Measured at TP2P per PCI Express base spec. rev 3.0. See Notes 4, 5
Eye height (-3dB Channel)	$V_{RX-SV-8G}$	200	—	—	mV	Measured at TP2P per PCI Express base spec. rev 3.0. See Notes 4, 5
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the package pins of the receiver
Notes: 1. Measured at the package pins with a test load of 50 Ω to GND on each pin. 2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port. 3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.						

Table 72. PCI Express 3.0 (8 GT/s) differential receiver input DC characteristics (SV_{DD} = 0.9V/1.0 V)[6]

Characteristic	Symbol	Min	Typ	Max	Units	Notes
4. $V_{RX-SV-8G}$ is tested at three different voltages to ensure the receiver device under test is capable of equalizing over a range of channel loss profiles. The "SV" in the parameter names refers to stressed voltage. 5. $V_{RX-SV-8G}$ is referenced to TP2P and is obtained after post processing data captured at TP2. 6. For recommended operating conditions, see Table 3.						

3.16.4.4 PCI Express AC physical layer specifications

This section describes the AC specifications for the physical layer of PCI Express on this device.

3.16.4.4.1 PCI Express AC physical layer transmitter specifications

This section describes the PCI Express AC physical layer transmitter specifications for 2.5 GT/s, 5 GT/s, and 8 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 73. PCI Express 2.0 (2.5 GT/s) differential transmitter output AC specifications[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit interval	UI	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum transmitter eye width	T_{TX-EYE}	0.75	-	-	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER}$ = 1 - T_{TX-EYE} = 0.25 UI. Does not include spread-spectrum or RefCLK jitter. Includes device random jitter at 10^{-12}. See Notes 1 and 2.
Maximum time between the jitter median and maximum deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.125	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. See Notes 1 and 2.
AC coupling capacitor	C_{TX}	75	-	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 3.

Table continues on the next page...

Table 73. PCI Express 2.0 (2.5 GT/s) differential transmitter output AC specifications[4] (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Notes: 1. Specified at the measurement point into a timing and voltage test load as shown in Figure 38 and measured over any 250 consecutive transmitter UIs. 2. A T_{TX-EYE} = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.25 UI for the transmitter collected over any 250 consecutive transmitter UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total transmitter jitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. 3. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required. 4. For recommended operating conditions, see Table 3.						

This table defines the PCI Express 2.0 (5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 74. PCI Express 2.0 (5 GT/s) differential transmitter output AC specifications[3]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	199.94	200.00	200.06	ps	Each UI is 200 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum transmitter eye width	T_{TX-EYE}	0.75	-	-	UI	The maximum transmitter jitter can be derived as: $T_{TX-MAX-JITTER}$ = 1 - T_{TX-EYE} = 0.25 UI. See Note 1.
Transmitter RMS deterministic jitter > 1.5 MHz	$T_{TX-HF-DJ-DD}$	-	-	0.15	ps	-
Transmitter RMS deterministic jitter < 1.5 MHz	$T_{TX-LF-RMS}$	-	3.0	-	ps	Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps
AC coupling capacitor	C_{TX}	75	-	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 2.
Notes: 1. Specified at the measurement point into a timing and voltage test load as shown in Figure 38 and measured over any 250 consecutive transmitter UIs. 2. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required. 3. For recommended operating conditions, see Table 3.						

This table defines the PCI Express 3.0 (8 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 75. PCI Express 3.0 (8 GT/s) differential transmitter output AC specifications[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	124.9625	125.00	125.0375	ps	Each UI is 125 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Transmitter uncorrelated total jitter	T_{TX-UTJ}	—	—	31.25	ps p-p	—
Transmitter uncorrelated deterministic jitter	$T_{TX-UDJ-DD}$	—	—	12	ps p-p	—
Total uncorrelated pulse width jitter (PWJ)	$T_{TX-UPW-TJ}$	—	—	24	ps p-p	See Note 1, 2
Deterministic data dependent jitter (DjDD) uncorrelated pulse width jitter (PWJ)	$T_{TX-UPW-DJDD}$	—	—	10	ps p-p	See Note 1, 2
Data dependent jitter	T_{TX-DDJ}	—	—	18	ps p-p	See Note 2
AC coupling capacitor	C_{TX}	176	—	265	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 3.

Notes:

1. PWJ parameters shall be measured after data dependent jitter (DDJ) separation.
2. Measured with optimized preset value after de-embedding to transmitter pin.
3. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.
4. For recommended operating conditions, see Table 3.

3.16.4.4.2 PCI Express AC physical layer receiver specifications

This section discusses the PCI Express AC physical layer receiver specifications for 2.5 GT/s, 5 GT/s, and 8 GT/s.

This table defines the AC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 76. PCI Express 2.0 (2.5 GT/s) differential receiver input AC specifications[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum receiver eye width	T_{RX-EYE}	0.4	-	-	UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER}$ = 1 - T_{RX-EYE}= 0.6 UI. See Notes 1 and 2.

Table continues on the next page...

Table 76. PCI Express 2.0 (2.5 GT/s) differential receiver input AC specifications[4] (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. See Notes 1, 2 and 3.

Notes:

1. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 38 must be used as the receiver device when taking measurements. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.

2. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.

3. It is recommended that the recovered transmitter UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

4. For recommended operating conditions, see Table 3.

This table defines the AC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 77. PCI Express 2.0 (5 GT/s) differential receiver input AC specifications[1]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	199.40	200.00	200.06	ps	Each UI is 200 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Max receiver inherent timing error	$T_{RX-TJ-CC}$	-	-	0.4	UI	The maximum inherent total timing error for common RefClk receiver architecture
Max receiver inherent deterministic timing error	$T_{RX-DJ-DD-CC}$	-	-	0.30	UI	The maximum inherent deterministic timing error for common RefClk receiver architecture

Note:

1. For recommended operating conditions, see Table 3.

This table defines the AC specifications for the PCI Express 3.0 (8 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 78. PCI Express 3.0 (8 GT/s) differential receiver input AC specifications[5]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	124.9625	125.00	125.0375	ps	Each UI is 125 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations. See Note 1.
Eye Width at TP2P	$T_{RX-SV-8G}$	0.3	—	0.35	UI	See Note 1
Differential mode interference	$V_{RX-SV-DIFF-8G}$	14	—	—	mV	Frequency = 2.1GHz. See Note 2.
Sinusoidal Jitter at 100 MHz	$T_{RX-SV-SJ-8G}$	—	—	0.1	UI p-p	Fixed at 100 MHz. See Note 3.
Random Jitter	$T_{RX-SV-RJ-8G}$	—	—	2.0	ps RMS	Random jitter spectrally flat before filtering. See Note 4.

Note:

1. $T_{RX-SV-8G}$ is referenced to TP2P and obtained after post processing data captured at TP2. $T_{RX-SV-8G}$ includes the effects of applying the behavioral receiver model and receiver behavioral equalization.
2. $V_{RX-SV-DIFF-8G}$ voltage may need to be adjusted over a wide range for the different loss calibration channels.
3. The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency as shown in Figure 37.
4. Random jitter (Rj) is applied over the following range: The low frequency limit may be between 1.5 and 10 MHz, and the upper limit is 1.0 GHz. See Figure 37 for details. Rj may be adjusted to meet the 0.3 UI value for $T_{RX-SV-8G}$.
5. For recommended operating conditions, see Table 3.

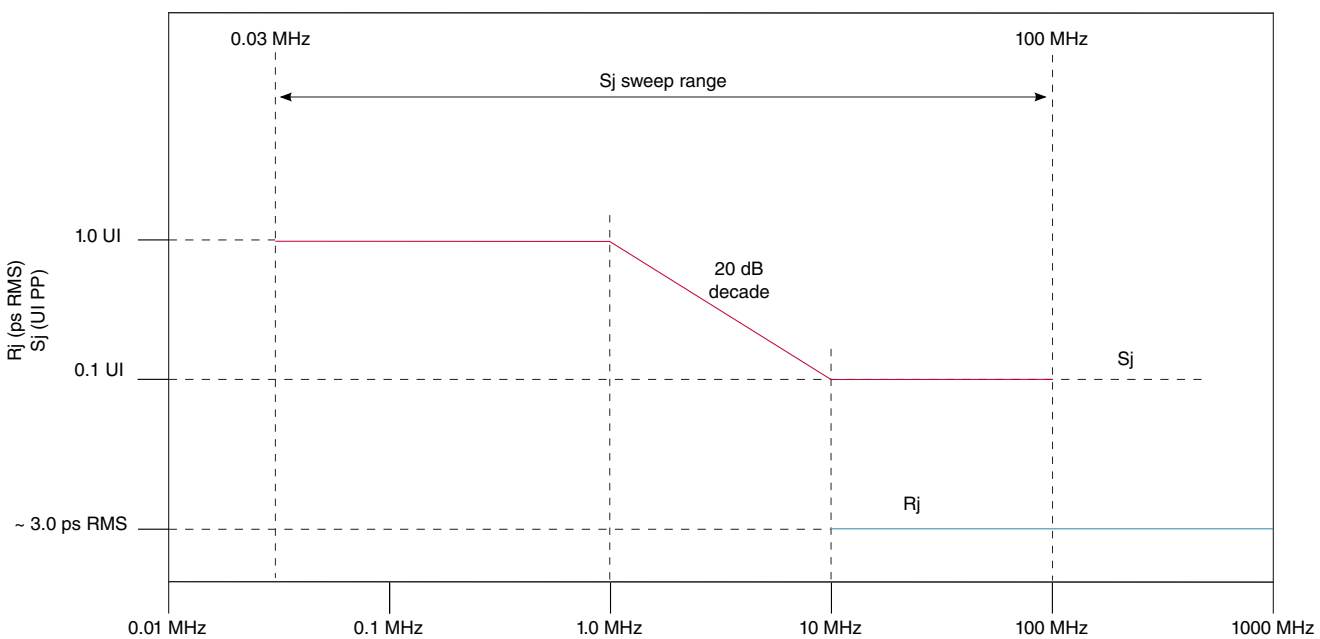


Figure 37. Swept sinusoidal jitter mask

3.16.4.5 Test and measurement load

The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in the following figure.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D- not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D- package pins.

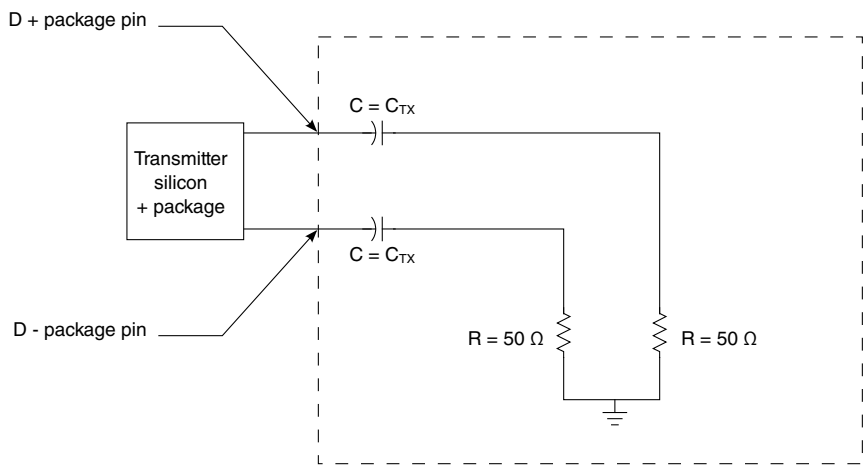


Figure 38. Test and measurement load

3.16.5 Serial ATA (SATA) interface

This section describes the DC and AC electrical specifications for the SATA interface.

3.16.5.1 SATA DC electrical characteristics

This section describes the DC electrical characteristics for SATA.

3.16.5.1.1 SATA DC transmitter output characteristics

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen1i/1m or 1.5 Gbits/s transmission.

Table 79. Gen1i/1m 1.5 G transmitter DC specifications (XV_{DD} = 1.35 V)[3]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Tx differential output voltage	V_{SATA_TXDIFF}	400	500	600	mV p-p	1
Tx differential pair impedance	$Z_{SATA_TXDIFFIM}$	85	100	115	Ω	2

Notes:

1. Terminated by 50 Ω load.
2. DC impedance.
3. For recommended operating conditions, see Table 3.

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen2i/2m or 3.0 Gbits/s transmission.

Table 80. Gen 2i/2m 3 G transmitter DC specifications (XV_{DD} = 1.35 V)[2]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmitter differential output voltage	V_{SATA_TXDIFF}	400	—	700	mV p-p	1
Transmitter differential pair impedance	$Z_{SATA_TXDIFFIM}$	85	100	115	Ω	—

Notes:

1. Terminated by 50 Ω load.
2. For recommended operating conditions, see Table 3.

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen 3i transmission.

Table 81. Gen 3i transmitter DC specifications (XV_{DD} = 1.35 V)[2]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmitter differential output voltage	V_{SATA_TXDIFF}	240	—	900	mV p-p	1
Transmitter differential pair impedance	$Z_{SATA_TXDIFFIM}$	85	100	115	Ω	—

Notes:

1. Terminated by 50 Ω load.
2. For recommended operating conditions, see Table 3.

3.16.5.1.2 SATA DC receiver input characteristics

This table provides the Gen1i/1m or 1.5 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 82. Gen1i/1m 1.5 G receiver input DC specifications (SV_{DD} = 0.9 V / 1.0 V)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	240	500	600	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	V_{SATA_OOB}	50	120	240	mV p-p	—

Notes:

1. Voltage relative to common of either signal comprising a differential pair.
2. DC impedance.
3. For recommended operating conditions, see Table 3.

This table provides the Gen2i/2m or 3 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 83. Gen2i/2m 3 G receiver input DC specifications (SV_{DD} = 0.9 V / 1.0 V)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	240	—	750	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	V_{SATA_OOB}	75	120	240	mV p-p	2

Notes:

1. Voltage relative to common of either signal comprising a differential pair.
2. DC impedance.
3. For recommended operating conditions, see Table 3.

This table provides the Gen 3i differential receiver input DC characteristics for the SATA interface.

Table 84. Gen 3i receiver input DC specifications (SV_{DD} = 0.9 V / 1.0 V)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	240	—	1000	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	—	75	120	200	mV p-p	—

Notes:

1. Voltage relative to common of either signal comprising a differential pair.
2. DC impedance.
3. For recommended operating conditions, see Table 3.

3.16.5.2 SATA AC timing specifications

This section describes the SATA AC timing specifications.

3.16.5.2.1 AC requirements for SATA REF_CLK

This table provides the AC requirements for the SATA reference clock. These requirements must be guaranteed by the customer's application design.

Table 85. SATA reference clock input requirements[6]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD*n*_REF_CLK1_P/SD*n*_REF_CLK1_N frequency range	t_{CLK_REF}	—	100/125	—	MHz	1
SD*n*_REF_CLK1_P/SD*n*_REF_CLK1_N clock frequency tolerance	t_{CLK_TOL}	-350	—	+350	ppm	—
SD*n*_REF_CLK1_P/SD*n*_REF_CLK1_N reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	5
SD*n*_REF_CLK1_P/SD*n*_REF_CLK1_N cycle-to-cycle clock jitter (period jitter)	t_{CLK_CJ}	—	—	100	ps	2
SD*n*_REF_CLK1_P/SD*n*_REF_CLK1_N total reference clock jitter, phase jitter (peak-to-peak)	t_{CLK_PJ}	-50	—	+50	ps	2, 3, 4

Notes:

1. **Caution:** Only 100 and 125 MHz have been tested. In-between values do not work correctly with the rest of the system.
2. At RefClk input.
3. In a frequency band from 150 kHz to 15 MHz at BER of 10^{-12}.
4. Total peak-to-peak deterministic jitter must be less than or equal to 50 ps.
5. Measurement taken from differential waveform.
6. For recommended operating conditions, see Table 3.

3.16.5.2.2 AC transmitter output characteristics

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen 1i/1m or 1.5 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 86. Gen 1i/1m 1.5 G transmitter AC specifications[2]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Channel speed	t_{CH_SPEED}	—	1.5	—	Gbps	—
Unit interval	T_{UI}	666.4333	666.6667	670.2333	ps	—
Total jitter data-data 5 UI	$U_{SATA_TXTJ5UI}$	—	—	0.355	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA_TXTJ250UI}$	—	—	0.47	UI p-p	1
Deterministic jitter, data-data 5 UI	$U_{SATA_TXDJ5UI}$	—	—	0.175	UI p-p	1
Deterministic jitter, data-data 250 UI	$U_{SATA_TXDJ250UI}$	—	—	0.22	UI p-p	1

Notes:

1. Measured at transmitter output pins peak-to-peak phase variation; random data pattern.
2. For recommended operating conditions, see Table 3.

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen 2i/2m or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 87. Gen 2i/2m 3 G transmitter AC specifications[2]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Channel speed	t_{CH_SPEED}	—	3.0	—	Gbps	—
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	—
Total jitter $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA_TXTJfB/500}$	—	—	0.37	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA_TXTJfB/1667}$	—	—	0.55	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA_TXDJfB/500}$	—	—	0.19	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA_TXDJfB/1667}$	—	—	0.35	UI p-p	1

Notes:

1. Measured at transmitter output pins peak-to-peak phase variation; random data pattern.
2. For recommended operating conditions, see Table 3.

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen 3i transmission. The AC timing specifications do not include RefClk jitter.

Table 88. Gen 3i transmitter AC specifications

Parameter	Symbol	Min	Typ	Max	Units
Speed	—	—	6.0	—	Gb/s
Total jitter before and after compliance interconnect channel	J_T	—	—	0.52	UI p-p
Random jitter before compliance interconnect channel	J_R	—	—	0.18	UI p-p
Unit interval	UI	166.6083	166.6667	167.5583	ps

3.16.5.2.3 AC differential receiver input characteristics

This table provides the Gen1i/1m or 1.5 Gbits/s differential receiver input AC characteristics for the SATA interface. The AC timing specifications do not include RefClk jitter.

Table 89. Gen 1i/1m 1.5 G receiver AC specifications[2]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit Interval	T_{UI}	666.4333	666.6667	670.2333	ps	—
Total jitter data-data 5 UI	$U_{SATA_RXTJ5UI}$	—	—	0.43	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA_RXTJ250UI}$	—	—	0.60	UI p-p	1

Table continues on the next page...

Table 89. Gen 1i/1m 1.5 G receiver AC specifications[2] (continued)

Parameter	Symbol	Min	Typical	Max	Units	Notes
Deterministic jitter, data-data 5 UI	$U_{SATA_RXDJ5UI}$	—	—	0.25	UI p-p	1
Deterministic jitter, data-data 250 UI	$U_{SATA_RXDJ250UI}$	—	—	0.35	UI p-p	1

Notes:

1. Measured at the receiver.
2. For recommended operating conditions, see Table 3.

This table provides the differential receiver input AC characteristics for the SATA interface at Gen2i/2m or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 90. Gen 2i/2m 3 G receiver AC specifications[2]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	—
Total jitter $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA_RXTJfB/500}$	—	—	0.60	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA_RXTJfB/1667}$	—	—	0.65	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA_RXDJfB/500}$	—	—	0.42	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA_RXDJfB/1667}$	—	—	0.35	UI p-p	1

Notes:

1. Measured at the receiver.
2. For recommended operating conditions, see Table 3.

This table provides the differential receiver input AC characteristics for the SATA interface at Gen 3i transmission The AC timing specifications do not include RefClk jitter.

Table 91. Gen 3i receiver AC specifications[2]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Total jitter after compliance interconnect channel	J_T	—	—	0.60	UI p-p	1
Random jitter before compliance interconnect channel	J_R	—	—	0.18	UI p-p	1
Unit interval: 6.0 Gb/s	UI	166.6083	166.6667	167.5583	ps	—

Notes:

1. Measured at the receiver.
2. The AC specifications do not include RefClk jitter.

3.16.6 SGMII interface

Each SGMII port features a 4-wire AC-coupled serial link from the SerDes interface of the chip, as shown in Figure 39, where C_{TX} is the external (on board) AC-coupled capacitor. Each SerDes transmitter differential pair features 100 Ω output impedance. Each input of the SerDes receiver differential pair features 50 Ω on-die termination to XGND*n*. The reference circuit of the SerDes transmitter and receiver is shown in Figure 36.

3.16.6.1 SGMII clocking requirements for SDn_REF_CLK1_P and SDn_REF_CLK1_N

When operating in SGMII mode, the EC*n*_GTX_CLK125 clock is not required for this port. Instead, a SerDes reference clock is required on SD1_REF_CLK[1:2]_P and SD1_REF_CLK[1:2]_N pins. SerDes lanes may be used for SerDes SGMII configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see SerDes reference clocks.

3.16.6.2 SGMII DC electrical characteristics

This section describes the electrical characteristics for the SGMII interface.

3.16.6.2.1 SGMII and SGMII 2.5 G transmit DC specifications

This table describes the SGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD*n*_TX*n*_P and SD*n*_TX*n*_N)as shown in Figure 40.

Table 92. SGMII DC transmitter electrical characteristics (XV_{DD} = 1.35 V)[4]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	-	-	1.5 x $\lvert V_{OD} \rvert_{-max}$	mV	1
Output low voltage	V_{OL}	$\lvert V_{OD} \rvert_{-min}/2$	-	-	mV	1
Output differential voltage[2, 3, 5] (XV_{DD-Typ} at 1.35 V)	$\lvert V_{OD} \rvert$	320	500.0	725.0	mV	TECR0[AMP_RED]=0b000000
		293.8	459.0	665.6		TECR0[AMP_RED]=0b000001
		266.9	417.0	604.7		TECR0[AMP_RED]=0b000011
		240.6	376.0	545.2		TECR0[AMP_RED]=0b000010

Table continues on the next page...

Table 92. SGMII DC transmitter electrical characteristics (XV_{DD} = 1.35 V)[4] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
		213.1	333.0	482.9		TECR0[AMP_RED]=0b000110
		186.9	292.0	423.4		TECR0[AMP_RED]=0b000111
		160.0	250.0	362.5		TECR0[AMP_RED]=0b010000
Output impedance (differential)	R_O	80	100	120	Ω	-

Notes:

1. This does not align to DC-coupled SGMII.
2. $|V_{OD}| = |V_{SD_TXn_P} - V_{SD_TXn_N}|$. $|V_{OD}|$ is also referred to as output differential peak voltage. $V_{TX\text{-}DIFFp\text{-}p} = 2 \times |V_{OD}|$.
3. The $|V_{OD}|$ value shown in the Typ column is based on the condition of XVDD_SRDSn-Typ = 1.35 V, no common mode offset variation. SerDes transmitter is terminated with 100-Ω differential load between SDn _TXn_P and SDn_TXn_N.
4. For recommended operating conditions, see Table 3.
5. Example amplitude reduction setting for SGMII on SerDes1 lane E: SRDS1LN4TECR0[AMP_RED] = 0b000001 for an output differential voltage of 459 mV typical.

This figure shows an example of a 4-wire AC-coupled SGMII serial link connection.

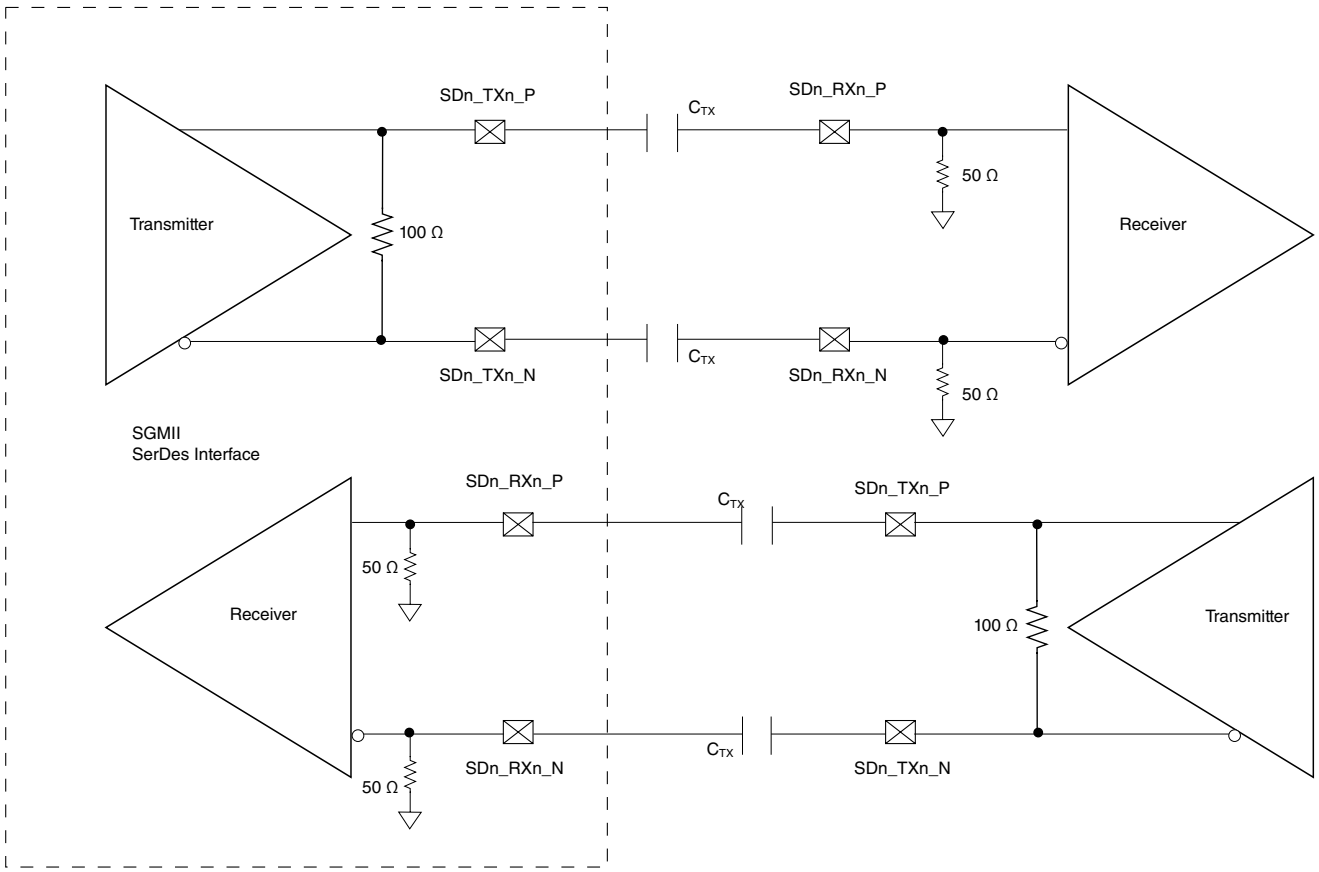


Figure 39. 4-wire AC-coupled SGMII serial link connection example

This figure shows the SGMII transmitter DC measurement circuit.

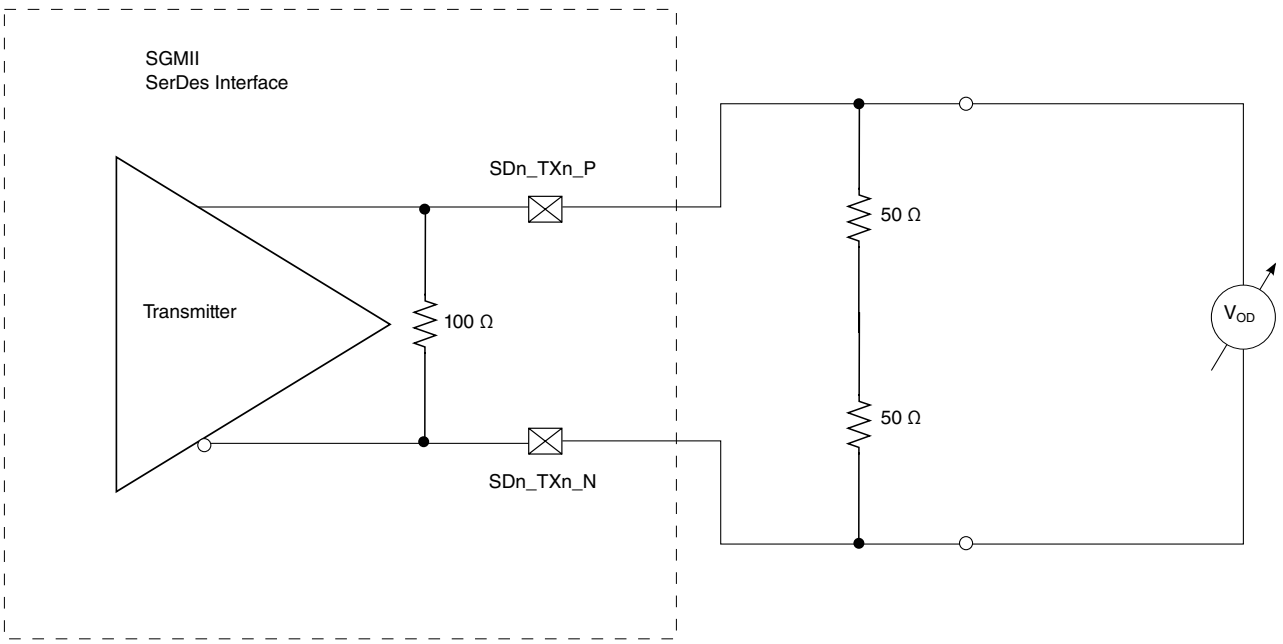


Figure 40. SGMII transmitter DC measurement circuit

This table defines the SGMII 2.5G transmitter DC electrical characteristics for 3.125 GBaud.

Table 93. SGMII 2.5G transmitter DC electrical characteristics (XV_{DD} = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output differential voltage	$\lvert V_{OD} \rvert$	400	-	600	mV	-
Output impedance (differential)	R_O	80	100	120	Ω	-
Notes: 1. For recommended operating conditions, see Table 3.						

3.16.6.2.2 SGMII and SGMII 2.5 G DC receiver electrical characteristics

This table lists the SGMII DC receiver electrical characteristics. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 94. SGMII DC receiver electrical characteristics (SV_{DD} = 0.9 V / 1.0 V)[4]

Parameter		Symbol	Min	Typ	Max	Unit	Notes
DC input voltage range		-	N/A			-	1
Input differential voltage	REIDL_TH = 001	$V_{RX_DIFFp-p}$	100	-	1200	mV	2, 5
	REIDL_TH = 100		175	-			
Loss of signal threshold	REIDL_TH = 001	V_{LOS}	30	-	100	mV	3, 5
	REIDL_TH = 100		65	-	175		

Table continues on the next page...

Table 94. SGMII DC receiver electrical characteristics (SV_{DD} = 0.9 V / 1.0 V)[4] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Receiver differential input impedance	Z_{RX_DIFF}	80	-	120	Ω	-

Notes:

1. Input must be externally AC coupled.
2. $V_{RX_DIFFp\text{-}p}$ is also referred to as peak-to-peak input differential voltage.
3. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express. See PCI Express DC physical layer receiver specifications for further explanation.
4. For recommended operating conditions, see Table 3.
5. The REIDL_TH shown in the table refers to the chip's SRDSxLNmGCR1[REIDL_TH] bit field.

This table defines the SGMII 2.5G receiver DC electrical characteristics for 3.125 GBaud.

Table 95. SGMII 2.5G receiver DC timing specifications (SV_{DD} = 0.9 V / 1.0 V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	$V_{RX_DIFFp\text{-}p}$	200	-	1200	mV	-
Loss of signal threshold	V_{LOS}	75	-	200	mV	-
Receiver differential input impedance	Z_{RX_DIFF}	80	-	120	Ω	-

Note:

1. For recommended operating conditions, see Table 3.

3.16.6.3 SGMII AC timing specifications

This section describes the AC timing specifications for the SGMII interface.

3.16.6.3.1 SGMII and SGMII 2.5 G transmit AC timing specifications

This table provides the SGMII and SGMII 2.5 G transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

Table 96. SGMII transmit AC timing specifications[4]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter	JD	-	-	0.17	UI p-p	-
Total jitter	JT	-	-	0.35	UI p-p	2
Unit Interval: 1.25 GBaud (SGMII)	UI	800 - 100 ppm	800	800 + 100 ppm	ps	1
Unit Interval: 3.125 GBaud (2.5G SGMII])	UI	320 - 100 ppm	320	320 + 100 ppm	ps	1
AC coupling capacitor	C_{TX}	10	-	200	nF	3

Table continues on the next page...

Table 96. SGMII transmit AC timing specifications[4] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Notes:						
1. Each UI is 800 ps ± 100 ppm or 320 ps ± 100 ppm.						
2. See Figure 42 for single frequency sinusoidal jitter measurements.						
3. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter output.						
4. For recommended operating conditions, see Table 3.						

3.16.6.3.2 SGMII AC measurement details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD*n*_TX*n*_P and SD*n*_TX*n*_N) or at the receiver inputs (SD*n*_RX*n*_P and SD*n*_RX*n*_N) respectively, as shown in this figure.

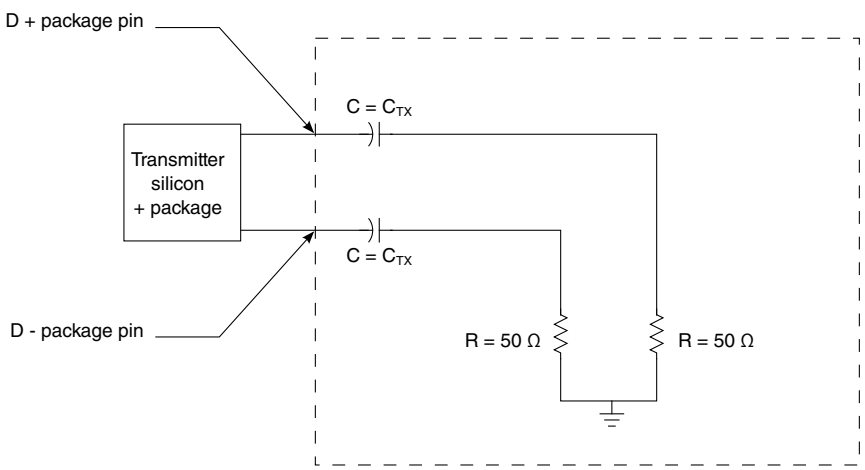


Figure 41. SGMII AC test/measurement load

3.16.6.3.3 SGMII and SGMII 2.5 G receiver AC timing specifications

This table provides the SGMII and SGMII 2.5 G receiver AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 97. SGMII receiver AC timing specifications[3]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter tolerance	J_D	-	-	0.37	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	-	-	0.55	UI p-p	1
Total jitter tolerance	J_T	-	-	0.65	UI p-p	1, 2

Table continues on the next page...

Table 97. SGMII receiver AC timing specifications[3] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Bit error ratio	BER	-	-	10^{-12}	-	-
Unit Interval: 1.25 GBaud (SGMII)	UI	800 - 100 ppm	800	800 + 100 ppm	ps	1
Unit Interval: 3.125 GBaud (2.5G SGMII])	UI	320 - 100 ppm	320	320 + 100 ppm	ps	1

Notes:

1. Measured at receiver.

2.Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 1. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

3. For recommended operating conditions, see Table 3.

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of this figure.

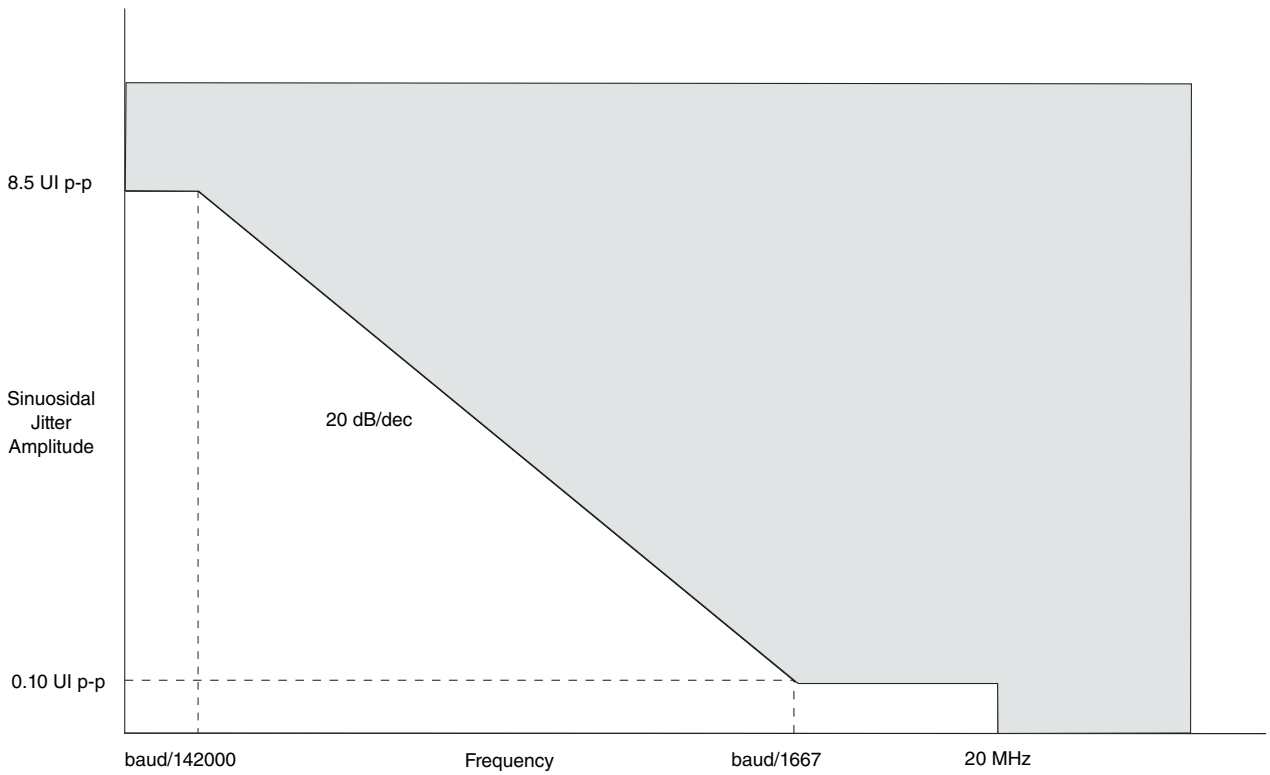


Figure 42. Single-frequency sinusoidal jitter limits

3.16.7 Quad serial media-independent interface (QSGMII)

This section describes the clocking as well as the DC and AC electrical characteristics for the QSGMII interface.

3.16.7.1 QSGMII clocking requirements for SDn_REF_CLKn_P and SDn_REF_CLKn_N

For more information on these specifications, see the SerDes reference clocks section of this data sheet.

3.16.7.2 QSGMII DC electrical characteristics

This table describes the QSGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SDn_TXn_P and SDn_TXn_N).

Table 98. QSGMII transmitter DC electrical characteristics (XV_{DD} = 1.35 V)[1]

Parameter	Symbol	Min	Typ	Max	Unit
Output differential voltage	V_{DIFF}	400.0	-	900.0	mV
Differential resistance	T_{RD}	80.0	100.0	120.0	Ω
1. For recommended operating conditions, see Table 3.					

This table defines the QSGMII receiver DC electrical characteristics.

Table 99. QSGMII receiver DC timing specifications (SV_{DD} = 0.9 V / 1.0 V)[1]

Parameter	Symbol	Min	Typ	Max	Unit
Input differential voltage	V_{DIFF}	100.0	-	900.0	mV
Differential resistance	R_{RDIN}	80.0	100.0	120.0	Ω
1. For recommended operating conditions, see Table 3.					

3.16.7.3 QSGMII AC timing specifications

This table provides the QSGMII transmitter AC timing specifications.

Table 100. QSGMII transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Transmitter baud rate	T_{BAUD}	5.000-100ppm	5.0	5.000+100ppm	Gb/s
Uncorrelated high probability jitter	T_{UHPJ}	-	-	0.15	UI p-p
Total jitter tolerance	J_T	-	-	0.3	UI p-p

This table provides the QSGMII receiver AC timing specifications.

Table 101. QSGMII receiver AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	5.000-100ppm	5.0	5.000+100ppm	Gb/s	-
Uncorrelated bounded high probability jitter	R_{DJ}	-	-	0.15	UI p-p	-
Correlated bounded high probability jitter	R_{CBHPJ}	-	-	0.3	UI p-p	The jitter (R_{CBHPJ}) and amplitude have to be correlated, for example, by a PCB trace.
Bounded high probability jitter	R_{BHPJ}	-	-	0.45	UI p-p	-
Sinusoidal jitter, maximum	R_{SJ-max}	-	-	5.0	UI p-p	-
Sinusoidal jitter, high frequency	R_{SJ-hf}	-	-	0.05	UI p-p	-
Total jitter (does not include sinusoidal jitter)	R_{TJ}	-	-	0.6	UI p-p	-

The sinusoidal jitter may have any amplitude and frequency in the unshaded region of this figure.

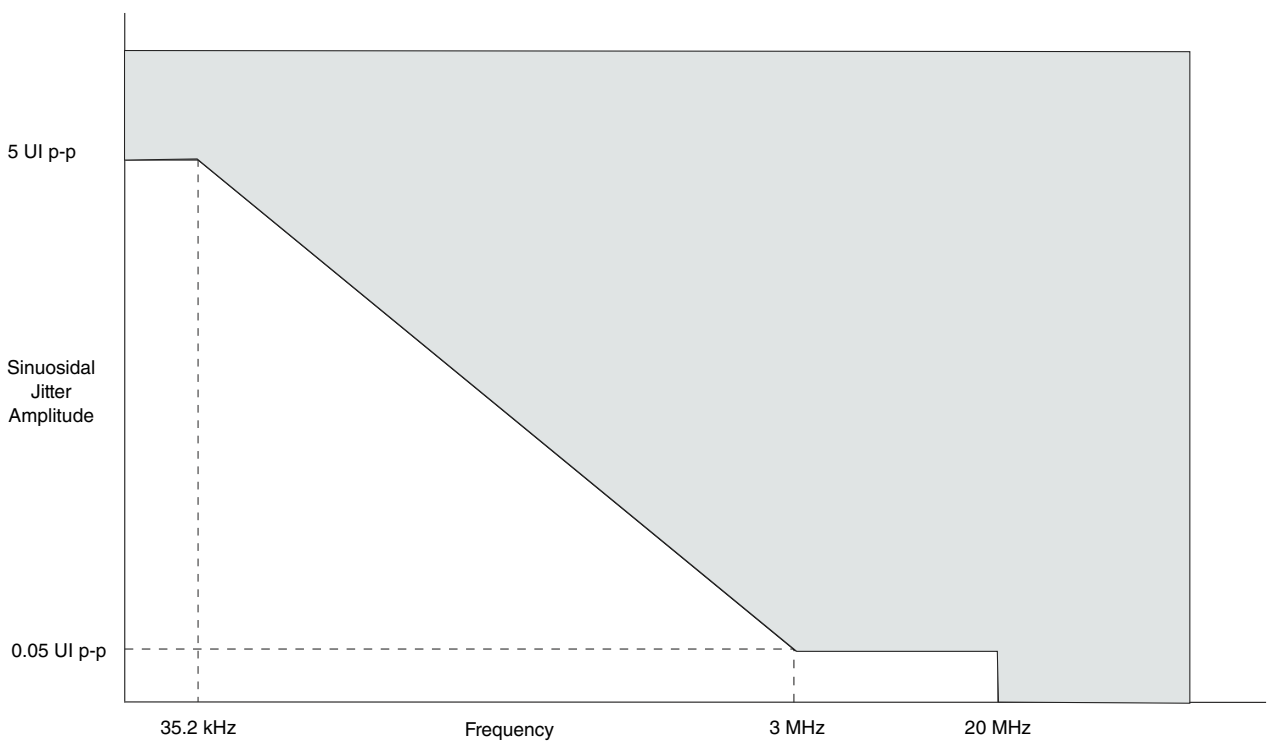


Figure 43. QSGMII single-frequency sinusoidal jitter limits

3.16.8 XFI interface

This section describes the DC and AC electrical characteristics for the XFI interface.

3.16.8.1 XFI clocking requirements for SDn_REF_CLKn_P and SDn_REF_CLKn_N

Only SerDes 1 (SD1_REF_CLK[1:2]_P and SD1_REF_CLK[1:2]_N) may be used for SerDes XFI configurations based on the RCW configuration field SRDS_PRTCL.

For more information on these specifications, see the SerDes reference clocks section of this data sheet.

3.16.8.2 XFI DC electrical characteristics

This table defines the XFI transmitter DC electrical characteristics.

Table 102. XFI transmitter DC electrical characteristics (XV_{DD} = 1.35 V)[1]

Parameter	Symbol	Min	Typ	Max	Unit
Output differential voltage	$V_{TX-DIFF}$	360.0	-	770.0	mV
De-emphasized differential output voltage (ratio at 1.14dB)	$V_{TX-DE-RATIO-1.14dB}$	0.6	1.1	1.6	dB
De-emphasized differential output voltage (ratio at 3.5dB)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB
De-emphasized differential output voltage (ratio at 4.66dB)	$V_{TX-DE-RATIO-4.66dB}$	4.1	4.6	5.1	dB
De-emphasized differential output voltage (ratio at 6.0dB)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB
De-emphasized differential output voltage (ratio at 9.5dB)	$V_{TX-DE-RATIO-9.5dB}$	9.0	9.5	10.0	dB
Differential resistance	T_{RD}	80.0	100.0	120.0	Ω
1. For recommended operating conditions, see Table 3.					

This table defines the XFI receiver DC electrical characteristics.

Table 103. XFI receiver DC electrical characteristics (SV_{DD} = 0.9 V / 1.0 V)[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential resistance	R_{RD}	80.0	100.0	120.0	Ω	-
Input differential voltage	$V_{RX-DIFF}$	110.0	-	1050.0	mV	2
1. For recommended operating conditions, see Table 3.						
2. Measured at receiver.						

3.16.8.3 XFI AC timing specifications

NOTE

The AC specifications do not include RefClk jitter.

This table defines the XFI transmitter AC timing specifications.

Table 104. XFI transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Transmitter baud Rate	T_{BAUD}	10.3125-100ppm	10.3125	10.3125+100ppm	Gb/s
Unit Interval	UI	-	96.96	-	ps
Deterministic jitter	D_J	-	-	0.15	UI p-p
Total jitter tolerance	T_J	-	-	0.3	UI p-p

This table defines the XFI receiver AC timing specifications. RefClk jitter is not included.

Table 105. XFI receiver AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	-	96.96	-	ps	-
Receiver baud rate	R_{BAUD}	10.3125-100ppm	10.3125	10.3125+100ppm	Gb/s	-
Total non-EQJ jitter	$T_{NON-EQJ}$	-	-	0.45	UI p-p	1
Total jitter tolerance	T_J	-	-	0.65	UI p-p	1, 2

1. The total jitter (TJ) consists of Random Jitter (RJ), Duty Cycle Distortion (DCD), Periodic Jitter (PJ), and Inter-Symbol Interference (ISI). Non-EQJ jitter can include duty cycle distortion (DCD), random jitter (RJ), and periodic jitter (PJ). Non-EQJ jitter is uncorrelated to the primary data stream with exception of the DCD and so cannot be equalized by the receiver under test. It can exhibit a wide spectrum. Non - EQJ = TJ - ISI = RJ + DCD + PJ.

2. The XFI channel has a loss budget of 9.6 dB @5.5GHz. The channel loss including connector @ 5.5GHz is 6dB. The channel crosstalk and reflection margin is 3.6dB. Manual tuning of TX Equalization and amplitude will be required for performance optimization.

This figure shows the sinusoidal jitter tolerance of XFI receiver.

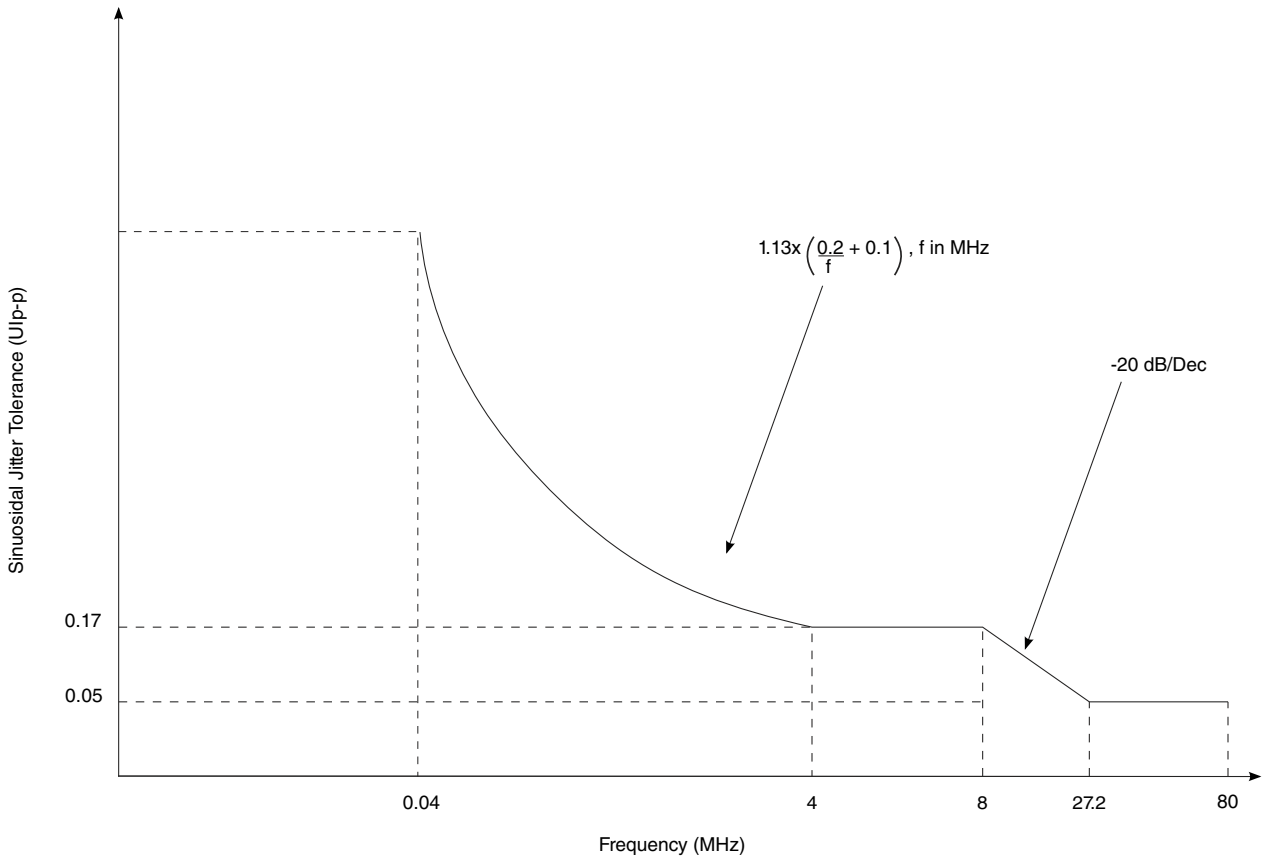


Figure 44. XFI host receiver input sinusoidal jitter tolerance

3.16.9 1000Base-KX interface

This section describes the electrical characteristics for the 1000Base-KX interface. Only AC-coupled operation is supported.

3.16.9.1 1000Base-KX DC electrical characteristics

This table describes the 1000Base-KX SerDes transmitter DC electrical characteristics at TP1 per IEEE Std 802.3ap-2007. Transmitter DC electrical characteristics are measured at the transmitter outputs (SDn_TXn_P and SDn_TXn_N).

Table 106. 1000Base-KX transmitter DC electrical characteristics[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output differential voltage	$V_{TX-DIFFp-p}$	800.0	-	1600.0	mV	2

Table continues on the next page...

Table 106. 1000Base-KX transmitter DC electrical characteristics[1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential resistance	T_{RD}	80.0	100.0	120.0	Ω	-
1. For recommended operating conditions, see Table 3. 2. SRDSxLNmTECR0[AMP_RED]=00_0000						

This table provides the 1000Base-KX receiver DC electrical characteristics.

Table 107. 1000Base-KX receiver DC electrical characteristics[1]

Parameter	Symbol	Min	Max	Unit
Input differential voltage	$V_{RX-DIFFp-p}$	-	1600.0	mV
Differential resistance	T_{RDIN}	80.0	120.0	Ω
1. For recommended operating conditions, see Table 3.				

3.16.9.2 1000Base-KX AC timing specifications

NOTE

The AC specifications do not include RefClk jitter.

This table provides the 1000Base-KX transmitter AC timing specifications.

Table 108. 1000Base-KX transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Baud rate	T_{BAUD}	1.25-100ppm	1.25	1.25+100ppm	Gb/s	-
Uncorrelated high probability jitter/Random Jitter	T_{UHPJ} / T_{RJ}	-	-	0.15	UI p-p	-
Deterministic jitter tolerance	T_{DJ}	-	-	0.1	UI p-p	-
Total jitter tolerance	T_{TJ}	-	-	0.25	UI p-p	Total jitter is specified at a BER of 10^{-12}.

This table provides the 1000Base-KX receiver AC timing specifications, which are based on the parameters defined in IEEE Std 802.3ap-2007.

Table 109. 1000Base-KX receiver AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Baud rate	R_{BAUD}	1.25-100ppm	1.25	1.25+100ppm	Gb/s	-

Table continues on the next page...

Table 109. 1000Base-KX receiver AC timing specifications (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Total jitter tolerance	R_{TJ}	-	-	Per IEEE 802.3ap-clause 70.	UI p-p	The receiver interference tolerance level of this parameter shall be measured as described in Annex 69A of the IEEE Std 802.3ap-2007.
Random jitter	R_{RJ}	-	-	0.15	UI p-p	Random jitter is specified at a BER of 10^{-12}.
Sinusoidal jitter (maximum)	R_{SJ-max}	-	-	0.1	UI p-p	The receiver interference tolerance level of this parameter shall be measured as described in Annex 69A of the IEEE Std 802.3ap-2007.

3.16.10 10GBase-KR interface

This section describes the clocking requirements as well as the DC and AC electrical characteristics for the 10GBase-KR interface.

3.16.10.1 10GBase-KR clocking requirements for SDn_REF_CLKn_P and SDn_REF_CLKn_N

Only SerDes 1 (SD1_REF_CLK[1:2]_P and SD1_REF_CLK[1:2]_N) may be used for SerDes 10GBase-KR configurations based on the RCW configuration field SRDS_PRTCL.

For more information on these specifications, see the SerDes reference clocks section of this data sheet.

3.16.10.2 10GBase-KR DC electrical characteristics

This table provides the 10GBase-KR transmitter DC electrical characteristics.

Table 110. 10GBase-KR transmitter DC electrical characteristics (SV_{DD} = 0.9 / 1.0 V)[1]

Parameter	Symbol	Min	Typ	Max	Unit
Output differential voltage	$V_{TX-DIFF}$	800.0	-	1200.0	mV
De-emphasized differential output voltage (ratio at 1.14dB)	$V_{TX-DE-RATIO-1.14dB}$	0.6	1.1	1.6	dB
De-emphasized differential output voltage (ratio at 3.5dB)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB
De-emphasized differential output voltage (ratio at 4.66dB)	$V_{TX-DE-RATIO-4.66dB}$	4.1	4.6	5.1	dB
De-emphasized differential output voltage (ratio at 6.0dB)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB
De-emphasized differential output voltage (ratio at 9.5dB)	$V_{TX-DE-RATIO-9.5dB}$	9.0	9.5	10.0	dB
Differential resistance	T_{RD}	80.0	100.0	120.0	Ω
1. For recommended operating conditions, see Table 3.					

This table provides the 10GBase-KR receiver DC electrical characteristics.

Table 111. 10GBase-KR receiver DC electrical characteristics (XV_{DD} = 1.35 V or 1.5 V)[1]

Parameter	Symbol	Min	Typ	Max	Unit
Input differential voltage	$V_{RX-DIFF}$	-	-	1200.0	mV
Differential resistance	R_{RD}	80.0	-	120.0	Ω
1. For recommended operating conditions, see Table 3.					

3.16.10.3 10GBase-KR AC timing specifications

NOTE

The AC specifications do not include RefClk jitter.

This table provides the 10GBase-KR transmitter AC timing specifications.

Table 112. 10GBase-KR transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Transmitter baud rate	T_{BAUD}	10.3125-100ppm	10.3125	10.3125+100ppm	Gb/s
Uncorrelated high probability jitter/ Random Jitter	T_{UHPJ}/T_{RJ}	-	-	0.15	UI p-p
Deterministic jitter tolerance	T_{DJ}	-	-	0.15	UI p-p
Total jitter tolerance	T_{TJ}	-	-	0.3	UI p-p

This table provides the 10GBase-KR receiver AC timing specifications.

Table 113. 10GBase-KR receiver AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Receiver baud rate	R_{BAUD}	10.3125-100ppm	10.3125	10.3125+100ppm	Gb/s
Total jitter tolerance	R_{TJ}	-	-	Per IEEE Std 802.3ap-2007, Annex 69a.	UI p-p
Random jitter	R_{RJ}	-	-	0.13	UI p-p
Sinusoidal jitter (maximum)	R_{SJ-max}	-	-	0.115	UI p-p
Duty cycle distortion	D_{CD}	-	-	0.035	UI p-p

3.17 I²C interface

This section describes the DC and AC electrical characteristics for the I²C interface.

3.17.1 I²C DC electrical characteristics

This table provides the DC electrical characteristics for the I²C interface when operating at DV_{DD} = 3.3 V.

Table 114. I²C DC electrical characteristics (DV_{DD} = 3.3 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.2 x DV_{DD}	V	2
Output low voltage (DV_{DD} = min, IOL = 3 mA, DV_{DD} > 2V)	V_{OL}	-	0.4	V	3
Pulse width of spikes that must be suppressed by the input filter	t_{I2KHKL}	0.0	50.0	ns	4
Input current each I/O pin (input voltage is between 0.1 x DV_{DD} (min) and 0.9 x DV_{DD} (max))	I_I	-50.0	50.0	µA	5
Capacitance for each I/O pin	C_I	-	10.0	pF	-

1. For recommended operating conditions, see Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 3.
3. The output voltage (open drain or open collector) condition = 3 mA sink current.
4. See the chip reference manual for information about the digital filter used.
5. I/O pins obstruct the SDA and SCL lines if DV_{DD} is switched off.

This table provides the DC electrical characteristics for the I^2C interface operating at DV_{DD} = 1.8 V.

Table 115. I^2C DC electrical characteristics (DV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x DV_{DD}	V	2
Output low voltage (DV_{DD} = min, IOL = 3 mA, $DV_{DD} \le 2V$)	V_{OL}	0.0	0.36	V	3
Pulse width of spikes that must be suppressed by the input filter	t_{I2KHKL}	0.0	50.0	ns	4
Input current each I/O pin (input voltage is between 0.1 x DV_{DD} (min) and 0.9 x DV_{DD} (max))	I_I	-50.0	50.0	µA	5
Capacitance for each I/O pin	C_I	-	10.0	pF	-

1. For recommended operating conditions, see Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 3.
3. The output voltage (open drain or open collector) condition = 3 mA sink current.
4. See the chip reference manual for information about the digital filter used.
5. I/O pins obstruct the SDA and SCL lines if DV_{DD} is switched off.

3.17.2 I^2C AC timing specifications

This table provides the AC timing specifications for the I^2C interface.

Table 116. I^2C AC timing specifications[1]

Parameter	Symbol	Min	Max	Unit	Notes
SCL clock frequency	f_{I2C}	0.0	400.0	kHz	-
Low period of the SCL clock	t_{I2CL}	1.3	-	µs	-
High period of the SCL clock	t_{I2CH}	0.6	-	µs	-
Setup time for a repeated START condition	t_{I2SVKH}	0.6	-	µs	-
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	-	µs	-
Data setup time	t_{I2DVKH}	100.0	-	ns	-
Data input hold time (CBUS compatible masters, I^2C bus devices)	t_{I2DXKL}	0.0	-	µs	As a transmitter, the chip provides a delay time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation

Table continues on the next page...

Table 116. I²C AC timing specifications[1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
					of a START or STOP condition. When the chip acts as the I²C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the chip does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern.
Data output delay time	t_{I2OVKL}	-	0.9	µs	The maximum t_{I2OVKL} has to be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
Setup time for STOP condition	t_{I2PVKH}	0.6	-	µs	-
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	-	µs	-
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 x DVDD	-	V	-
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 x DVDD	-	V	-
Capacitive load for each bus line	Cb	-	400.0	pF	-

1.The symbols used for timing specifications herein follow these patterns: $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I2C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the tI2C clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I2C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the tI2C clock reference (K) going to the low (L) state or hold time. Also, tI2PVKH symbolizes I2C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the tI2C clock reference (K) going to the high (H) state or setup time.

This figure shows the AC test load for the I²C interface.

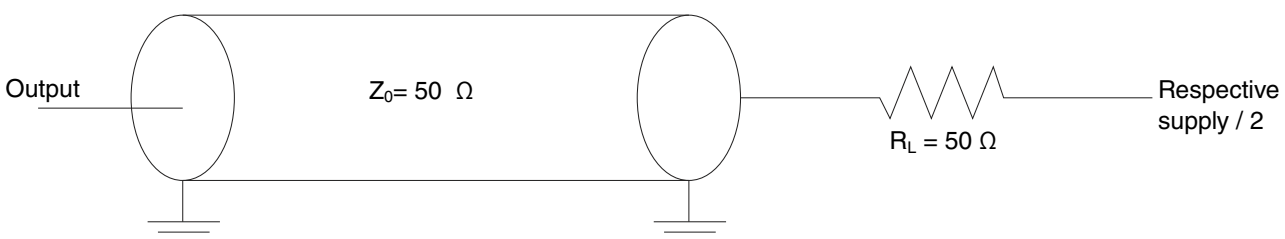


Figure 45. I²C AC test load

This figure shows the AC timing diagram for the I²C interface.

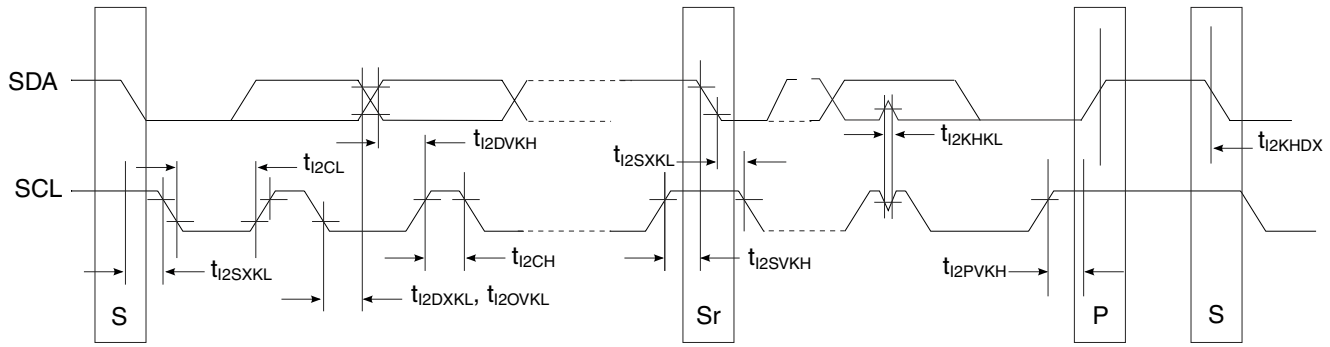


Figure 46. I²C bus AC timing diagram

3.18 Integrated Flash Controller

This section describes the DC and AC electrical specifications for the integrated flash controller.

3.18.1 Integrated Flash Controller DC electrical characteristics

Table below provides the DC electrical characteristics for the integrated flash controller when operating at OV_{DD} = 1.8 V.

Table 117. Integrated Flash Controller DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	1
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN} = OV_{DD})	I_{IN}	-	±50	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.6	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.32	V	-

NOTE:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.
3. For recommended operating conditions, see Table 3.

3.18.2 Integrated Flash Controller AC timing specifications

This section describes the AC timing specifications for the integrated flash controller.

3.18.2.1 Test condition

The figure below provides the AC test load for the integrated flash controller.

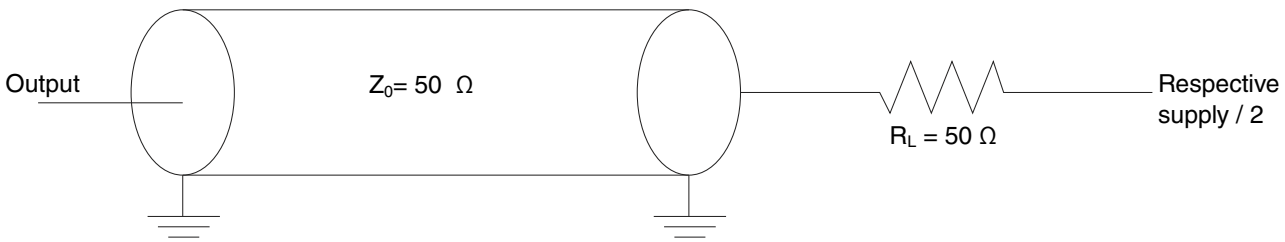


Figure 47. Integrated Flash Controller AC test load

3.18.2.2 IFC AC timing specifications (GPCM/GASIC)

The table below describes the input AC timing specifications for the IFC-GPCM and IFC-GASIC interface.

Table 118. Integrated flash controller input timing specifications for GPCM and GASIC mode (OV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input setup	$t_{IBIVKH1}$	4	-	ns	-
Input hold	$t_{IBIXKH1}$	1	-	ns	-

NOTE:

1. For recommended operating conditions, see Table 3.

The figure below shows the input AC timing diagram for the IFC-GPCM, IFC-GASIC interface.

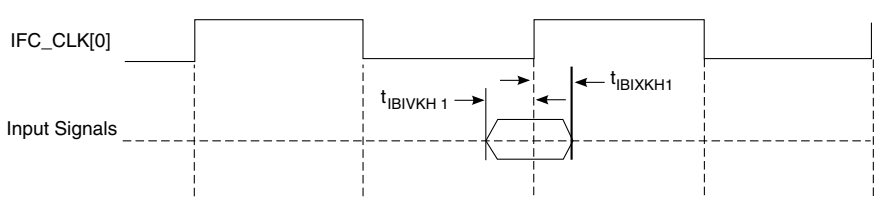


Figure 48. IFC-GPCM, IFC-GASIC input AC timing specifictions

The table below describes the output AC timing specifications for the IFC-GPCM and IFC-GASIC interfaces.

Table 119. Integrated flash controller IFC-GPCM and IFC-GASIC interface output timing specifications (OV_{DD} = 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
IFC_CLK cycle time	t_{IBK}	10	-	ns	-
IFC_CLK duty cycle	t_{IBKH}/t_{IBK}	45	55	%	-
Output delay	$t_{IBKLOV1}$	-	1.5	ns	-
Output hold	t_{IBKLOX}	-	-2	ns	1
IFC_CLK[0] to IFC_CLK[m] skew	$t_{IBKSKEW}$	0	±75	ps	-

NOTE:

1. The output hold is negative. This means that output transition happens earlier than the falling edge of IFC_CLK.
2. For recommended operating conditions, see Table 3.

The figure below shows the output AC timing diagram for the IFC-GPCM, IFC-GASIC interface.

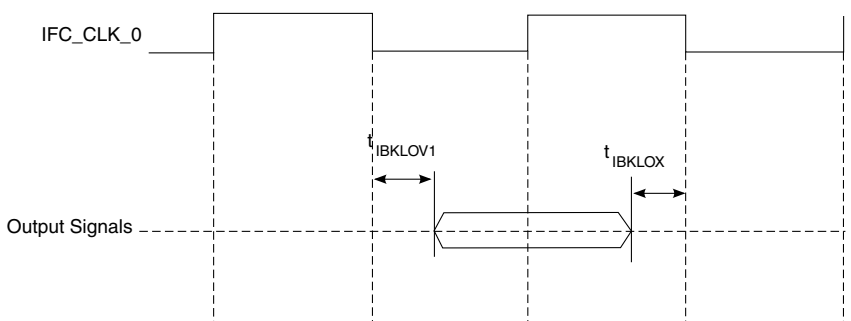


Figure 49. IFC-GPCM, IFC-GASIC signals

3.18.2.3 IFC AC timing specifications (NOR)

The table below describes the input timing specifications for the IFC-NOR interface.

Table 120. Integrated flash controller input timing specifications for NOR mode (OV_{DD} = 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
Input setup	$t_{IBIVKH2}$	$(2 \times t_{IP_CLK}) + 2$	-	ns	1
Input hold	$t_{IBIXKH2}$	$(1 \times t_{IP_CLK}) + 1$	-	ns	1

Notes:

1. t_{IP_CLK} is the period of ip clock (not the IFC_CLK) on which IFC is running.
2. For recommended operating conditions, see Table 3.

The figure below shows the AC input timing diagram for input signals for the IFC-NOR interface. Here TRAD is a programmable delay parameter. See the IFC section of the chip reference manual for more information.

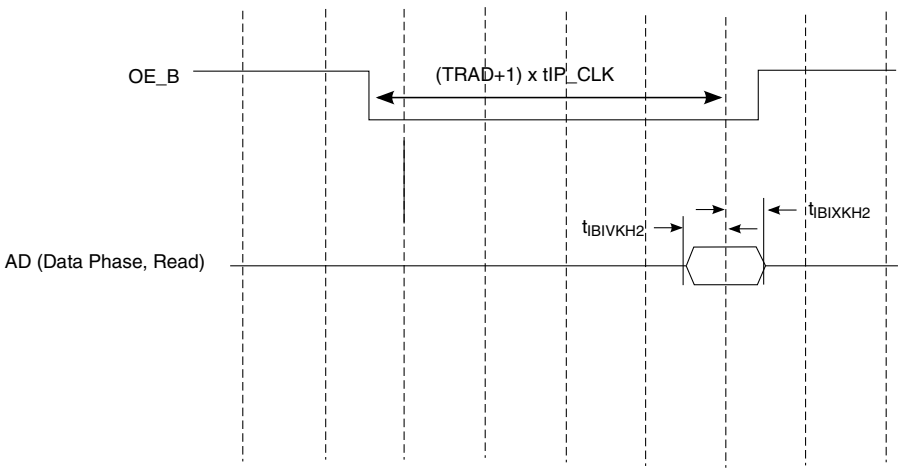


Figure 50. IFC-NOR interface input AC timings

The table below describes the output AC timing specifications of IFC-NOR interface.

Table 121. Integrated flash controller IFC-NOR interface output timing specifications (OV_{DD} = 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
Output delay	$t_{IBKLOV2}$	-	±1.5	ns	1

NOTE:

1. This effectively means that a signal change may appear anywhere within $\pm t_{IBKLOV2}$ (max) duration, from the point where it's expected to change.

2. For recommended operating conditions, see Table 3.

The figure below shows the AC timing diagram for IFC-NOR interface output signals. The timing specs have been illustrated here by taking timings between two signals, CS_B and OE_B as an example. In a read operation, OE_B is supposed to change the TACO (a programmable delay; see the IFC section of the chip reference manual for more information) time after CS_B. Because of the skew between the signals, OE_B may change anywhere within the window of time defined by tIBKLOV2. This concept applies to other IFC-NOR interface output signals as well. The diagram is an example that shows the skew between any two chronological toggling signals as per the protocol. The list of IFC-NOR output signals is as follows: NRALE, NRAVD_B, NRWE_B, NROE_B, CS_B, AD (Address phase).

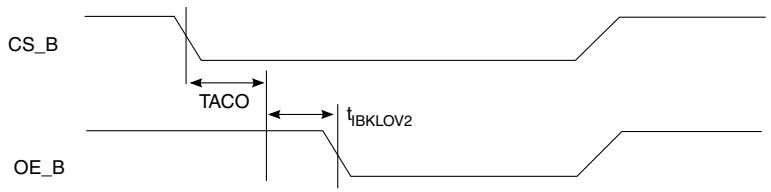


Figure 51. IFC-NOR interface output AC timings

3.18.2.4 IFC AC timing specifications (NAND)

The table below describes the input timing specifications of the IFC-NAND interface.

Table 122. Integrated flash controller input timing specifications for NAND mode (OV_{DD} = 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
Input setup	$t_{IBIVKH3}$	(2 x t_{IP_CLK}) + 2	-	ns	1
Input hold	$t_{IBIXKH3}$	1	-	ns	1
IFC_RB_B pulse width	t_{IBCH}	2	-	t_{IP_CLK}	1
NOTE: 1. t_{IP_CLK} is the period of ip clock on which IFC is running. 2. For recommended operating conditions, see Table 3.					

The figure below shows the AC input timing diagram for input signals of IFC-NAND interface. Here TRAD is a programmable delay parameter. See the IFC section of the chip reference manual for more information.

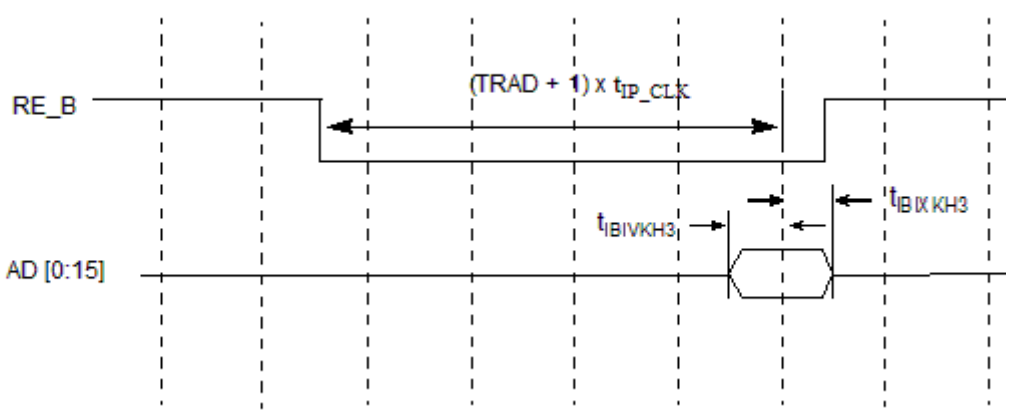


Figure 52. IFC-NAND interface input AC timings

NOTE

t_{IP_CLK} is the period of ip clock (not the IFC_CLK) on which IFC is running.

The table below describes the output AC timing specifications for the IFC-NAND interface.

Table 123. Integrated flash controller IFC-NAND interface output timing specifications (OV_{DD} = 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
Output delay	$t_{IBKLOV3}$	-	±1.5	ns	1

NOTE:

1. This effectively means that a signal change may appear anywhere within $t_{IBKLOV3}$ (min) to $t_{IBKLOV3}$ (max) duration, from the point where it's expected to change.

2. For recommended operating conditions, see Table 3.

The figure below shows the AC timing diagram for output signals of IFC-NAND interface.The timing specs are shown here by taking the timings between two signals, CS_B and CLE as an example. CLE is supposed to change TCCST (a programmable delay; see the IFC section of the chip reference manual for more information) time after CS_B. Because of the skew between the signals, CLE may change anywhere within window of time defined by $t_{IBKLOV3}$. This concept applies to other output signals of the IFC-NAND interface as well. The diagram is an example to show the skew between any two chronological toggling signals as per the protocol. The list of output signals is as follows: NDWE_B, NDRE_B, NDALE, WP_B, NDCLE, CS_B, AD.

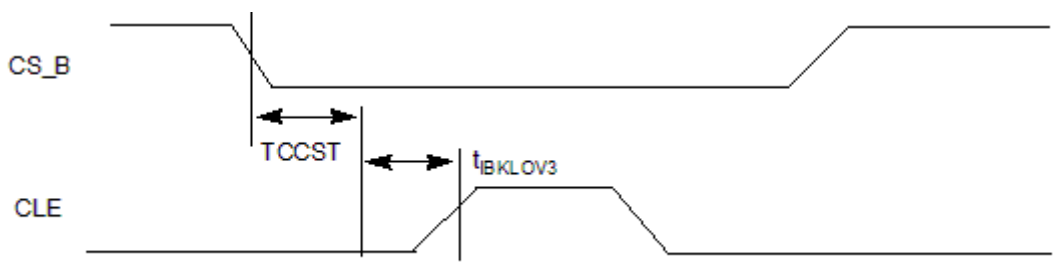


Figure 53. IFC-NAND interface output AC timings

3.18.2.5 IFC-NAND SDR AC timing specifications

This table describes the AC timing specifications for the IFC-NAND SDR interface. These specifications are compliant to the SDR mode of the ONFI specification revision 3.0.

Table 124. Integrated flash controller IFC-NAND SDR interface AC timing specifications (OVDD = 1.8 V)

Parameter	Symbol	I/O	Min	Max	Unit	Notes
Address cycle to data loading time	t_{ADL}	O	TADLE - 1500(ps)	TADLE + 1500(ps)	t_{IP_CLK}	Figure 54
ALE hold time	t_{ALH}	O	TWCHT - 1500(ps)	TWCHT + 1500(ps)	t_{IP_CLK}	Figure 55
ALE setup time	t_{ALS}	O	TWP - 1500(ps)	TWP + 1500(ps)	t_{IP_CLK}	Figure 55
ALE to RE_n delay	t_{AR}	O	TWHRE - 1500(ps)	TWHRE + 1500(ps)	t_{IP_CLK}	Figure 56
CE_n hold time	t_{CH}	O	5 + 1500(ps)	-	ns	Figure 55
CE_n high to input hi-Z	t_{CHZ}	I	TRHZ - 1500(ps)	TRHZ + 1500(ps)	t_{IP_CLK}	Figure 57
CLE hold time	t_{CLH}	O	TWCHT - 1500(ps)	TWCHT + 1500(ps)	t_{IP_CLK}	Figure 55
CLE to RE_n delay	t_{CLR}	O	TWHRE - 1500(ps)	TWHRE - 1500(ps)	t_{IP_CLK}	Figure 58
CLE setup time	t_{CLS}	O	TWP - 1500(ps)	TWP + 1500(ps)	t_{IP_CLK}	Figure 55
CE_n high to input hold	t_{COH}	I	150 - 1500(ps)	-	ns	Figure 57
CE_n setup time	t_{CS}	O	TCS - 1500(ps)	TCS + 1500(ps)	t_{IP_CLK}	Figure 55
Data hold time	t_{DH}	O	TWCHT - 1500(ps)	TWCHT + 1500(ps)	t_{IP_CLK}	Figure 55
Data setup time	t_{DS}	O	TWP - 1500(ps)	TWP + 1500(ps)	t_{IP_CLK}	Figure 55
Busy time for Set Features and Get Features	t_{FEAT}	O	-	FTOCNT	t_{IP_CLK}	Figure 59
Output hi-Z to RE_n low	t_{IR}	O	TWHRE - 1500(ps)	TWHRE + 1500(ps)	t_{IP_CLK}	Figure 60
Interface and Timing Mode Change time	t_{ITC}	O	-	FTOCNT	t_{IP_CLK}	Figure 59
RE_n cycle time	t_{RC}	O	TRP + TREH - 1500(ps)	TRP + TREH + 1500(ps)	t_{IP_CLK}	Figure 57
RE_n access time	t_{REA}	I	-	(TRAD - 1) + 2(ns)	t_{IP_CLK}	Figure 57
RE_n high hold time	t_{REH}	I	TREH	TREH	t_{IP_CLK}	Figure 57
RE_n high to input hold	t_{RHOH}	I	0	-	ns	Figure 57
RE_n high to WE_n low	t_{RHW}	O	100 + 1500(ps)	-	ns	Figure 61
RE_n high to input hi-Z	t_{RHZ}	I	TRHZ - 1500(ps)	TRHZ + 1500(ps)	t_{IP_CLK}	Figure 57
RE_n low to input data hold	t_{RLOH}	I	0	-	ns	Figure 62
RE_n pulse width	t_{RP}	O	TRP	TRP	t_{IP_CLK}	Figure 57
Ready to data input cycle (data only)	t_{RR}	O	TRR - 1500(ps)	TRR + 1500(ps)	t_{IP_CLK}	Figure 57

Table continues on the next page...

Table 124. Integrated flash controller IFC-NAND SDR interface AC timing specifications (OVDD = 1.8 V) (continued)

Parameter	Symbol	I/O	Min	Max	Unit	Notes
Device reset time, measured from the falling edge of R/B_n to the rising edge of R/B_n.	t_{RST} (raw NAND)	O	-	FTOCNT	t_{IP_CLK}	Figure 63
Device reset time, measured from the falling edge of R/B_n to the rising edge of R/B_n.	t_{RST2} (EZ NAND)	O	-	FTOCNT	t_{IP_CLK}	Figure 63
(WE_n high or CLK rising edge) to SR[6] low	t_{WB}	O	TWBE + TWH - 1500(ps)	TWBE + TWH + 1500(ps)	t_{IP_CLK}	Figure 55
WE_n cycle time	t_{WC}	O	TWP + TWH	TWP + TWH	t_{IP_CLK}	Figure 64
WE_n high hold time	t_{WH}	O	TWH	TWH	t_{IP_CLK}	Figure 64
Command, address, or data input cycle to data output cycle	t_{WHR}	O	TWHRE + TWH - 1500(ps)	TWHRE + TWH + 1500(ps)	t_{IP_CLK}	Figure 65
WE_n pulse width	t_{WP}	O	TWP	TWP	t_{IP_CLK}	Figure 55
WP_n transition to command cycle	t_{WW}	O	TWW - 1500(ps)	TWW + 1500(ps)	t_{IP_CLK}	Figure 66
Data Input hold	$t_{IBIXKH4}$	I	1	-	t_{IP_CLK}	Figure 67

NOTE:

1. t_{IP_CLK} is the clock period of the IP clock (on which the IFC IP is running). Note that that the IFC IP clock does not come out of the device.

This figure shows the t_{ADL} timing.

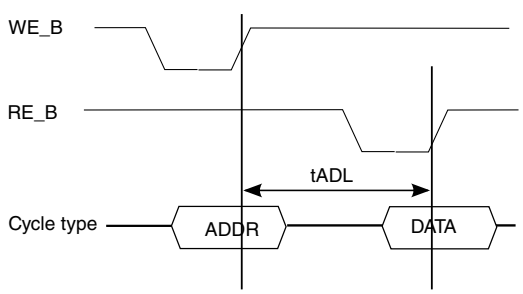


Figure 54. t_{ADL} timing

This figure shows the command cycle.

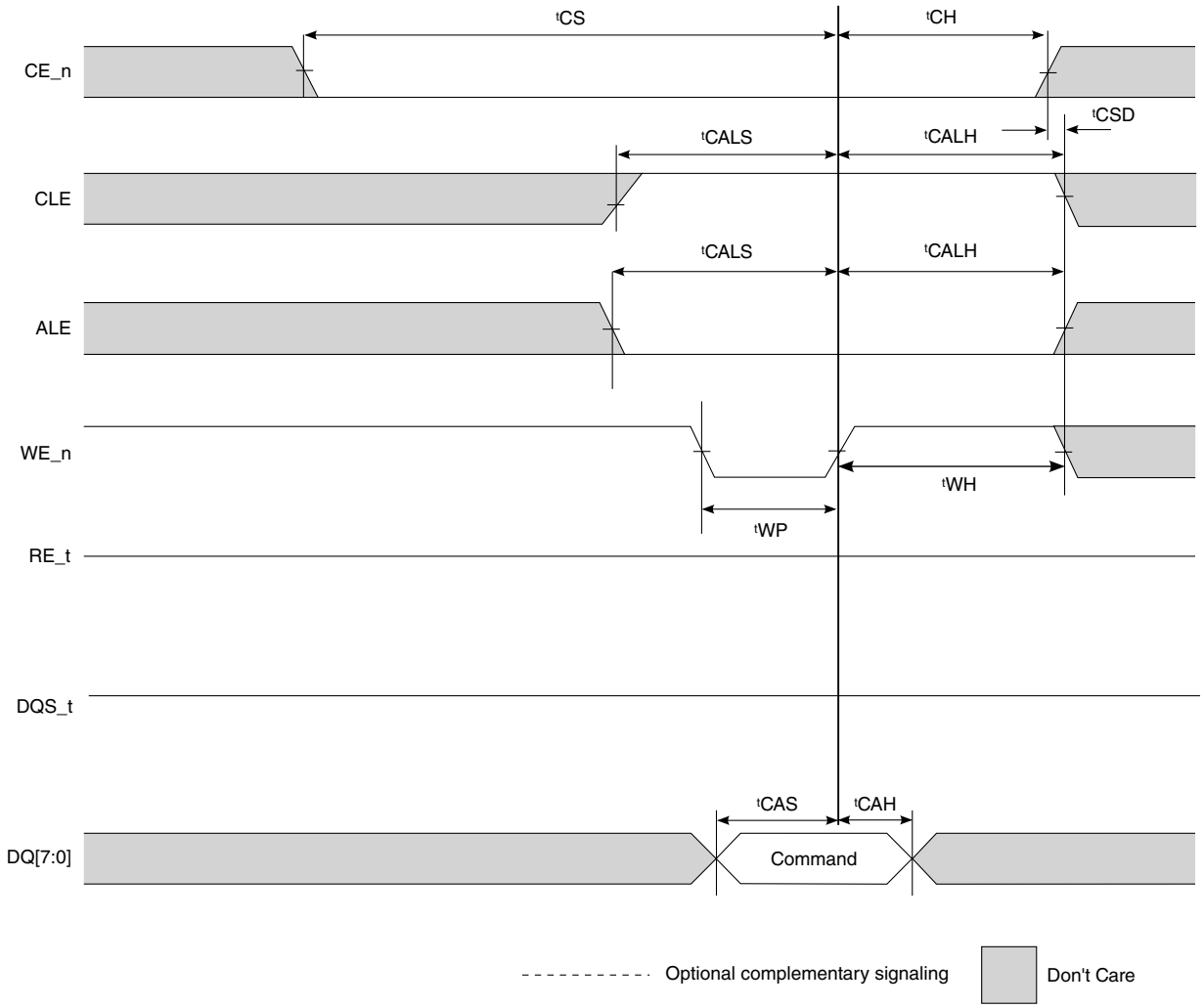


Figure 55. Command cycle

This figure shows the t_{AR} timings.

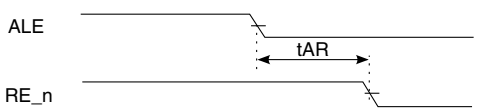


Figure 56. t_{AR} timings

This figure shows the data input cycle timings.

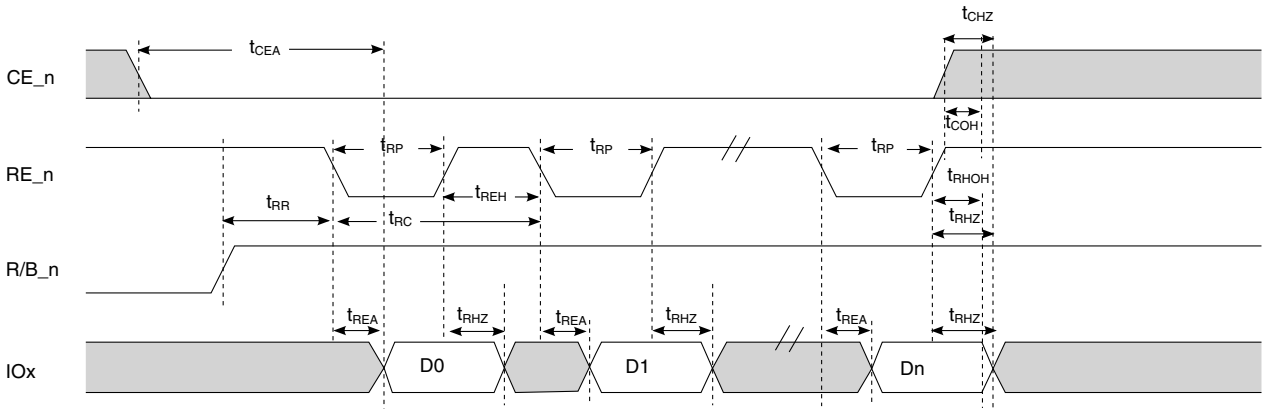


Figure 57. Data input cycle timings

This figure shows the t_{CLR} timings.

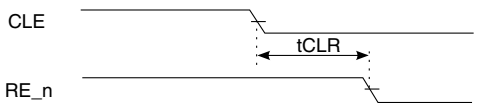


Figure 58. t_{CLR} timings

This figure shows the t_{WB}, t_{FEAT}, t_{ITC}, and t_{RR} timings.

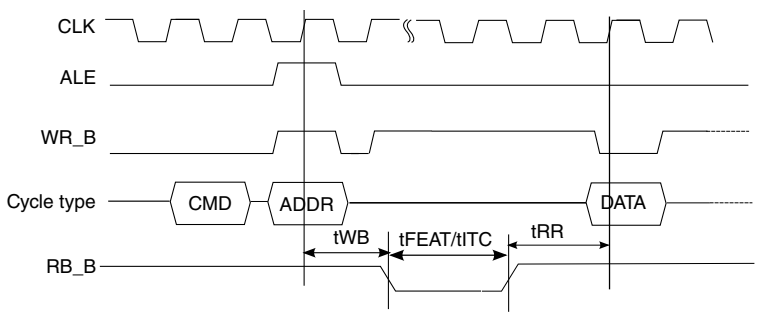


Figure 59. t_{WB}, t_{FEAT}, t_{ITC}, and t_{RR} timings

This figure shows the read status timings.

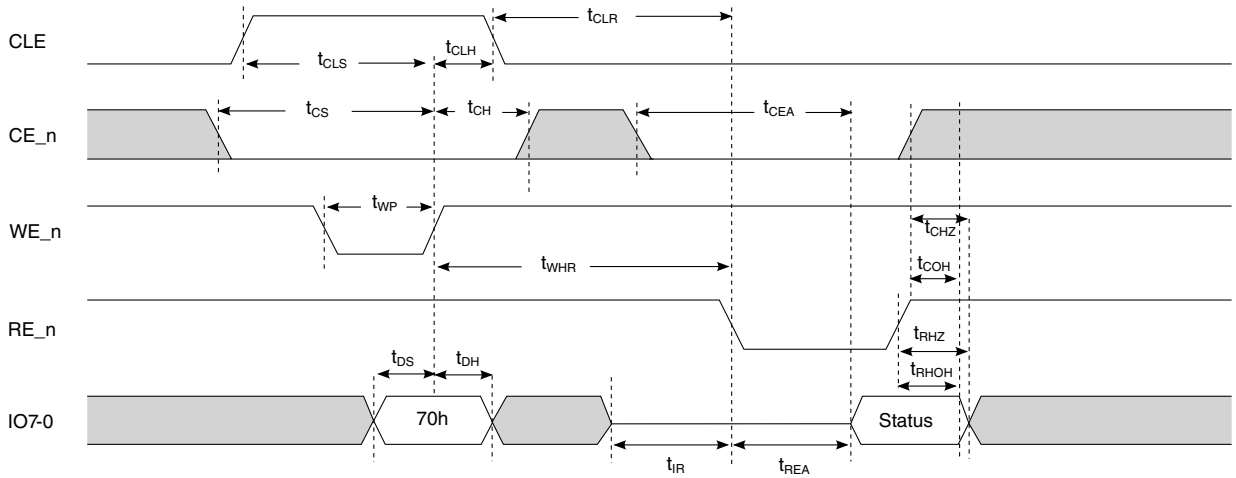


Figure 60. Read status timings

This figure shows the t_{RHW} timings.

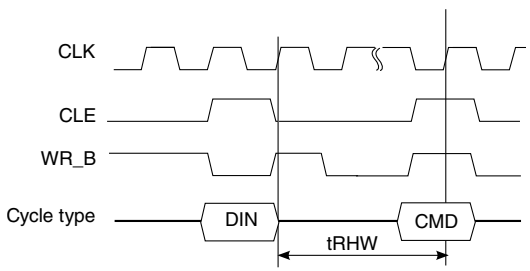


Figure 61. t_{RHW} timings

This figure shows the EDO mode data input cycle timings.

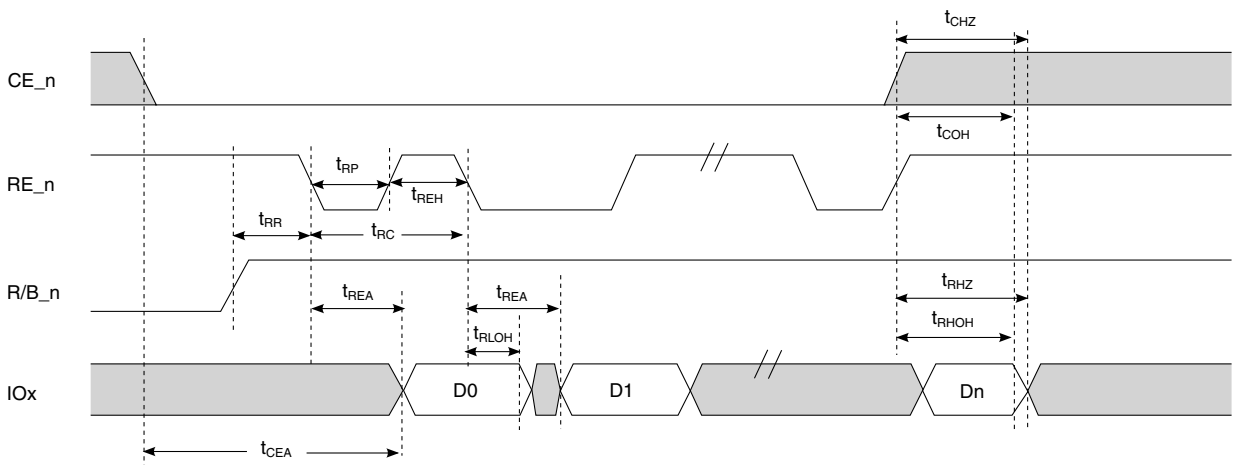


Figure 62. EDO mode data input cycle timings

This figure shows the t_{WB} and t_{RST} timings.

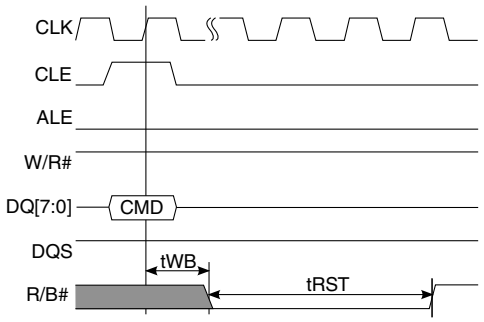


Figure 63. t_{WB} and t_{RST} timings

This figure shows the address latch timings.

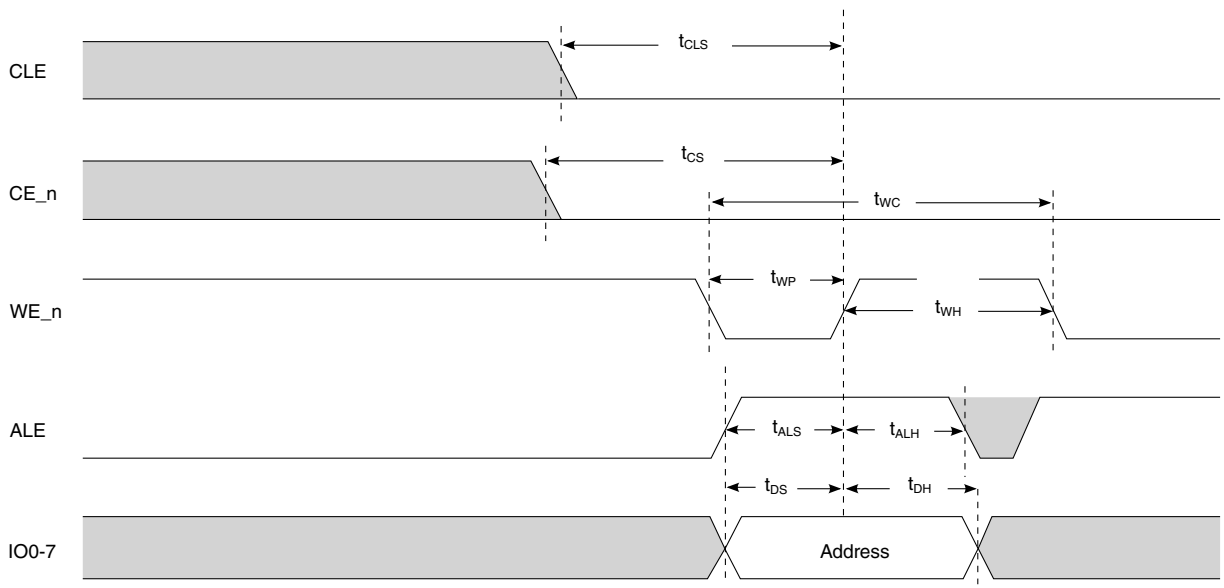


Figure 64. Address latch timings

This figure shows the t_{WHR} timings.

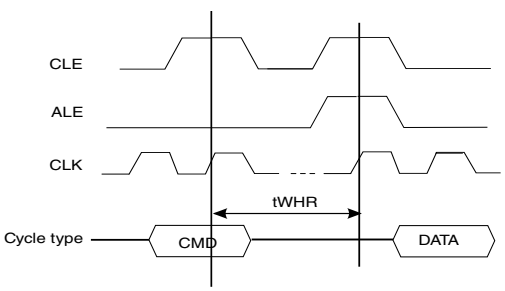


Figure 65. t_{WHR} timings

This figure shows the t_{WW} timings.

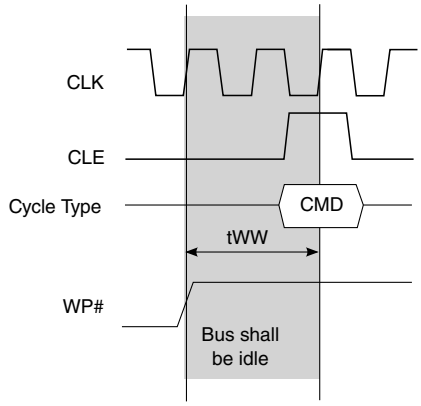


Figure 66. t_{WW} timings

This figure shows the $t_{IBIXKH4}$ timings.

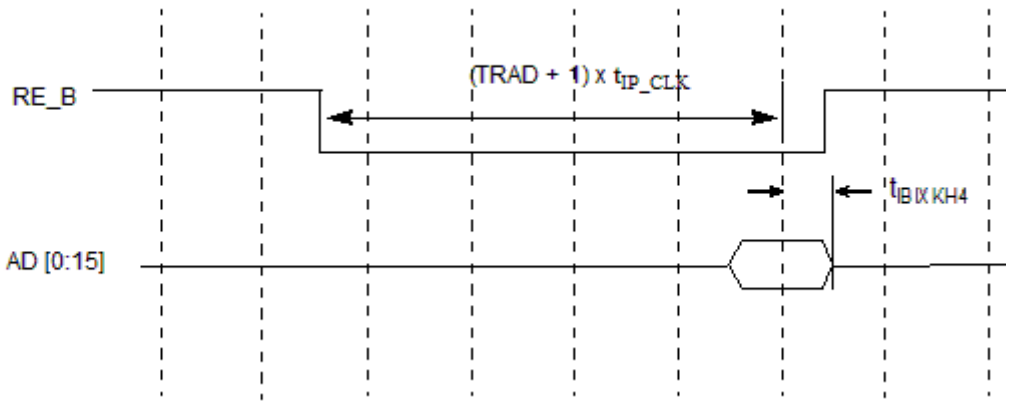


Figure 67. $t_{IBIXKH4}$ timings

3.18.2.6 IFC-NAND NVDDR AC timing specification

The table below describes the AC timing specifications for the IFC-NAND NVDDR interface. These specifications are compliant to NVDDR mode of ONFI specification revision 3.0.

Table 125. Integrated flash controller IFC-NAND NVDDR interface AC timing specifications (OVDD = 1.8 V)

Parameter	Symbol	I/O	Min	Max	Unit	Notes
Access window of DQ[7:0] from CLK	t_{AC}	I	3 - 150 (ps)	20 + 150 (ps)	ns	Figure 71
Address cycle to data loading time	t_{ADL}	I	TADL	-	t_{IP_CLK}	Figure 72

Table continues on the next page...

Table 125. Integrated flash controller IFC-NAND NVDDR interface AC timing specifications (OVDD = 1.8 V) (continued)

Parameter	Symbol	I/O	Min	Max	Unit	Notes
Command, Address, Data delay (command to command, address to address, command to address, address to command, command/ address to start of data) Fast	tCADf	O	TCAD - 150 (ps)	TCAD + 150 (ps)	t_{IP_CLK}	Figure 68
Command, Address, Data delay (command to command, address to address, command to address, address to command, command/ address to start of data) slow	tCADs	O	TCAD - 150 (ps)	TCAD + 150 (ps)	t_{IP_CLK}	Figure 68
Command/address DQ hold time	t_{CAH}	O	2 + 150 (ps)	-	ns	Figure 68
CLE and ALE hold time	t_{CALH}	O	2 + 150 (ps)	-	ns	Figure 68
CLE and ALE setup time	t_{CALS}	O	2 + 150 (ps)	-	ns	Figure 68
Command/address DQ setup time	t_{CAS}	O	2 + 150 (ps)	-	ns	Figure 68
CE# hold time	t_{CH}	O	2 + 150 (ps)	-	ns	Figure 68
Average clock cycle time, also known as tCK	t_{CK}(avg) or t_{CK}	O	10	-	ns	Figure 68
Absolute clock period, measured from rising edge to the next consecutive rising edge	t_{CK}(abs)	O	tCK(avg) + tJIT(per) min	tCK(avg) + tJIT(per) max	ns	Figure 68
Clock cycle high	t_{CKH}(abs)	O	0.45	0.55	tCK	Figure 68
Clock cycle low	t_{CKL}(abs)	O	0.45	0.55	tCK	Figure 68
Data input end to W/R# high B16	t_{CKWR}	O	TCKWR - 150 (ps)	TCKWR + 150 (ps)	t_{IP_CLK}	Figure 71
CE# setup time	t_{CS}	O	TCS - 150 (ps)	TCS + 150 (ps)	t_{IP_CLK}	Figure 70
Data DQ hold time	t_{DH}	O	1050	-	ps	Figure 70
Access window of DQS from CLK	t_{DQSCK}	I	-	20 + 150 (ps)	ns	Figure 71
W/R# low to DQS/DQ driven by device	t_{DQSD}	I	-150 (ps)	18 + 150 (ps)	ns	Figure 71
DQS output high pulse width	t_{DQSH}	O	0.45	0.55	tCK	Figure 70
W/R# high to DQS/DQ tri-state by device	t_{DQSHZ}	O	RHZ - 150 (ps)	RHZ + 150 (ps)	t_{IP_CLK}	Figure 68
DQS output low pulse width	t_{DQSL}	O	0.45	0.55	tCK	Figure 70

Table continues on the next page...

Table 125. Integrated flash controller IFC-NAND NVDDR interface AC timing specifications (OVDD = 1.8 V) (continued)

Parameter	Symbol	I/O	Min	Max	Unit	Notes
DQS-DQ skew, DQS to last DQ valid, per access	t_{DQSQ}	I	-	1000	ps	Figure 71
Data output to first DQS latching transition	t_{DQSS}	O	0.75 + 150 (ps)	1.25 - 150 (ps)	tCK	Figure 70
Data DQ setup time	t_{DS}	O	1050	-	ps	Figure 70
DQS falling edge to CLK rising - hold time	t_{DSH}	O	0.2 + 150 (ps)	-	tCK	Figure 70
DQS falling edge to CLK rising - setup time	t_{DSS}	O	0.2 + 150 (ps)	-	tCK	Figure 70
Input data valid window	t_{DVW}	I	tDVW = tQH - tDQSQ	-	ns	Figure 71
Busy time for Set Features and Get Features	t_{FEAT}	I	-	FTOCNT	t_{IP_CLK}	Figure 73
Half-clock period	t_{HP}	O	tHP = min(tCKL, tCKH)	-	ns	Figure 71
Interface and Timing Mode Change time	t_{ITC}	I	-	FTOCNT	t_{IP_CLK}	Figure 73
The deviation of a given tCK(abs) from tCK(avg)	t_{JIT}(per)	O	-0.5	0.5	ns	NA
DQ-DQS hold, DQS to first DQ to go non-valid, per access	t_{QH}	I	tQH = tHP - tQHS	-	t_{IP_CLK}	Figure 71
Data hold skew factor	tQHS	I	-	1+150 (ps)		-
Data input cycle to command, address, or data output cycle	t_{RHW}	O	TRHW	-	t_{IP_CLK}	Figure 74
Ready to data input cycle (data only)	t_{RR}	I	TRR	-	t_{IP_CLK}	Figure 73
Device reset time, measured from the falling edge of R/B# to the rising edge of R/B#.	t_{RST} (raw NAND)	O	FTOCNT	FTOCNT	t_{IP_CLK}	Figure 75
Device reset time, measured from the falling edge of R/B# to the rising edge of R/B#.	t_{RST2} (EZ NAND)	O	FTOCNT	FTOCNT	t_{IP_CLK}	Figure 75
CLK rising edge to SR[6] low	t_{WB}	O	TWB - 150 (ps)	TWB + 150 (ps)	t_{IP_CLK}	Figure 75
Command, address or data output cycle to data input cycle	t_{WHR}	O	TWHR	-	t_{IP_CLK}	Figure 76
DQS write preamble	t_{WPRE}	O	1.5	-	tCK	Figure 70
DQS write postamble	t_{WPST}	O	1.5	-	tCK	Figure 70
W/R# low to data input cycle	t_{WRCK}	I	TWRCK - 150 (ps)	TWRCK + 150 (ps)	t_{IP_CLK}	Figure 71

Table continues on the next page...

Table 125. Integrated flash controller IFC-NAND NVDDR interface AC timing specifications (OVDD = 1.8 V) (continued)

Parameter	Symbol	I/O	Min	Max	Unit	Notes
WP# transition to command cycle	t_{WW}	O	TWW - 150 (ps)	TWW + 150 (ps)	t_{IP_CLK}	Figure 77

NOTE:

1. t_{IP_CLK} is the clock period of IP clock (on which IFC IP is running). Note that that the IFC IP clcok doesn't come out of device.

The following diagrams show the AC timing for the IFC-NAND NVDDR interface.

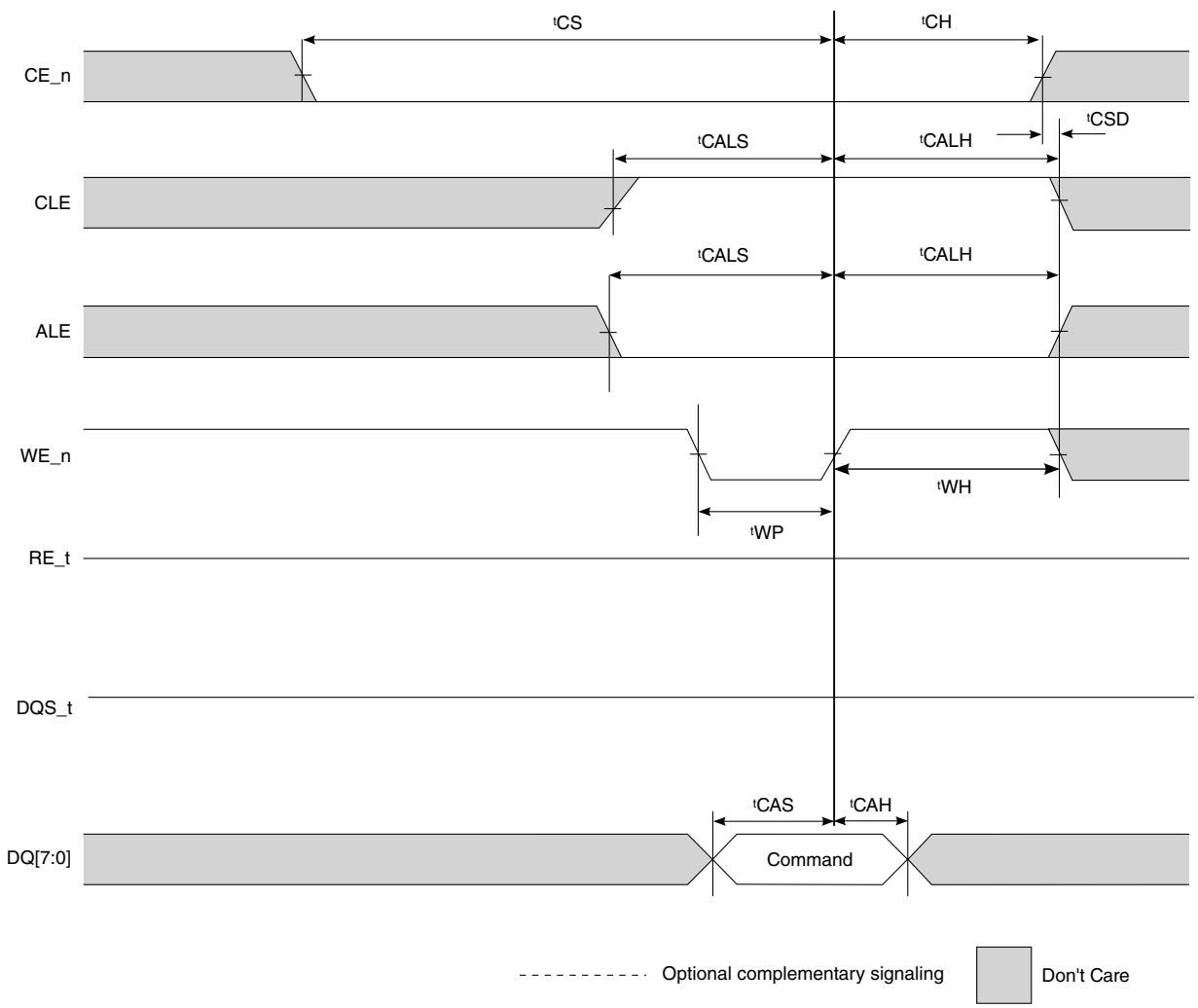


Figure 68. Command cycle

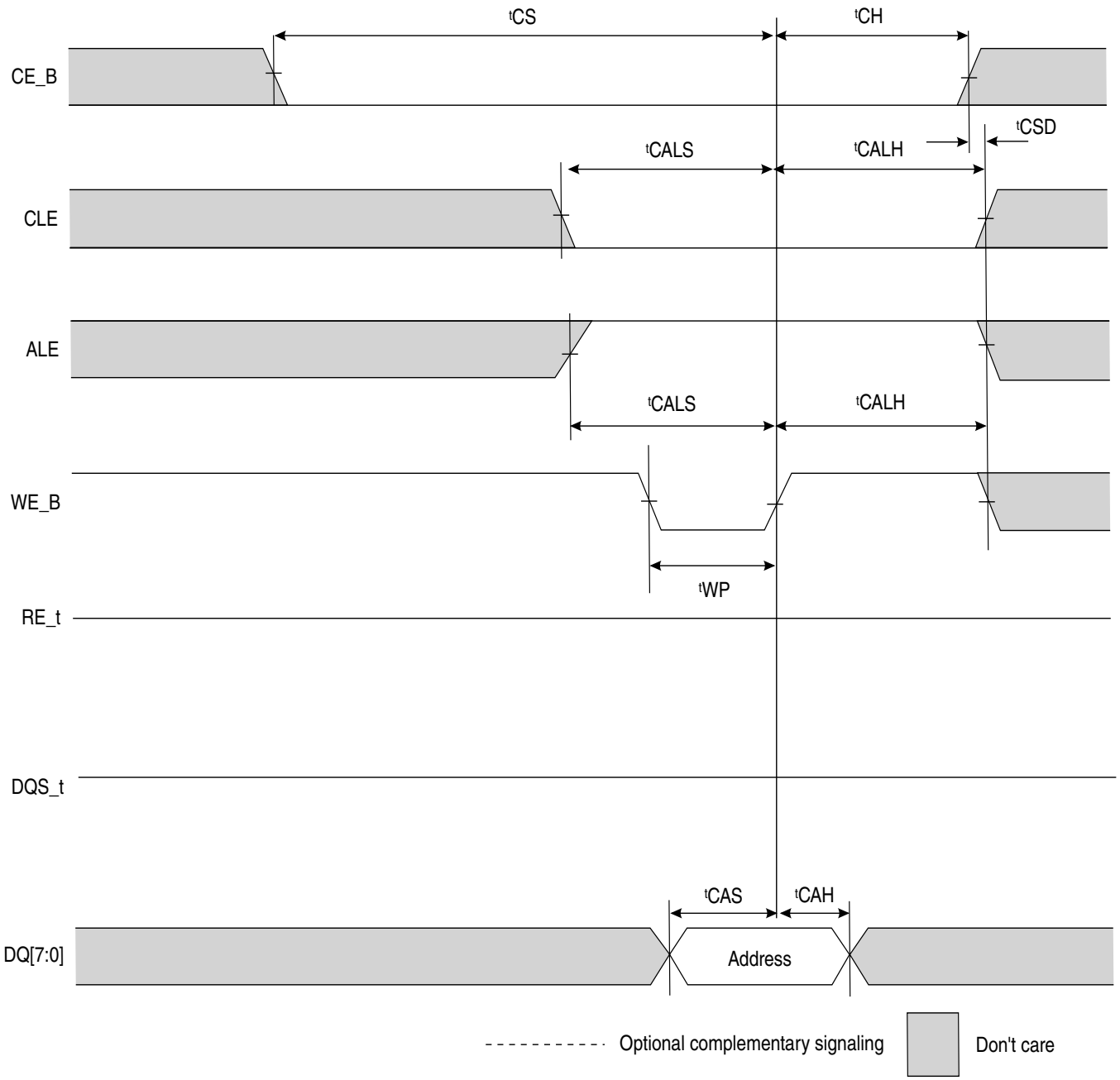


Figure 69. Address cycle

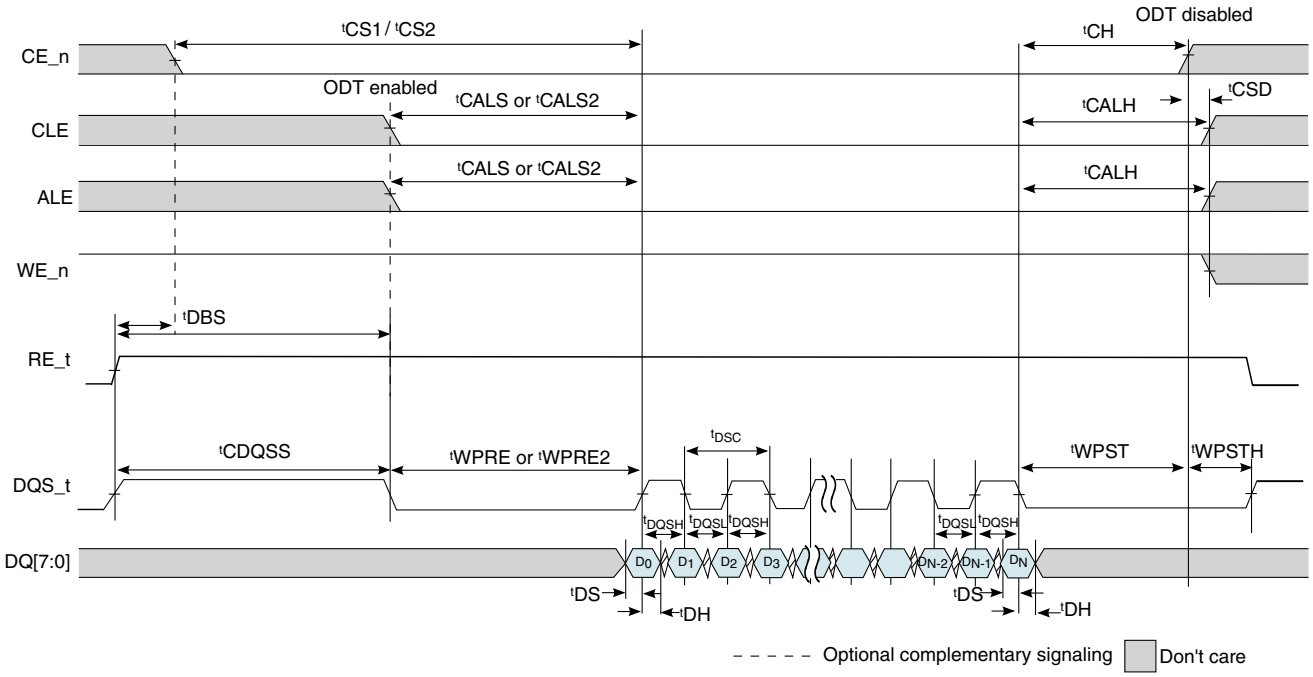


Figure 70. Write cycle

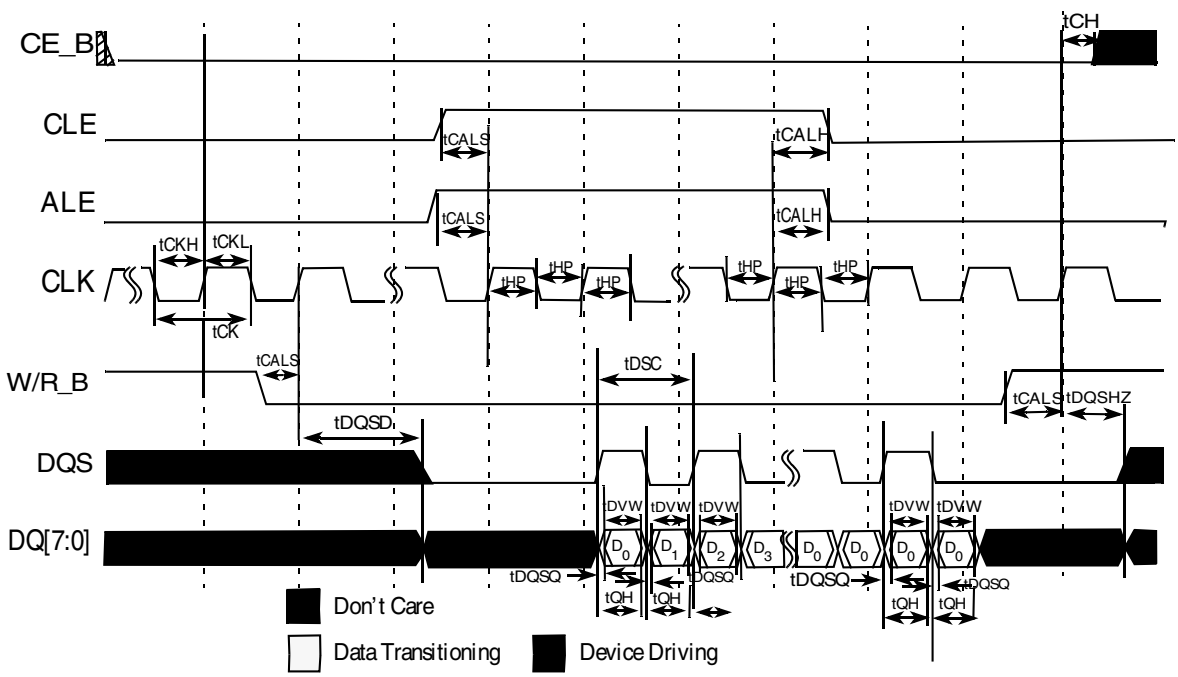


Figure 71. Read cycle

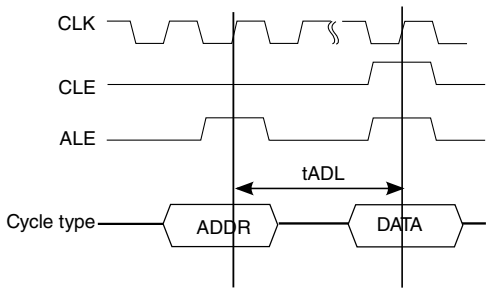


Figure 72. t_{ADL} timings

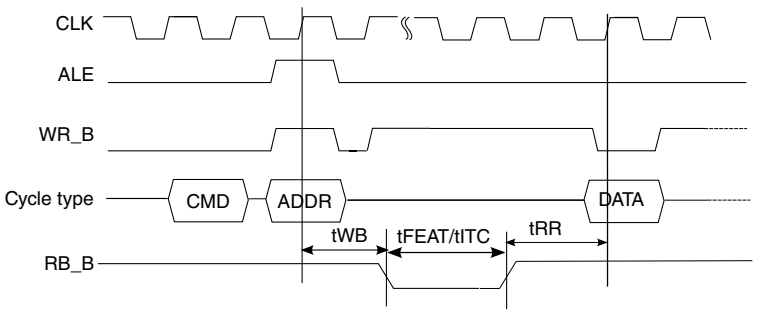


Figure 73. t_{WB}, t_{FEAT}, t_{ITC}, t_{RR} timings

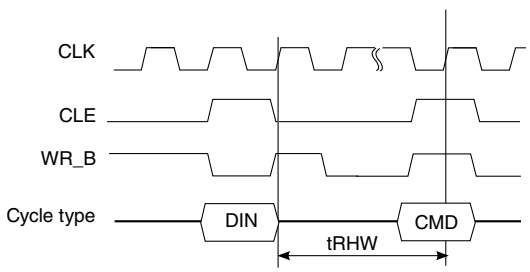


Figure 74. t_{RHW} timings

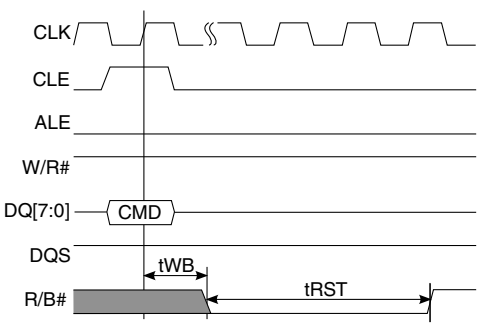


Figure 75. t_{WB} and t_{RST} timings

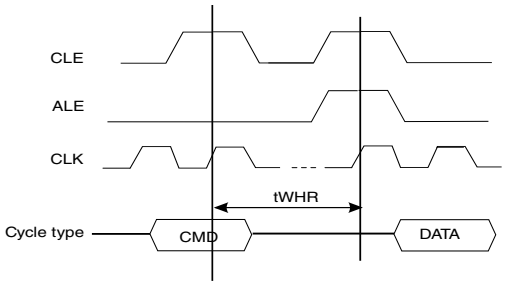


Figure 76. tWHR timings

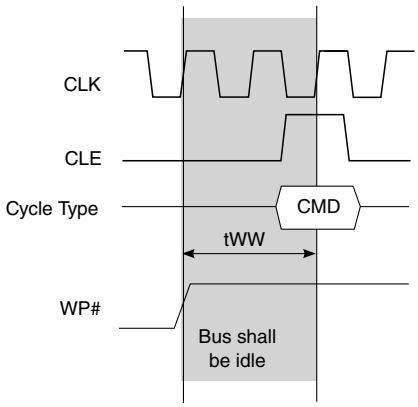


Figure 77. tWW timings

3.19 JTAG interface

This section describes the DC and AC electrical specifications for the JTAG (IEEE 1149.1) interface.

3.19.1 JTAG DC electrical characteristics

This table provides the DC electrical characteristics for the JTAG interface operating at OV_{DD} = 1.8 V.

Table 126. JTAG DC electrical characteristics (OV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN} = OV_{DD})	I_{IN}	-	-100/+50	µA	3, 4
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

Table continues on the next page...

Table 126. JTAG DC electrical characteristics (OV_{DD} = 1.8 V)[1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
1. For recommended operating conditions, see Table 3.					
2. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in the Recommended Operating Conditions table.					
3. Note that the symbol V_{IN}, in this case, represents the OVIN symbol found in the Recommended Operating Conditions table.					
4. TDI, TMS, and TRST_B have internal pull-ups per the IEEE Std. 1149.1 specification.					

3.19.2 JTAG AC timing specifications

This table provides the JTAG AC timing specifications as defined in Figure 78, Figure 79, Figure 80, and Figure 81.

Table 127. JTAG AC timing specifications[1]

Parameter	Symbol	Min	Max	Unit	Notes
JTAG external clock frequency of operation	F_{JTG}	0.0	33.3	MHz	-
JTAG external clock cycle time	t_{JTG}	30.0	-	ns	-
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15.0	-	ns	-
JTAG external clock rise and fall times	t_{JTGR}/t_{JTGF}	0.0	2.0	ns	-
TRST_B assert time	t_{TRST}	25.0	-	ns	TRST_B is an asynchronous level sensitive signal. The setup time is for test purposes only.
Input setup times	t_{JTDVKH}	4.0	-	ns	TA_BB_TMP_DETECT pin requires 13.5ns input setup time for the board JTAG test to go through runTESTIdle.
Input hold times	t_{JTDXKH}	10.0	-	ns	-
Output valid times: boundary-scan data	t_{JTKLDV}	-	15.0	ns	All outputs are measured from the midpoint voltage of the falling edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
Output valid times: TDO	t_{JTKLDV}	-	10.0	ns	All outputs are measured from the midpoint voltage of the falling edge of t_{TCLK} to the midpoint of the signal in

Table continues on the next page...

Table 127. JTAG AC timing specifications[1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
					question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
Output hold times	t_{JTKLDX}	0.0	-	ns	All outputs are measured from the midpoint voltage of the falling edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

1. The symbols used for timing specifications follow these patterns: $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the tJTG clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the invalid state (X) relative to the tJTG clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular function. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the AC test load for TDO and the boundary-scan outputs of the device.

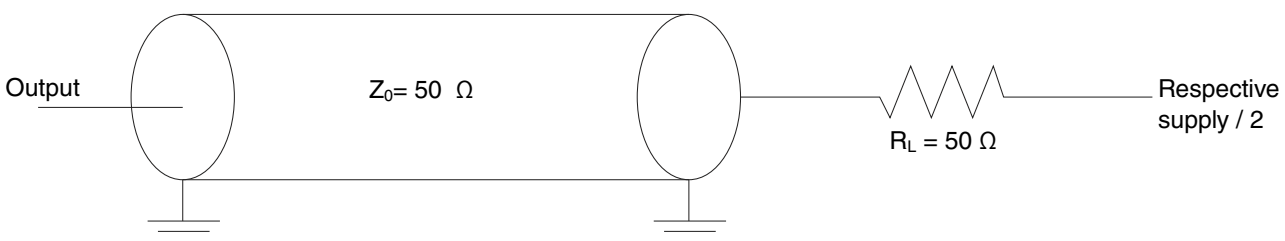


Figure 78. AC test load for the JTAG interface

This figure shows the JTAG clock input timing diagram.

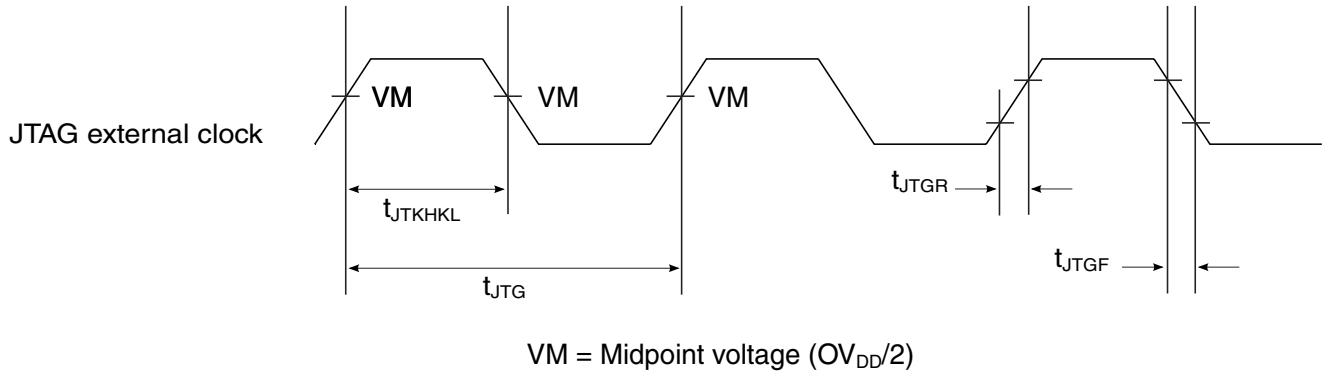


Figure 79. JTAG clock input timing diagram

This figure shows the TRST_B timing diagram.

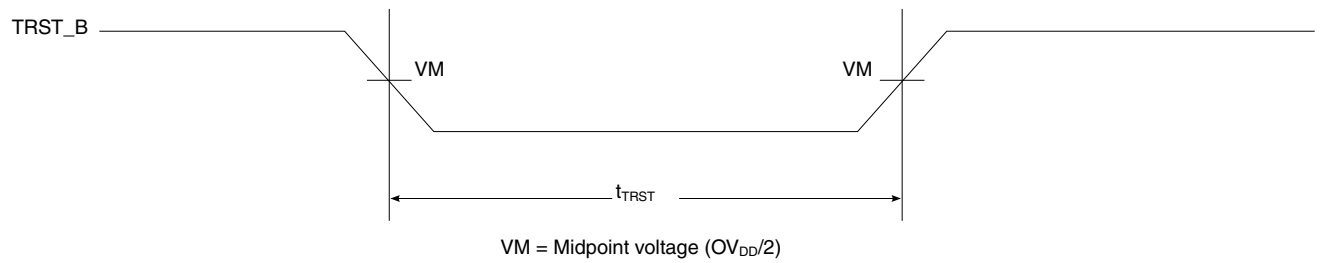


Figure 80. TRST_B timing diagram

This figure shows the boundary-scan timing diagram.

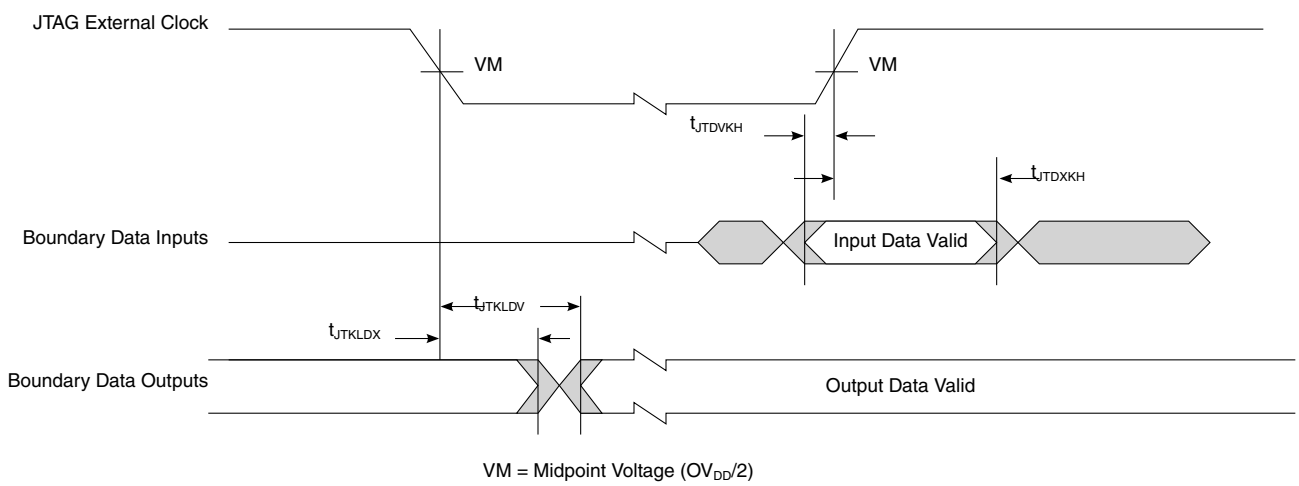


Figure 81. Boundary-scan timing diagram

3.20 Quad serial peripheral interface (QuadSPI)

This section describes the DC and AC electrical characteristics for the QuadSPI interface.

3.20.1 QuadSPI DC electrical characteristics

This table provides the DC electrical characteristics for the QuadSPI interface operating at OV_{DD} = 1.8V.

Table 128. QuadSPI DC electrical characteristics[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (0V ≤ V_{IN} ≤ OV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (OV_{DD} = min, I_{OH} = -100 μA)	V_{OH}	OV_{DD} - 0.2	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 100 μA)	V_{OL}	-	0.2	V	-

1. For recommended operating conditions, see Table 3.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.

3. Note that the symbol OV_{IN} represents the input voltage of the supply referenced in the Recommended Operating Conditions table.

3.20.2 QuadSPI AC timing specifications

This section describes the QuadSPI timing specifications in both SDR and DDR modes. All data is based on a negative edge data launch from the device and a positive edge data capture, as shown in the timing figures in this section.

This table provides the QuadSPI input and output timing in SDR mode (MCR[DQS_EN] = 0, regarding to the 1st sample point. See qSPI_SMPR[xSDLY, xSPHS] in the corresponding chip reference manual for different sampling points). Note that T represents the clock period, j represents qSPI_FLSHCR[TCSH], and k depends on qSPI_FLSHCR[TCSS].

Table 129. QuadSPI SDR mode input and output timing

Parameter	Symbol	Min	Max	Unit
Clock rise/fall time	T_{RISE}/T_{FALL}	1.0	-	ns
CS output hold time	$t_{NIKHOX2}$	-3.3 + j * T	-	ns
CS output delay	$t_{NIKHOV2}$	-3.0 + k * T	-	ns

Table continues on the next page...

Table 129. QuadSPI SDR mode input and output timing (continued)

Parameter	Symbol	Min	Max	Unit
Setup time for incoming data	t_{NIIVKH}	5.0	-	ns
Hold time requirement for incoming data	t_{NIIXKH}	1.0	-	ns
Output data delay	t_{NIKHOV}	-	1.95	ns
Output data hold	t_{NIKHOX}	-1.45	-	ns

This table provides the QuadSPI input and output timing in SDR mode with internal DQS (MCR[DQS_EN]=1 with regard to the 1st sample point). Note that T represents the clock period, the value of i depends on qSPI_SMPR[xSDLY, xSPHS], j depends on qSPI_FLSHCR[TCSH], k depends on qSPI_FLSHCR[TCSS], Tcoars depends on SCLK_CONFIG[7:5], and Ttapx depends on SOCCFG[7:0]/SOCCFG[23:16].

Table 130. QuadSPI SDR mode input and output timing

Parameter	Symbol	Min	Max	Unit
Clock rise/fall time	T_{RISE}/T_{FALL}	1.0	-	ns
CS output hold time	$t_{NIKHOX2}$	-3.3 + j * T	-	ns
CS output delay	$t_{NIKHOV2}$	-3.0 + k * T	-	ns
Setup time for incoming data	t_{NIIVKH}	2.5 - T_{coars} - T_{tap}	-	ns
Hold time requirement for incoming data	t_{NIIXKH}	1 + T_{coars} + T_{tap}	-	ns
Output data delay	t_{NIKHOV}	-	1.45	ns
Output data hold	t_{NIKHOX}	-1.45	-	ns

This figure shows the QuadSPI AC timing in SDR mode.

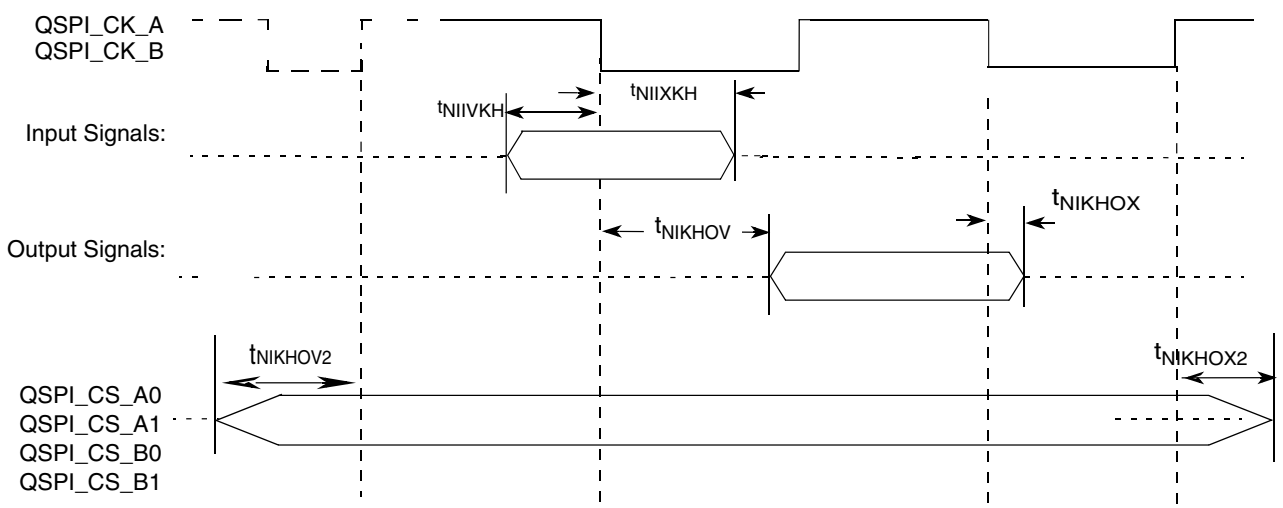


Figure 82. QuadSPI AC timing — SDR mode

This table provides the QuadSPI input and output timing in DDR mode with external DQS/delay chain (MCR[DQS_EN] = 1, regarding to the 1st sample point). Note that T represents the clock period, j depends on the value of qSPI_FLSHCR[TCSH], k depends on qSPI_FLSHCR[TCSS], and m depends on QSPI_FLSHCR[TDH].

Table 131. QuadSPI DDR mode input and output timing

Parameter	Symbol	Min	Max	Unit
Clock rise/fall time	T_{RISE}/T_{FALL}	1.0	-	ns
CS output hold time	$t_{NIKHOX2}$	3.3 + T * j	-	ns
CS output delay	$t_{NIKHOV2}$	-3.0 + k * T		ns
DQS to data skew	t_{NIDSH}/t_{NIIDSL}	-0.9	0.9	ns
Output data valid	t_{NIKHOV}	-	0.9 + m * T/8	ns
Output data hold	t_{NIKHOX}	-0.9 + m * T/8	-	ns

This figure shows the QuadSPI AC timing in DDR mode.

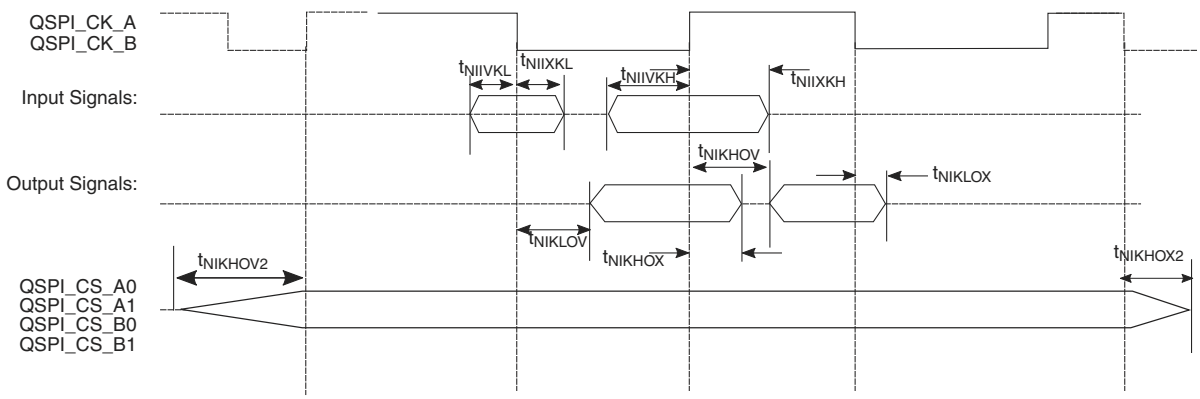


Figure 83. QuadSPI AC timing — DDR mode

This figure shows the QuadSPI data input timing in DDR mode with an external DQS.

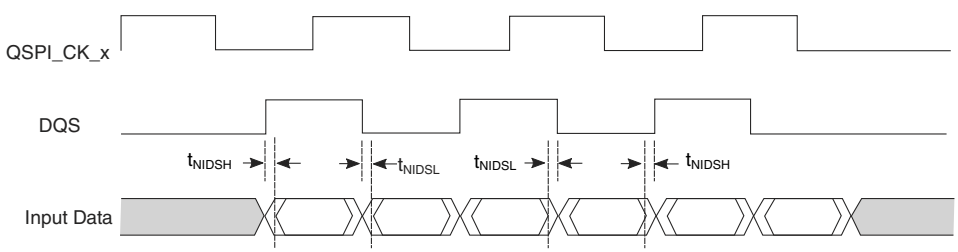


Figure 84. QuadSPI input AC timing — DDR mode with an external DQS

This figure shows the QuadSPI clock input timing diagram.

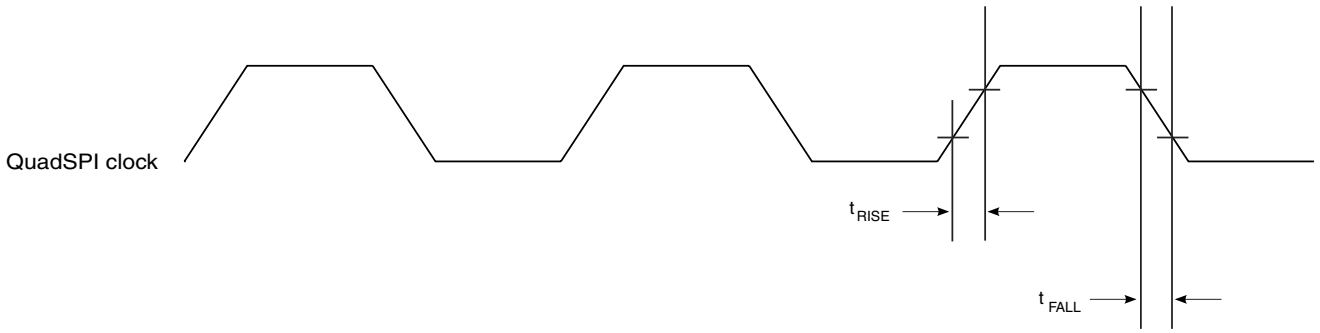


Figure 85. QuadSPI clock input timing diagram

This figure shows the AC test load for QuadSPI.

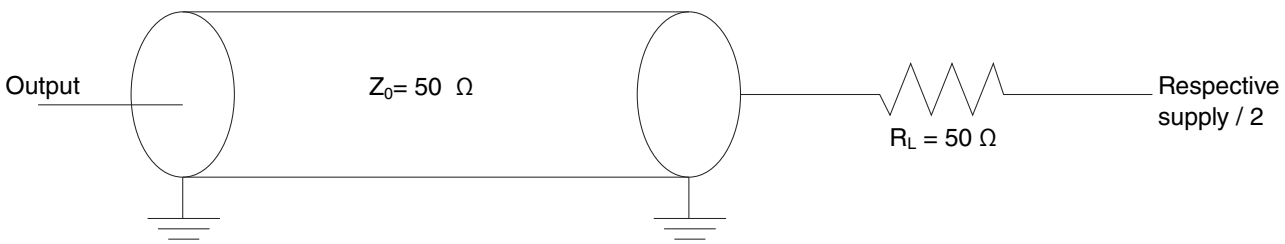


Figure 86. AC test load for QuadSPI

3.21 QUICC engine specifications

The rise/fall time on QUICC engine block input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of V_{DD}. Fall time refers to transitions from 90% to 10% of V_{DD}.

3.21.1 High-level data link control (HDLC) interface

This section describes the DC and AC electrical characteristics for the high-level data link control (HDLC) interface.

3.21.1.1 HDLC DC electrical characteristics

This table provides the DC electrical characteristics for the HDLC and synchronous UART protocols when operating at DV_{DD} = 3.3 V.

Table 132. HDLC and synchronous UART DC electrical characteristics (DV_{DD} = 3.3 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DVDD	-	V	2
Input low voltage	V_{IL}	-	0.2 x DVDD	V	2
Input current (V_{IN} = 0V or V_{IN} = DV_{DD})	I_{IN}	-50	50	µA	3
Output high voltage (DV_{DD}=min, I_{OH} = -2 mA)	V_{OH}	2.4	-	V	-
Output low voltage (DV_{DD}=min, I_{OL} = 2 mA)	V_{OL}	-	0.4	V	-

1. For recommended operating conditions, see Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 3.
3. The symbol V_{IN} represents the input voltage of the supply referenced in Table 3.

This table provides the DC electrical characteristics for the HDLC and Synchronous UART protocols when DV_{DD} = 1.8 V.

Table 133. HDLC and synchronous UART DC electrical characteristics (DV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DVDD	-	V	2
Input low voltage	V_{IL}	-	0.3 x DVDD	V	2
Input current (V_{IN} = 0V or V_{IN} = DV_{DD})	I_{IN}	-50	50	µA	3
Output high voltage (DV_{DD}=min, I_{OH} = -2 mA)	V_{OH}	1.35	-	V	-
Output low voltage (DV_{DD}=min, I_{OL} = 2 mA)	V_{OL}	-	0.45	V	-

1. For recommended operating conditions, see Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 3.
3. The symbol V_{IN} represents the input voltage of the supply referenced in Table 3.

3.21.1.2 HDLC and synchronous UART AC timing specifications

NOTE

Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

This table provides the input and output AC timing specifications for the HDLC and synchronous UART protocols.

Table 134. HDLC AC timing specifications

Parameter	Symbol	Min	Max	Unit
Internal clock delay	t_{HIKHOV}	0.0	5.5	-
External clock delay	t_{HEKHOV}	1.0	13.0	ns
Internal clock high impedance	t_{HIKHOX}	0.0	5.5	ns
External clock high impedance	t_{HEKHOX}	1.0	8.0	ns
Internal clock input setup time	t_{HIIVKH}	12.6	-	ns
External clock input setup time	t_{HEIVKH}	4.0	-	ns
Internal clock input hold time	t_{HIIXKH}	0.0	-	ns
External clock input hold time	t_{HEIXKH}	1.0	-	ns

This table provides the input and output AC timing specifications for the synchronous UART protocols.

Table 135. Synchronous UART AC timing specifications

Parameter	Symbol	Min	Max	Unit
Internal clock delay	t_{HIKHOV}	0.0	11.0	-
External clock delay	t_{HEKHOV}	1.0	14.0	ns
Internal clock high impedance	t_{HIKHOX}	0.0	11.0	ns
External clock high impedance	t_{HEKHOX}	1.0	14.0	ns
Internal clock input setup time	t_{HIIVKH}	10.0	-	ns
External clock input setup time	t_{HEIVKH}	8.0	-	ns
Internal clock input hold time	t_{HIIXKH}	0.0	-	ns
External clock input hold time	t_{HEIXKH}	1.0	-	ns

This figure shows the AC test load for the HDLC interface.

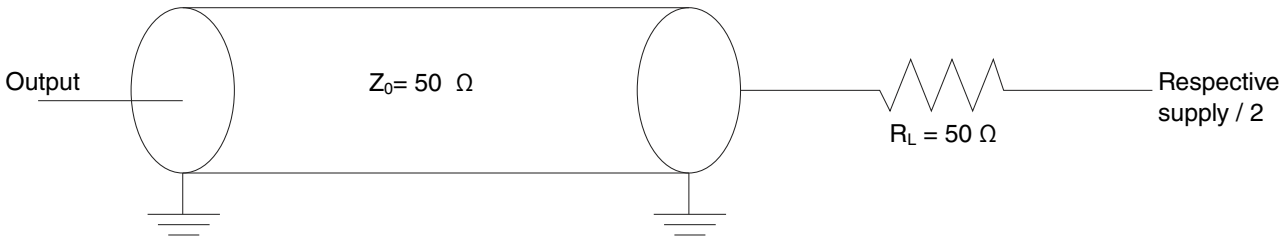
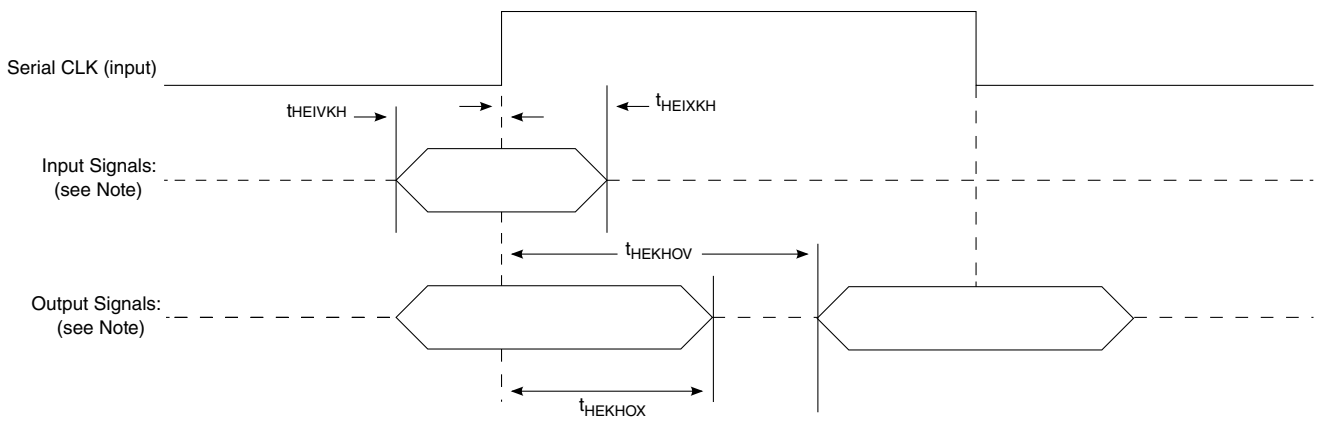


Figure 87. AC test load for HDLC

These figures represent the AC timing from the tables in section HDLC and synchronous UART AC timing specifications. Note that, although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

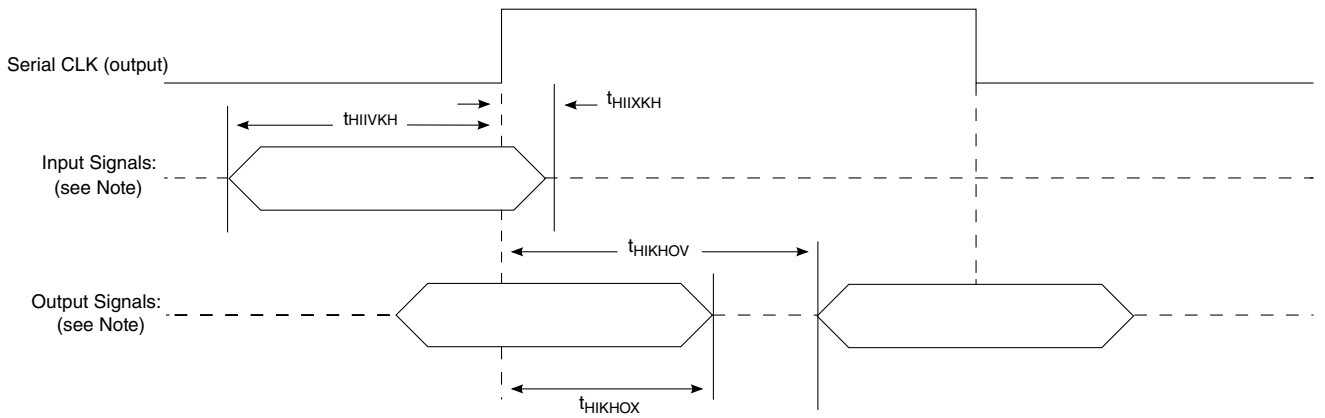
This figure shows the timing with an external clock.



Note: The clock edge is selectable.

Figure 88. AC timing (external clock) diagram

This figure shows the timing with an internal clock.



Note: The clock edge is selectable.

Figure 89. AC timing (internal clock) diagram

3.21.2 Time division multiplexed/serial interface (TDM/SI)

This section describes the DC and AC electrical characteristics for the TDM/SI interface.

3.21.2.1 TDM/SI DC electrical characteristics

This table provides the DC electrical characteristics for the TDM/SI interface when operating at DV_{DD} = 3.3 V.

Table 136. TDM/SI DC electrical characteristics (DV_{DD} = 3.3 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DVDD	-	V	2
Input low voltage	V_{IL}	-	0.2 x DVDD	V	2
Input current (V_{IN} = 0V or V_{IN} = DV_{DD})	I_{IN}	-50	50	µA	3
Output high voltage (DV_{DD}=min, I_{OH} = -2 mA)	V_{OH}	2.4	-	V	-
Output low voltage (DV_{DD}=min, I_{OL} = 2 mA)	V_{OL}	-	0.4	V	-
1. For recommended operating conditions, see Table 3.					
2. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 3.					
3. The symbol V_{IN} represents the input voltage of the supply referenced in Table 3.					

This table provides the TDM/SI DC electrical characteristics when DV_{DD} = 1.8 V.

Table 137. TDM/SI DC electrical characteristics (DV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.65 x DVDD	-	V	2
Input low voltage	V_{IL}	-	0.35 x DVDD	V	2
Input current (V_{IN} = 0V or V_{IN} = DV_{DD})	I_{IN}	-50	50	µA	3
Output high voltage (DV_{DD}=min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (DV_{DD}=min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

1. For recommended operating conditions, see Table 3.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 3.

3. The symbol V_{IN} represents the input voltage of the supply referenced in Table 3.

3.21.2.2 TDM/SI AC timing specifications

NOTE

Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

This table provides the AC timing specifications for the TDM/SI interface.

Table 138. TDM/SI AC timing specifications

Parameter	Symbol	Min	Max	Unit
External clock delay	t_{SEKHOV}	2.0	11.0	ns
External clock high impedance	t_{SEKHOX}	2.0	10.0	ns
External clock input setup time	t_{SEIVKH}	5.0	-	ns
External clock input hold time	t_{SEIXKH}	2.0	-	ns

This figure shows the AC test load for the TDM/SI.

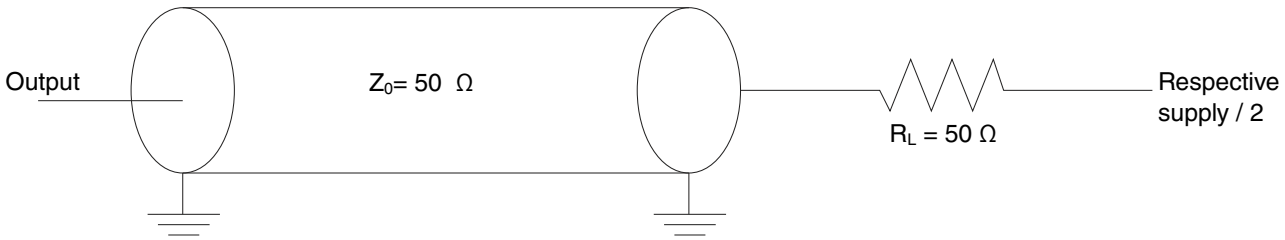
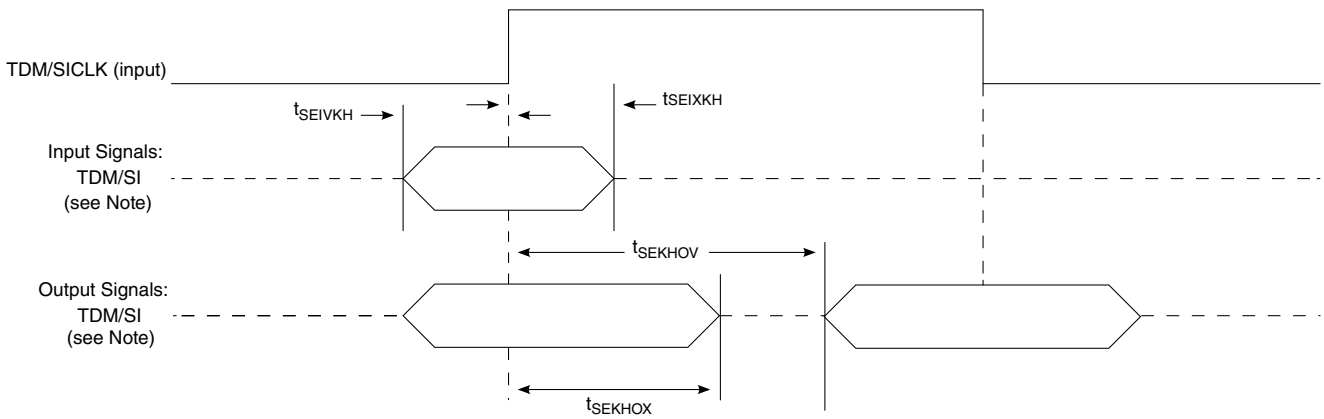


Figure 90. TDM/SI AC test load

This figure represents the AC timing from the TDM/SI AC timing specifications table. Note that, although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

This figure shows the TDM/SI timing with an external clock.



Note: The clock edge is selectable on TDM/SI.

Figure 91. TDM/SI AC timing (external clock) diagram

3.22 Serial peripheral interface (SPI)

This section describes the DC and AC electrical characteristics for the SPI interface.

3.22.1 SPI DC electrical characteristics

This table provides the DC electrical characteristics for the SPI interface operating at OV_{DD} = 1.8 V.

Table 139. SPI DC electrical characteristics (OV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN} = OV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

1. For recommended operating conditions, see Table 3.

2. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in the Recommended Operating Conditions table.

3. Note that the symbol OV_{IN} represents the input voltage of the supply referenced in the Recommended Operating Conditions table.

3.22.2 SPI AC timing specifications

This table provides the AC timing specifications for the SPI interface when operating with a single master device.

Table 140. SPI AC timing specifications

Parameter	Symbol	Min	Condition	Max	Unit
SCK clock pulse width	t_{SDC}	40	-	60	%
CS to SCK delay	t_{CSC}	16.0	Master	-	ns
After SCK delay	t_{ASC}	16.0	Master	-	ns
Slave access time (SS active to SOUT driven)	t_{A}	-	Slave	15	ns
Slave disable time (SS inactive to SOUT High-Z or invalid)	t_{DI}	-	Slave	10	ns
Data setup time for inputs	t_{NIIVKH}	9.0	Master	-	ns
Data setup time for inputs	t_{NEIVKH}	8.0	Slave	-	ns
Data hold time for inputs	t_{NIIXKH}	0.0	Master	-	ns
Data hold time for inputs	t_{NEIXKH}	2.0	Slave	-	ns
Data valid (after SCK edge) for outputs	t_{NIKHOV}	-	Master	5.0	ns

Table continues on the next page...

Table 140. SPI AC timing specifications (continued)

Parameter	Symbol	Min	Condition	Max	Unit
Data valid (after SCK edge) for outputs	t_{NEKHOV}	-	Slave	7.6	ns
Data hold time for outputs	t_{NIKHOX}	0.0	Master	-	ns
Data hold time for outputs	t_{NEKHOX}	0.0	Slave	-	ns

This figure shows the SPI timing master when CPHA = 0.

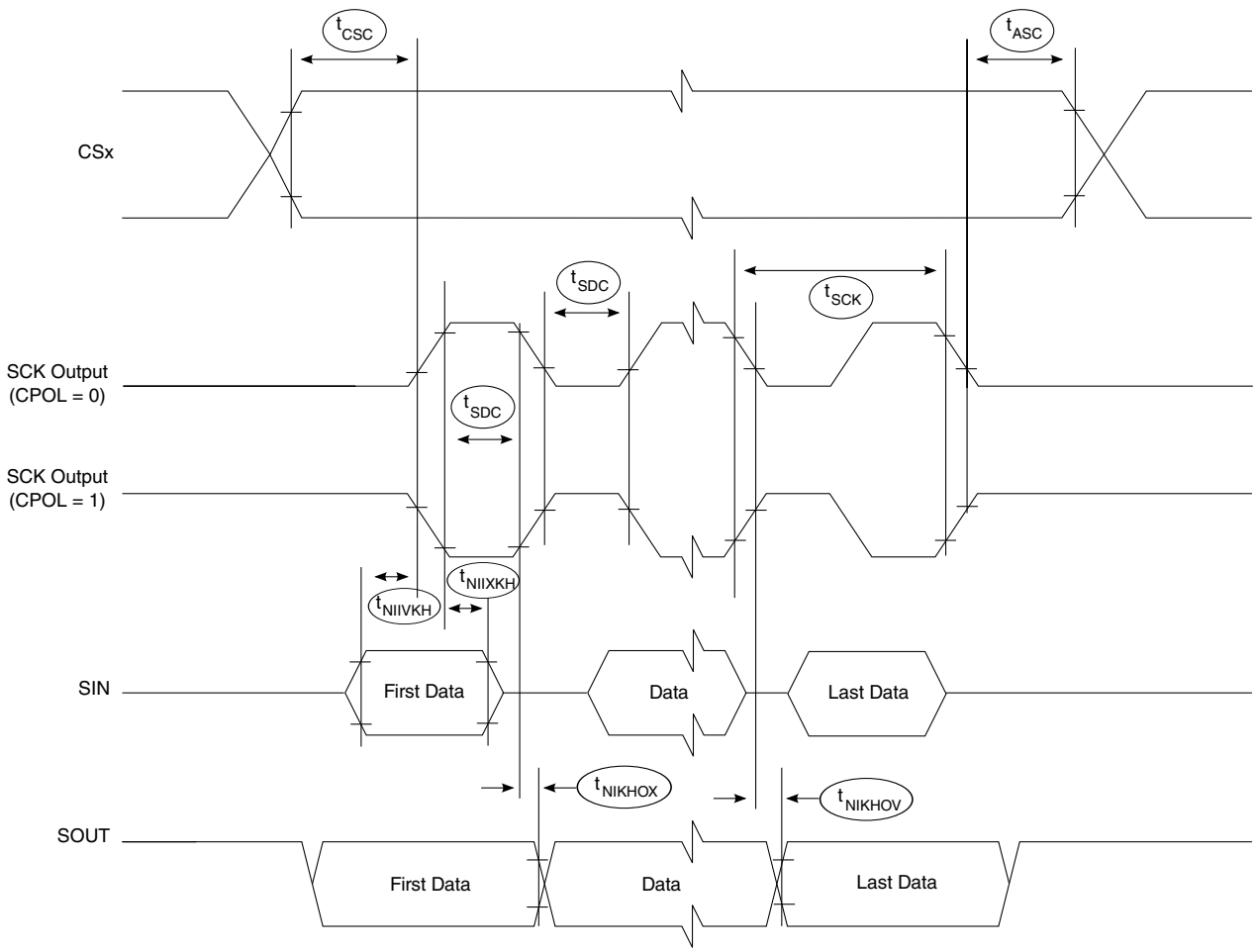


Figure 92. SPI timing master, CPHA = 0

This figure shows the SPI timing master when CPHA = 1.

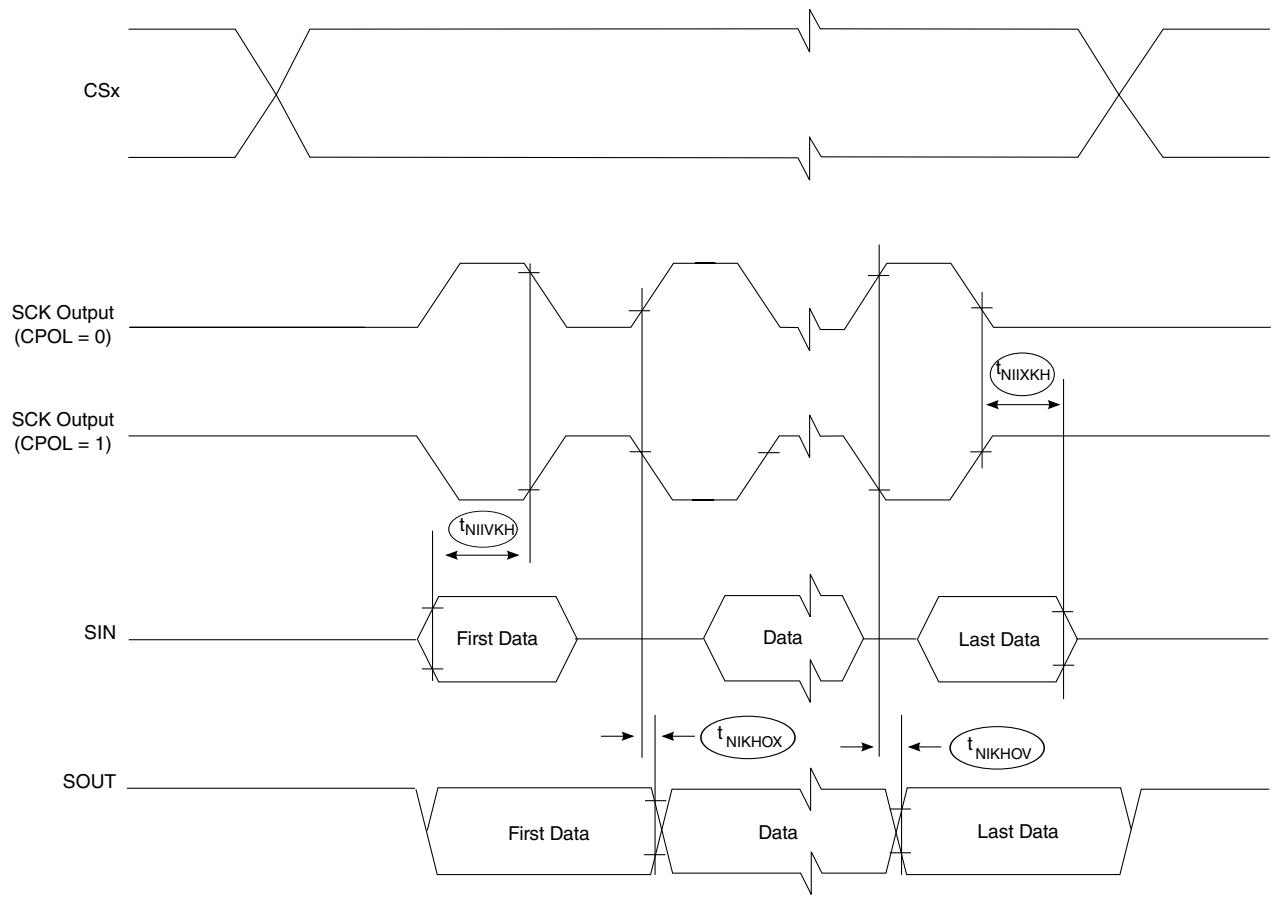


Figure 93. SPI timing master, CPHA = 1

3.23 Universal serial bus (USB) interface

This section describes the DC and AC electrical characteristics for the USB interface.

3.23.1 USB 3.0 interface

This section describes the electrical characteristics for the USB 3.0 interface.

3.23.1.1 USB 3.0 DC electrical characteristics

This table provides the DC electrical characteristics for the USB 3.0 interface when operating at USB_HV_{DD} = 3.3 V.

Table 141. USB 3.0 PHY transceiver supply DC voltage (USB_HV_{DD} = 3.3 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	-	V	2
Input low voltage	V_{IL}	-	0.8	V	2
Input current (USB_HVIN = 0V or USB_HV_{IN} = USB_HV_{DD})	I_{IN}	-50.0	50.0	µA	3
Output high voltage (USB_HV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.8	-	V	-
Output low voltage (USB_HV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	-	0.3	V	-
1. For recommended operating conditions, see Table 3. 2. The min V_{IL} and max V_{IH} values are based on the respective min and max USB_HV_{IN} values found in Table 3. 3. The symbol USB_HV_{IN} represents the input voltage of the supply referenced in Table 3.					

This table provides the USB 3.0 transmitter DC electrical characteristics at package pins.

Table 142. USB 3.0 transmitter DC electrical characteristics[1]

Parameter	Symbol	Min	Typ	Max	Unit
Differential output voltage	$V_{tx\text{-}diff\text{-}pp}$	800.0	1000.0	1200.0	mVp-p
Low power differential output voltage	$V_{tx\text{-}diff\text{-}pp\text{-}low}$	400.0	-	1200.0	mVp-p
Transmit de-emphasis	$V_{tx\text{-}de\text{-}ratio}$	3.0	-	4.0	dB
Differential impedance	Z_{diffTX}	72.0	100.0	120.0	Ω
Transmit common mode impedance	$R_{TX\text{-}DC}$	18.0	-	30.0	Ω
Absolute DC common mode voltage between U1 and U0	$T_{TX\text{-}CM\text{-}DC\text{-}ACTIVEIDLE\text{-}DELTA}$	-	-	200.0	mV
DC electrical idle differential output voltage	$V_{TX\text{-}IDLE\text{-}DIFF\text{-}DC}$	0.0	-	10.0	mV
1. For recommended operating conditions, see Table 3.					

This table provides the USB 3.0 transmitter DC electrical characteristics at receiver package pins.

Table 143. USB 3.0 receiver DC electrical characteristics[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential receiver input impedance	$R_{RX\text{-}DIFF\text{-}DC}$	72.0	100.0	120.0	Ω	-
Receiver DC common mode impedance	$R_{RX\text{-}DC}$	18.0	-	30.0	Ω	-
DC input CM input impedance for V > 0 during reset or power down	$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC}$	25000.0	-	-	Ω	-

Table continues on the next page...

Table 143. USB 3.0 receiver DC electrical characteristics[1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
LFPS detect threshold	$V_{TRX-IDLE-DET-DC-DIFFpp}$	100.0	-	300.0	mV	2
1. For recommended operating conditions, see Table 3.						
2. Below the minimum is noise. Must wake up above the maximum.						

3.23.1.2 USB 3.0 AC timing specifications

This table provides the USB 3.0 transmitter AC timing specifications at package pins.

Table 144. USB 3.0 transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Speed	-	-	5.0	-	Gb/s	-
Transmitter eye	T_{TX-EYE}	0.625	-	-	UI	-
Unit Interval	UI	199.94	-	200.06	ps	UI does not account for SSC-caused variations.
AC coupling capacitor	AC_{CAP}	75.0	-	200.0	nF	-

This table provides the USB 3.0 receiver AC timing specifications at receiver package pins.

Table 145. USB 3.0 receiver AC timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
Unit Interval	UI	199.94	200.06	ps	UI does not account for SSC-caused variations.

3.23.1.3 USB 3.0 LFPS specifications

This table provides the key LFPS electrical specifications at the transmitter.

Table 146. LFPS electrical specifications at the transmitter

Parameter	Symbol	Min	Max	Unit	Notes
Period	t_{Period}	20.0	100.0	ns	-

Table continues on the next page...

Table 146. LFPS electrical specifications at the transmitter (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Peak-to-peak differential amplitude	$V_{tx\text{-}diff\text{-}pp\text{-}lfps}$	800.0	1200.0	mV	-
Low-power peak-to-peak differential amplitude	$V_{tx\text{-}diff\text{-}pp\text{-}lfps\text{-}lp}$	400.0	600.0	mV	-
Rise/fall time	$t_{rise/fall}$	-	4.0	ns	Measured at compliance TP1. See the Transmit normative setup figure below for details.
Duty cycle	DC_{LFPS}	40.0	60.0	%	Measured at compliance TP1. See the Transmit normative setup figure below for details.

This figure shows the Tx normative setup with reference channel per USB 3.0 specifications.

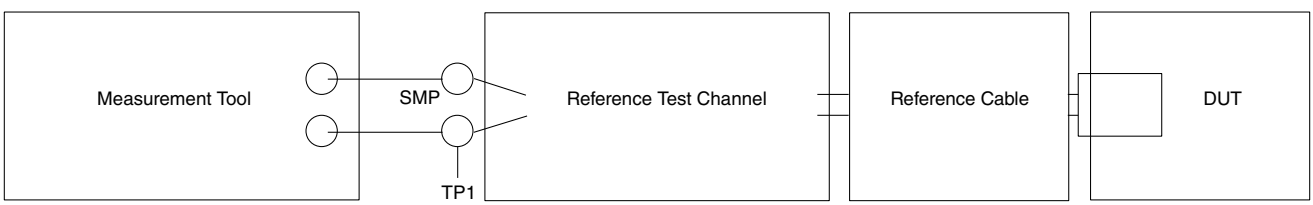


Figure 94. Transmit normative setup

4 Hardware design considerations

4.1 Clock ranges

This table provides the clocking specifications for the processor core, platform, memory, and integrated flash controller.

Table 147. Processor, platform, and memory clocking specifications

Characteristic	Maximum processor core frequency						Unit	Notes
	1200 MHz		1400 MHz		1600 MHz			
	Min	Max	Min	Max	Min	Max		
Core cluster group PLL frequency	600	1200	600	1400	600	1600	MHz	1
Platform clock frequency	400	500	400	600	400	700	MHz	1
Memory bus clock frequency	650	800	650	900	650	1050	MHz	1, 2
IFC clock frequency	-	100	-	100	-	100	MHz	3

1. **Caution:**The coherency domain clock to SYSCLK ratio and core to SYSCLK ratio settings must be chosen such that the resulting SYSCLK frequency, core frequency, coherency domain and platform clock frequency do not exceed their respective maximum or minimum operating frequencies.

2. The memory bus clock speed is half the DDR4 data rate.

3. The integrated flash controller (IFC) clock speed on IFC_CLK[0:1] is determined by the platform clock divided by the IFC ratio programmed in CCR[CLKDIV]. See the chip reference manual for more information.

4.2 Power supply design

For additional details on the power supply design, see AN5144, QorIQ LS1088A Design Checklist.

4.2.1 Voltage ID (VID) controllable supply

To guarantee performance and power specifications, a specific method of selecting the optimum voltage-level must be implemented when the chip is used. As part of the chip's boot process, software must read the VID efuse values stored in the Fuse Status register (FUSESR) and then configure the external voltage regulator based on this information. This method requires a point of load voltage regulator for each chip. When VID option is used, the V_{DD} supply should be separated from the SerDes 1.0 V supply SnV_{DD}. It is required in order to control the V_{DD} supply only.

NOTE

During the power-on reset process, the fuse values are read and stored in the FUSESR. It is expected that the chip's boot code reads the FUSESR value very early in the boot sequence and updates the regulator accordingly.

The default voltage regulator setting that is safe for the system to boot is the recommended operating V_{DD} at initial start-up of 1.025 V. It is highly recommended to select a regulator with a Vout range of at least 0.9 V to 1.1 V, with a resolution of 12.5 mV or better, when implementing a VID solution.

The table below lists the valid VID fuse values that will be programmed at the factory for this chip.

Table 148. Fuse Status Register (DCFG_CCSR_FUSESR)

Binary value of DA_V / DA_ALT_V	V_{DD} voltage
00000b	1.025 V (default)
00001b	0.9875 V
00010b	0.9750 V
01000b	0.9000 V
10000b	1.0000 V
10001b	1.0125 V
10010b	1.0250 V
All other values	Reserved

For additional information on VID, see the chip reference manual.

5 Thermal

This table shows the thermal characteristics for the chip. Note that these numbers are based on design estimates and are preliminary.

Table 149. Package thermal characteristics

Rating	Board	Symbol	Value	Unit	Notes
Junction-to-ambient, natural convection	Single-layer board (1s)	$R_{\Theta JA}$	23.5	°C/W	1
Junction-to-ambient, natural convection	Four-layer board (2s2p)	$R_{\Theta JA}$	15.2	°C/W	1
Junction-to-ambient (at 200 ft./min.)	Single-layer board (1s)	$R_{\Theta JMA}$	14.8	°C/W	1
Junction-to-ambient (at 200 ft./min.)	Four-layer board (2s2p)	$R_{\Theta JMA}$	10.1	°C/W	1
Junction-to-board	-	$R_{\Theta JB}$	4.4	°C/W	2
Junction-to-case (top)	-	$R_{\Theta JCtop}$	0.56	°C/W	3
Junction-to-lid-top	-	$R_{\Theta JClid}$	0.20	°C/W	4

1. Junction-to-ambient thermal resistance determined per JEDEC JESD51-2A and JESD51-6. Thermal test board meets JEDEC specification for this package (JESD51-9).

2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

3. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

4. Junction-to-lid-top thermal resistance is determined using the MIL-STD 883 Method 1012.1. However, instead of the cold plate, the lid top temperature is used here for the reference case temperature. Reported value does not include the thermal resistance layer between the package and cold plate.

5. See Thermal management information for additional details.

5.1 Recommended thermal model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local NXP sales office.

5.2 Temperature diode

The chip has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461A). These devices feature series resistance cancellation using three current measurements, where up to 1.5 kΩ of resistance can be automatically cancelled from the temperature result, allowing noise filtering and a more accurate reading.

The following are the specifications of the chip's on-board temperature diode:

Operating range: TBD

Ideality factor TBD; Temperature range TBD

5.3 Thermal management information

This section provides thermal management information for the flip-chip, plastic-ball, grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design-the heat sink, airflow, and thermal interface material.

The recommended attachment method to the heat sink is illustrated in Figure 95. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 15 pounds force.

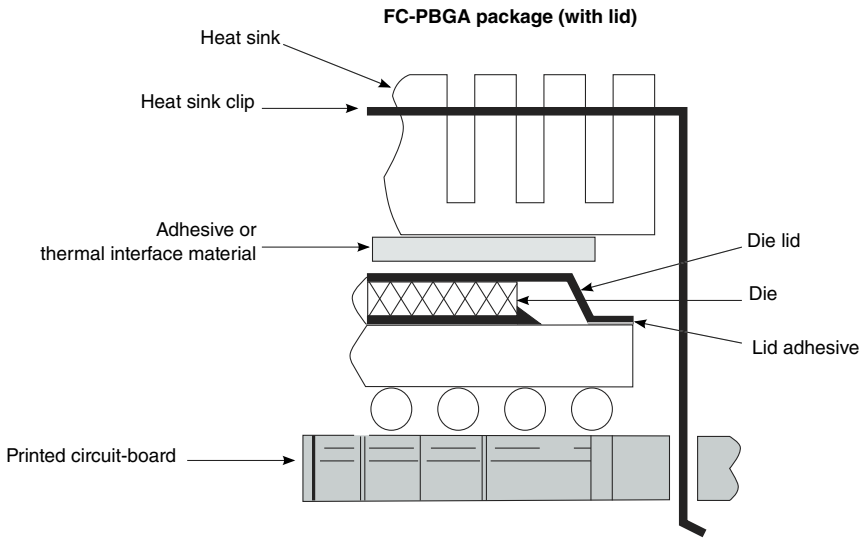


Figure 95. Package exploded, cross-sectional view-FC-PBGA (with lid)

The system board designer can choose between several types of heat sinks to place on the device. There are several commercially available thermal interfaces to choose from in the industry. Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

5.3.1 Internal package conduction resistance

For the package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

This figure shows the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

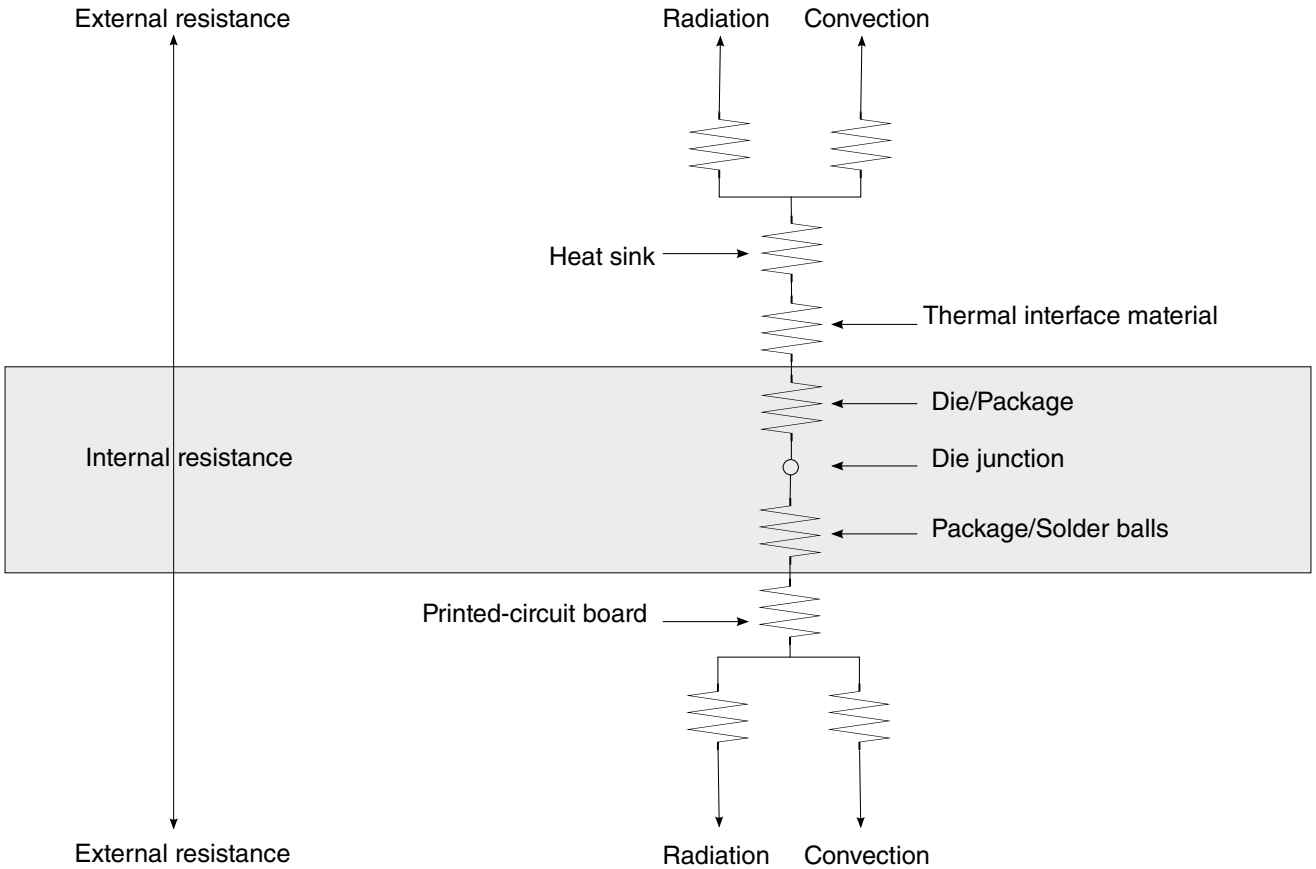


Figure 96. Package with heat sink mounted to a printed-circuit board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

5.3.2 Thermal interface materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increasing contact pressure; this performance characteristic chart is generally provided by the thermal interface vendor. The recommended method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board (see Figure 95).

The system board designer can choose among several types of commercially available thermal interface materials.

6 Package information

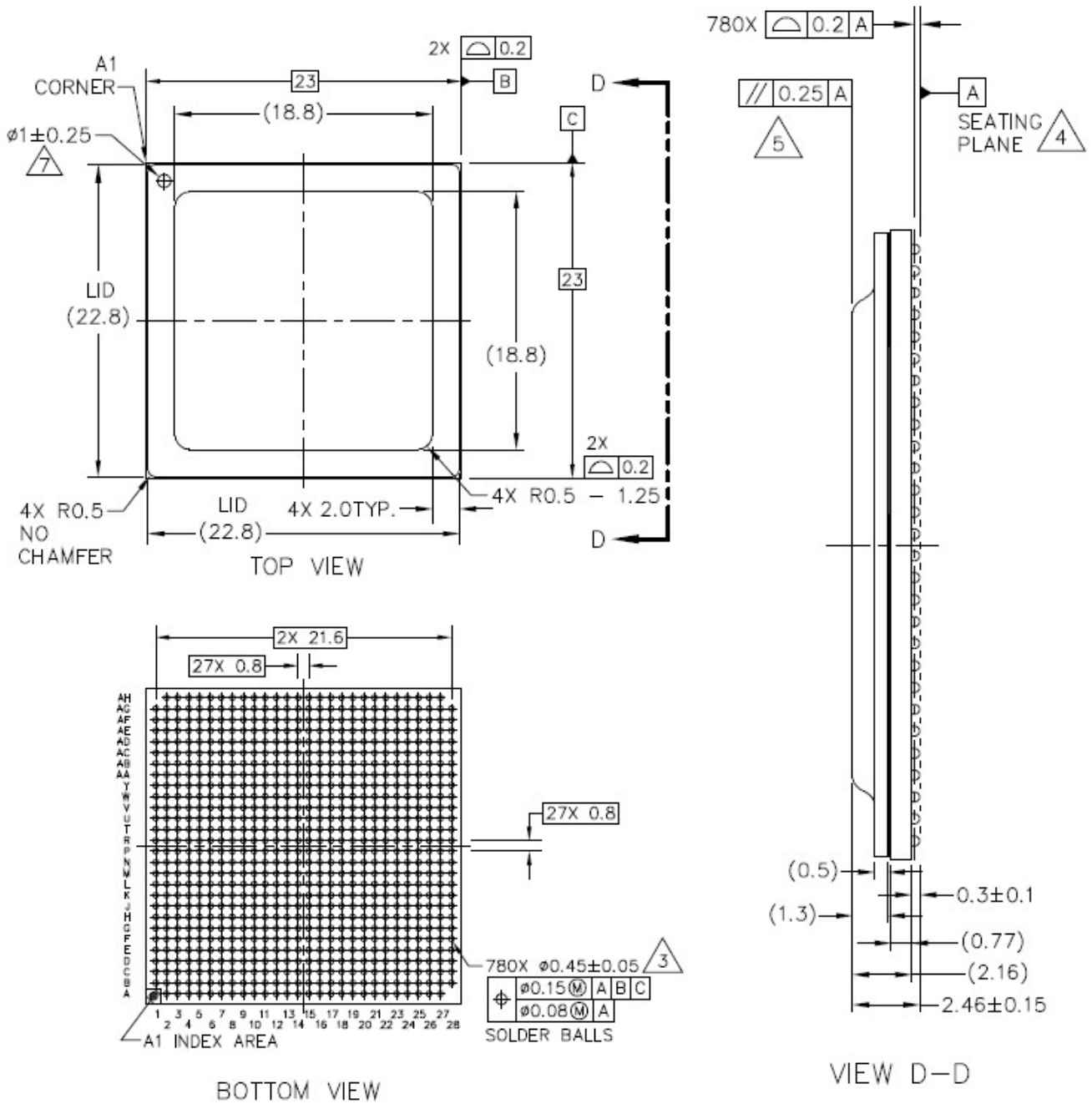
6.1 Package parameters for the FC-PBGA

The package parameters are as provided in the following list. The package type is 23 mm x 23 mm, 780 flip-chip, plastic-ball, grid array.

- Package outline - 23 mm x 23 mm
- Interconnects - 780
- Ball Pitch - 0.8 mm
- Ball Diameter (nominal) - 0.45 mm
- Ball Height (nominal) - 0.3 mm
- Solder Balls Composition - 96.5% Sn, 3% Ag, 0.5% Cu
- Module height (typical) - 2.31 mm (minimum), 2.46 mm (typical), 2.61 mm (maximum)

6.2 Mechanical dimensions of the FC-PBGA

This figure shows the mechanical dimensions and bottom surface nomenclature of the chip.



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: FCPBGA, WITH LID, 23 X 23 X 2.46 PKG, 0.8 MM PITCH, 780 I/O	DOCUMENT NO: 98ASA00854D	REV: O
	STANDARD: NON–JEDEC	
	03 DEC 2014	

Figure 97. Mechanical dimensions of the FC-PBGA

NOTES:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.
6. All dimensions are symmetric across the package center lines, unless dimensioned otherwise.
7. Pin 1 thru hole shall be centered within foot area.
8. 23.2 mm maximum package assembly (lid + laminate) X and Y.

7 Security fuse processor

This chip implements trust architecture 3.0, which supports capabilities such as secure boot. Use of the trust architecture features is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the trust architecture and SFP can be found in the chip reference manual.

To program SFP fuses, the user is required to supply 1.8 V to the TA_PROG_SFP pin per Power sequencing. TA_PROG_SFP should only be powered for the duration of the fuse programming cycle, with a per device limit of two fuse programming cycles. All other times, TA_PROG_SFP should be connected to GND. The sequencing requirements for raising and lowering TA_PROG_SFP are shown in Power sequencing. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

NOTE

Users not implementing the QorIQ platform's trust architecture features should connect TA_PROG_SFP to GND.

8 Ordering information

Contact your local NXP sales office or regional marketing team for order information.

8.1 Part numbering nomenclature

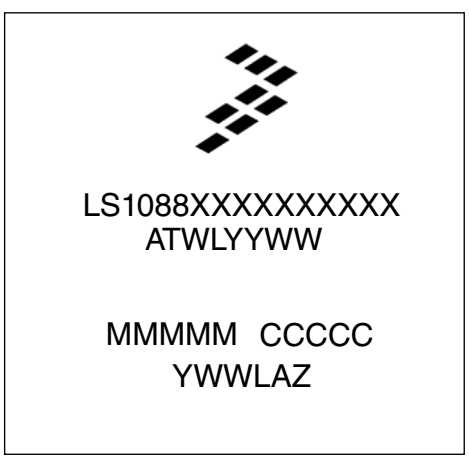
This table provides the NXP Layerscape platform part numbering nomenclature.

Table 150. Part numbering nomenclature

q	*p*	*g*	*c*	*u*	*c*	*t*	*e*	*n*	*c*	*d*	r
Qual status	**Product generation**	**Performance level**	**Number of cores**	**Unique ID**	**Core Type**	**Temperature Range**	**Encryption**	**Package type**	**CPU speed[1]**	**DDR data rate**	**Revision**
(blank) = Qualified P = Pre-qual	LS = Layerscape	1	08 = Eight cores 04 = Four cores	8 = with AIOP 4 = without AIOP	A = ARM	S = Standard (0–105°C) X = Extended (-40–105°C)	E = Encryption N = Non-Encryption	7 = FC-PBGA	M = 1200 MHz P = 1400 MHz Q = 1600 MHz	Q = 1600 MHz T = 1800 MHz 1 = 2100 MHz	A = Rev 1.0
1. For the LS1088A family of devices, parts marked with "M" require 0.9 V operating voltage. All others require VID.											

8.2 Part marking

Parts are marked as in the example shown in this figure.



FC-PBGA

Legend:
LS1088XXXXXXXXXX is the part marking on the die.
ATWLYYWW is the test traceability code.
MMMMM is the mask number.
CCCCC is the country code.
YWWLAZ is the assembly traceability code.

Figure 98. Part marking for FC-PBGA chip

9 Revision history

This table summarizes revisions to this document.

Table 151. Revision history

Revision	Date	Description
0	01/2018	Initial release.

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