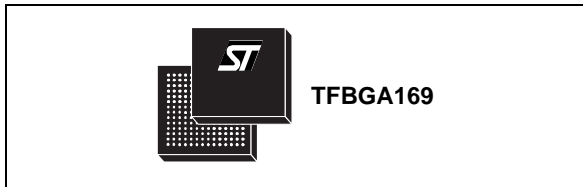


Flexible GPS/Galileo/Glonass/QZSS receiver with high performance processing (ARM9)

Data brief



Features

- STMicroelectronics® 3rd generation positioning receiver with 32 tracking channels and 2 fast acquisition channels compatible with GPS, Galileo, Glonass and QZSS systems
- Embedded RF front-end with built-in LNA
- -162dBm indoor sensitivity (tracking mode)
- Fast TTFB < 1 s in hot start and 35 s in cold start
- Support of ST-AGPSTM Multimode Assisted GPS (extended ephemeris solution)
- High performance ARM946 MCU (up to 208 MHz)
- 256 Kbyte embedded TCM/SRAM
- FSMC external memory interface (NAND, NOR and SRAM)
- External SQI Flash interface
- One 16-bit Extended Function Timer (EFT) with input capture/ output compare and PWM.
- Four 32-bit free running timers/ counters
- Real Time Clock (RTC) circuit
- 3 UARTs (one full for modem support)
- 1 I²C master/slave interface
- 1 Synchronous Serial Port (SSP, Motorola-SPI supported)
- USB2.0 dual role full speed (12 MHz) with integrated physical layer transceiver
- 2 Secure-Digital Multimedia Memory Card Interfaces (SDMMC)
- 2 Controller Area Network (CAN)
- 1 Multichannel Serial Port (MSP)
- GPIO port for a total of up to 64 GPIOs
- 8-channels ADC (10 bit)
- Selectable 1.8 V or 3.3 V I/Os for specific I/O ports
- 3 embedded 1.8 V voltage regulators
- Operating condition:
 - V_{DD12}: 1.2 V ±10 %
 - V_{DD18/RF18}: 1.8 V ±5 %
 - V_{LPVR}: 1.62 V to 3.6 V
 - V_{ddIO}: 1.8 V -5 %/ +10 %; 3.3 V ±10 %
- Package:
 - TFBGA169 9 x 9 x 1.2 mm 0.65 pitch
 - TFBGA169 12 x 12 x 1.2 mm 0.8 pitch
- Ambient temperature range: -40/ +85 °C

Description

STA8088EXG is a single die standalone positioning receiver IC working on multiple constellations (GPS/Galileo/Glonass/QZSS).

By combining the ARM946 microcontroller core with the large number of peripherals/ interfaces, STA8088EXG provides a highly-flexible and cost effective solution for hand-held and telematic applications.

The device is the ideal solution for sensor-based and sensor-less ST Dead Reckoning technologies which enhance positioning accuracy even in areas without GNSS signals, like tunnels and indoor parking.

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1 Overview

STA8088EXG is an integrated System-On-Chip device designed for a highly-flexible and cost effective solution for vehicle, hand-held navigation and telematic applications.

It combines a high performance ARM946 microprocessor with embedded enhanced peripherals and I/O capabilities, RF front-end and base band processor to support GPS, Galileo, Glonass and QZSS satellite systems.

It also provides clock generation via PLL, backup logic with real time clock and it supports USB2.0 standard at full speed.

STA8088EXG is software compatible with the ARM processor family. The device is power supplied with 1.8 V and uses three on-chip voltage regulators to internally supply the RF front-end, core logic the backup logic. In order to reduce the power consumption the chip can be directly powered with 1.2 V bypassing the embedded voltage regulators.

I/O lines are compatible with 1.8 V and 3.3 V.

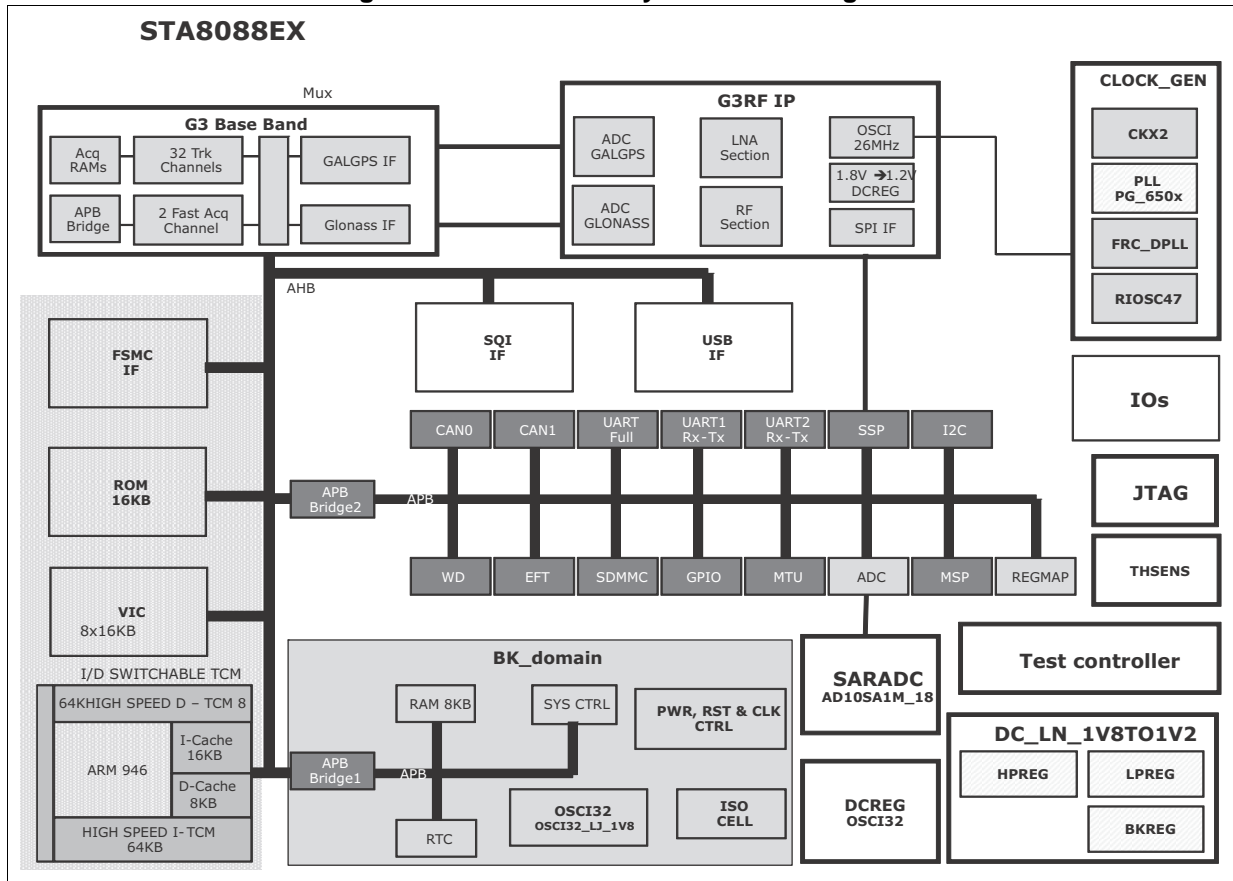
The chip, using STMicroelectronics CMOSRF technology, is housed in a TFBGA169 (9 x 9 x 1.2 mm) and TFBGA169 (12 x 12 x 1.2 mm) packages.

The Automotive Grade devices (see [Figure 4: Ordering information scheme](#)) fulfilling high quality and service level automotive market requirements, is the ideal solution for OEM telematic applications.

2 Pin description

2.1 Block diagram

Figure 1. STA8088EXG system block diagram





2.2 TFBGA169 ball out

Table 1. TFBGA169 ball out Automotive Grade (with CAN)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
|----------|---------------------------|----------------------------|--------------------------------------|-------------------|--------------------------|--------------------------|-------------------------|--------------------------|--------------------------|---------------------|------------------------------------|--------------------------|-------------------------------|
| A | GNDIO | USB_DM (UART1_RX) | USB_DP (UART1_TX) | CAN0TX | FSMC ADD22 (P1.30) | FSMC ADD18 (P1.26) | FSMC ADD9 (P1.17) | FSMC ADD16 (P1.24) | FSMC DATA15 | FSMC DATA8 | FSMC DATA5 | FSMC DATA4 | GNDIO |
| B | VDDIO_r2 | CAN1TX (P0.8) | CAN1RX (P0.9) | CAN0RX | FSMC ADD23 (P1.31) | FSMC ADD19 (P1.27) | FSMC ADD6 (P1.14) | FSMC ADD10 (P1.18) | FSMC DATA14 | FSMC DATA2 | VDDIO_r3 | FSMC BLn1 | FSMC BLn0 |
| C | MSPOUT SCLK (P0.31) | MSPOUT LRCLK (P0.30) | MSPOUT_SD/ Iopwrsel_r2 (P0.29) | VDDIO_r5 | FSMC WTn | FSMC ADD20 (P1.28) | FSMC ADD1 (P1.9) | FSMC ADD14 (P1.22) | FSMC DATA12 | FSMC DATA10 | FSMC CS2 | FSMC_CS3/ Iopwrsel_r3 | FSMC DATA0 |
| D | MMC_CLK | MMC_CMD (P0.28) | VDD18 MVR | VDD12_MVR | FSMC WEN | FSMC ADD21 (P1.29) | FSMC ADD2 (P1.10) | FSMC ADD11 (P1.19) | FSMC CLK | FSMC ADV | FSMC DATA9 | FSMC CS1 | FSMC CS0 |
| E | MMC_D0 (P0.20) | MMC_D1 (P0.21) | MMC_D2 (P0.22) | MMC_D3 (P0.23) | FSMC OutEN | FSMC ADD4 (P1.12) | FSMC ADD7 (P1.15) | FSMC ADD17 (P1.25) | FSMC ADD13 (P1.21) | FSMC DATA1 | FSMC DATA3 | GPIO2 (P0.2) | GPIO5 (P0.5) |
| F | MMC_D4 (P0.24) | MMC_D5 (P0.25) | MMC_D6 (P0.26) | MMC_D7 (P0.27) | FSMC ADD5 (P1.13) | FSMC ADD3 (P1.11) | FSMC ADD0 (P1.8) | FSMC ADD8 (P1.16) | FSMC ADD12 (P1.20) | FSMC DATA7 | SPI_CLK (P1.1) | GPIO1 (P0.1) | GPIO4 (P0.4) |
| G | TMS | TRSTn | TDI | TCK | GND | GND | GND | VDD18 MVR | FSMC DATA11 | FSMC DATA6 | SPI_DO (P1.3) | VDDIO_r1 | GPIO7 (P0.7) |
| H | VRF12 RFADC | TP_IF_P | GND_RF | TDO | VDD12 LPVR | GNDIO | GND | GND | FSMC ADD15 (P1.23) | FSMC DATA13 | SPI_DI (P1.2) | GPIO3 (P0.3) | GPIO6 (P0.6) |
| J | VRF12 LNA | TP_IF_N | GND_RF | GND_RF | STBY_OUT | STBYn | VDD12_MVR | VDD LPVR | VDD12_MVR | PPS_OUT | SPI_CSN/ IOpwrsel_r1 (P1.0) | UART0 RTS (P0.14) | GPIO0 (P0.0) |
| K | LNA IN | GND LNA | GND_RF | GND_RF | GND_RF | GND_RF | WAKEUP | RSTn | ADC_IN8 | VDDIO_r4 | UART2_TX/ BOOT_0 (P1.5) | UART2_RX (P1.4) | UART0_TX/ BOOT_1 (P1.7) |
| L | GND LNA | GND LNA | GND_RF | GND_RF | VRF12 RFVCO | VRF12 RFDIG | ADC_IN1 | ADC_IN4 | ADC_IN2 | SQI_SIO2 (P0.12) | SQI_SCK | UART0 DTR (P0.18) | UART0_RX (P1.6) |
| M | LNA OUT | VRF18 RFVR | GND_RF | GND_RF | VRF12 MIX | XTAL OUT | ADC_IN3 | ADC_IN6 | RTC_XTI | SQI_SIO1 (P0.11) | SQI_Cen/ Iopwrsel_r4 (P0.19) | UART0 CTS (P0.15) | UART0 DSR (P0.16) |
| N | GND_RF | VRF12OUT RFVR | VRF12 RFA | RFA IN | VRF12_IF | XTAL IN | ADC_IN7 | ADC_IN5 | RTC_XTO | SQI_SIO3 (P0.13) | SQI_SIO0 (P0.10) | UART0 DCD (P0.17) | GNDIO |



Table 2. TFBGA169 ball out (no CAN)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
|----------|---------------------------|----------------------------|--------------------------------------|-------------------|--------------------------|--------------------------|-------------------------|--------------------------|--------------------------|---------------------|------------------------------------|--------------------------|-------------------------------|
| A | GNDIO | USB_DM (UART1_RX) | USB_DP (UART1_TX) | N.C. | FSMC ADD22 (P1.30) | FSMC ADD18 (P1.26) | FSMC ADD9 (P1.17) | FSMC ADD16 (P1.24) | FSMC DATA15 | FSMC DATA8 | FSMC DATA5 | FSMC DATA4 | GNDIO |
| B | VDDIO_r2 | I2C_SD (P0.8) | I2C_SCLK (P0.9) | N.C. | FSMC ADD23 (P1.31) | FSMC ADD19 (P1.27) | FSMC ADD6 (P1.14) | FSMC ADD10 (P1.18) | FSMC DATA14 | FSMC DATA2 | VDDIO_r3 | FSMC BLn1 | FSMC BLn0 |
| C | MSPOUT SCLK (P0.31) | MSPOUT LRCLK (P0.30) | MSPOUT_SD/ Iopwrse1_r2 (P0.29) | VDDIO_r5 | FSMC WTn | FSMC ADD20 (P1.28) | FSMC ADD1 (P1.9) | FSMC ADD14 (P1.22) | FSMC DATA12 | FSMC DATA10 | FSMC CS2 | FSMC_CS3/ Iopwrse1_r3 | FSMC DATA0 |
| D | MMC_CLK | MMC_CMD (P0.28) | VDD18 MVR | VDD12_MVR | FSMC WEN | FSMC ADD21 (P1.29) | FSMC ADD2 (P1.10) | FSMC ADD11 (P1.19) | FSMC CLK | FSMC ADV | FSMC DATA9 | FSMC CS1 | FSMC CS0 |
| E | MMC_D0 (P0.20) | MMC_D1 (P0.21) | MMC_D2 (P0.22) | MMC_D3 (P0.23) | FSMC OutEN | FSMC ADD4 (P1.12) | FSMC ADD7 (P1.15) | FSMC ADD17 (P1.25) | FSMC ADD13 (P1.21) | FSMC DATA1 | FSMC DATA3 | GPIO2 (P0.2) | GPIO5 (P0.5) |
| F | MMC_D4 (P0.24) | MMC_D5 (P0.25) | MMC_D6 (P0.26) | MMC_D7 (P0.27) | FSMC ADD5 (P1.13) | FSMC ADD3 (P1.11) | FSMC ADD0 (P1.8) | FSMC ADD8 (P1.16) | FSMC ADD12 (P1.20) | FSMC DATA7 | SPI_CLK (P1.1) | GPIO1 (P0.1) | GPIO4 (P0.4) |
| G | TMS | TRSTn | TDI | TCK | GND | GND | GND | VDD18 MVR | FSMC DATA11 | FSMC DATA6 | SPI_DO (P1.3) | VDDIO_r1 | GPIO7 (P0.7) |
| H | VRF12 RFADC | TP_IF_P | GND_RF | TDO | VDD12 LPVR | GNDIO | GND | GND | FSMC ADD15 (P1.23) | FSMC DATA13 | SPI_DI (P1.2) | GPIO3 (P0.3) | GPIO6 (P0.6) |
| J | VRF12 LNA | TP_IF_N | GND_RF | GND_RF | STBY_OUT | STBYn | VDD12_MVR | VDD LPVR | VDD12_MVR | PPS_OUT | SPI_CSN/ Iopwrse1_r1 (P1.0) | UART0 RTS (P0.14) | GPIO0 (P0.0) |
| K | LNA IN | GND LNA | GND_RF | GND_RF | GND_RF | GND_RF | WAKEUP | RSTn | ADC_IN8 | VDDIO_r4 | UART2_TX/ BOOT_0 (P1.5) | UART2_RX (P1.4) | UART0_TX/ BOOT_1 (P1.7) |
| L | GND LNA | GND LNA | GND_RF | GND_RF | VRF12 RFVCO | VRF12 RFDIG | ADC_IN1 | ADC_IN4 | ADC_IN2 | SQI_SIO2 (P0.12) | SQI_SCK | UART0 DTR (P0.18) | UART0_RX (P1.6) |
| M | LNA OUT | VRF18 RFVR | GND_RF | GND_RF | VRF12 MIX | XTAL OUT | ADC_IN3 | ADC_IN6 | RTC_XTI | SQI_SIO1 (P0.11) | SQI_Cen/ Iopwrse1_r4 (P0.19) | UART0 CTS (P0.15) | UART0 DSR (P0.16) |
| N | GND_RF | VRF12OUT RFVR | VRF12 RFA | RFA IN | VRF12_IF | XTAL IN | ADC_IN7 | ADC_IN5 | RTC_XTO | SQI_SIO3 (P0.13) | SQI_SIO0 (P0.10) | UART0 DCD (P0.17) | GNDIO |

2.3 Power supply pins

Table 3. Power supply pins

| Symbol | I/O | Functions | TFBGA169 |
|---------------|-----|--|--|
| VDD18_MVR | Pwr | Digital supply voltage for main voltage regulator (1.8 V) | D3, G8 |
| VDD12_MVR | Pwr | Digital supply voltage for core circuitry (1.2 V). When using the MVR, this pin shall not be driven by an external voltage supply, but a capacitance shall be connected between these pins and GND to guarantee on-chip voltage stability. | J7, D4, J9 |
| VDD_LPVR | Pwr | Digital supply voltage for low power voltage regulator (1.62 V - 3.6 V) | J8 |
| VDD12_LPVR | Pwr | Digital supply voltage for backup logic (1.2 V). When using the LPVR, this pin shall not be driven by an external voltage supply, but a capacitance shall be connected between these pins and GND to guarantee on-chip voltage stability. | H5 |
| VDD_IOR1 | Pwr | Digital supply voltage for I/O ring 1 (1.8 V or 3.3 V) | G12 |
| VDD_IOR2 | Pwr | Digital supply voltage for I/O ring 2 (1.8 V or 3.3 V) | B1 |
| VDD_IOR3 | Pwr | Digital supply voltage for I/O ring 3 (1.8 V or 3.3 V) | B11 |
| VDD_IOR4 | Pwr | Digital supply voltage for I/O ring 4 (1.8 V or 3.3 V) | K10 |
| VDD_IOR5 | Pwr | Digital supply voltage for I/O ring 5 (3.3 V) | C4 |
| VRF18_RFVR | Pwr | Analog supply voltage for RF voltage regulator (1.8 V) | M2 |
| GND | GND | Digital supply ground for core (5 pins) | G5, G6, G7, H7, H8 |
| GND_IO | GND | Digital supply ground for I/O circuitry (4 pins) | A1, A13, H6, N13 |
| VRF12OUT_RFVR | Pwr | RF voltage regulator 1.2 V output | N2 |
| VRF12_LNA | Pwr | Analog supply voltage for LNA (1.2 V) | J1 |
| VRF12_RFA | Pwr | Analog supply voltage for RFA (1.2 V) | N3 |
| VRF12_Mix | Pwr | Analog supply voltage for Mixer (1.2 V) | M5 |
| VRF12_IF | Pwr | Analog supply voltage for IF (1.2 V) | N5 |
| VRF12_RFDig | Pwr | Analog supply voltage for RF Digital (1.2 V) | L6 |
| VRF12_RFVCO | Pwr | Analog supply voltage for VCO (1.2 V) | L5 |
| VRF12_RFADC | Pwr | Analog supply voltage for RF ADC (1.2 V) | H1 |
| GND_LNA | GND | Analog supply ground for LNA (3 pins) | K2, L1, L2 |
| GND_RF | GND | Analog supply ground to RF (12 pins) | H3, J3, J4, K3, K4, K5, K6, L3, L4, M3, M4, N1 |

2.4 Main function pins

Table 4. Main function pins

| Symbol | I/O voltage | I/O | Functions | TFBGA169 |
|-----------------------|--------------------------|-------|---|--------------------------------------|
| RSTn ⁽¹⁾ | 1.2 V | I | Reset Input with Schmitt-Trigger characteristics and noise filter. | K8 |
| STDBYn | 1.2 V | I | When low, the chip is forced in Standby mode. All pins in high impedance except the ones powered by backup supply | J6 |
| WAKEUP ⁽²⁾ | 1.2 V | I | WAKEUP from STANDBY mode | K7 |
| STDBY_Out | 1.2 V | O | When low, indicates the chip is in Standby mode. | J5 |
| PPS_Out | VDD_IOR1 | O | Pulsed per second output | J10 |
| RTC_XTI | 1.5 V (max) | I | Input of the 32 KHz oscillator amplifier circuit and input of the internal real time clock circuit. | M9 |
| RTC_XTO | 1.5 V (max) | O | Output of the oscillator amplifier circuit. | N9 |
| CAN0TX ⁽³⁾ | VDD_IOR5 | O | CAN 0 - transmit data output | A4 |
| CAN0RX ⁽³⁾ | VDD_IOR5 | I | CAN 0 - receive data input | B4 |
| USB_DM/UART1_RX | VDD_IOR5 | USB/I | USB D- signal / UART 1 Rx data | A2 |
| USB_DP/UART1_TX | VDD_IOR5 | USB/O | USB D+ signal / UART 1 Tx data | A3 |
| ADC_IN[1:8] | 1.4 V – 0 V typ range | I | ADC analog input [1:8] | L7, L9, M7, L8, N8, M8, N7, K9 |
| MMC_CLK | VDD_IOR2 | O | MMC_CLK: multimedia clock line | D1 |

1. When RSTn is de-asserted, pin WAKEUP must be low.
2. The WAKEUP pulse must be longer than 500 µs.
3. Only for Automotive Grade devices.

2.5 Test / emulated dedicated pins

Table 5. Test/emulated dedicated pins

| Symbol | I/O Voltage | I/O | Functions | TFBGA169 |
|----------------------|-------------|-----|------------------------------------|----------|
| TCK | VDD_IOR5 | I | JTAG test clock | G4 |
| TDI | VDD_IOR5 | I | JTAG test data in | G3 |
| TDO | VDD_IOR5 | O | JTAG test data out | H4 |
| TMS | VDD_IOR5 | I | JTAG test mode select | G1 |
| TRSTn ⁽¹⁾ | VDD_IOR5 | I | JTAG test circuit reset | G2 |
| TP_IF_P | VRF12_IF | O | Diff. test point for IF – positive | H2 |
| TP_IF_N | VRF12_IF | O | Diff. test point for IF – negative | J2 |

1. If JTAG interface is not used, pin TRSTn must be asserted low.

2.6 FSMC external memory interface pins

Table 6. FSMC memory interface pins

| Symbol | I/O Voltage | I/O | Functions | TFBGA169 |
|----------------------------------|-------------|-----|--|--|
| FSMC_Data[15:0] | VDD_IOR3 | I/O | FSMC EMI data bus | C13, E10, B10, E11, A12, A11, G10, F10, A10, D11, C10, G9, C9, H10, B9, A9 |
| FSMC_Add[23:0] ⁽¹⁾⁽²⁾ | VDD_IOR3 | O | FSMC EMI address bus | F7, C7, D7, F6, E6, F5, B7, E7, F8, A7, B8, D8, F9, E9, C8, H9, A8, E8, A6, B6, C6, D6, A5, B5 |
| FSMC_OutEN | VDD_IOR3 | O | FSMC EMI output enable | E5 |
| FSMC_WEN | VDD_IOR3 | O | FSMC EMI write enable | D5 |
| FSMC_WTn | VDD_IOR3 | I | FSMC EMI wait (SNOR, CRAM) | C5 |
| FSMC_BLn[0,1] | VDD_IOR3 | O | FSMC EMI byte lane | B13, B12 |
| FSMC_CLK | VDD_IOR3 | O | FSMC EMI clk | D9 |
| FSMC_ADV | VDD_IOR3 | O | FSMC EMI address valid | D10 |
| FSMC_CS0 | VDD_IOR3 | O | FSMC EMI chip select for external memory bank 0 | D13 |
| FSMC_CS1 | VDD_IOR3 | O | FSMC EMI chip select for external memory bank 1 | D12 |
| FSMC_CS2 | VDD_IOR3 | O | FSMC EMI chip select for external memory bank 2 | C11 |
| FSMC_CS3/ iopwrsel_r3 | VDD_IOR3 | O | FSMC EMI chip select for external memory bank 3 / I/O ring 3 power selection | C12 |

1. FSMC_Add[23:0] are multiplexed with P1[31:8] - see [Table 9](#)
2. In case of NAND memory usage the
FSMC_Add16 is used as CLE
FSMC_Add17 is used as ALE

2.7 SQI pins

Table 7. SQI pins

| Symbol | I/O Voltage | I/O | Functions | TFBGA169 |
|-------------|-------------|-----|-------------------------------|----------|
| SQI_SIO3 | VDD_IOR4 | I/O | SQI Flash data I/O 3 | N10 |
| SQI_SIO2 | VDD_IOR4 | I/O | SQI Flash data I/O 2 | L10 |
| SQI_SIO1/SO | VDD_IOR4 | I/O | SQI Flash data I/O 1 / ser. O | M10 |
| SQI_SIO0/SI | VDD_IOR4 | I/O | SQI Flash data I/O 0 / ser. I | N11 |

Table 7. SQI pins (continued)

| Symbol | I/O Voltage | I/O | Functions | TFBGA169 |
|-------------------------|-------------|-----|--|----------|
| SQI_SCK | VDD_IOR4 | O | SQI Flash clock | L11 |
| SQI_CEn/ iopwrsel_r4 | VDD_IOR4 | O | SQI Flash chip enable / I/O ring 4 power selection | M11 |

SQI pins are multiplexed with P0[13:10] and P0[19] (see [Table 8](#)).

2.8 Port 0 pins

Port 0 consists of a 32-bit bidirectional I/O port. It can be either used as general purpose input or output port, or configured according to the associated alternate functions.

Table 8. Port 0 pins

| Symbol | I/O voltage | I/O | Mode | Functions | TFBGA169 |
|--------|-------------|-----|---------|--|----------|
| P0.0 | VDD_IOR1 | I/O | Default | GPIO.0: general purpose I/O | J13 |
| | | I | A | PPS_IN: pulse per second input | |
| | | O | B | PPS_Out: pulse per second output | |
| | | O | C | SQI_CEn: SQI Flash chip enable | |
| P0.1 | VDD_IOR1 | I/O | Default | GPIO.1: general purpose I/O | F12 |
| | | O | A | RTC_CLKO: RTC clock out | |
| P0.2 | VDD_IOR1 | I/O | Default | GPIO.2: general purpose I/O | E12 |
| | | O | A | MMC2_CLK: MMC 2 clock line | |
| P0.3 | VDD_IOR1 | I/O | Default | GPIO.3: general purpose I/O | H12 |
| | | I/O | A | MMC2_CMD: MMC 2 command line | |
| P0.4 | VDD_IOR1 | I/O | Default | GPIO.4: general purpose I/O | F13 |
| | | I/O | A | MMC2_DATA3: MMC 2 data 3 | |
| P0.5 | VDD_IOR1 | I/O | Default | GPIO.5: general purpose I/O | E13 |
| | | I/O | A | MMC2_DATA2: MMC 2 data 2 | |
| P0.6 | VDD_IOR1 | I/O | Default | GPIO.6: general purpose I/O | H13 |
| | | I/O | A | MMC2_DATA1: MMC 2 data 1 | |
| P0.7 | VDD_IOR1 | I/O | Default | GPIO.7: general purpose I/O | G13 |
| | | I/O | A | MMC2_DATA0: MMC 2 data 0 | |
| P0.8 | VDD_IOR5 | O | Default | CAN1TX ⁽¹⁾ : CAN 1 transmit data output | B2 |
| | | I/O | A | GPIO.8: general purpose I/O | |
| | | I/O | B | I2C_SD: I2C serial data | |

Table 8. Port 0 pins (continued)

| Symbol | I/O voltage | I/O | Mode | Functions | TFBGA169 |
|--------|-------------|-----|---------|---|----------|
| P0.9 | VDD_IOR5 | I | Default | CAN1RX ⁽¹⁾ : CAN 1 receive data input | B3 |
| | | I/O | A | GPIO.9: general purpose I/O | |
| | | O | B | I2C_SCLK: I2C clock | |
| P0.10 | VDD_IOR4 | I/O | Default | SQI_SIO0/SI: SQI Flash data I/O 0 / ser. I | N11 |
| | | I/O | A | GPIO10: general purpose I/O | |
| P0.11 | VDD_IOR4 | I/O | Default | SQI_SIO1/SO: SQI Flash data I/O 1 / ser. O | M10 |
| | | I/O | A | GPIO11: general purpose I/O | |
| P0.12 | VDD_IOR4 | I/O | Default | SQI_SIO2: SQI Flash data I/O 2 | L10 |
| | | I/O | A | GPIO12: general purpose I/O | |
| P0.13 | VDD_IOR4 | I/O | Default | SQI_SIO3: SQI Flash data I/O 3 | N10 |
| | | I/O | A | GPIO13: general purpose I/O | |
| P0.14 | VDD_IOR1 | O | Default | UART0_RTS: UART0 request to send | J12 |
| | | I/O | A | GPIO14: general purpose I/O | |
| | | I | C | MSPIN_sclk: MSP serial clock input | |
| P0.15 | VDD_IOR1 | I | Default | UART0_CTS: UART0 clear to send | M12 |
| | | I/O | A | GPIO15: general purpose I/O | |
| | | I | B | Timer_ICAPA: extended function timer - input capture A | |
| | | I | C | MSPIN_lrcclk: MSP left/right clock input | |
| P0.16 | VDD_IOR1 | I | Default | UART0_DSR: UART0 data set ready | M13 |
| | | I/O | A | GPIO16: general purpose I/O | |
| | | O | B | Timer_OCMPA: extended function timer – output compare A | |
| | | I | C | MSPIN_SD: MSP serial data input | |
| P0.17 | VDD_IOR1 | I | Default | UART0_DCD: UART0 data carrier detect | N12 |
| | | I/O | A | GPIO17: general purpose I/O | |
| | | I | B | Timer_ICAPB: extended function timer - input capture B | |
| P0.18 | VDD_IOR1 | O | Default | UART0_DTR: UART0 data terminal read | L12 |
| | | I/O | A | GPIO18: general purpose I/O | |
| | | O | B | Timer_OCMPB: extended function timer – output compare B | |
| P0.19 | VDD_IOR4 | O | Default | SQI_Cen/iopwrsel_r4: SQI Flash chip enable / I/O ring 4 power selection | M11 |
| | | I/O | A | GPIO19: general purpose I/O | |

Table 8. Port 0 pins (continued)

| Symbol | I/O voltage | I/O | Mode | Functions | TFBGA169 |
|--------|-------------|-----|---------|--|----------|
| P0.20 | VDD_IOR2 | I/O | Default | MMC_DATA0: multimedia card data 0 | E1 |
| | | I/O | A | GPIO20: general purpose I/O | |
| | | O | B | MAG_0GNS: GNS 3bit coding output (MAG0) | |
| P0.21 | VDD_IOR2 | I/O | Default | MMC_DATA1: multimedia card data 1 | E2 |
| | | I/O | A | GPIO21: general purpose I/O | |
| | | O | B | MAG_1GNS: GNS 3bit coding output (MAG1) | |
| P0.22 | VDD_IOR2 | I/O | Default | MMC_DATA2: multimedia card data 2 | E3 |
| | | I/O | A | GPIO22: general purpose I/O | |
| | | I/O | B | MAG_0GGPS: GGPS 3bit coding output (MAG0) | |
| P0.23 | VDD_IOR2 | I/O | Default | MMC_DATA3: multimedia card data 3 | E4 |
| | | I/O | A | GPIO23: general purpose I/O | |
| | | I/O | B | MAG_1GGPS: GGPS 3bit coding output (MAG1) | |
| P0.24 | VDD_IOR2 | I/O | Default | MMC_DATA4: multimedia card data 4 | F1 |
| | | I/O | A | GPIO24: general purpose I/O | |
| P0.25 | VDD_IOR2 | I/O | Default | MMC_DATA5: multimedia card data 5 | F2 |
| | | I/O | A | GPIO25: general purpose I/O | |
| P0.26 | VDD_IOR2 | I/O | Default | MMC_DATA6: multimedia card data 6 | F3 |
| | | I/O | A | GPIO26: general purpose I/O | |
| P0.27 | VDD_IOR2 | I/O | Default | MMC_DATA7: multimedia card data 7 | F4 |
| | | I/O | A | GPIO27: general purpose I/O | |
| P0.28 | VDD_IOR2 | I/O | Default | MMC_CMD: multimedia card command line | D2 |
| | | I/O | A | GPIO28: general purpose I/O | |
| P0.29 | VDD_IOR2 | O | Default | MSPout_SDAT/iopwrse1_r2: MSP serial data output/ I/O ring 2 power selection | C3 |
| | | I/O | A | GPIO29: general purpose I/O | |
| P0.30 | VDD_IOR2 | O | Default | MSPout_LRCLK MSP left/right clock output | C2 |
| | | I/O | A | GPIO30: general purpose I/O | |
| P0.31 | VDD_IOR2 | O | Default | MSPout_SCLK: MSP serial clock output | C1 |
| | | I/O | A | GPIO31: general purpose I/O | |
| | | O | B | PRNSEQ0 | |

1. Only for Automotive Grade devices.

2.9 Port 1 pins

Port 1 consists of a 32-bit bidirectional I/O port. It can be either used as general purpose input or output port, or configured according to the associated alternate functions.

Table 9. Port 1 pins

| Symbol | I/O Voltage | I/O | Mode | Functions | TFBGA169 |
|--------|-------------|-----|---------|--|----------|
| P1.0 | VDD_IOR1 | O | Default | SSP_CSN/iopwrsel_r1: SSP chip select active low / I/O ring 1 power selection | J11 |
| | | I/O | A | GPIO32: general purpose I/O | |
| | | I/O | B | SignGGPS: GGPS 3bit coding output (Sign) | |
| | | O | C | SQI_Cen: SQI Flash chip enable | |
| P1.1 | VDD_IOR1 | I/O | Default | SSP_CLK: SSP clock | F11 |
| | | I/O | A | GPIO33: general purpose I/O | |
| | | I/O | B | Clock_GGPS: GGPS clock out | |
| | | O | C | SQI_Clk: SQI Flash clock | |
| P1.2 | VDD_IOR1 | I | Default | SSP_DI: SSP serial data input | H11 |
| | | I/O | A | GPIO34: general purpose I/O | |
| | | I/O | B | SignGNS: GNS 3bit coding output (Sign) | |
| | | I/O | C | SQI_SIO0/SI: SQI Flash data I/O 0 / ser. I | |
| P1.3 | VDD_IOR1 | O | Default | SSP_DO: SSP serial data output | G11 |
| | | I/O | A | GPIO35: general purpose I/O | |
| | | I/O | B | Clock_GNS: GNS clock out | |
| | | I/O | C | SQI_SIO1/SO: SQI Flash data I/O 1 / ser. O | |
| P1.4 | VDD_IOR1 | I | Default | UART2_RX: UART 2 Rx data | K12 |
| | | I/O | A | GPIO36: general purpose I/O | |
| P1.5 | VDD_IOR1 | O | Default | UART2_TX: UART 2 Tx data / ARM Boot 0 | K11 |
| | | I/O | A | GPIO37: general purpose I/O | |
| P1.6 | VDD_IOR1 | I | Default | UART0_RX: UART 0 Rx data | L13 |
| | | I/O | A | GPIO38: general purpose I/O | |
| | | I/O | C | SQI_SIO2: SQI Flash data I/O 2 | |
| P1.7 | VDD_IOR1 | O | Default | UART0_TX: UART 0 Tx data / ARM Boot 1 | K13 |
| | | I/O | A | GPIO39: general purpose I/O | |
| | | I/O | C | SQI_SIO3: SQI Flash data I/O 3 | |
| P1.8 | VDD_IOR3 | O | Default | FSMC_Add0: FSMC EMI address bus 0 | F7 |
| | | I/O | A | GPIO40: general purpose I/O | |

Table 9. Port 1 pins (continued)

| Symbol | I/O Voltage | I/O | Mode | Functions | TFBGA169 |
|--------|-------------|-----|---------|---|----------|
| P1.9 | VDD_IOR3 | O | Default | FSMC_Add1: FSMC EMI address bus 1 | C7 |
| | | I/O | A | GPIO41: general purpose I/O | |
| P1.10 | VDD_IOR3 | O | Default | FSMC_Add2: FSMC EMI address bus 2 | D7 |
| | | I/O | A | GPIO42: general purpose I/O | |
| P1.11 | VDD_IOR3 | O | Default | FSMC_Add3: FSMC EMI address bus 3 | F6 |
| | | I/O | A | GPIO43: general purpose I/O | |
| P1.12 | VDD_IOR3 | O | Default | FSMC_Add4: FSMC EMI address bus 4 | E6 |
| | | I/O | A | GPIO44: general purpose I/O | |
| P1.13 | VDD_IOR3 | O | Default | FSMC_Add5: FSMC EMI address bus 5 | F5 |
| | | I/O | A | GPIO45: general purpose I/O | |
| P1.14 | VDD_IOR3 | O | Default | FSMC_Add6: FSMC EMI address bus 6 | B7 |
| | | I/O | A | GPIO46: general purpose I/O | |
| P1.15 | VDD_IOR3 | O | Default | FSMC_Add7: FSMC EMI address bus 7 | E7 |
| | | I/O | A | GPIO47: general purpose I/O | |
| P1.16 | VDD_IOR3 | O | Default | FSMC_Add8: FSMC EMI address bus 8 | F8 |
| | | I/O | A | GPIO48: general purpose I/O | |
| P1.17 | VDD_IOR3 | O | Default | FSMC_Add9: FSMC EMI address bus 9 | A7 |
| | | I/O | A | GPIO49: general purpose I/O | |
| P1.18 | VDD_IOR3 | O | Default | FSMC_Add10: FSMC EMI address bus 10 | B8 |
| | | I/O | A | GPIO50: general purpose I/O | |
| P1.19 | VDD_IOR3 | O | Default | FSMC_Add11: FSMC EMI address bus 11 | D8 |
| | | I/O | A | GPIO51: general purpose I/O | |
| P1.20 | VDD_IOR3 | O | Default | FSMC_Add12: FSMC EMI address bus 12 | F9 |
| | | I/O | A | GPIO52: general purpose I/O | |
| P1.21 | VDD_IOR3 | O | Default | FSMC_Add13: FSMC EMI address bus 13 | E9 |
| | | I/O | A | GPIO53: general purpose I/O | |
| P1.22 | VDD_IOR3 | O | Default | FSMC_Add14: FSMC EMI address bus 14 | C8 |
| | | I/O | A | GPIO54: general purpose I/O | |
| P1.23 | VDD_IOR3 | O | Default | FSMC_Add15: FSMC EMI address bus 15 | H9 |
| | | O | A | TCXO_CLK | |
| P1.24 | VDD_IOR3 | O | Default | FSMC_Add16/CLE: FSMC EMI address bus 16/CLE | A8 |
| | | I/O | A | GPIO56: general purpose I/O | |

Table 9. Port 1 pins (continued)

| Symbol | I/O Voltage | I/O | Mode | Functions | TFBGA169 |
|--------|-------------|-----|---------|---|----------|
| P1.25 | VDD_IOR3 | O | Default | FSMC_Add17/ALE: FSMC EMI address bus 17/ALE | E8 |
| | | I/O | A | GPIO57: general purpose I/O | |
| P1.26 | VDD_IOR3 | O | Default | FSMC_Add18: FSMC EMI address bus 18 | A6 |
| | | I/O | A | GPIO58: general purpose I/O | |
| P1.27 | VDD_IOR3 | O | Default | FSMC_Add19: FSMC EMI address bus19 | B6 |
| | | I/O | A | GPIO59: general purpose I/O | |
| P1.28 | VDD_IOR3 | O | Default | FSMC_Add20: FSMC EMI address bus 20 | C6 |
| | | I/O | A | GPIO60: general purpose I/O | |
| P1.29 | VDD_IOR3 | O | Default | FSMC_Add21: FSMC EMI address bus 21 | D6 |
| | | I/O | A | GPIO61: general purpose I/O | |
| P1.30 | VDD_IOR3 | O | Default | FSMC_Add22: FSMC EMI address bus 22 | A5 |
| | | I/O | A | GPIO62: general purpose I/O | |
| P1.31 | VDD_IOR3 | O | Default | FSMC_Add23: FSMC EMI address bus 23 | B5 |
| | | I/O | A | GPIO63: general purpose I/O | |

2.10 RF front-end pins

Table 10. RF front-end pins

| Symbol | I/O Voltage | I/O | Functions | TFBGA169 |
|----------|-------------|-----|--|----------|
| LNA_IN | VRF12_LNA | I | Low noise amplifier input | K1 |
| LNA_OUT | VRF12_LNA | O | Low noise amplifier output | M1 |
| RFA_IN | VRF12_RFA | I | RF amplifier input | N4 |
| XTAL_In | VRF12_RFDig | I | Input side of crystal oscillator or TCXO input | N6 |
| XTAL_Out | VRF12_RFDig | O | Output side of crystal oscillator | M6 |

3 Package and packing information

3.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

3.2 TFBGA169 9 x 9 x 1.2 mm package information

Table 11. TFBGA169 9 x 9 x 1.2 mm mechanical data

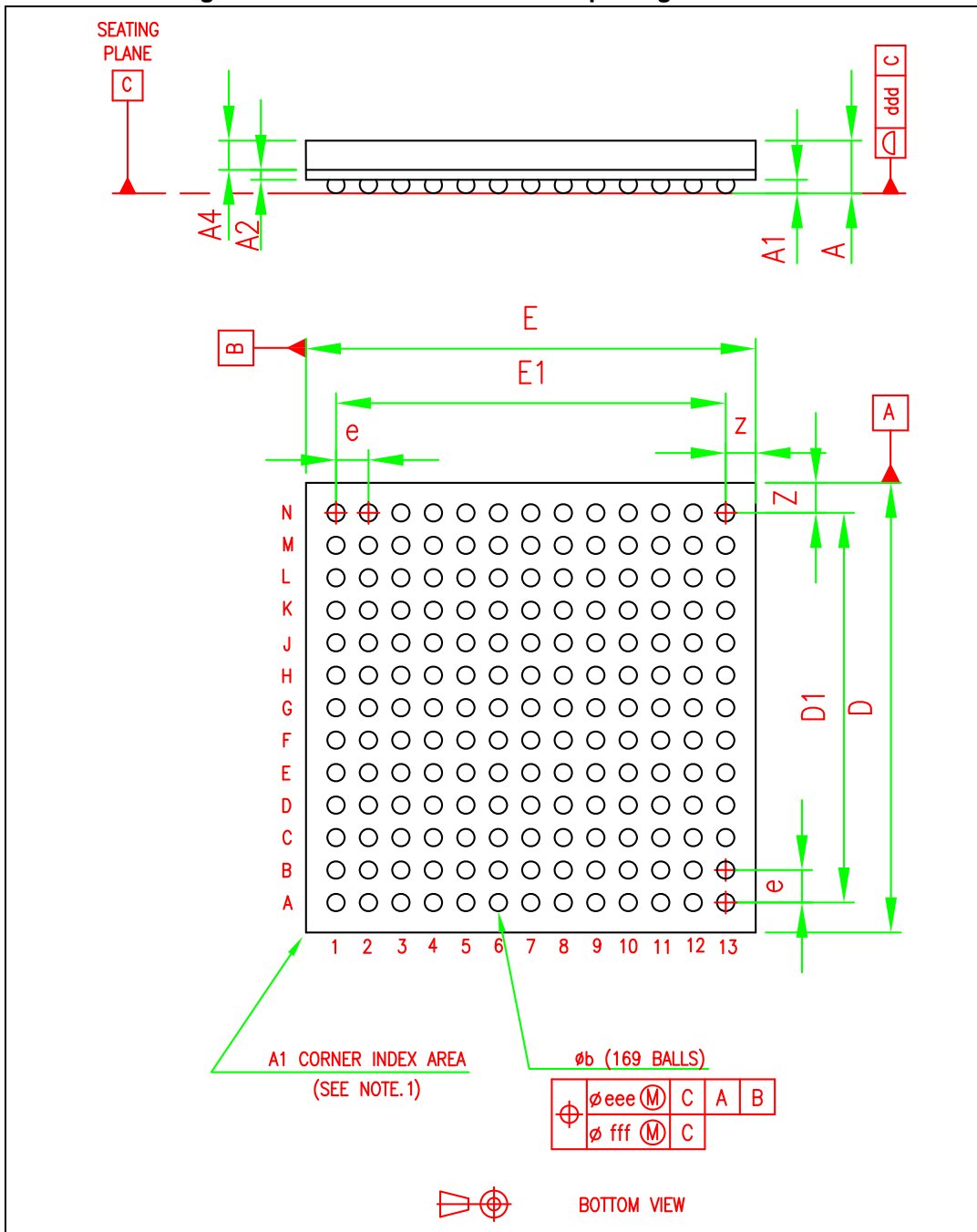
| Ref. dim | Data book (mm) | | | Drawing (mm) | | |
|--------------------|----------------|-------|------|--------------|-------|------|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A ⁽¹⁾ | | | 1.20 | | | 1.07 |
| A1 ⁽²⁾ | 0.21 | | | 0.22 | 0.27 | 0.32 |
| A2 | | 0.20 | | 0.16 | 0.20 | 0.24 |
| A4 | | 0.585 | | 0.57 | 0.585 | 0.60 |
| b ⁽³⁾ | 0.30 | 0.35 | 0.40 | 0.30 | 0.35 | 0.40 |
| D | 8.85 | 9.00 | 9.15 | 8.90 | 9.00 | 9.10 |
| D1 | | 7.80 | | | 7.80 | |
| E | 9.85 | 9.00 | 9.15 | 8.90 | 9.00 | 9.10 |
| E1 | | 7.80 | | | 7.80 | |
| e | | 0.65 | | | 0.65 | |
| Z | | 0.60 | | | 0.60 | |
| ddd | | | 0.08 | | | 0.08 |
| eee ⁽⁴⁾ | | | 0.15 | | | 0.15 |
| fff ⁽⁵⁾ | | | 0.05 | | | 0.05 |

- TFBGA stands for Thin profile Fine Pitch Ball Grid Array.
 - The total profile height (Dim A) is measured from the seating plane to the top of the component
 - The maximum total package height is calculated by the following methodology:
 $A_{Max} = A1_{Typ} + A2_{Typ} + A4_{Typ} + \sqrt{A1^2 + A2^2 + A4^2}$ tolerance values
 - Thin profile: 1.00 mm < A ≤ 1.20 mm / Fine pitch: e < 1.00 mm pitch.
- The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug.
 - A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.
- The typical ball diameter before mounting is 0.35 mm.
- The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.



- The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e . The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.

Figure 2. TFBGA169 9 x 9 x 1.2 mm package dimension



- The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug.
 - A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

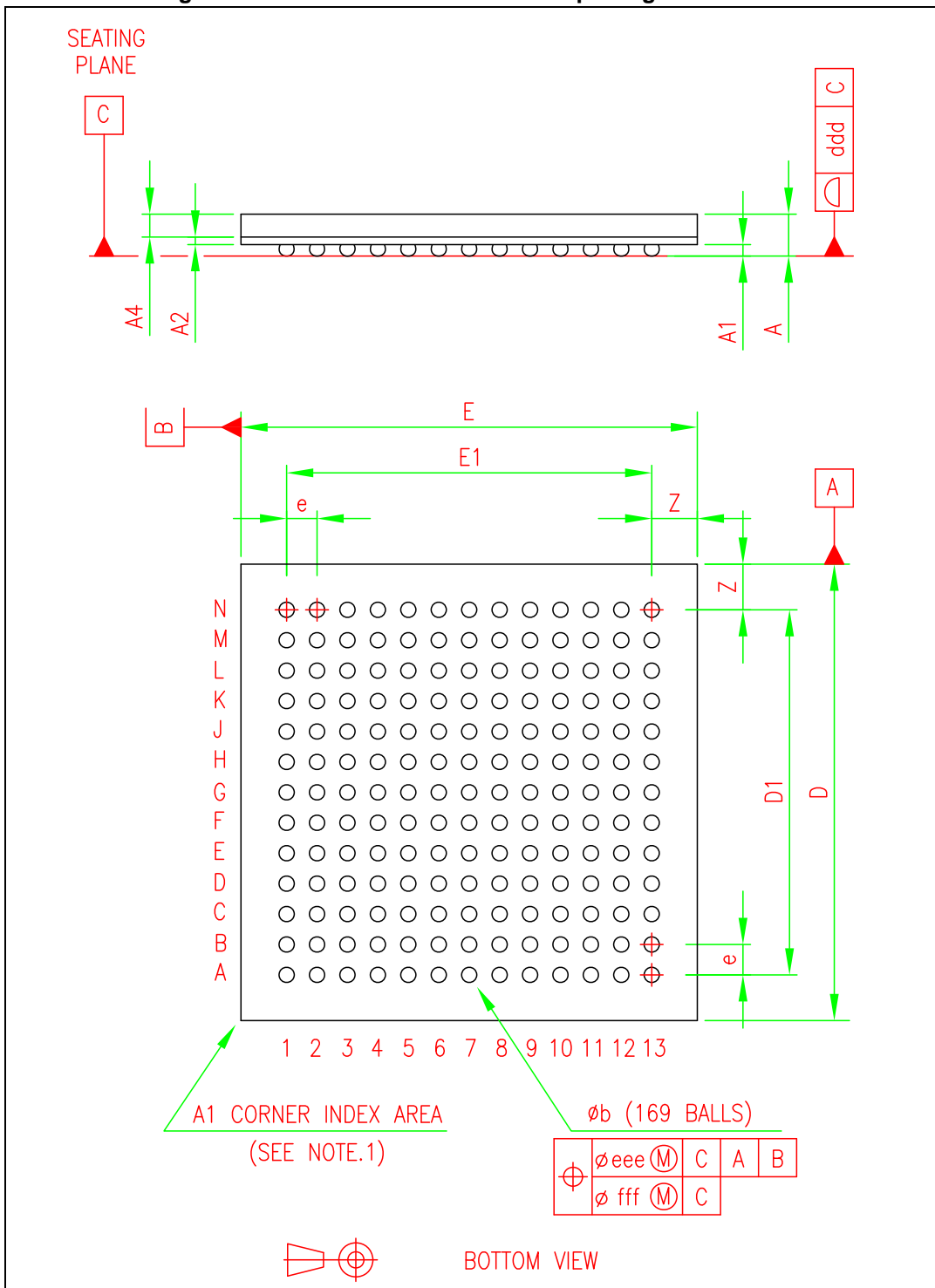
3.3 TFBGA169 12 x 12 x 1.2 mm package information

Table 12. TFBGA169 12 x 12 x 1.2 mm mechanical data

| Ref. dim | Data book (mm) | | | Drawing (mm) | | |
|--------------------|----------------|-------|-------|--------------|-------|-------|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A ⁽¹⁾ | | | 1.20 | | | 1.15 |
| A1 ⁽²⁾ | 0.21 | | | 0.25 | 0.30 | 0.35 |
| A2 | | 0.20 | | 0.16 | 0.20 | 0.24 |
| A4 | | | 0.60 | 0.57 | 0.585 | 0.60 |
| b ⁽³⁾ | 0.35 | 0.40 | 0.45 | 0.35 | 0.40 | 0.45 |
| D | 11.85 | 12.00 | 11.85 | 11.90 | 12.00 | 12.10 |
| D1 | | 9.60 | | | 9.60 | |
| E | 11.85 | 12.00 | 11.85 | 11.90 | 12.00 | 12.10 |
| E1 | | 9.60 | | | 9.60 | |
| e | | 0.80 | | | 0.80 | |
| Z | | 1.20 | | | 1.20 | |
| ddd | | | 0.10 | | | 0.10 |
| eee ⁽⁴⁾ | | | 0.15 | | | 0.15 |
| fff ⁽⁵⁾ | | | 0.08 | | | 0.08 |

- TFBGA stands for Thin Profile Fine Pitch Ball Grid Array.
 - Thin profile: 1.00mm < A . 1.20mm / Fine pitch: e < 1.00mm.
 - The total profile height (Dim A) is measured from the seating plane gCh to the top of the component.
 - The maximum total package height is calculated by the RSS method (Root Sum Square):
 $A_{Max} = A1_{Typ} + A2_{Typ} + A4_{Typ} + \tilde{a}$ (A12 + A22 + A42 tolerance values).
- The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heat slug.
 - A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.
- The typical ball diameter before mounting is 0.40 mm.
- The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
- The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above The axis of each ball must lie simultaneously in both tolerance zones.

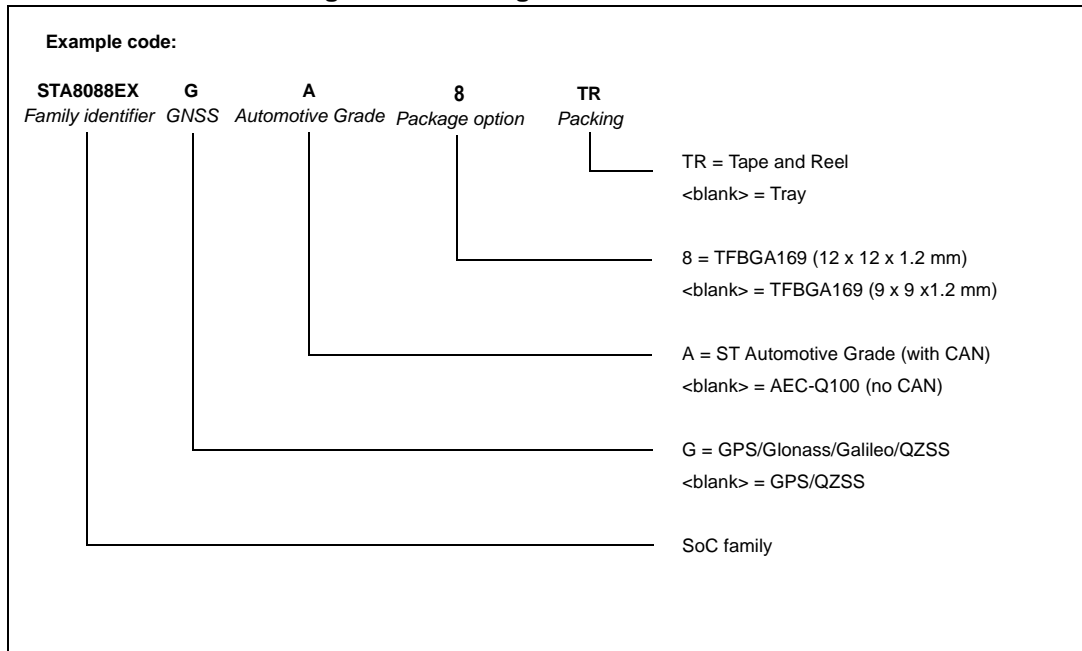
Figure 3. TFBGA169 12 x 12 x 1.2 mm package dimension



- The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heat slug.
 - A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

4 Ordering information

Figure 4. Ordering information scheme



5 Revision history

Table 13. Document revision history

| Date | Revision | Changes |
|--------------|----------|--|
| 23-Jan-2012 | 1 | Initial release. |
| 26-Mar-2012 | 2 | Updated Features list Table 4: Main function pins : – USB_DP/UART1_TX, USB_DM/UART1_RX: updated I/O Added Section 3.3: TFBGA169 12 x 12 x 1.2 mm package information Updated Figure 4: Ordering information scheme |
| 14-Dec-2012 | 3 | Changed document title from “Flexible GPS/Galileo/Glonass/QZSS receiver with high performance processing (ARM9)” to “Flexible GPS/Galileo/Glonass/Compass/QZSS receiver with high performance processing (ARM9)” Features , Description , Chapter 1: Overview and Figure 4: Ordering information scheme : added Compass constellation |
| 16-Sept-2013 | 4 | Updated Disclaimer |
| 07-Jan-2014 | 5 | Removed Compass features. |
| 24-Sep-2014 | 6 | Table 4: Main function pins : – RSTn, WAKEUP: added note Table 5: Test/emulated dedicated pins : – TRSTn: added note |

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