

## E Series Power MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V) at $T_J$ max.	650
$R_{DS(on)}$ typ. ( $\Omega$ ) at 25 °C	$V_{GS} = 10$ V   0.082
$Q_g$ max. (nC)	132
$Q_{gs}$ (nC)	22
$Q_{gd}$ (nC)	46
Configuration	Single

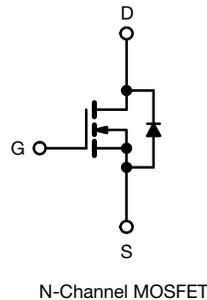
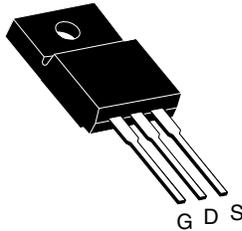
### FEATURES

- A specific on resistance ( $m\Omega\text{-cm}^2$ ) reduction of 25 %
- Low figure-of-merit (FOM)  $R_{on} \times Q_g$
- Low input capacitance ( $C_{iss}$ )
- Reduced switching and conduction losses
- Ultra low gate charge ( $Q_g$ )
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### TO-220 FULLPAK



### APPLICATIONS

- Power factor correction power supplies (PFC)
- Hard switching PWM stages
- Computing
  - Switch mode power supplies (SMPS)
- Lighting
  - Light emitting diode (LED)
  - High intensity discharge (HID)
- Telecom
  - Server power supplies
- Renewable energy
  - Photovoltaic inverters
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Uninterruptable power supplies

### ORDERING INFORMATION

Package	TO-220 FULLPAK
Lead (Pb)-free and Halogen-free	SiHF35N60E-GE3

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	600	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	
Continuous Drain Current ( $T_J = 150$ °C) <sup>e</sup>	$V_{GS}$ at 10 V	$T_C = 25$ °C	32
		$T_C = 100$ °C	20
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	80	A
Linear Derating Factor		0.31	W/°C
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	691	mJ
Maximum Power Dissipation	$P_D$	39	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	°C
Drain-Source Voltage Slope	$dV/dt$	57	V/ns
Reverse Diode $dV/dt$ <sup>d</sup>			
Soldering Recommendations (Peak temperature) <sup>c</sup>	For 10 s	300	°C
Mounting Torque	M3 screw	0.6	Nm

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 140$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 7$  A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$ ,  $dI/dt = 100$  A/ $\mu$ s, starting  $T_J = 25$  °C.
- Limited by maximum junction temperature.

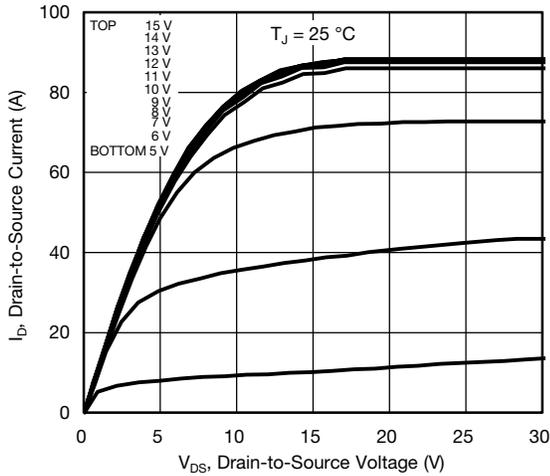
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	65	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	3.2	

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		600	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$		-	0.70	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2	-	4	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
		$V_{GS} = \pm 30\text{ V}$		-	-	$\pm 1$	$\mu\text{A}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$		-	-	1	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	25	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 17\text{ A}$	-	0.082	0.094	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 30\text{ V}, I_D = 17\text{ A}$		-	13	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V},$ $V_{DS} = 100\text{ V},$ $f = 1\text{ MHz}$		-	2760	-	pF
Output Capacitance	$C_{oss}$			-	118	-	
Reverse Transfer Capacitance	$C_{rss}$			-	5	-	
Effective Output Capacitance, Energy Related <sup>a</sup>	$C_{o(er)}$			-	118	-	
Effective Output Capacitance, Time Related <sup>b</sup>	$C_{o(tr)}$	$V_{DS} = 0\text{ V to } 480\text{ V}, V_{GS} = 0\text{ V}$		-	429	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 17\text{ A}, V_{DS} = 480\text{ V}$	-	88	132	nC
Gate-Source Charge	$Q_{gs}$			-	22	-	
Gate-Drain Charge	$Q_{gd}$			-	46	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 480\text{ V}, I_D = 17\text{ A},$ $V_{GS} = 10\text{ V}, R_g = 9.1\text{ }\Omega$		-	29	58	ns
Rise Time	$t_r$			-	61	92	
Turn-Off Delay Time	$t_{d(off)}$			-	78	117	
Fall Time	$t_f$			-	32	64	
Gate Input Resistance	$R_g$			$f = 1\text{ MHz}, \text{ open drain}$		0.25	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	32	A
Pulsed Diode Forward Current	$I_{SM}$			-	-	80	
Diode Forward Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 17\text{ A}, V_{GS} = 0\text{ V}$		-	0.9	1.2	V
Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = I_S = 17\text{ A},$ $di/dt = 100\text{ A}/\mu\text{s}, V_R = 25\text{ V}$		-	455	910	ns
Reverse Recovery Charge	$Q_{rr}$			-	8	16	$\mu\text{C}$
Reverse Recovery Current	$I_{RRM}$			-	30	-	A

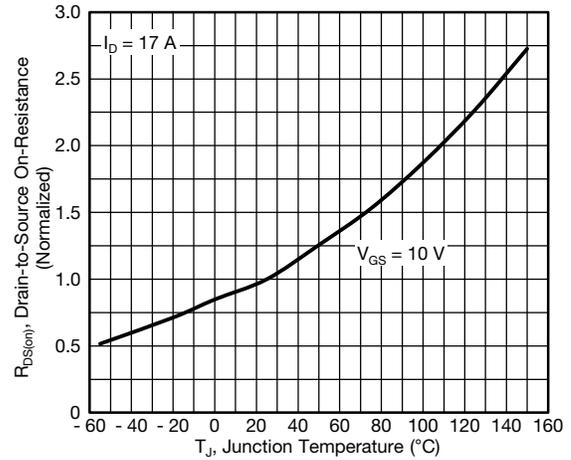
**Notes**

- a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .
- b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .

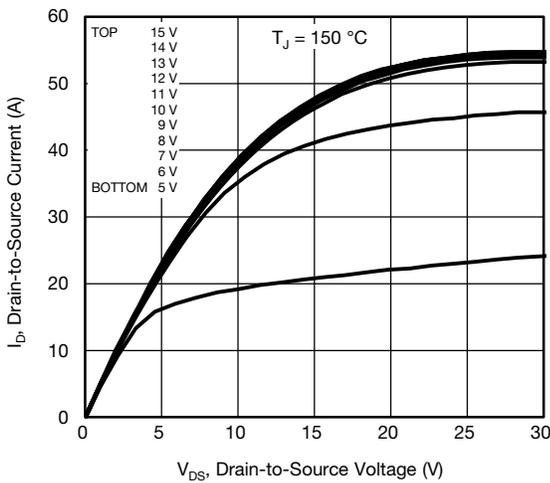
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



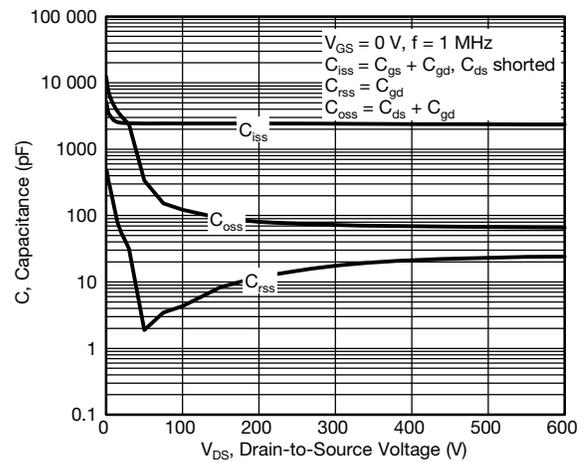
**Fig. 1 - Typical Output Characteristics**



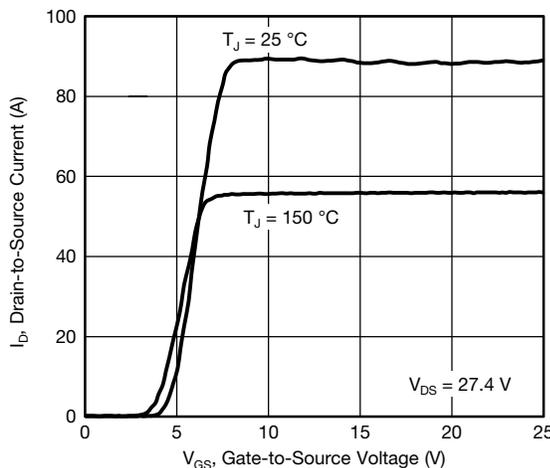
**Fig. 4 - Normalized On-Resistance vs. Temperature**



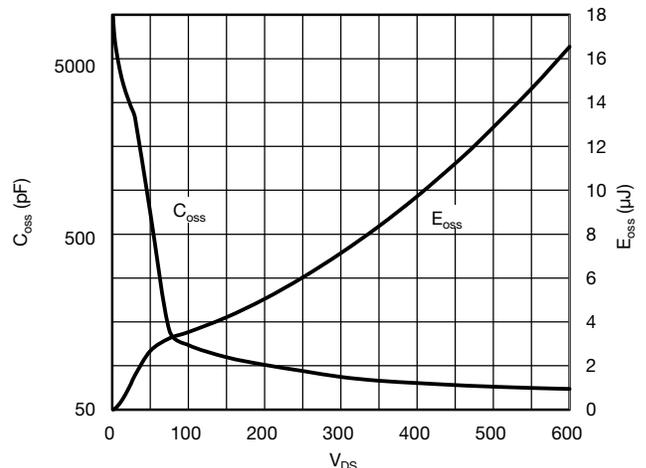
**Fig. 2 - Typical Output Characteristics**



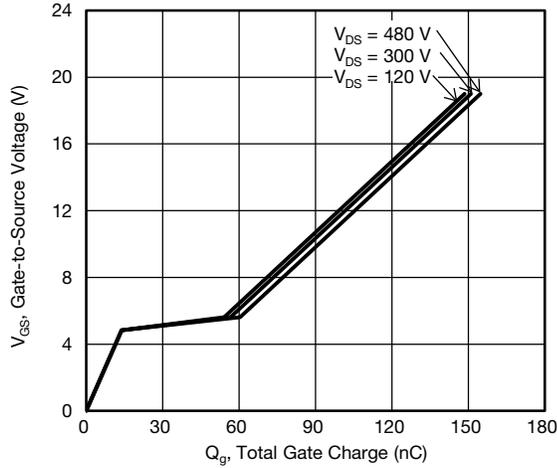
**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



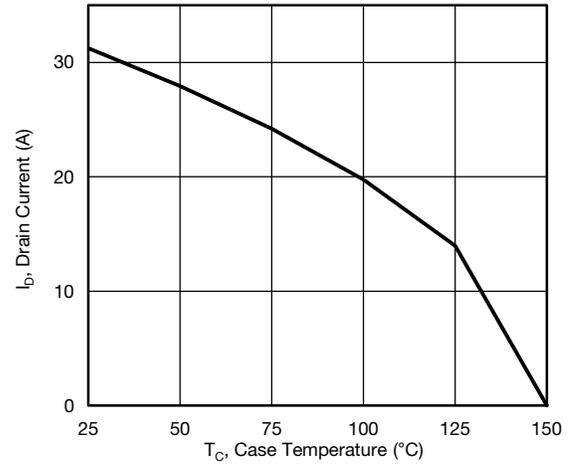
**Fig. 3 - Typical Transfer Characteristics**



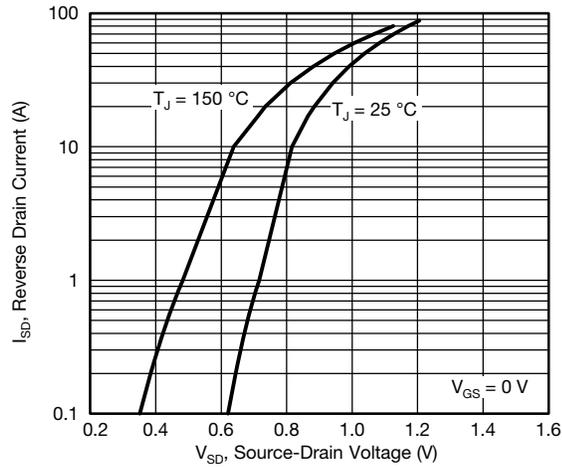
**Fig. 6 -  $C_{oss}$  and  $E_{oss}$  vs.  $V_{ds}$**



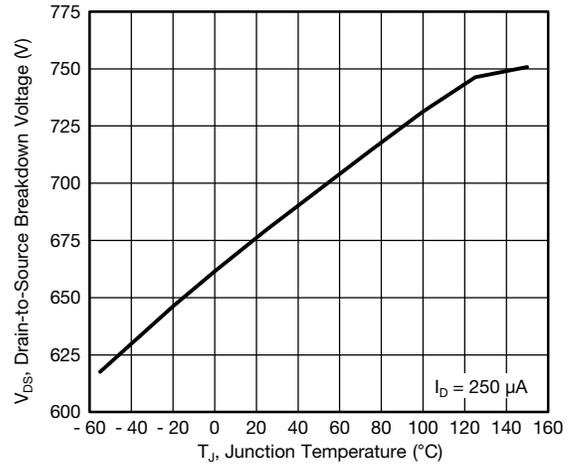
**Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage**



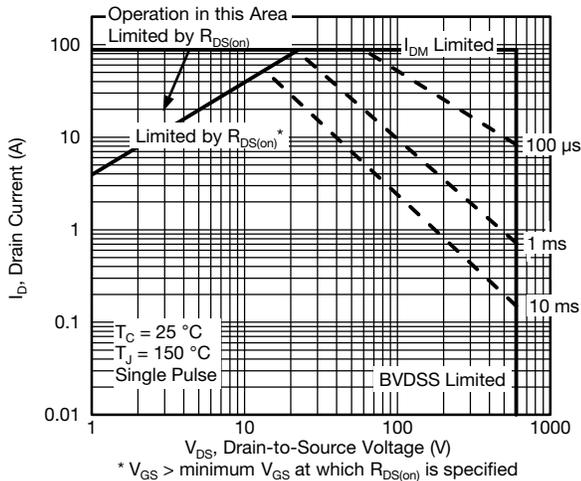
**Fig. 10 - Maximum Drain Current vs. Case Temperature**



**Fig. 8 - Typical Source-Drain Diode Forward Voltage**



**Fig. 11 - Temperature vs. Drain-to-Source Voltage**



**Fig. 9 - Maximum Safe Operating Area**

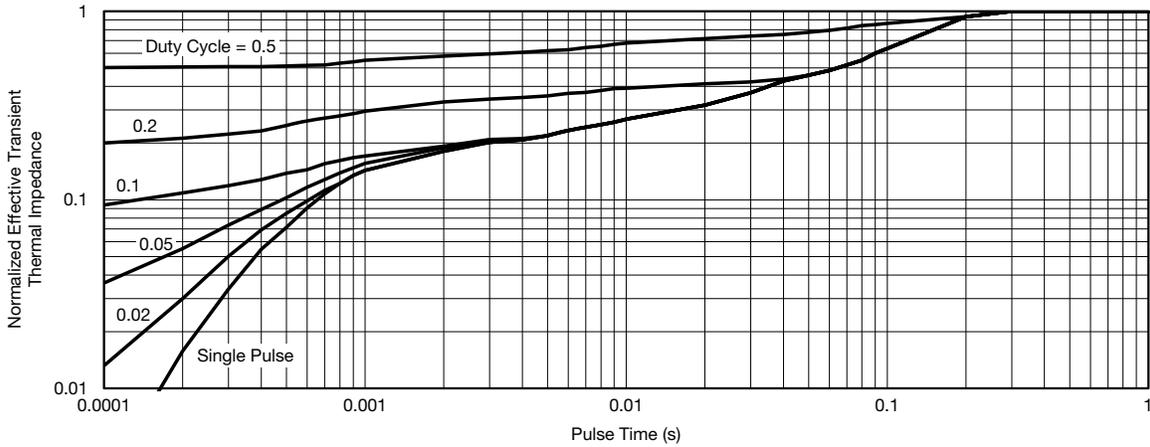


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

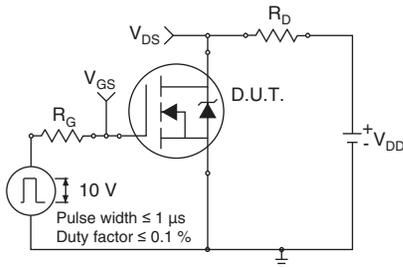


Fig. 13 - Switching Time Test Circuit

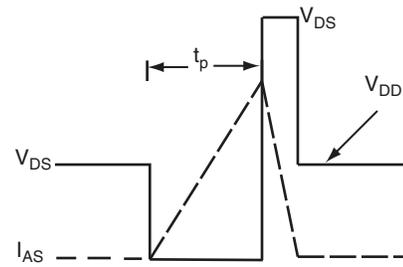


Fig. 16 - Unclamped Inductive Waveforms

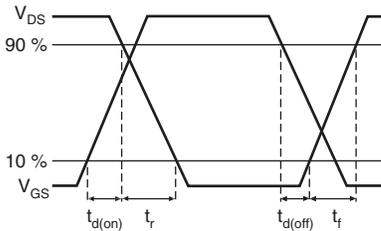


Fig. 14 - Switching Time Waveforms

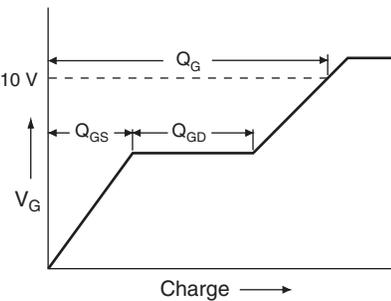


Fig. 17 - Basic Gate Charge Waveform

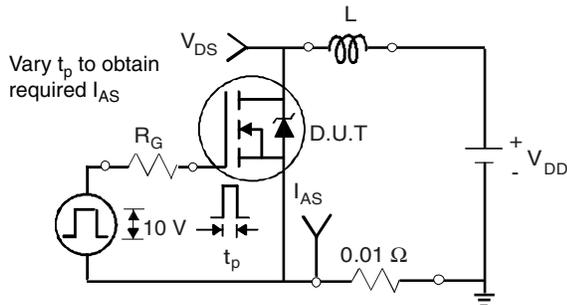


Fig. 15 - Unclamped Inductive Test Circuit

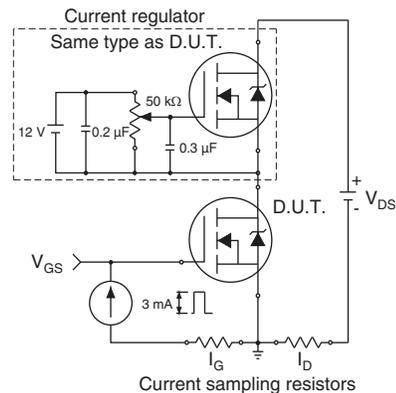
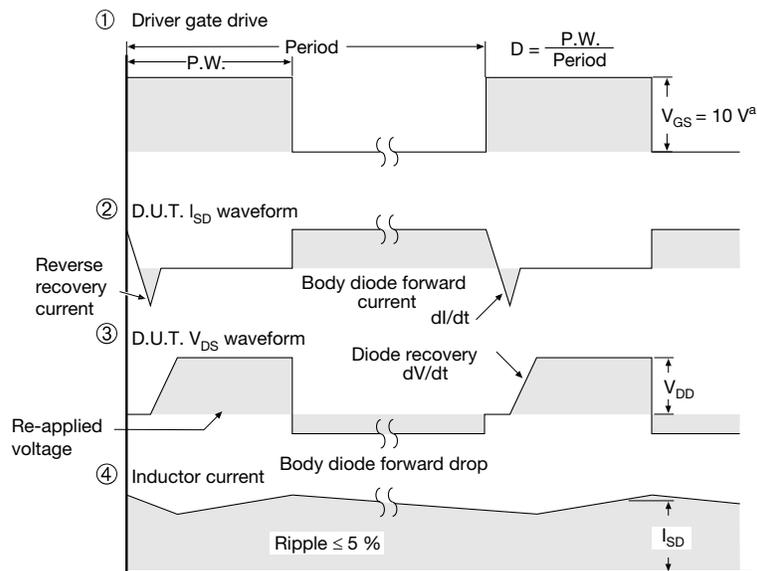
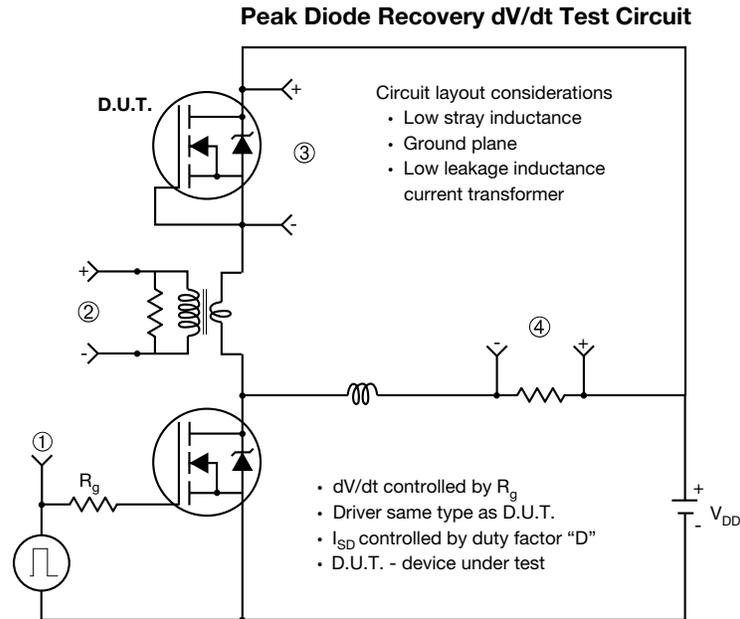


Fig. 18 - Gate Charge Test Circuit



**Note**

a.  $V_{GS} = 5\text{ V}$  for logic level devices

**Fig. 19 - For N-Channel**

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