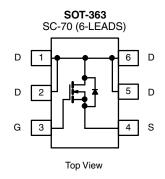




N-Channel 12 V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	$R_{DS(on)}(\Omega)$ (Max.)	I _D (A) ^a	Q _g (Typ.)			
	0.020 at V _{GS} = 4.5 V	4				
12	0.024 at V _{GS} = 2.5 V	4	13.1 nC			
	0.030 at V _{GS} = 1.8 V	4				



Ordering Information:

Si1442DH-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

- TrenchFET® Power MOSFET
- 100 % R_g Tested
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



HALOGEN FREE

APPLICATIONS

- Load Switch and Battery Switch for Portable Devices
- DC/DC Converters
- Low On-Resistance for Low Voltage Drop



N-Channel MOSFET

Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	V _{DS}	12			
Gate-Source Voltage		V _{GS}	± 8	V	
	T _F = 25 °C		4 ^a		
Continuous Dusin Comment /T 450 °C\	T _F = 70 °C		4 ^a		
Continuous Drain Current (T _J = 150 °C)	T _A = 25 °C	I _D	4a, b, c	A	
	T _A = 70 °C		4a, b, c		
Pulsed Drain Current (t = 300 μs)	I _{DM} 20	20			
0 11 0 0 0 1	T _F = 25 °C		2.3		
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	1.3 ^{b, c}		
	T _F = 25 °C		2.8		
Mayimum Dayyar Dissination	T _F = 70 °C	В	1.8	w	
Maximum Power Dissipation	T _A = 25 °C	P _D	1.56 ^{b, c}	vv	
	T _A = 70 °C		1 ^{b, c}		
Operating Junction and Storage Temperature Ra	T _J , T _{stg}	- 55 to 150	°C		
Soldering Recommendations (Peak Temperature		260			

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient ^{b, d}	t ≤ 5 s	R _{thJA}	60	80	°C/W		
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	34	45	C/VV		

Notes:

- a. T_F = 25 °C, package limited.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 5 s.
- d. Maximum under steady state conditions is 125 °C/W.

Document Number: 63772 S12-0546-Rev. A, 12-Mar-12 For technical support, please contact: pmostechsupport@vishav.com

Si1442DH

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static					L		
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	12			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	L = 250 HA		5		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA		- 2.7			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	0.4		1	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$			± 100	nA	
Zava Cata Valtana Busin Courset		V _{DS} = 12 V, V _{GS} = 0 V	1		1		
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 12 V, V _{GS} = 0 V, T _J = 55 °C			10	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	15			Α	
	. ,	V _{GS} = 4.5 V, I _D = 6 A		0.017	0.020		
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 2.5 V, I _D = 5 A		0.019	0.024	Ω	
		V _{GS} = 1.8 V, I _D = 3 A			0.030		
Forward Transconductance ^a	9 _{fs}	V _{DS} = 6 V, I _D = 6 A		33		S	
Dynamic ^b		20 2		ļ		ļ	
Input Capacitance	C _{iss}			1010			
Output Capacitance	C _{oss}	V _{DS} = 6 V, V _{GS} = 0 V, f = 1 MHz		323		pF	
Reverse Transfer Capacitance	C _{rss}	50 / G5 /		305			
Total Gate Charge	Q _g	V _{DS} = 6 V, V _{GS} = 8 V, I _D = 7 A		21.8	33		
		26 7 46 7 2		13.1	20		
Gate-Source Charge		$V_{DS} = 6 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 7 \text{ A}$		2		nC	
Gate-Drain Charge	Q_{gd}			2.7			
Gate Resistance	R_{g}	f = 1 MHz	0.3	1.6	3.2	Ω	
Turn-On Delay Time	t _{d(on)}			8	16		
Rise Time	t _r	$V_{DD} = 6 \text{ V}, R_1 = 1.07 \Omega$		13	20		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 5.6 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		22	33	1	
Fall Time	t _f			9	18		
Turn-On Delay Time	t _{d(on)}			6	12	ns	
Rise Time	t _r	$V_{DD} = 6 \text{ V}, R_{L} = 1.07 \Omega$		12	18		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 5.6 \text{ A}, V_{GEN} = 8 \text{ V}, R_g = 1 \Omega$		22	33		
Fall Time	t _f	-		8	16		
Drain-Source Body Diode Characterist	ics			l			
Continuous Source-Drain Diode Current	Is	T _C = 25 °C			4		
Pulse Diode Forward Current	I _{SM}				20	A	
Body Diode Voltage	V_{SD}	I _S = 5.6 A, V _{GS} = 0 V		0.75	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			19	30	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	1		7	14	nC	
Reverse Recovery Fall Time	t _a	$I_F = 5.6 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$		13		1	
Reverse Recovery Rise Time	t _b			6		ns	

Notes:

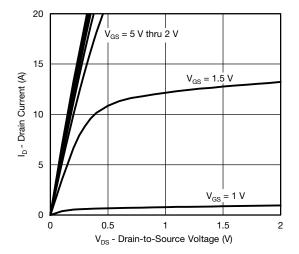
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.

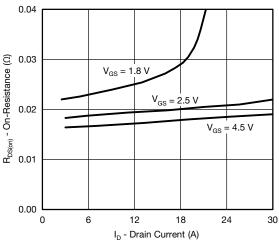
b. Guaranteed by design, not subject to production testing.



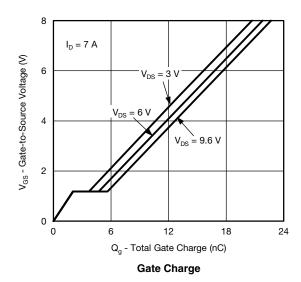
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

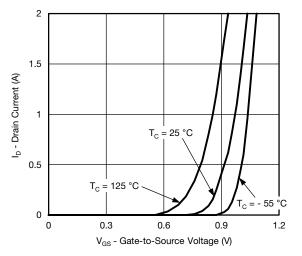


Output Characteristics

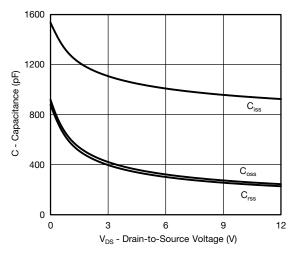


On-Resistance vs. Drain Current

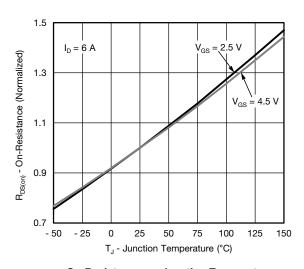




Transfer Characteristics



Capacitance

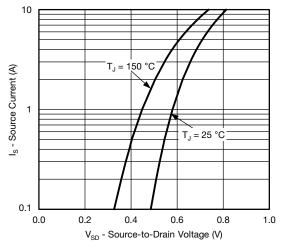


On-Resistance vs. Junction Temperature

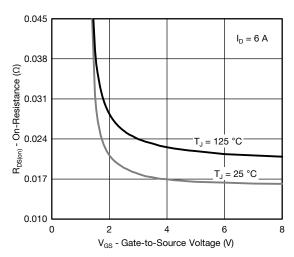
Si1442DH

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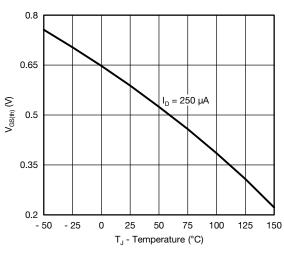
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



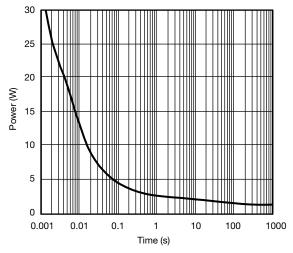




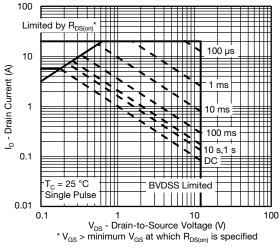
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



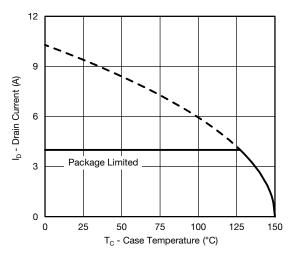
Single Pulse Power, Junction-to-Ambient



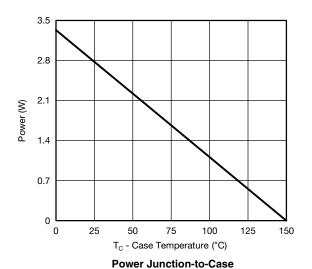
Safe Operating Area, Junction-to-Ambient

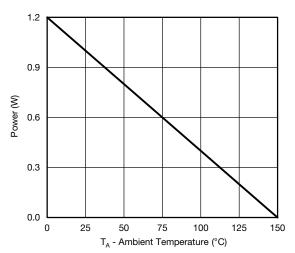


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*





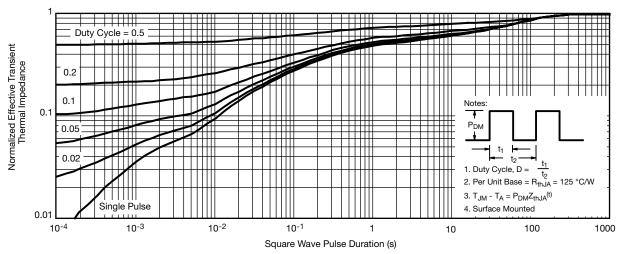
Power Junction-to-Ambient

^{*} The power dissipation P_D is based on $T_{J(max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

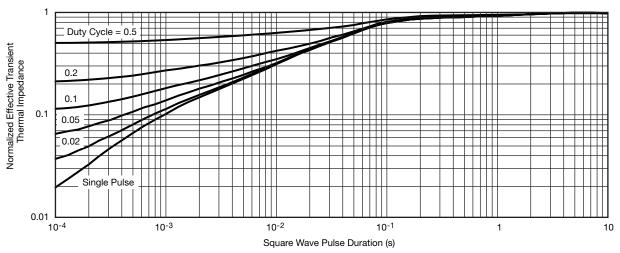
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



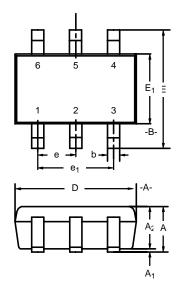
Normalized Thermal Transient Impedance, Junction-to-Foot

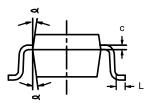
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SC-70: 6-LEADS





	MILLIMETERS			INCHES		
Dim	Min	Nom	Max	Min	Nom	Max
Α	0.90	_	1.10	0.035	_	0.043
A ₁	-	_	0.10	-	_	0.004
A ₂	0.80	_	1.00	0.031	_	0.039
b	0.15	_	0.30	0.006	_	0.012
С	0.10	-	0.25	0.004	-	0.010
D	1.80	2.00	2.20	0.071	0.079	0.087
Ε	1.80	2.10	2.40	0.071	0.083	0.094
E ₁	1.15	1.25	1.35	0.045	0.049	0.053
е	0.65BSC				0.026BSC	;
e ₁	1.20	1.30	1.40	0.047	0.051	0.055
L	0.10	0.20	0.30	0.004	0.008	0.012
کے	7°Nom				7°Nom	

DWG: 5550





Single-Channel LITTLE FOOT® SC-70 6-Pin MOSFET Copper Leadframe Version Recommended Pad Pattern and Thermal Performance

INTRODUCTION

The new single 6-pin SC-70 package with a copper leadframe enables improved on-resistance values and enhanced thermal performance as compared to the existing 3-pin and 6-pin packages with Alloy 42 leadframes. These devices are intended for small to medium load applications where a miniaturized package is required. Devices in this package come in a range of on-resistance values, in n-channel and p-channel versions. This technical note discusses pin-outs, package outlines, pad patterns, evaluation board layout, and thermal performance for the single-channel version.

BASIC PAD PATTERNS

See Application Note 826, Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs, (http://www.vishay.com/doc?72286) for the basic pad layout and dimensions. These pad patterns are sufficient for the low to medium power applications for which this package is intended. Increasing the drain pad pattern yields a reduction in thermal resistance and is a preferred footprint. The availability of four drain leads rather than the traditional single drain lead allows a better thermal path from the package to the PCB and external environment.

PIN-OUT

Figure 1 shows the pin-out description and Pin 1 identification. The pin-out of this device allows the use of four pins as drain leads, which helps to reduce on-resistance and junction-to-ambient thermal resistance.

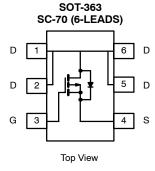


FIGURE 1.

For package dimensions see outline drawing SC-70 (6-Leads) (http://www.vishay.com/doc?71154)

EVALUATION BOARDS — SINGLE SC70-6

The evaluation board (EVB) measures 0.6 inches by 0.5 inches. The copper pad traces are the same as in Figure 2. The board allows examination from the outer pins to 6-pin DIP connections, permitting test sockets to be used in evaluation testing. See Figure 3.

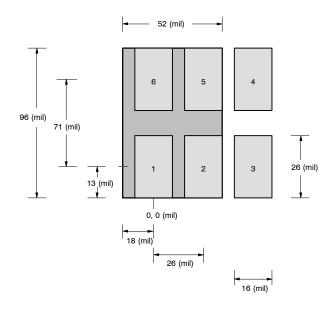
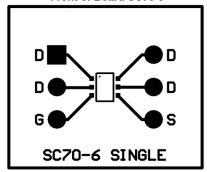


FIGURE 2. SC-70 (6 leads) Single

The thermal performance of the single 6-pin SC-70 has been measured on the EVB, comparing both the copper and Alloy 42 leadframes. This test was first conducted on the traditional Alloy 42 leadframe and was then repeated using the 1-inch² PCB with dual-side copper coating.



Front of Board SC70-6



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Back of Board SC70-6

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FIGURE 3.

THERMAL PERFORMANCE

Junction-to-Foot Thermal Resistance (Package Performance)

The junction to foot thermal resistance is a useful method of comparing different packages thermal performance.

A helpful way of presenting the thermal performance of the 6-Pin SC-70 copper leadframe device is to compare it to the traditional Alloy 42 version.

Thermal performance for the 6-pin SC-70 measured as junction-to-foot thermal resistance, where the "foot" is the drain lead of the device at the bottom where it meets the PCB. The junction-to-foot thermal resistance is typically 40°C/W in the copper leadframe and 163°C/W in the Alloy 42 leadframe - a four-fold improvement. This improved performance is obtained by the enhanced thermal conductivity of copper over Alloy 42.

Power Dissipation

The typical $R\theta_{JA}$ for the single 6-pin SC-70 with copper leadframe is 103°C/W steady-state, compared with 212°C/W for the Alloy 42 version. The figures are based on the 1-inch² FR4 test board. The following example shows how the thermal resistance impacts power dissipation for the two different leadframes at varying ambient temperatures.

ALLOY 42 LEADFRAME					
Room Ambient 25 °C	Elevated Ambient 60 °C				
$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$	$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$				
$P_{D} = \frac{150^{\circ}C - 25^{\circ}C}{212^{\circ}C/W}$	$P_{D} = \frac{150^{\circ}C - 25^{\circ}C}{212^{\circ}C/W}$				
$P_D = 590 \text{ mW}$	$P_D = 425 \text{ mW}$				

COOPER LEADFRAME				
Room Ambient 25 °C	Elevated Ambient 60 °C			
$P_{D} = \frac{T_{J(max)} - T_{A}}{R\theta_{JA}}$ $P_{D} = \frac{150^{\circ}C - 25^{\circ}C}{124^{\circ}C/W}$	$P_{D} = \frac{T_{J(max)} - T_{A}}{R\theta_{JA}}$ $P_{D} = \frac{150^{\circ}C - 60^{\circ}C}{124^{\circ}C/W}$			
$P_{D} = 1.01 \text{ W}$	P _D = 726 mW			

As can be seen from the calculations above, the compact 6-pin SC-70 copper leadframe LITTLE FOOT power MOSFET can handle up to 1 W under the stated conditions.

Testing

To further aid comparison of copper and Alloy 42 leadframes, Figure 5 illustrates single-channel 6-pin SC-70 thermal performance on two different board sizes and two different pad patterns. The measured steady-state values of $R\theta_{\text{JA}}$ for the two leadframes are as follows:

LITTLE FOOT 6-PIN SC-70					
	Alloy 42	Copper			
1) Minimum recommended pad pattern on the EVB board V (see Figure 3.	329.7°C/W	208.5°C/W			
 Industry standard 1-inch² PCB with maximum copper both sides. 	211.8°C/W	103.5°C/W			

The results indicate that designers can reduce thermal resistance ($R\theta_{1\Delta}$) by 36% simply by using the copper leadframe device rather than the Alloy 42 version. In this example, a 121°C/W reduction was achieved without an increase in board area. If increasing in board size is feasible, a further 105°C/W reduction could be obtained by utilizing a 1-inch² square PCB area.

The copper leadframe versions have the following suffix:

Single: Si14xxEDH Dual: Si19xxEDH Complementary: Si15xxEDH

Document Number: 71334 www.vishay.com





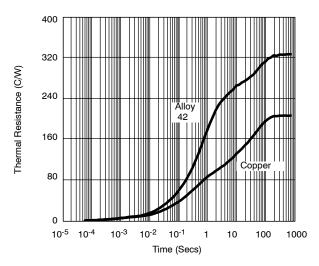


FIGURE 4. Leadframe Comparison on EVB

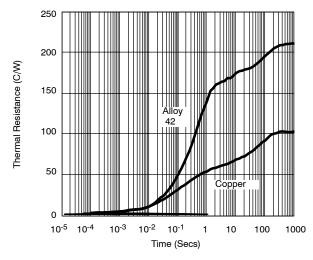
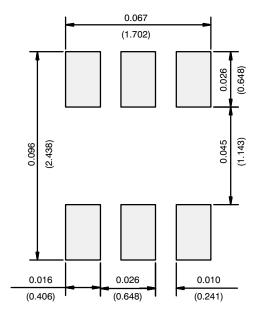


FIGURE 5. Leadframe Comparison on Alloy 42 1-inch² PCB



RECOMMENDED MINIMUM PADS FOR SC-70: 6-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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Revision: 02-Oct-12 Document Number: 91000

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http://moschip.ru/get-element

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