

# **BUK9660-100A**

# N-channel TrenchMOS logic level FET Rev. 02 — 16 February 2011

Product data sheet

#### 1. **Product profile**

## 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

#### 1.2 Features and benefits

- AEC Q101 compliant
- Low conduction losses due to low on-state resistance
- Suitable for logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

## 1.3 Applications

- 12 V, 24 V and 42 V loads
- Automotive and general purpose power switching
- Motors, lamps and solenoids

#### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \ge 25 \text{ °C}; T_j \le 175 \text{ °C}$	-	-	100	V
I <sub>D</sub>	drain current	$V_{GS} = 5 \text{ V}; T_{mb} = 25 \text{ °C};$ see <u>Figure 1</u> ; see <u>Figure 3</u>	-	-	26	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 2</u>	-	-	106	W



Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
R <sub>DSon</sub>	drain-source on-state	$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A};$ $T_j = 25 \text{ °C}$	-	49	58	mΩ
	resistance	$V_{GS} = 4.5 \text{ V}; I_D = 15 \text{ A};$ $T_j = 25 \text{ °C}$	-	-	67	mΩ
		$V_{GS} = 5 \text{ V}; I_D = 15 \text{ A};$ $T_j = 25 \text{ °C}; \text{ see } \frac{\text{Figure 12}}{\text{see } \frac{\text{Figure 13}}{\text{Figure 13}}}$	-	51	60	mΩ
Avalanche	ruggedness					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$\begin{split} I_D &= 20 \text{ A; } V_{sup} \leq 100 \text{ V;} \\ R_{GS} &= 50  \Omega;  V_{GS} = 5 \text{ V;} \\ T_{j(\text{init})} &= 25 ^{\circ}\text{C; } \text{ unclamped} \end{split}$	-	-	30	mJ

# 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain	mb	D
3	S	source		
mb	D	mounting base; connected to drain		mbb076 S
			SOT404 (D2PAK)	

# 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9660-100A	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

# 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C	-	100	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	100	V
$V_{GS}$	gate-source voltage		-10	10	V
I <sub>D</sub>	drain current	$T_{mb} = 25 \text{ °C}$ ; $V_{GS} = 5 \text{ V}$ ; see <u>Figure 1</u> ; see <u>Figure 3</u>	-	26	Α
		$T_{mb} = 100 \text{ °C}; V_{GS} = 5 \text{ V}; \text{ see } \frac{\text{Figure 1}}{}$	-	19	Α
I <sub>DM</sub>	peak drain current	$T_{mb}$ = 25 °C; pulsed; $t_p \le 10 \mu s$ ; see Figure 3	-	106	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 2</u>	-	106	W
T <sub>stg</sub>	storage temperature		-55	175	°C
Tj	junction temperature		-55	175	°C
$V_{GSM}$	peak gate-source voltage	pulsed; $t_p \le 50 \mu s$	-15	15	V
Source-drain	n diode				
Is	source current	T <sub>mb</sub> = 25 °C	-	26	Α
I <sub>SM</sub>	peak source current	pulsed; $t_p \le 10 \mu s$ ; $T_{mb} = 25 \text{ °C}$	-	106	Α
Avalanche r	uggedness				
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$I_D$ = 20 A; $V_{sup} \le$ 100 V; $R_{GS}$ = 50 $\Omega$ ; $V_{GS}$ = 5 V; $T_{j(init)}$ = 25 °C; unclamped	-	30	mJ

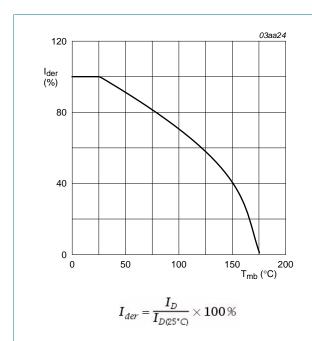


Fig 1. Normalized continuous drain current as a function of mounting base temperature

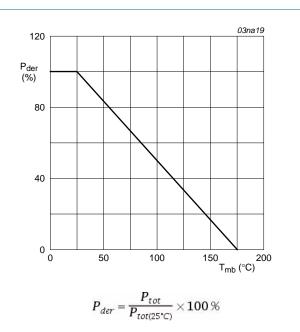
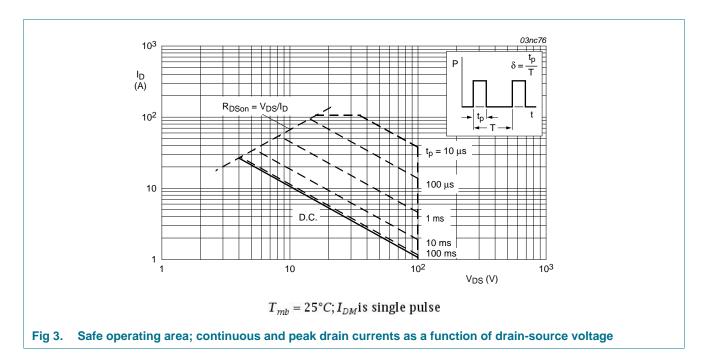


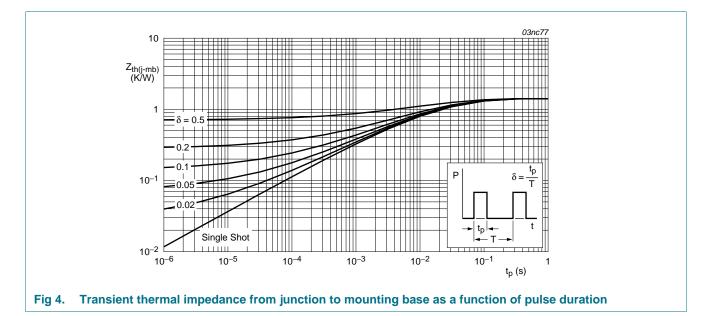
Fig 2. Normalized total power dissipation as a function of mounting base temperature



# 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	1.4	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; minimum footprint	-	50	-	K/W



# 6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	racteristics					
$V_{(BR)DSS}$	drain-source	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	100	-	-	V
	breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ °C}$	89	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1$ mA; $V_{DS} = V_{GS}$ ; $T_j = 25$ °C; see <u>Figure 11</u>	1	1.5	2	V
		$I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$ ; $T_j$ = -55 °C; see <u>Figure 11</u>	-	-	2.3	V
		$I_D = 1$ mA; $V_{DS} = V_{GS}$ ; $T_j = 175$ °C; see Figure 11	0.5	-	-	V
I <sub>DSS</sub>	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ °C}$	-	-	500	μΑ
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.05	10	μΑ
I <sub>GSS</sub>	gate leakage current	$V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nA
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nA
R <sub>DSon</sub>		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ °C}$	-	49	58	mΩ
resistance	resistance	$V_{GS} = 5 \text{ V}; I_D = 15 \text{ A}; T_j = 175 °C;$ see <u>Figure 12</u> ; see <u>Figure 13</u>	-	-	150	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ °C}$	-	-	67	mΩ
		$V_{GS} = 5 \text{ V}; I_D = 15 \text{ A}; T_j = 25 ^{\circ}\text{C};$ see <u>Figure 12</u> ; see <u>Figure 13</u>	-	51	60	mΩ
Dynamic (	characteristics					
C <sub>iss</sub>	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$	-	1440	1924	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C; see <u>Figure 14</u>	-	155	186	pF
$C_{rss}$	reverse transfer capacitance		-	100	138	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \Omega; V_{GS} = 5 \text{ V};$	-	20	-	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 10 \Omega$ ; $T_j = 25 ^{\circ}C$	-	124	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	68	-	ns
t <sub>f</sub>	fall time		-	67	-	ns
L <sub>D</sub>	internal drain inductance	from drain lead 6 mm from package to centre of die; $T_j = 25$ °C	-	4.5	-	nΗ
		from upper edge of drain mounting base to centre of die; $T_j = 25$ °C	-	2.5	-	nΗ
L <sub>S</sub>	internal source inductance	from source lead to source bond pad; $T_j = 25  ^{\circ}\text{C}$	-	7.5	-	nΗ
Source-dr	ain diode					
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C};$ see <u>Figure 15</u>	-	0.85	1.2	V
t <sub>rr</sub>	reverse recovery time	$I_S = 20 \text{ A}$ ; $dI_S/dt = -100 \text{ A/}\mu\text{s}$ ;	-	61	-	ns
Q <sub>r</sub>	recovered charge	recovered charge $V_{GS} = -10 \text{ V}; V_{DS} = 30 \text{ V}; T_j = 25 ^{\circ}\text{C}$	_	200	-	nC

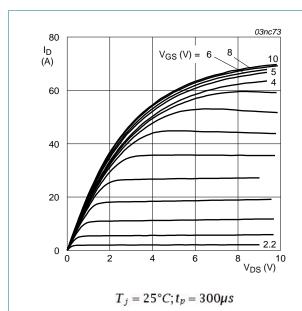


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

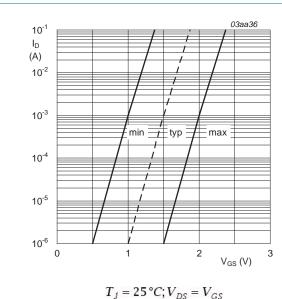
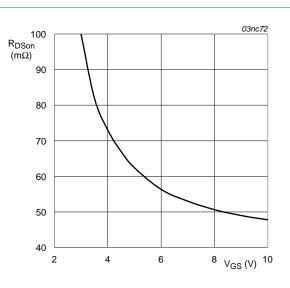
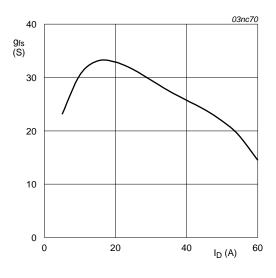


Fig 7. Sub-threshold drain current as a function of gate-source voltage



 $T_j = 25^{\circ}C; I_D = 15A$ 

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values



 $T_j = 25^{\circ}C; V_{DS} = 25V$ 

Fig 8. Forward transconductance as a function of drain current; typical values

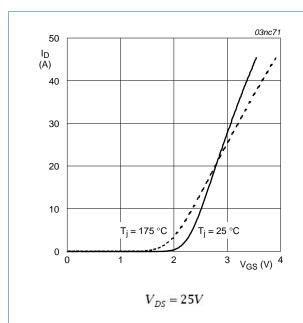


Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

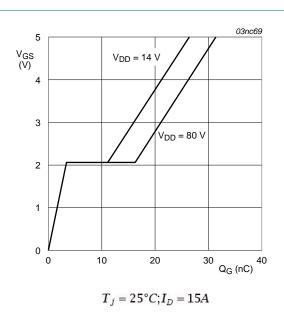


Fig 10. Gate-source voltage as a function of turn-on

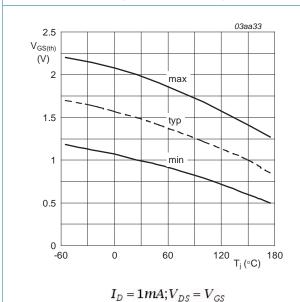


Fig 11. Gate-source threshold voltage as a function of junction temperature

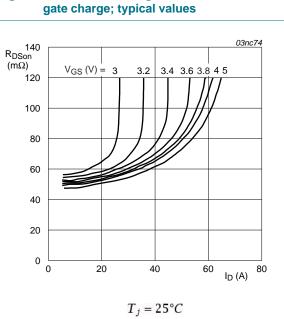


Fig 12. Drain-source on-state resistance as a function of drain current; typical values

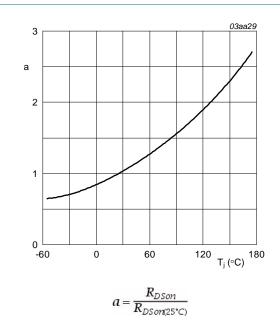


Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

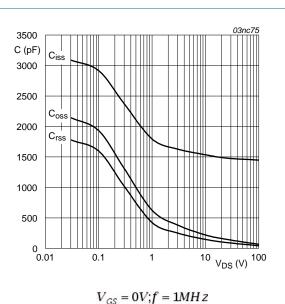
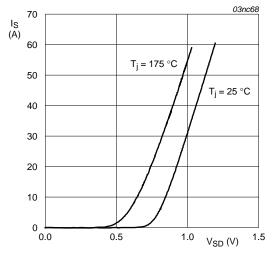


Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



 $V_{GS} = 0V$ 

Fig 15. Reverse diode current as a function of reverse diode voltage; typical value

# 7. Package outline

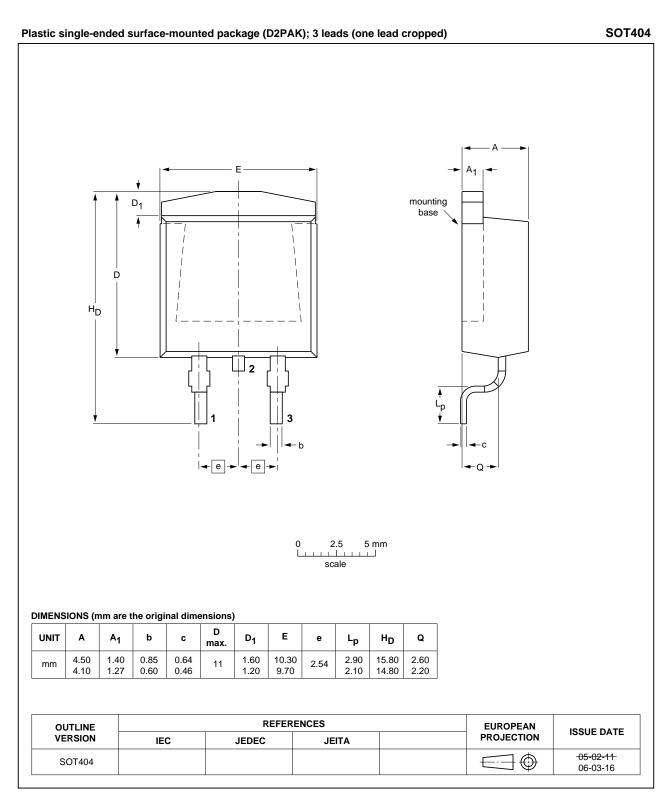


Fig 16. Package outline SOT404 (D2PAK)

# 8. Revision history

## Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9660-100A v.2	20110216	Product data sheet	-	BUK9560_9660_100A v.1
Modifications:		his data sheet has been r	redesigned to comply	with the new identity
	<ul> <li>Legal texts have</li> </ul>	ve been adapted to the ne	w company name wh	ere appropriate.
	<ul> <li>Type number E</li> </ul>	BUK9660-100A separated	I from data sheet BUK	9560_9660_100A v.1.
BUK9560_9660_100A v.1	20010122	Product specification	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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# **BUK9660-100A**

# **Nexperia**

N-channel TrenchMOS logic level FET

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