

Automotive-grade N-channel 40 V, 0.8 mΩ typ., 200 A STripFET™ F7 Power MOSFETs in H<sup>2</sup>PAK-2 and H<sup>2</sup>PAK-6 packages

Datasheet - production data

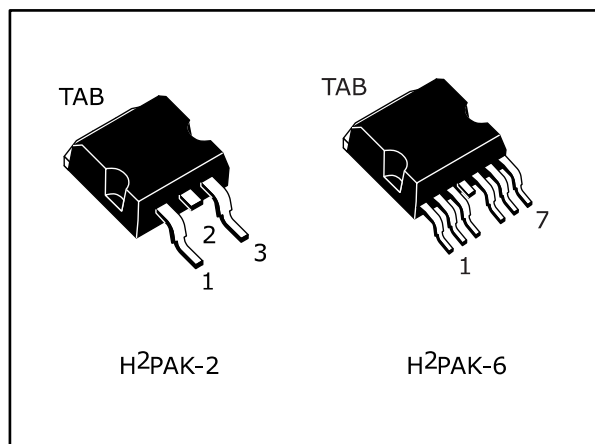
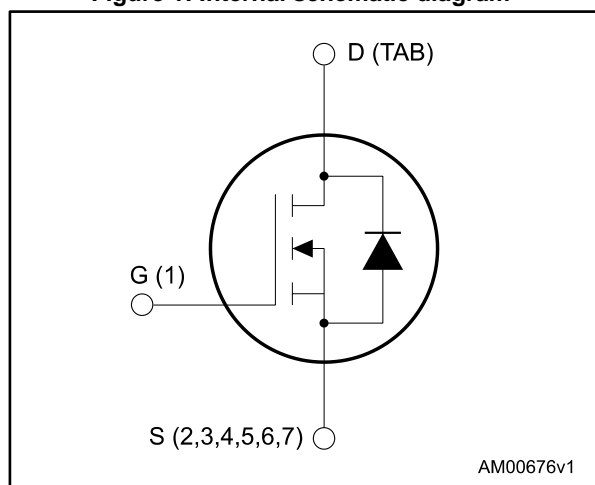


Figure 1: Internal schematic diagram



## Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>TOT</sub>
STH410N4F7-2AG	40 V	1.1 mΩ	200 A	365 W
STH410N4F7-6AG				

- Designed for automotive applications and AEC-Q101 qualified
- Among the lowest R<sub>DS(on)</sub> on the market
- Excellent figure of merit (FoM)
- Low C<sub>rss</sub>/C<sub>iss</sub> ratio for EMI immunity
- High avalanche ruggedness

## Applications

- Switching applications

## Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packing
STH410N4F7-2AG	410N4F7	H <sup>2</sup> PAK-2	Tape And Reel
STH410N4F7-6AG		H <sup>2</sup> PAK-6	

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# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	40	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_{case} = 25\text{ }^\circ\text{C}$	200	A
	Drain current (continuous) at $T_{case} = 100\text{ }^\circ\text{C}$	200	
$I_{DM}^{(2)}$	Drain current (pulsed)	800	A
$P_{TOT}$	Total dissipation at $T_{case} = 25\text{ }^\circ\text{C}$	365	W
$E_{AS}^{(3)}$	Single pulse avalanche energy	1.9	J
$T_{stg}$	Storage temperature range	-55 to 175	$^\circ\text{C}$
$T_j$	Operating junction temperature range		

**Notes:**

<sup>(1)</sup> Current is limited by package, the current capability of the silicon is 420 A at 25  $^\circ\text{C}$ .

<sup>(2)</sup> Pulse width is limited by safe operating area.

<sup>(3)</sup>  $T_j \leq 175\text{ }^\circ\text{C}$ ,  $I_{av}=80\text{A}$

**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.41	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	35	

**Notes:**

<sup>(1)</sup> When mounted on a 1-inch<sup>2</sup> FR-4 board, 2oz Cu.

## 2 Electrical characteristics

( $T_{\text{case}} = 25\text{ °C}$  unless otherwise specified)

**Table 4: Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	40			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 40\text{ V}$			10	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 40\text{ V}$ , $T_{\text{case}} = 125\text{ °C}$			100	
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = 20\text{ V}$			200	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 90\text{ A}$		0.8	1.1	m $\Omega$

**Table 5: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	11500	-	$\text{pF}$
$C_{oss}$	Output capacitance		-	3500	-	
$C_{rss}$	Reverse transfer capacitance		-	390	-	
$Q_g$	Total gate charge	$V_{DD} = 20\text{ V}$ , $I_D = 180\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 14: "Test circuit for gate charge behavior"</a> )	-	141	-	nC
$Q_{gs}$	Gate-source charge		-	65	-	
$Q_{gd}$	Gate-drain charge		-	27	-	

**Table 6: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 20\text{ V}$ , $I_D = 90\text{ A}$ $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 13: "Test circuit for resistive load switching times"</a> and <a href="#">Figure 18: "Switching time waveform"</a> )	-	35	-	ns
$t_r$	Rise time		-	198	-	
$t_{d(off)}$	Turn-off delay time		-	108	-	
$t_f$	Fall time		-	44.2	-	

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		200	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 90\text{ A}$	-		1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 180\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 32\text{ V}$ , $T_j = 25\text{ }^\circ\text{C}$ (see <a href="#">Figure 15: "Test circuit for inductive load switching and diode recovery times"</a> )	-	74.4		ns
$Q_{rr}$	Reverse recovery charge		-	115		nC
$I_{RRM}$	Reverse recovery current		-	3.1		A

**Notes:**

<sup>(1)</sup> Limited by package, 420 A current allowed by silicon.

<sup>(2)</sup> Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.2 Electrical characteristics (curves)

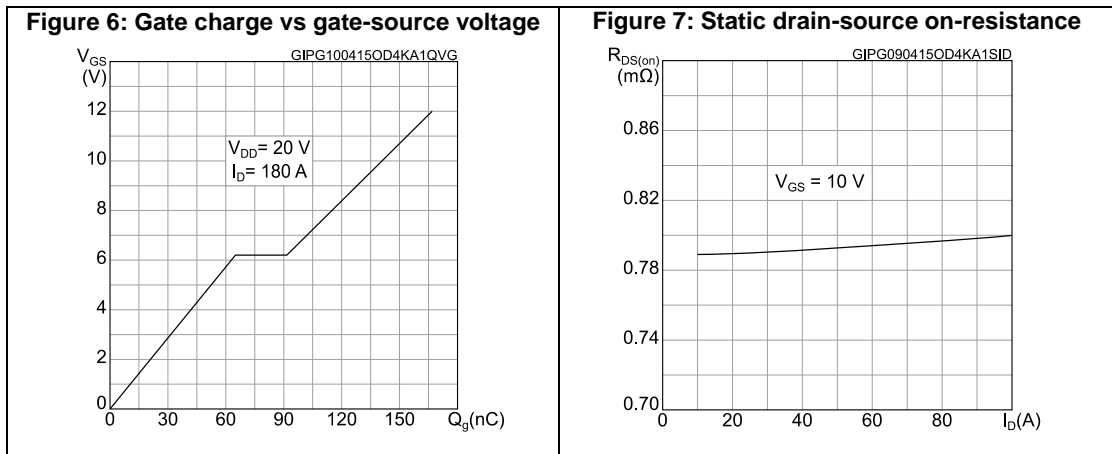
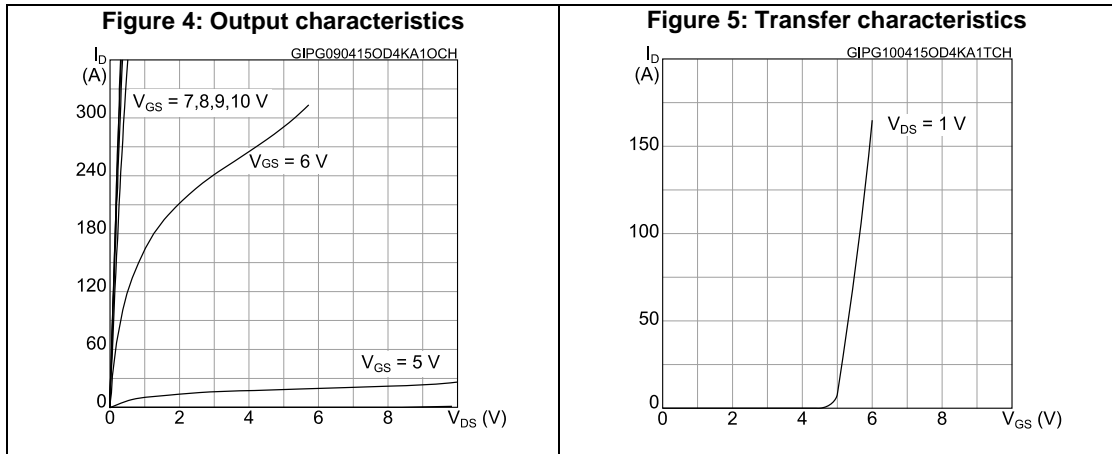
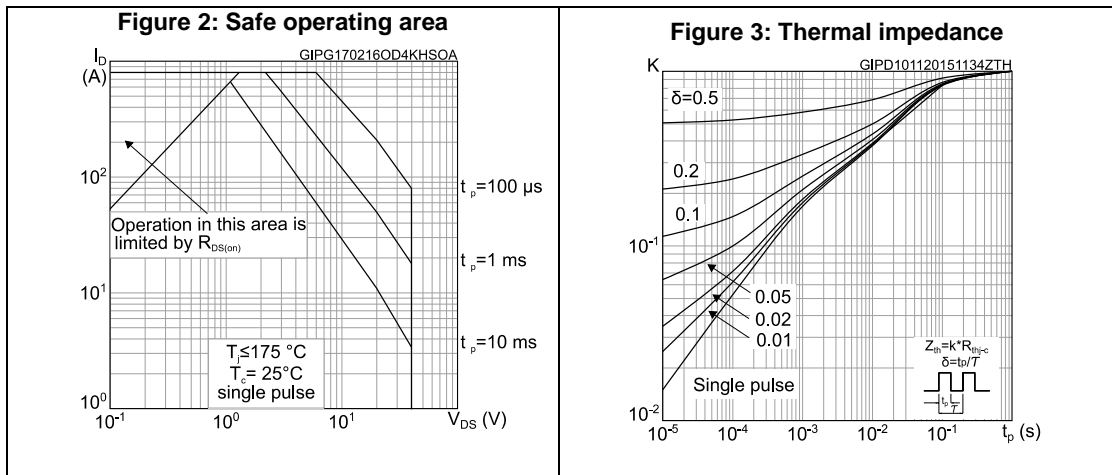


Figure 8: Capacitance variations

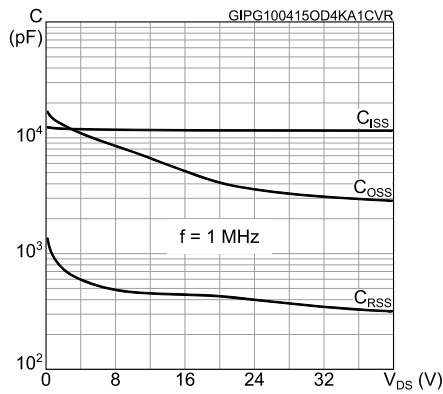


Figure 9: Normalized gate threshold voltage vs temperature

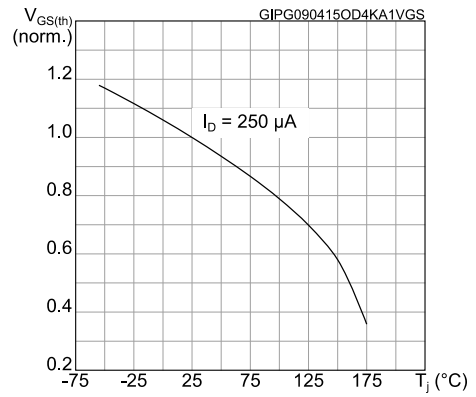


Figure 10: Normalized on-resistance vs temperature

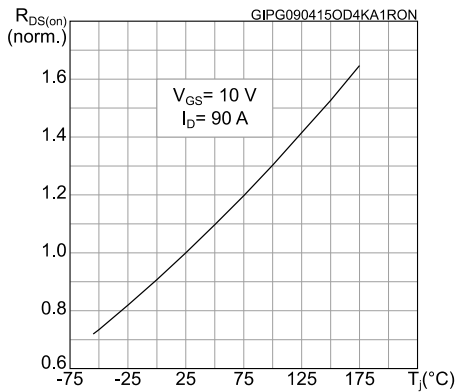


Figure 11: Normalized  $V_{(BR)DSS}$  vs temperature

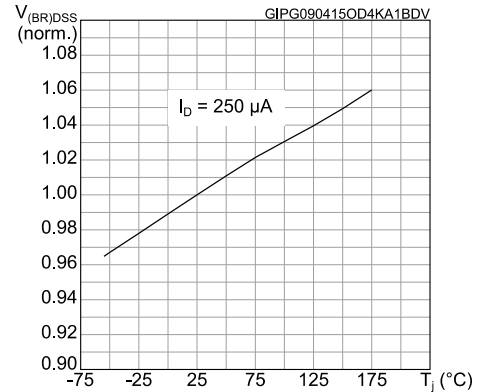
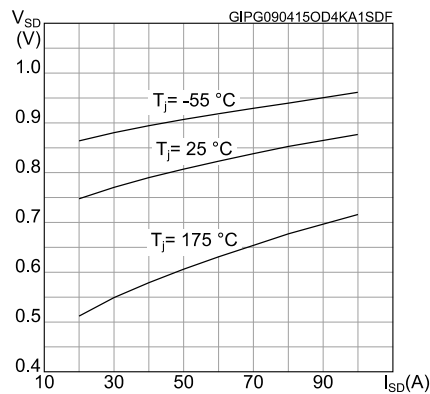
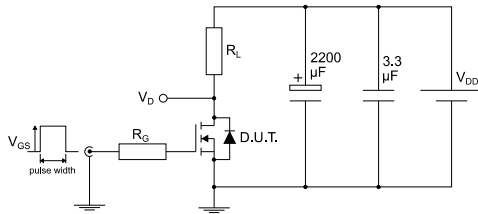


Figure 12: Source-drain diode forward characteristics



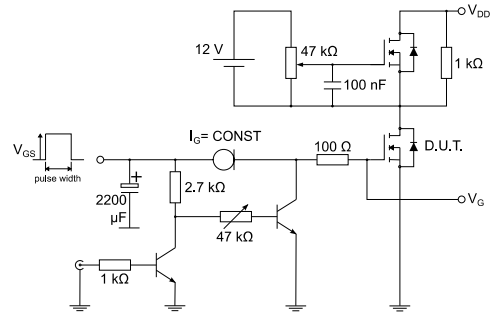
### 3 Test circuits

**Figure 13: Test circuit for resistive load switching times**



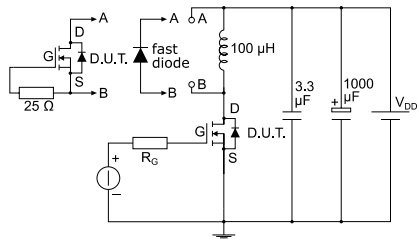
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**Figure 14: Test circuit for gate charge behavior**



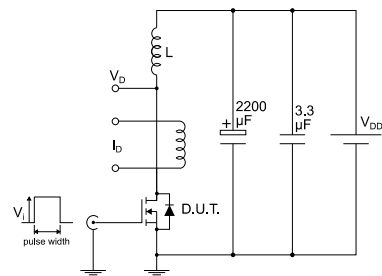
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**Figure 15: Test circuit for inductive load switching and diode recovery times**



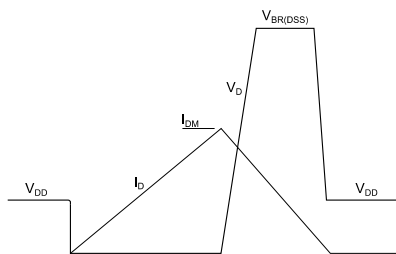
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**Figure 16: Unclamped inductive load test circuit**



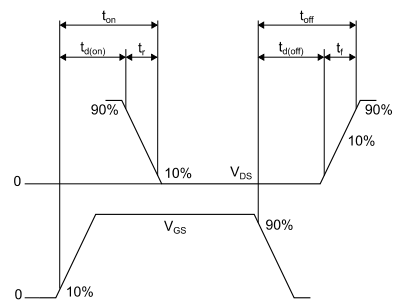
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**Figure 17: Unclamped inductive waveform**



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**Figure 18: Switching time waveform**



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## 4 Package information

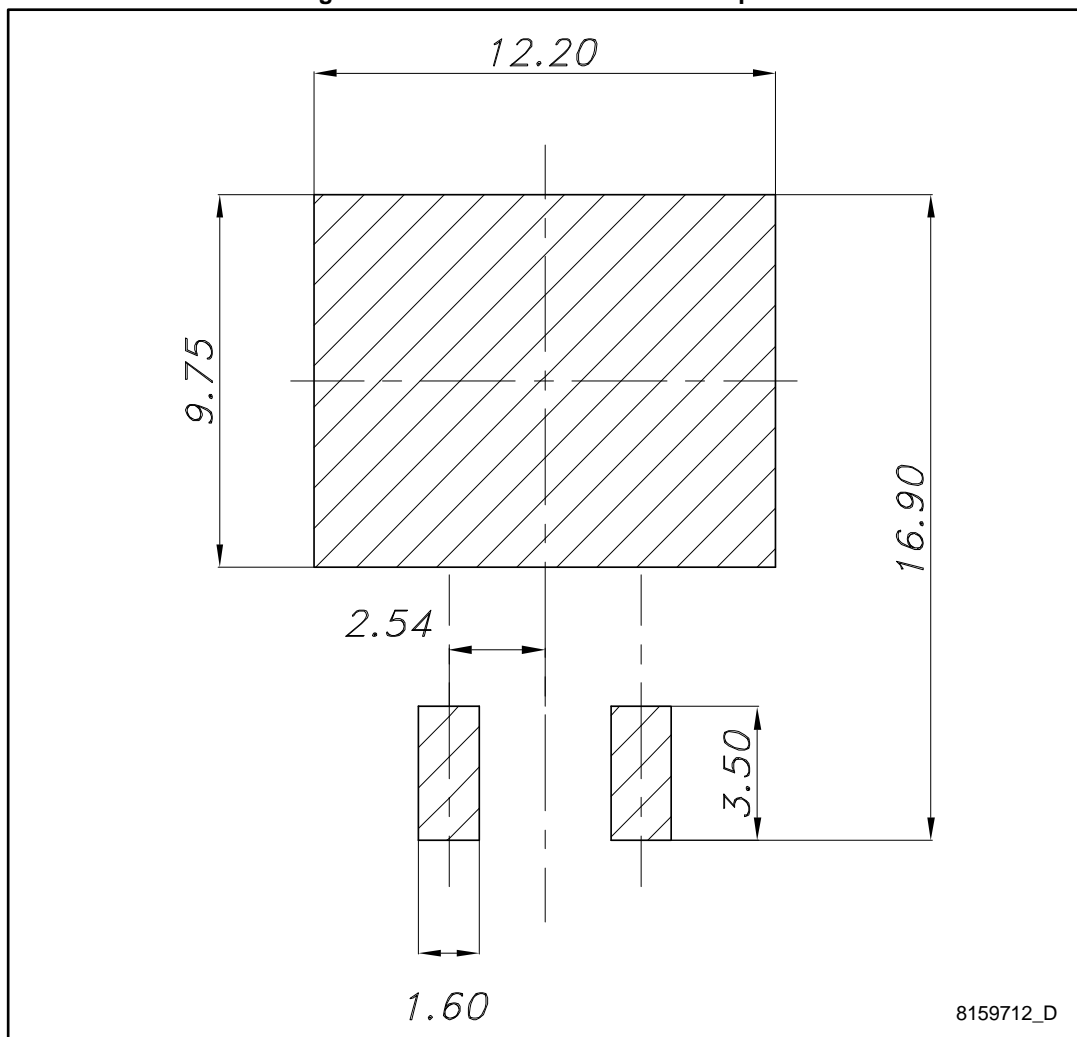
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Table 8: H<sup>2</sup>PAK-2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30	-	4.80
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.40		7.80
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

Figure 20: H<sup>2</sup>PAK-2 recommended footprint



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### 4.2 H<sup>2</sup>PAK-6 package information

Figure 21: H<sup>2</sup>PAK-6 package outline

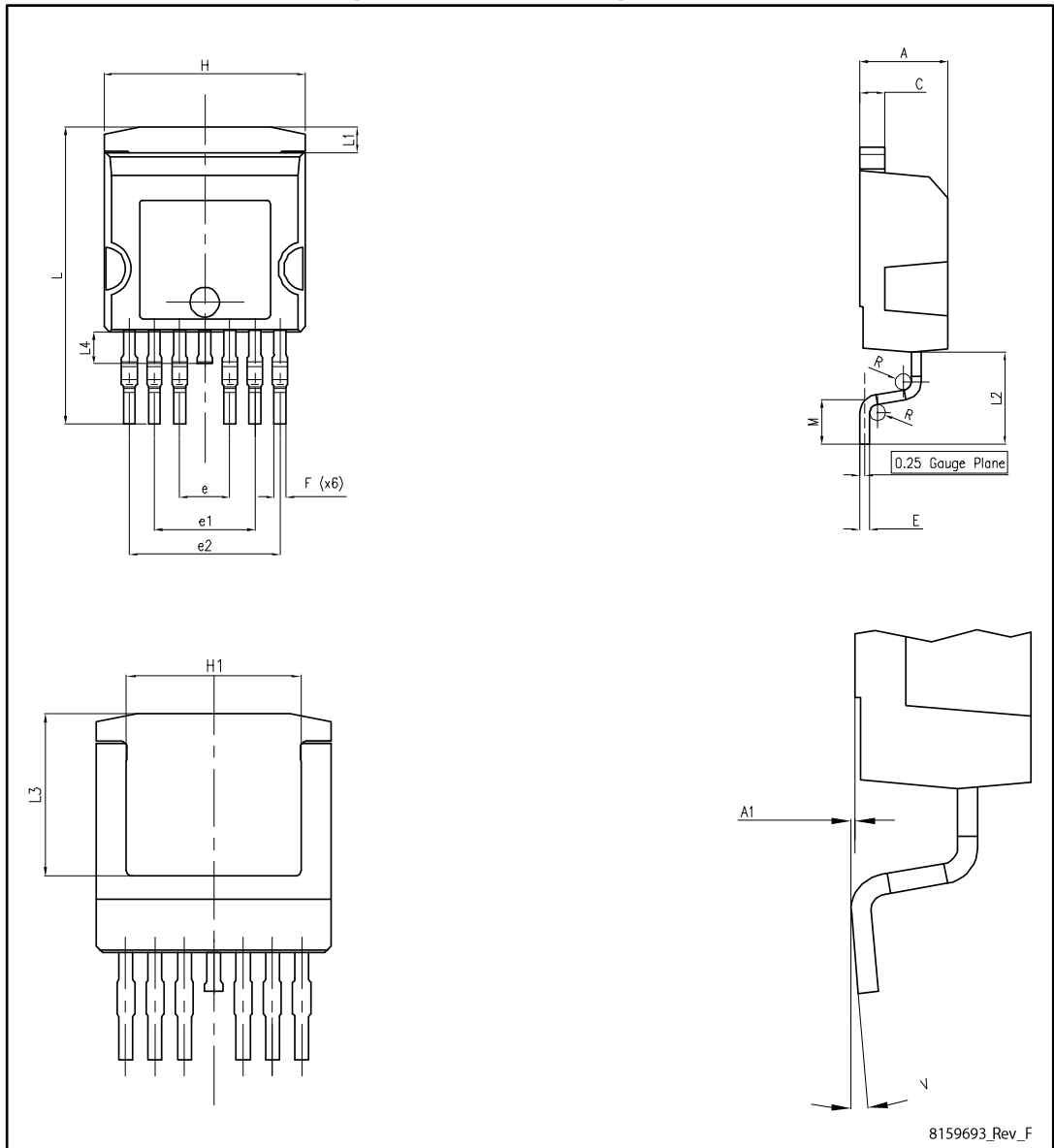
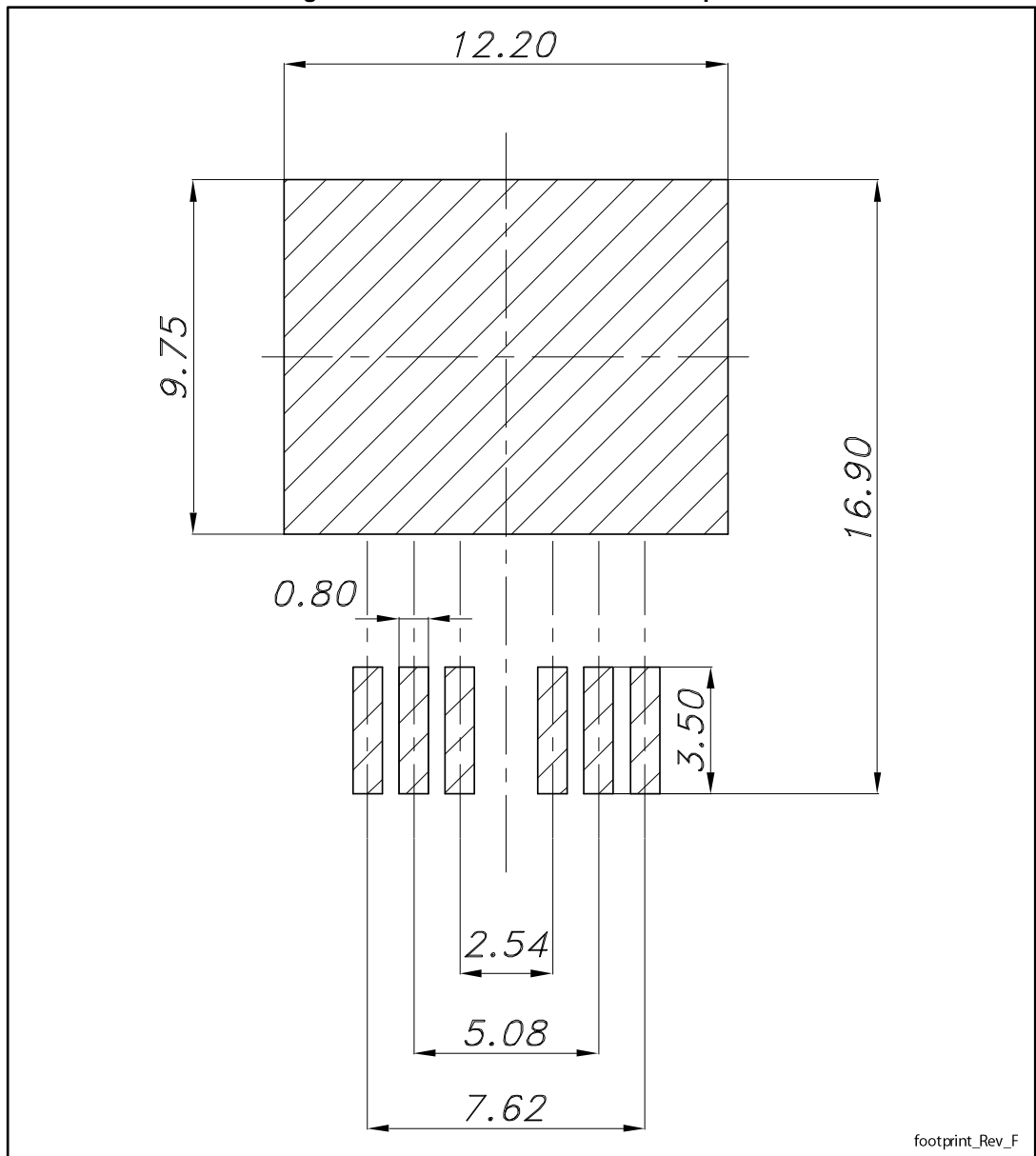


Table 9: H<sup>2</sup>PAK-6 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	0.03		0.20
C	1.17		1.37
e	2.34		2.74
e1	4.88		5.28
e2	7.42		7.82
E	0.45		0.60
F	0.50		0.70
H	10.00		10.40
H1	7.40		7.80
L	14.75		15.25
L1	1.27		1.40
L2	4.35		4.95
L3	6.85		7.25
L4	1.5		1.75
M	1.90		2.50
R	0.20		0.60
V	0°		8°

Figure 22: H<sup>2</sup>PAK-6 recommended footprint



Dimensions are in mm.

### 4.3 H<sup>2</sup>PAK packing information

Figure 23: Tape outline

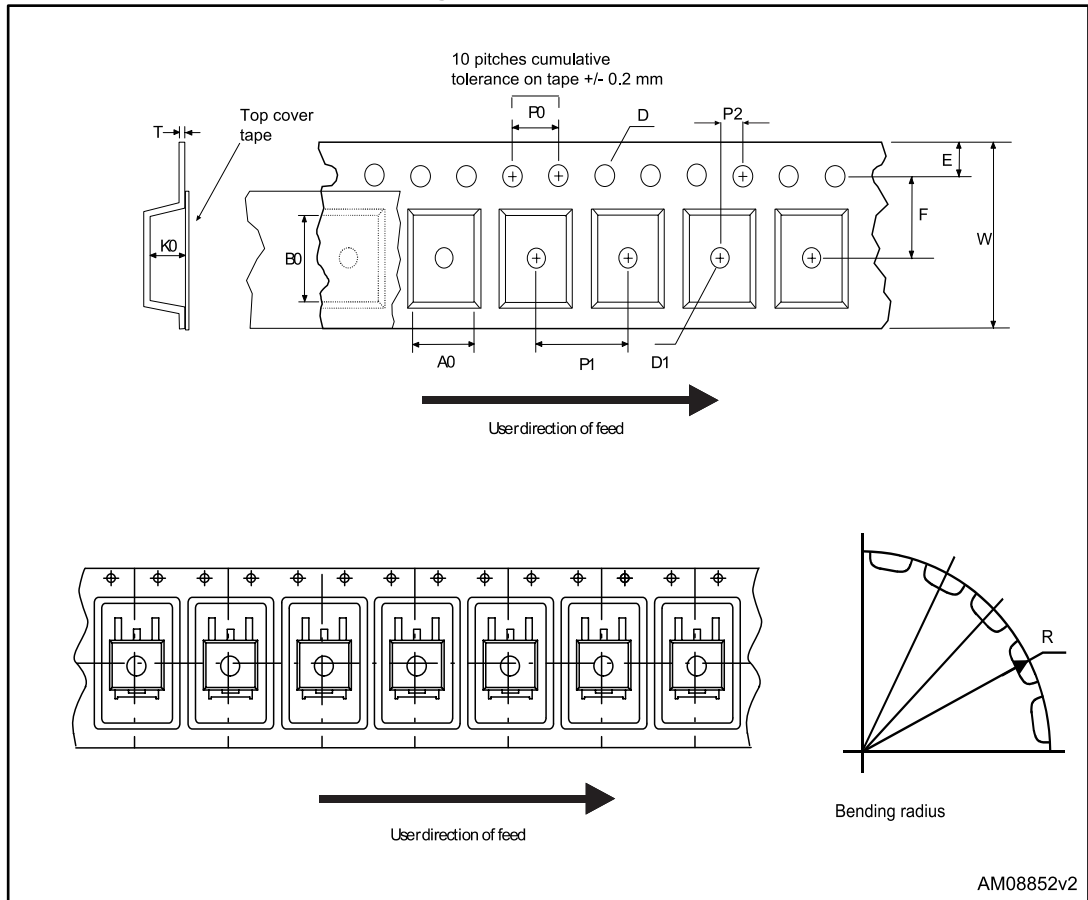


Figure 24: Reel outline

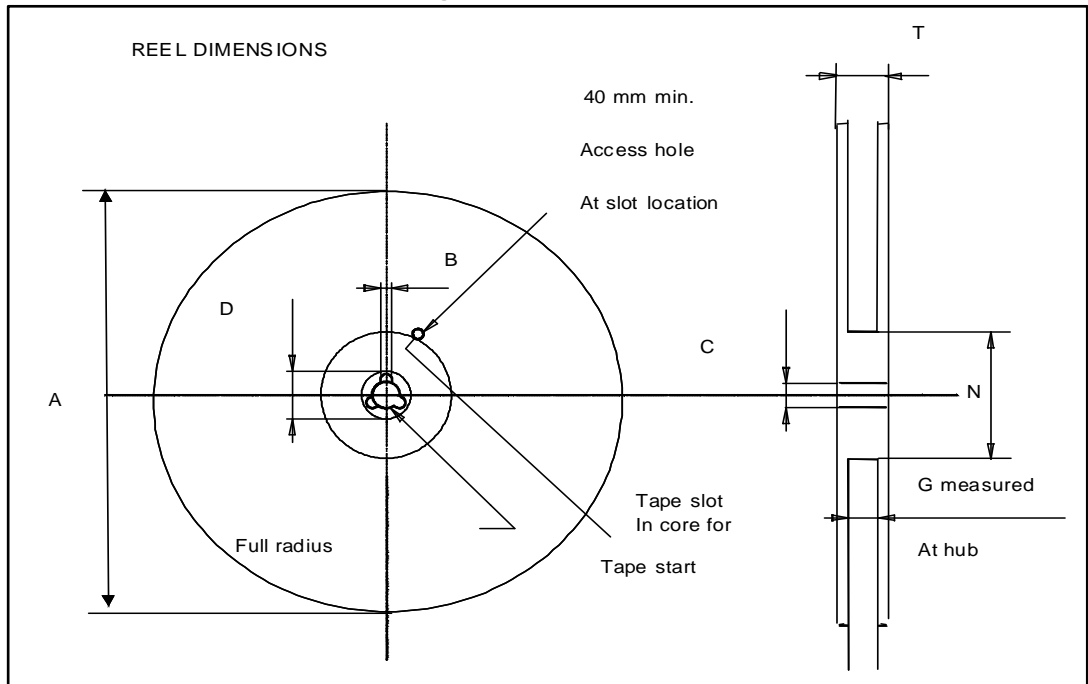




Table 10: Tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

## 5 Revision history

Table 11: Document revision history

Date	Revision	Changes
10-Apr-2015	1	First release.
13-May-2015	2	Updated Static.
04-Dec-2015	3	Updated note 1 in Table 2: "Absolute maximum ratings", Figure 2: "Safe operating area" and Figure 3: "Thermal impedance".
17-Feb-2016	4	Modified: <i>Table 2: "Absolute maximum ratings"</i> , <i>Table 4: "Static"</i> Modified: <i>Figure 2: "Safe operating area"</i> Minor text changes

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