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April 2000 Revised January 2005

NC7WZ38

TinyLogic® UHS Dual 2-Input NAND Gate (Open Drain Output)

General Description

The NC7WZ38 is a dual 2-Input NAND Gate with open drain output stage from Fairchild's Ultra High Speed Series of TinyLogic®. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad $V_{\rm CC}$ operating range. The device is specified to operate over the 1.65V to 5.5V $V_{\rm CC}$ range. The inputs and output are high impedance when $V_{\rm CC}$ is 0V. Inputs tolerate voltages up to 7V independent of $V_{\rm CC}$ operating voltage. The open drain output stage will tolerate voltages up to 7V independent of $V_{\rm CC}$ when in the high impedance state.

Features

- Space saving US8 surface mount package
- MicroPak™ Pb-Free leadless package
- Open Drain output stage for OR tied applications
- Ultra High Speed; t_{PD} 2.2 ns Typ into 50 pF at 5V V_{CC}
- High Output Sink Drive; 24 mA at 3V V_{CC}
- Broad V_{CC} Operating Range; 1.65V to 5.5V
- \blacksquare Matches the performance of LCX when operated at 3.3V V_{CC}
- Power down high impedance inputs/output
- Overvoltage Tolerant inputs facilitate 5V to 3V translation
- Patented noise/EMI reduction circuitry implemented

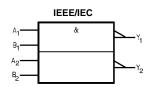
Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7WZ38K8X	MAB08A	WZ38	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide	3k Units on Tape and Reel
NC7WZ38L8X	MAC08A	U5	Pb-Free 8-Lead MicroPak, 1.6 mm Wide	5k Units on Tape and Reel

Pb-Free package per JEDEC J-STD-020B.

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Logic Symbol



Pin Descriptions

Pin Names	Description
A _n , B _n	Inputs
Y _n	Output

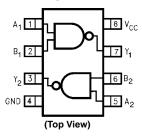
Function Table

 $Y = \overline{AB}$

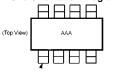
Inp	Output			
Α	A B			
L	L	*H		
L	Н	*H		
Н	L	*H		
Н	Н	L		

H = HIGH Logic Level L = LOW Logic Level *H = HIGH Impedance output state (Open Drain)

Connection Diagrams



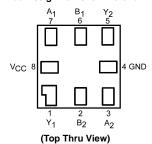
Pin One Orientation Diagram



AAA represents Product Code Top Mark - see ordering code

Note: Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

Pad Assignments for MicroPak



Absolute Maximum Ratings(Note 1)

DC Input Diode Current (I_{IK})

 $@V_{IN} < -0.5V$ -50 mA

DC Output Diode Current (I_{OK})

Junction Temperature under Bias (T_J) Junction Lead Temperature (T_L) ;

 $(\mbox{Soldering, 10 seconds}) \mbox{ 260°C} \\ \mbox{Power Dissipation ($P_{\rm D}$) @ +85°C} \mbox{ 250 mW}$

Recommended Operating Conditions (Note 2)

Input Rise and Fall Time (t_r, t_f)

Note 1: Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	v _{cc}	7	$T_A = +25^{\circ}C$;	$T_A = -40^{\circ}$	C to +85°C	Units	Conditions	
Syllibol	Parameter	(V)	Min Typ		Max	Min	Max	Ullits	Conditions	
V _{IH}	HIGH Level	1.65 to 1.95	0.75 V _{CC}			0.75 V _{CC}		V		
	Input Voltage	2.3 to 5.5	0.7 V _{CC}			0.7 V _{CC}		٧		
V _{IL}	LOW Level	1.65 to 1.95			0.25 V _{CC}		0.25 V _{CC}	V		
	Input Voltage	2.3 to 5.5			$0.3~\mathrm{V}_{\mathrm{CC}}$		$0.3 \mathrm{V_{CC}}$	V		
I _{LKG}	HIGH Level Output Leakage	5.5			±5		±10	μА	$V_{IN} = V_{IL}$ $V_{OUT} = V_{CC}$	or GND
V _{OL}	LOW Level	1.65		0.0	0.1		0.1			
	Output Voltage	2.3		0.0	0.1	İ	0.1	V	V -V	_ 1004
		3.0		0.0	0.1	İ	0.1	V	$V_{IN} = V_{IH}$	$I_{OL} = 100 \mu A$
		4.5		0.0	0.1		0.1			
		1.65		0.08	0.24		0.24			$I_{OL} = 4 \text{ mA}$
		2.3		0.10	0.3	İ	0.3			$I_{OL} = 8 \text{ mA}$
		3.0		0.15	0.4		0.4	V		I _{OL} = 16 mA
		3.0		0.22	0.55	İ	0.55			I _{OL} = 24 mA
		4.5		0.22	0.55		0.55			I _{OL} = 32 mA
I _{IN}	Input Leakage Current	5.5			±0.1		±1	μΑ	$V_{IN} = 5.5V, 0$	GND
I _{OFF}	Power Off Leakage Current	0.0			1		10	μА	V _{IN} or V _{OUT}	= 5.5V
I _{CC}	Quiescent Supply Current	1.65 to 5.5			1		10	μΑ	$V_{IN} = 5.5V, 0$	GND

150°C

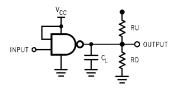
AC Electrical Characteristics

Symbol	Parameter	V _{CC}	V_{CC} $T_{A} = +25^{\circ}C$ $T_{A} = -40^{\circ}C$ $T_{C} = -40^{\circ}C$ (V) Min Typ Max Min		$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		Units	Conditions	Figure	
Cymbol		(V)			Max	Ullits	Conditions	Number		
t _{PZL}	Propagation Delay	1.8 ± 0.15	2.0	5.2	9.2	2.0	9.6		C _L = 50 pF	
		2.5 ± 0.2	1.5	3.5	5.7	1.5	6.1	ns	$RU=500\Omega$	Figures
		3.3 ± 0.3	1.0	2.8	4.1	1.0	4.5	115	$RD=500\Omega$	1, 3
		5.0 ± 0.5	0.5	2.2	3.4	0.5	3.6		$V_I = 2 \times V_{CC}$	
t _{PLZ}	Propagation Delay	1.8 ± 0.15	2.0	4.6	9.2	2.0	9.6		C _L = 50 pF	
		2.5 ± 0.2	1.5	3.2	5.7	1.5	6.1	ns	$RU = 500\Omega$	Figures
		3.3 ± 0.3	1.0	2.4	4.1	1.0	4.5	115	$RD = 500\Omega$	1, 3
		5.0 ± 0.5	0.5	1.6	3.4	0.5	3.6		$V_I = 2 \times V_{CC}$	
C _{IN}	Input Capacitance	0		2.5				pF		
C_{OUT}	Output Capacitance	0		4.2				pF		
C _{PD}	Power Dissipation	3.3		7				pF	(Note 3)	Figure 2
	Capacitance	5.0		9				PΓ	(Note 3)	i igule 2

Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression:

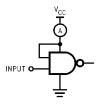
I_{CCD} = (C_{PD}) (V_{CC}) (f_{IN}) + (I_{CC} static).

AC Loading and Waveforms



 ${
m C_L}$ includes load and stray capacitance Input PRR = 1.0 MHz; ${
m t_w}$ = 500 ns

FIGURE 1. AC Test Circuit



$$\label{eq:lower_lower} \begin{split} & \text{Input} = \text{AC Waveform; } t_r = t_f = 1.8 \text{ ns} \\ & \text{PRR} = 10 \text{ MHz; Duty Cycle} = 50\% \end{split}$$

FIGURE 2. I_{CCD} Test Circuit

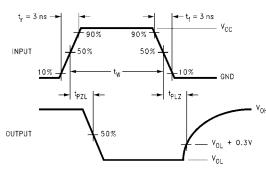


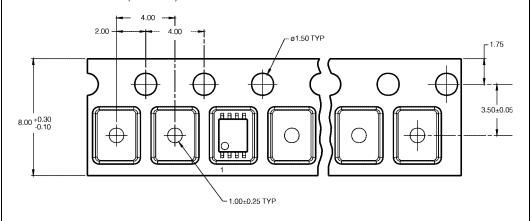
FIGURE 3. AC Waveforms

Tape and Reel Specification

TAPE FORMAT for US8

Package	Tape	Number	Cavity	Cover Tape	
Designator	Section	Cavities	Status	Status	
K8X	Leader (Start End)	125 (typ)	Empty	Sealed	
	Carrier	3000	Filled	Sealed	
	Trailer (Hub End)	75 (typ)	Empty	Sealed	

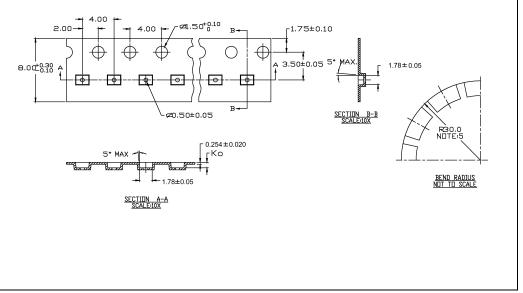
TAPE DIMENSIONS inches (millimeters)



TAPE FORMAT for MicroPak

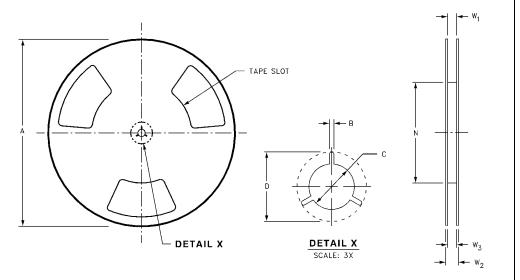
Package	Tape	Number	Cavity	Cover Tape Status	
Designator	Section	Cavities	Status		
	Leader (Start End)	125 (typ)	Empty	Sealed	
L8X	Carrier	3000	Filled	Sealed	
	Trailer (Hub End)	75 (typ)	Empty	Sealed	

TAPE DIMENSIONS inches (millimeters)



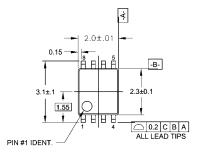
Tape and Reel Specification (Continued)

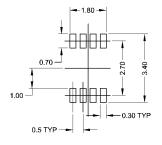
REEL DIMENSIONS inches (millimeters)



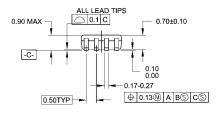
Tape Size	Α	В	C	D	N	W1	W2	W3
0	7.0	0.059	0.512	0.795	2.165	0.331 + 0.059/-0.000	0.567	W1 + 0.078/-0.039
8 mm	(177.8)	(1.50)	(13.00)	(20.20)	(55.00)	(8.40 + 1.50/-0.00)	(14.40)	(W1 + 2.00/-1.00)

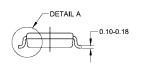
Physical Dimensions inches (millimeters) unless otherwise noted

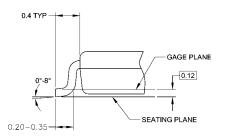




LAND PATTERN RECOMMENDATION







NOTES:

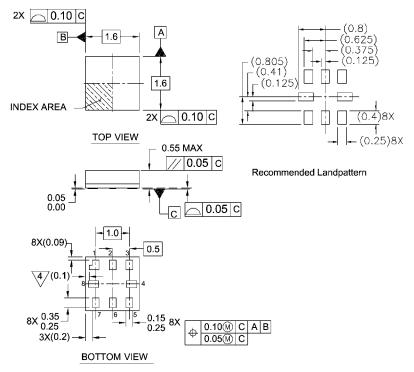
- CONFORMS TO JEDEC REGISTRATION MO-187
 B. DIMENSIONS ARE IN MILLIMETERS.
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

DETAIL A

MAB08AREVC

8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide Package Number MAB08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Notes:

- 1. PACKAGE CONFORMS TO JEDEC MO-255 VARIATION UAAD
- 2. DIMENSIONS ARE IN MILLIMETERS
- 3. DRAWING CONFORMS TO ASME Y.14M-1994

4/PIN 1 FLAG, END OF PACKAGE OFFSET.

MAC08AREVC

Pb-Free 8-Lead MicroPak, 1.6 mm Wide Package Number MAC08A

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