

LTC2358/LTC2357/
LTC2353/LTC2333:
16-/18-Bit, Octal, Quad and Dual
200ksps/350ksps/550ksps/800ksps SAR ADCs

DESCRIPTION

Demonstration circuit 2365A highlights the **LTC®2358** family of buffered input ADCs. The LTC2358/LTC2357/LTC2353/LTC2333 are low noise, high speed, 16-/18-bit successive approximation register (SAR) ADCs with integrated front end buffers. These ADCs accept a wide common mode range. Pico-amp inputs and high CMRR enable these ADCs to connect directly to a wide range of sensors without compromising measurement accuracy. The following text refers to the LTC2358-18 but applies to all parts in the family, the only differences being the number of bits, number of channels and the maximum sample rate. The LTC2358-18 has a flexible SoftSpan™ interface that allows conversion-by-conversion control of the input voltage span on a per-channel basis. An internal 2.048V reference and 2X buffer simplify basic operation while an external reference can be used to increase the input range and the SNR of the ADC.

The DC2365A demonstrates the DC and AC performance of the LTC2358-18 in conjunction with the DC590/DC2026 and DC890 data collection boards. Use the DC590/DC2026 to demonstrate DC performance such as peak-to-peak noise and DC linearity. Use the DC890 if precise sampling rates are required or to demonstrate AC performance such as SNR, THD, SINAD and SFDR. The DC2365A is intended to demonstrate recommended grounding, component placement and selection, routing and bypassing for this ADC. A simple driver circuit for the analog inputs is also presented.

Design files for this circuit board including schematics, BOM and layout are available at <http://www.linear.com/demo/DC2365A>

LT, LTC, LTM, Linear Technology, LinDuino and the Linear logo are registered trademarks and SoftSpan, PScope and QuikEval are trademarks of Analog Devices, Inc. All other trademarks are the property of their respective owners.

DEMO MANUAL DC2365A

BOARD PHOTO

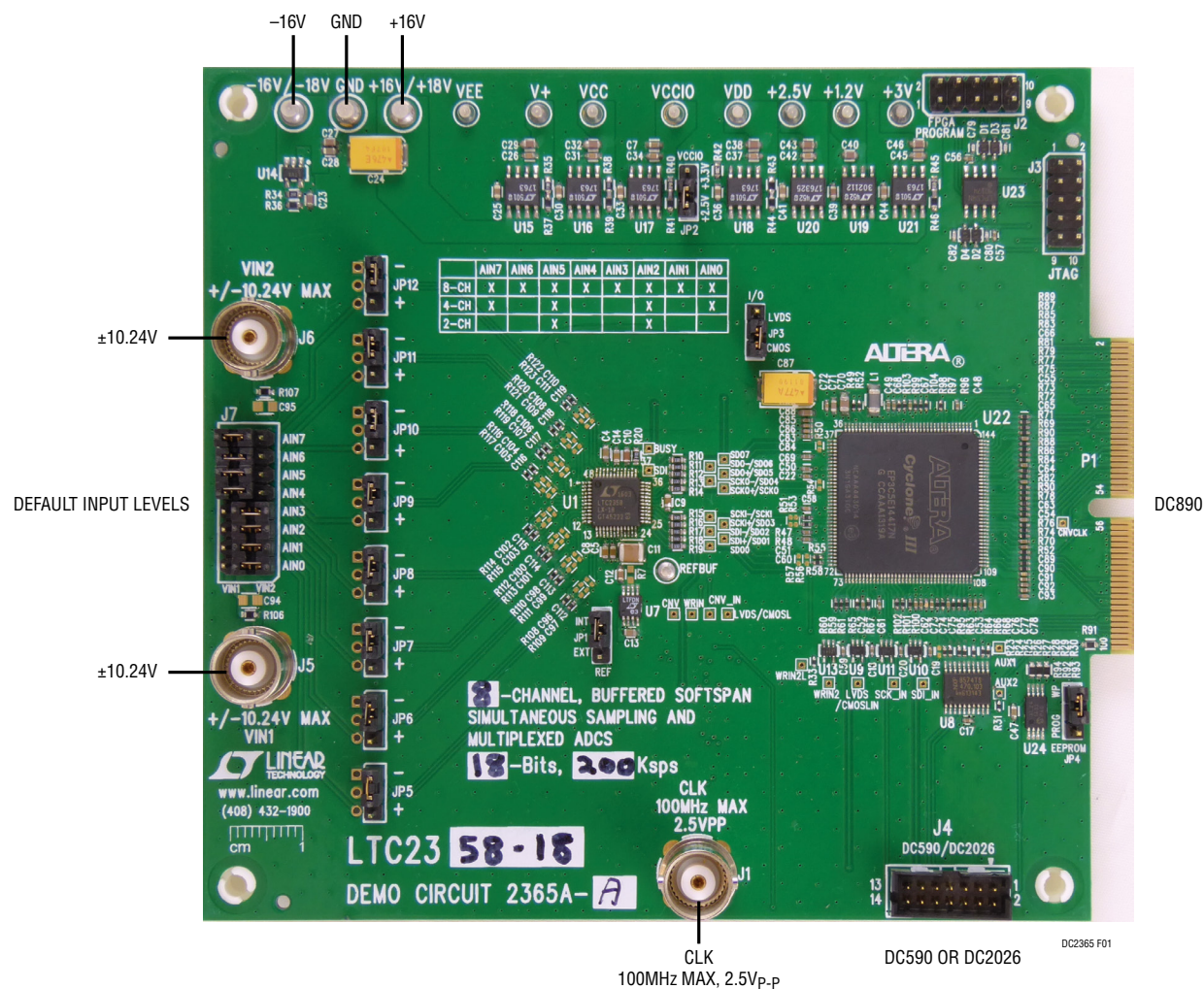


Figure 1. DC2365A Connection Diagram

ASSEMBLY OPTIONS

Table 1. DC2365A Assembly Options

ASSEMBLY VERSION	U1 PART NUMBER	MAX CONVERSION RATE	NUMBER OF CHANNELS	NUMBER OF BITS	MAX CLKIN FREQUENCY	CLKIN/fs RATIO
DC2365A-A	LTC2358-18	200ksps	8 Simultaneous	18	60MHz	300
DC2365A-B	LTC2357-18	350ksps	4 Simultaneous	18	60.2MHz	172
DC2365A-C	LTC2353-18	550ksps	2 Simultaneous	18	49.5MHz	90
DC2365A-D	LTC2333-18	800ksps	8 Multiplexed	18	50.4MHz	63
DC2365A-E	LTC2358-16	200ksps	8 Simultaneous	16	60MHz	300
DC2365A-F	LTC2357-16	350ksps	4 Simultaneous	16	60.2MHz	172
DC2365A-G	LTC2353-16	550ksps	2 Simultaneous	16	49.5MHz	90
DC2365A-H	LTC2333-16	800ksps	8 Multiplexed	16	50.4MHz	63

DC890 QUICK START PROCEDURE

Check to make sure that all switches and jumpers are set to their default settings as described in the DC2365A Jumpers section of this manual. The default connections configure the ADC to use the onboard reference and regulators to generate all the required bias voltages. The analog inputs by default are DC-coupled. Connect the DC2365A to a DC890 USB high speed data collection board using connector P1. Then, connect the DC890 to a host PC with a standard USB A/B cable. Apply $\pm 16V$ to the indicated terminals. Then apply a low jitter signal source to J5 and J6. Use J7 to route the signal sources of J5 and J6 to the desired AIN0–AIN7 inputs. Observe the recommended input voltage range for each analog input. Connect a low jitter 2.5V_{P-P} sine wave or square wave to connector J1. See Table 1 for the appropriate clock frequency. Note that J1 has a 50 Ω termination resistor to ground.

Run the PScope™ software (Pscope.exe version K94 or later) which can be downloaded from www.linear.com/designtools/software.

Complete software documentation is available from the Help menu. Updates can be downloaded from the Tools menu. Check for updates periodically as new features may be added.

The PScope software should recognize the DC2365A and configure itself automatically.

Click the Collect button (Figure 2) to begin acquiring data. The Collect button then changes to Pause, which can be clicked to stop data acquisition.

DC890 QUICK START PROCEDURE

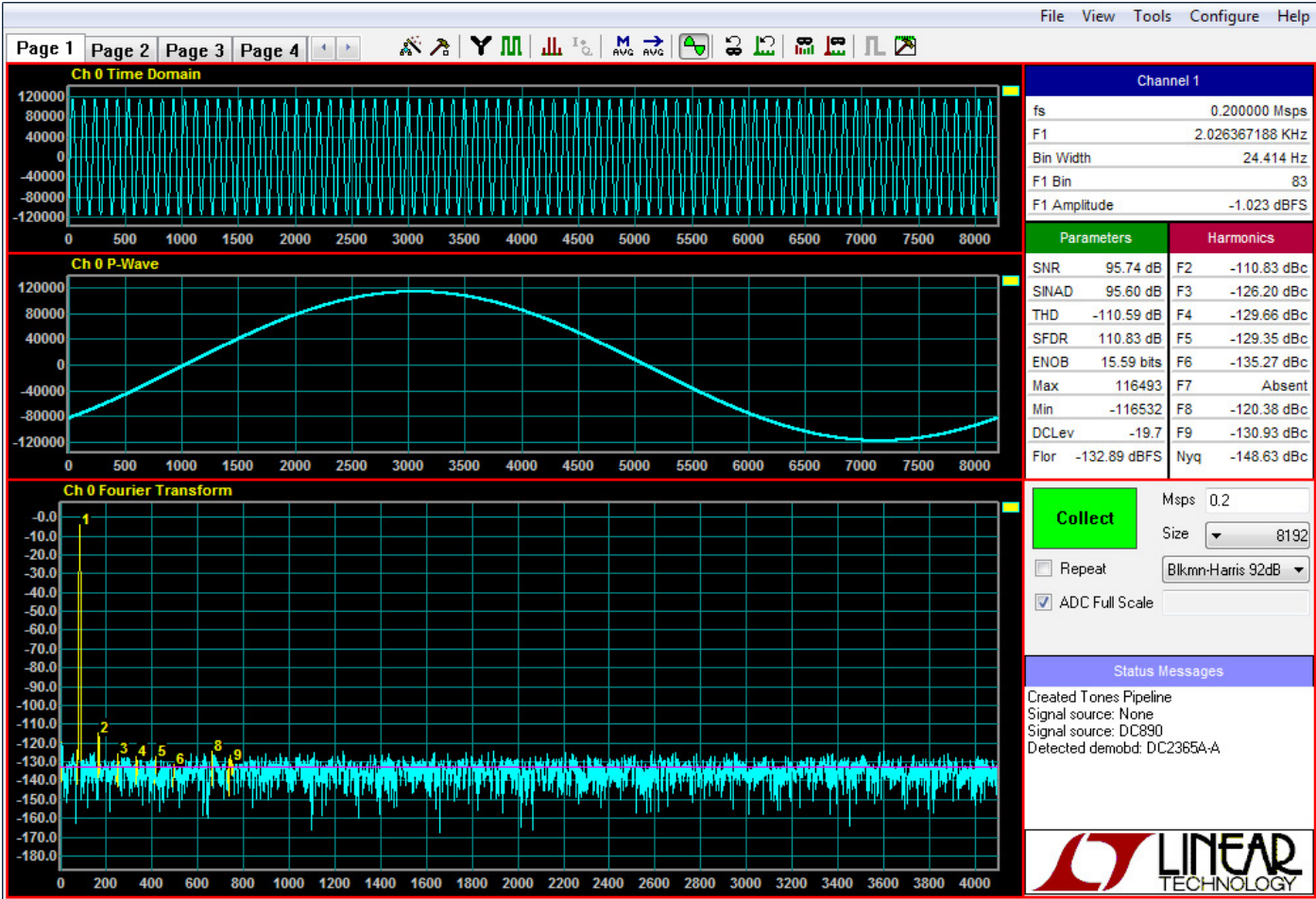


Figure 2. PScope Screen Capture

DC590/DC2026 QUICK START PROCEDURE

IMPORTANT! TO AVOID DAMAGE TO THE DC2365A, MAKE SURE THAT VCCIO (JP6 OF THE DC590, JP3 OF THE DC2026) OF THE DC590/DC2026 IS SET TO 3.3V BEFORE CONNECTING THE DC590/DC2026 TO THE DC2365A.

To use the DC590/DC2026 with the DC2365A, it is necessary to apply $\pm 16\text{V}$ and ground to the $\pm 16\text{V}$ and GND terminals of the DC2365A. Connect the DC590/DC2026 to a host PC with a standard USB A/B cable. Connect the DC2365A to a DC590/DC2026 USB serial controller using

the supplied 14-conductor ribbon cable. Apply a signal source to J5 and J6. Use J7 to route the signal sources of J5 and J6 to the desired AIN0–AIN7 inputs. No clock is required on J1 when using the DC590/DC2026. The clock signal is provided by the DC590/DC2026.

Run the QuikEval™ software (quikeval.exe version K108 or later) which is available from www.linear.com/designtools/software. The correct control panel will be loaded automatically. Click the Collect button (Figure 3) to begin reading the ADC.

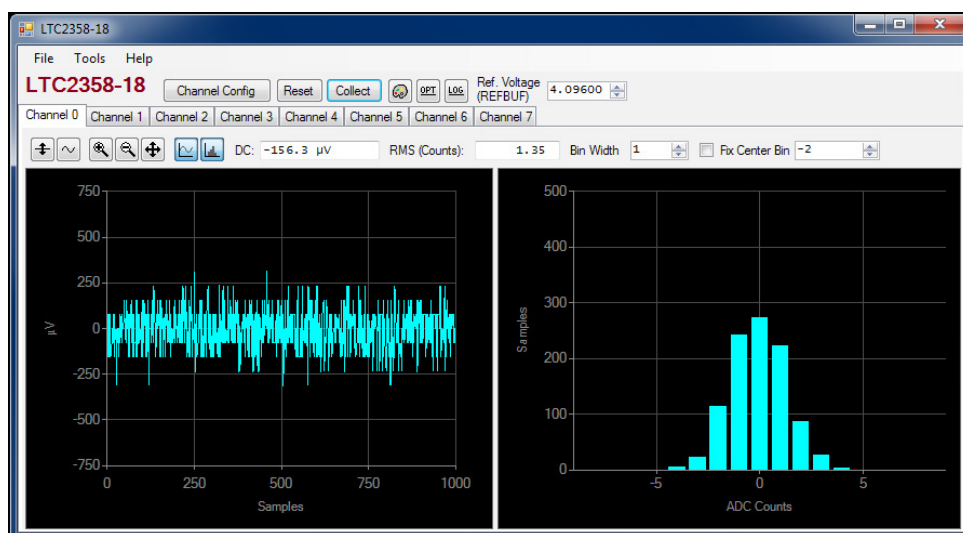
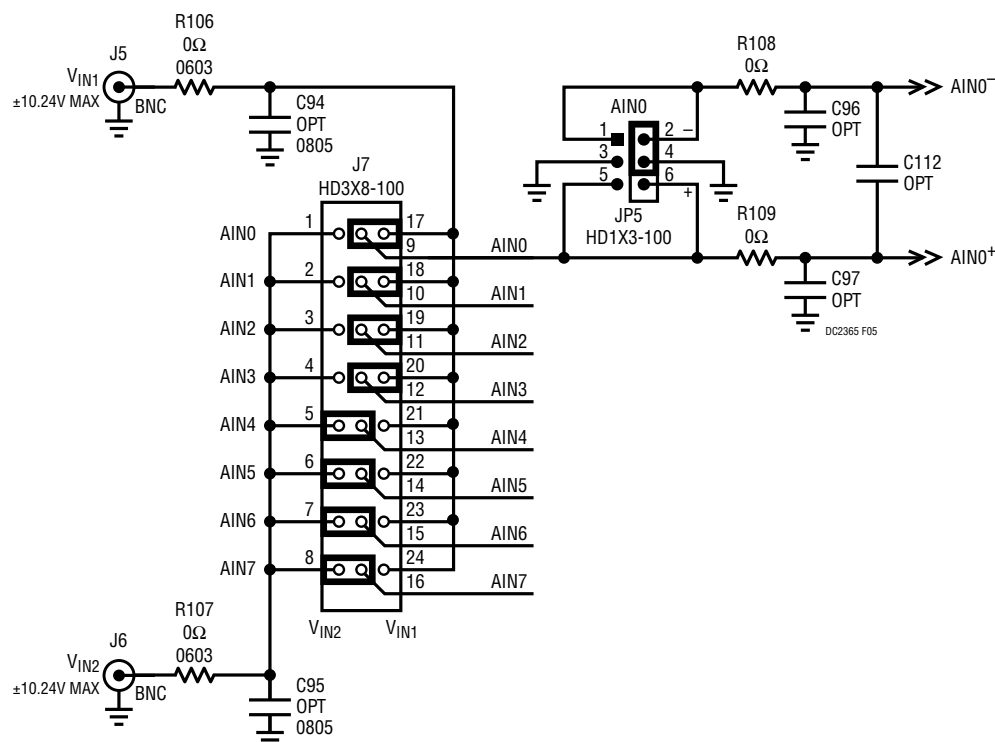


Figure 3. QuikEval Screen Capture

DC2365A SETUP

Figure 5. $\pm 10.24\text{V}$ Pseudo-Differential DC Coupled Driver

Performance Characteristics section of the LTC2358-18 data sheet. This involves using a 60MHz clock source along with a sinusoidal generator at a frequency of approximately 2kHz. The input signal level is approximately -1dBFS . A typical FFT obtained with the DC2365A is shown in Figure 2. Note that to calculate the real SNR, the signal level (F1 amplitude = -1.023dB) has to be added back to the SNR that PScope displays. With the example shown in Figure 2, this means that the actual SNR would be 96.76dB instead of the 95.74dB that PScope displays. Taking the RMS sum of the recalculated SNR and the THD yields a SINAD of 96.58dB which is fairly close to the typical number for this ADC.

To change the default settings for the LTC2358-18 in PScope, click on the Set Demo Bd Options button in the PScope tool bar shown in Figure 6. This will open the Configure Channels menu of Figure 7. In this menu it is possible to set the input SoftSpan range setting for each channel. There is also a button to return PScope to the

default DC2365A settings which are optimized for the default hardware settings of the DC2365A.

There are a number of scenarios that can produce misleading results when evaluating an ADC. One that is common is feeding the converter with an input frequency, that is a sub-multiple of the sample rate, and which will only exercises a small subset of the possible output codes. The proper method is to pick an M/N frequency for the input sine wave frequency. N is the number of samples in the FFT. M is a prime number between one and $N/2$. Multiply M/N by the sample rate to obtain the input sine wave frequency. Another scenario that can yield poor results is if you do not have a signal generator capable of ppm frequency accuracy or if it cannot be locked to the clock frequency. You can use an FFT with windowing to reduce the “leakage” or spreading of the fundamental to get a close approximation of the ADC performance. If an amplifier or clock source with poor phase noise is used, the windowing will not improve the SNR.

DC2365A SETUP



Figure 6. PScope Tool Bar

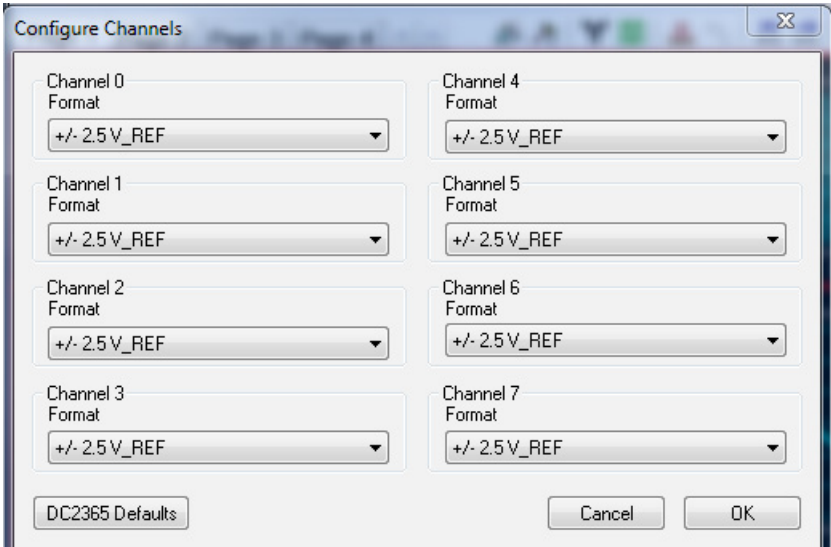


Figure 7. PScope Channel Configuration Menu

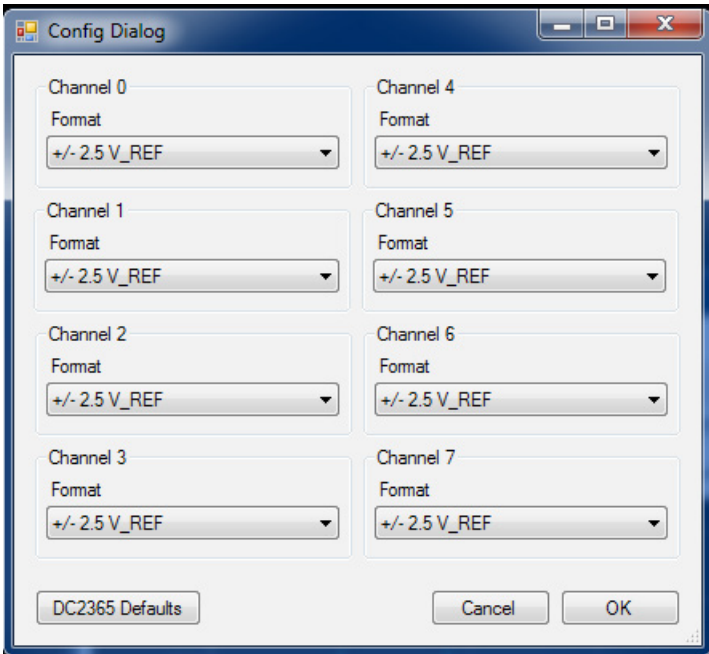


Figure 8. QuikEval Channel Configuration Menu

DC2365A SETUP

DC590/DC2026 Data Collection

Due to the relatively low and somewhat unpredictable sample rate of the DC590/DC2026, its usefulness is limited to noise measurement and data collection of slowly moving signals. A typical data capture and histogram are shown in Figure 3. To change the default settings for the LTC2358-18 in QuikEval, click on the Channel Config button. This will open the Config Dialog menu of Figure 8. Using the Config Dialog menu, it is possible to set the input signal range for each sequence. There is also a button to return QuikEval to the default DC2365A settings which are optimized for the default hardware settings of the DC2365A.

Layout

As with any high performance ADC, this part is sensitive to layout. The area immediately surrounding the ADC on the DC2365A should be used as a guideline for placement and routing of the various components associated with the ADC. Here are some things to remember when

laying out a board for the LTC2358-18. A ground plane is necessary to obtain maximum performance. Keep bypass capacitors as close to supply pins as possible. Use individual low impedance returns for all bypass capacitors. Use of a symmetrical layout around the analog inputs will minimize the effects of parasitic elements. Shield analog input traces with ground to minimize coupling from other traces. Keep traces as short as possible.

Component Selection

When driving a low noise, low distortion ADC such as the LTC2358-18, component selection is important so as to not degrade performance. Resistors should have low values to minimize noise and distortion. Metal film resistors are recommended to reduce distortion caused by self heating. Because of their low voltage coefficients, to further reduce distortion, NP0 or silver mica capacitors should be used. Any buffer used to drive the LTC2358-18 should have low distortion and low noise such as the LT1355 or LTC2057.

DC2365A JUMPERS

Definitions

JP1: REF selects INT or EXT reference for the ADC. The default setting is INT.

JP2: VCCIO sets the output levels at P1 to either 3.3V or 2.5V. Use 2.5V to interface to the DC890 which is the default setting. Use 3.3V to interface to the DC2026.

JP3: I/O selects LVDS or CMOS logic levels. The default setting is CMOS. LVDS is not supported at this time.

JP4: EEPROM is for factory use only. The default position is WP.

JP5-JP12: Can be used to short either the + or – input of AIN0–AIN7 to ground. The individual AIN inputs can also be driven directly through these terminals. The default is to short the – input of AIN0–AIN7 to ground.

DC2365A CONNECTORS

Definitions

P1: DC890 interface is used to communicate with the DC890 controller.

J1: CLK provides the master clock for the DC2365A when interfaced to the DC890. This is not used for QuikEval.

J2: FPGA PROGRAM is used to program the FPGA. This is for factory use only.

J3: JTAG is for factory use only.

J4: DC590/DC2026 interface is used to communicate with the DC2026 Linduino® controller or DC590.

J5 and J6: V_{IN1} , V_{IN2} provide analog input voltages to AIN0–AIN7 of the ADC.

J7: Routes the signals of J5 and J6 to AIN0–AIN7.

DEMO MANUAL DC2365A

DEMONSTRATION BOARD IMPORTANT NOTICE

Linear Technology Corporation (LTC) provides the enclosed product(s) under the following **AS IS** conditions:

This demonstration board (DEMO BOARD) kit being sold or provided by Linear Technology is intended for use for **ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY** and is not provided by LTC for commercial use. As such, the DEMO BOARD herein may not be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including but not limited to product safety measures typically found in finished commercial goods. As a prototype, this product does not fall within the scope of the European Union directive on electromagnetic compatibility and therefore may or may not meet the technical requirements of the directive, or other regulations.

If this evaluation kit does not meet the specifications recited in the DEMO BOARD manual the kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY THE SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THIS INDEMNITY, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user releases LTC from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge. Also be aware that the products herein may not be regulatory compliant or agency certified (FCC, UL, CE, etc.).

No License is granted under any patent right or other intellectual property whatsoever. **LTC assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or any other intellectual property rights of any kind.**

LTC currently services a variety of customers for products around the world, and therefore this transaction **is not exclusive**.

Please read the DEMO BOARD manual prior to handling the product. Persons handling this product must have electronics training and observe good laboratory practice standards. **Common sense is encouraged.**

This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

Mailing Address:

Linear Technology
1630 McCarthy Blvd.
Milpitas, CA 95035

Copyright © 2004, Linear Technology Corporation

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru

moschip.ru_4

moschip.ru_6

moschip.ru_9