CY2213

High Frequency Programmable PECL Clock Generator

Features

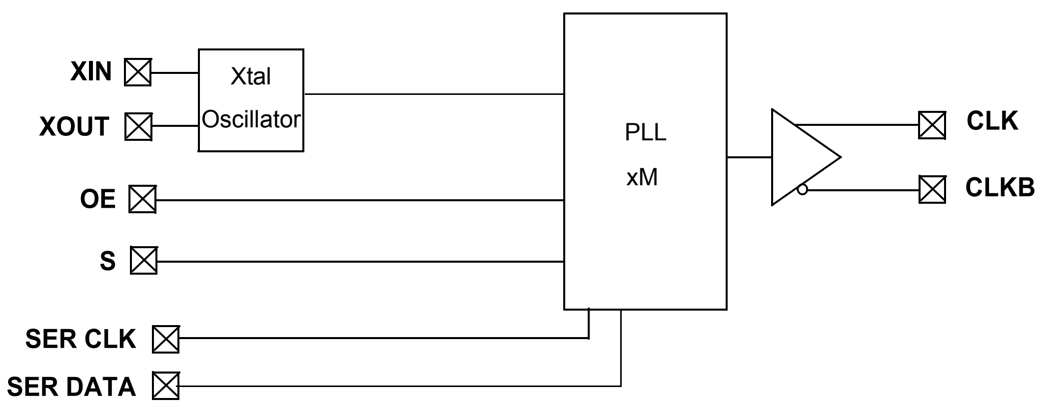
- Jitter peak-peak (Typical) = 35 ps
- LVPECL output
- Default Select option
- Serially configurable multiply ratios
- Output edge rate control
- 16-pin TSSOP
- High frequency
- 3.3 V operation

Benefits

- High accuracy clock generation
- One pair of differential output drivers
- Phase-locked loop (PLL) multiplier select
- 8-bit feedback counter and 6-bit reference counter for high accuracy
- Minimize electromagnetic interference (EMI)
- Industry standard, low cost package saves on board space

For a complete list of related documentation, click here.

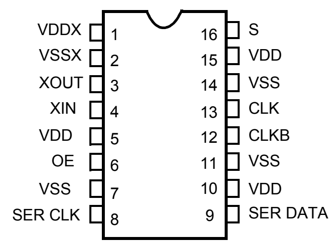
Logic Block Diagram



Contents

Pinouts

Figure 1. 16-pin TSSOP pinout



Pin Definitions

Pin Name	Pin Number	Pin Description
VDDX	1	3.3 V Power Supply for Crystal Driver
VSSX	2	Ground for Crystal Driver
XOUT	3	Reference Crystal Feedback
XIN	4	Reference Crystal Input
VDD	5	3.3 V Power Supply (all V_{DD} pins must be tied directly on board)
OE	6	Output Enable, 0 = output disable, 1 = output enable (no internal pull up)
VSS	7	Ground
SER CLK	8	Serial Interface Clock
SER DATA	9	Serial Interface Data
VDD	10	3.3 V Power Supply (all V_{DD} pins must be tied directly on board)
VSS	11	Ground
CLKB	12	LVPECL Output Clock (complement)
CLK	13	LVPECL Output Clock
VSS	14	Ground
VDD	15	3.3 V Power Supply (all V_{DD} pins must be tied directly on board)
S	16	PLL Multiplier Select Input, Pull up Resistor Internal

Frequency Table

S	M (PLL Multiplier)	Example Input Crystal Frequency	CLK, CLKB
0	× 16	25 MHz	400 MHz
1	× 8	15.625 MHz	125 MHz

CY2213 Two-Wire Serial Interface

Introduction

The CY2213 has a two-wire serial interface designed for data transfer operations, and is used for programming the P and Q values for frequency generation. S_{clk} is the serial clock line controlled by the master device. S_{data} is a serial bidirectional data line. The CY2213 is a slave device and can either read or write information on the dataline upon request from the master device.

Figure 2 shows the basic bus connections between master and slave device. The buses are shared by a number of devices and are pulled high by a pull up resistor.

Serial Interface Specifications

Figure 3 shows the Basic Transmission Specification. To begin and end a transmission, the master device generates a start signal (S) and a stop signal (P). Start (S) is defined as switching the S_{data} from HIGH to LOW while the S_{clk} is at HIGH. Similarly, stop (P) is defined as switching the S_{data} from LOW to HIGH while holding the S_{clk} HIGH. Between these two signals, data on S_{data} is synchronous with the clock on the S_{clk}. Data is allowed to change only at LOW period of clock, and must be stable at the HIGH period of clock. To acknowledge, drive the S_{data} LOW before the S_{clk} rising edge and hold it LOW until the S_{clk} falling edge.

Serial Interface Format

Each slave carries an address. The data transfer is initiated by a start signal (S). Each transfer segment is 1 byte in length. The slave address and the read/write bit are first sent from the master device after the start signal. The addressed slave device must acknowledge (Ack) the master device. Depending on the Read/Write bit, the master device either writes data into (logic 0) or reads data (logic 1) from the slave device. Each time a byte of data is successfully transferred, the receiving device must acknowledge. At the end of the transfer, the master device generates a stop signal (P).

Serial Interface Transfer Format

Figure 3 shows the serial interface transfer format used with the CY2213. Two dummy bytes must be transferred before the first data byte. The CY2213 has only three bytes of latches to store information, and the third byte of data is reserved. Extra data is ignored.

Figure 2. Device Connections

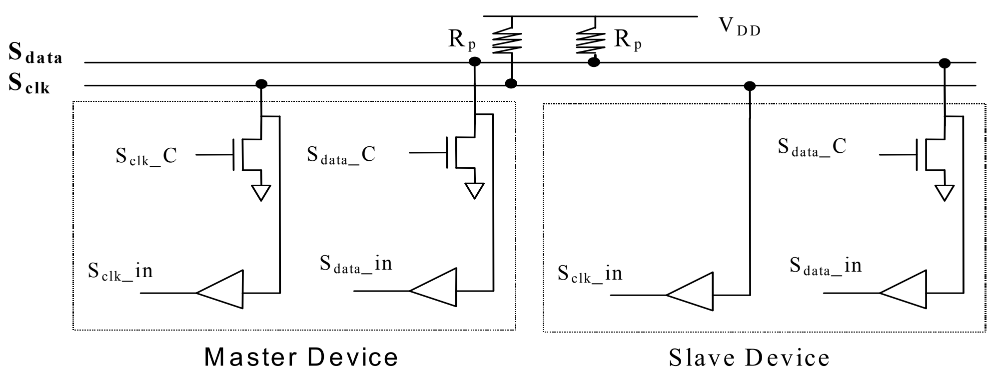


Figure 3. Serial Interface Specifications

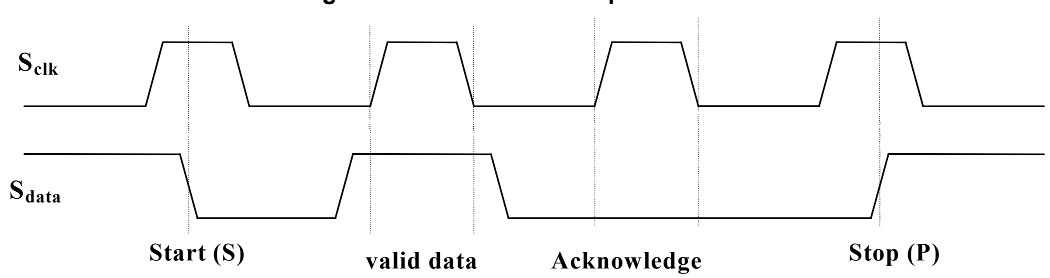


Figure 4. CY2213 Transfer Format

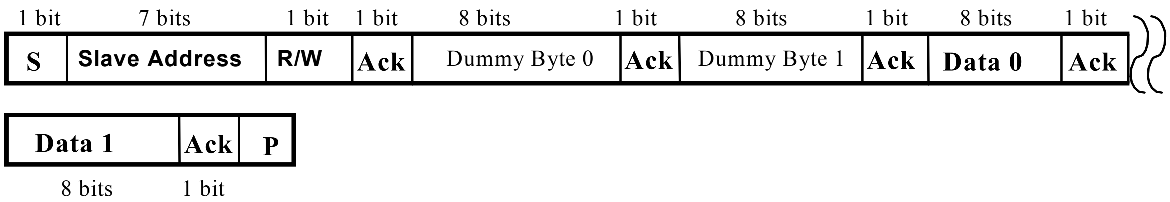


Table 1. Serial Interface Address for the CY2213

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	0	1	0	1	0

Table 2. Serial Interface Programming for the CY2213

	b7	b6	b5	b4	b3	b2	b1	b0
Data0	QCNTBYP	SELPQ	Q<5>	Q<4>	Q<3>	Q<2>	Q<1>	Q<0>
Data1	P<7>	P<6>	P<5>	P<4>	P<3>	P<2>	P<1>	P<0>
Data2	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

To program the CY2213 using the two-wire serial interface, set the SELPQ bit HIGH. The default setting of this bit is LOW. The P and Q values are determined by the following formulas:

$P_{final} = (P_{7..0} + 3) \times 2$

$Q_{final} = Q_{5..0} + 2.$

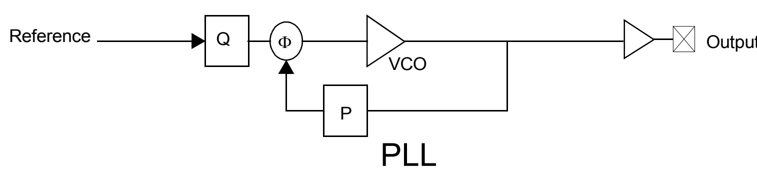
PLL Frequency = Reference x P/Q = Output

If the QCNTBYP bit is set HIGH, then Q_{final} defaults to a value of 1. The default setting of this bit is LOW.

If the SELPQ bit is set LOW, the PLL multipliers are set using the values in the Select Function Table.

CyberClocks™ has been developed to generate P and Q values for stable PLL operation. This software is downloadable from www.cypress.com

Figure 5. PLL Block Diagram



Absolute Maximum Conditions

The following table reflects stress ratings only, and functional operation at the maximums are not guaranteed.

Parameter	Description	Min	Max	Unit
$V_{DD, ABS}$	Maximum voltage on V_{DD}, or V_{DDX} with respect to ground	–0.5	4.0	V
$V_{I, ABS}$	Maximum voltage on any pin with respect to ground	–0.5	V_{DD} + 0.5	V

Crystal Requirements

Requirements to use parallel mode fundamental xtal. External capacitors are required in the crystal oscillator circuit. Please refer to the application note entitled **Crystal Oscillator Topics** for details.

Parameter	Description	Min	Max	Unit
X_F	Crystal fundamental frequency	10	31.25	MHz

Electrical Characteristics

DC Electrical Specifications

Parameter	Description	Min	Max	Unit
V_{DD}	Supply voltage	3.00	3.60	V
T_A	Ambient operating temperature	0	70	°C
V_{IL}	Input signal low voltage at pin S	–	0.35	V_{DD}
V_{IH}	Input signal high voltage at pin S	0.65	–	V_{DD}
R_{PUP}	Internal pull up resistance	10	100	kΩ
t_{PU}	Power up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	0.05	500	ms

3.3 V DC Device Characteristics

(Driving load, Figure 6)

Parameter	Description	Min	Typ	Max	Unit
V_{OH}	Output high voltage, referenced to V_{DD}	–1.02	–0.95	–0.88	V
V_{OL}	Output low voltage, referenced to V_{DD}	–1.81	–1.70	–1.62	V

(Driving load, Figure 7)

Parameter	Description	Min	Typ	Max	Unit
V_{OH}	Output high voltage	1.1	1.2	1.3	V
V_{OL}	Output low voltage	0	0	0	V

AC Electrical Specifications

Parameter	Description	Min	Max	Unit
f_{IN}	Input frequency with driven reference	1	133	MHz
$f_{XTAL,IN}$	Input frequency with crystal input	10	31.25	MHz
$C_{IN,CMOS}$	Input capacitance at S pin [1]	–	10	pF

AC Device Characteristics

Parameter	Description	Min	Max	Unit
t_{CYCLE}	Clock cycle time	2.50 (400 MHz)	8.00 (125 MHz)	ns
t_{JCRMS}	Cycle-to-cycle RMS jitter	–	0.25%	% t_{CYCLE}
	At 125 MHz frequency	–	20	ps
	At 400 MHz frequency	–	6.25	ps
t_{JCPK}	Cycle-to-cycle jitter (pk-pk)	–	1.75%	% t_{CYCLE}
	At 125 MHz frequency	–	140	ps
	At 200 MHz frequency, XF = 25 MHz	–	55	ps
	At 400 MHz frequency	–	43.75	ps
t_{JPRMS}	Period jitter RMS	–	0.25%	% t_{CYCLE}
	At 125 MHz frequency	–	20	ps
	At 400 MHz frequency	–	6.25	ps
t_{JPPK}	Period jitter (pk-pk)	–	2.0%	% t_{CYCLE}
	At 125 MHz frequency	–	160	ps
	At 200 MHz frequency, XF = 25 MHz	–	65	ps
	At 400 MHz frequency	–	50	ps
t_{JLT}	Long term RMS Jitter (P < 20)	–	1.75%	% t_{CYCLE}
	At 125 MHz frequency	–	140	ps
	At 400 MHz frequency	–	43.75	ps
t_{JLT}	Long term RMS Jitter ($20 \le P < 40$)	–	2.5%	% t_{CYCLE}
	At 125 MHz frequency	–	200	ps
	At 400 MHz frequency	–	62.5	ps
t_{JLT}	Long term RMS Jitter ($40 \le P < 60$)	–	3.5%	% t_{CYCLE}
	At 125 MHz frequency	–	280	ps
	At 400 MHz frequency	–	87.5	ps
Phase Noise	Phase Noise at 10 kHz (x8 mode) at 125 MHz	–107	–92	dBc
DC	Long term average output duty cycle	45	55	%
$t_{DC,ERR}$	Cycle-cycle duty cycle error at x8 with 15.625 MHz input	–	70	ps
t_{CR}, t_{CF}	Output rise and fall times (measured at 20% – 80% of V_{OHmin} and V_{OLmax})	100	400	ps
BW_{LOOP}	PLL Loop Bandwidth	50 kHz (–3 dB)	8 MHz (–20 dB)	

Note
1. Capacitance measured at frequency = 1 MHz, DC Bias = 0.9V, and VAC < 100 mV

State Transition Characteristics

Specifies the maximum settling time of the CLK and CLKB outputs from device power up. For V_{DD} and V_{DDX} any sequences are allowed to power up and power down the CY2213.

From	To	Transition Latency	Description
V_{DD}/V_{DDX} On	CLK/CLKB Normal	3 ms	Time from V_{DD}/V_{DDX} is applied and settled to CLK/CLKB outputs settled.

Functional Specifications

Crystal Input

The CY2213 receives its reference from an external crystal. Pin XIN is the reference crystal input, and pin XOUT is the reference crystal feedback. The parameters for the crystal are illustrated in AC Device Characteristics on page 7. The oscillator circuit requires external capacitors. Please refer to the application note entitled **Crystal Oscillator Topics** for details.

Select Input

There is only one select input, pin S. This pin selects the frequency multiplier in the PLL, and is a standard LVCMOS input. The S pin has an internal pull up resistor. The multiplier selection is illustrated in Frequency Table on page 3.

PECL Clock Output Driver

Figure 6 and Figure 7 show the Clock Output Driver.

Figure 6. Output Driving Load (-1)

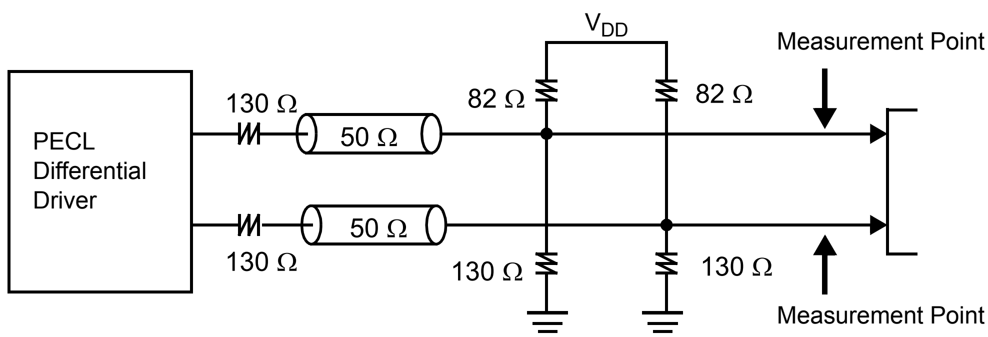
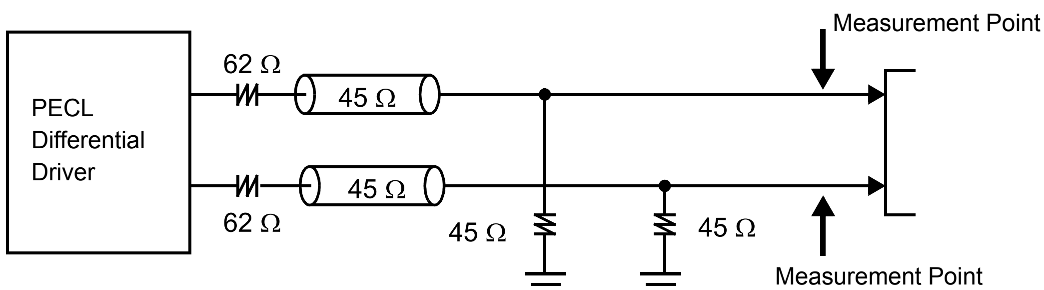
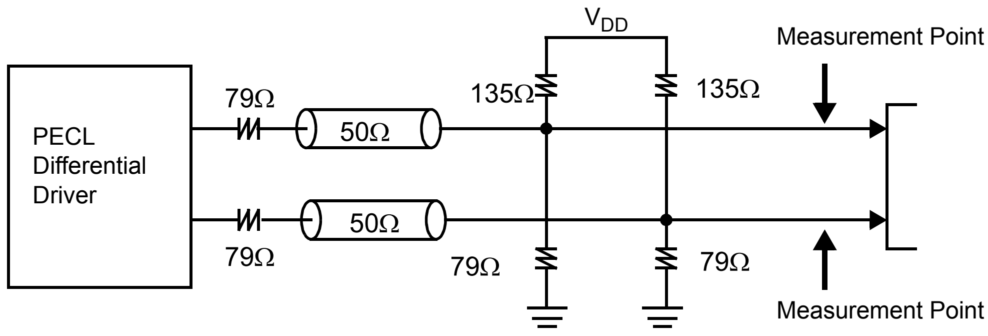


Figure 7. Output Driving Load (-2)



An alternative termination scheme can be used to drive a standard PECL fanout buffer.

Figure 8. Output Driving Load (-3)



The PECL differential driver is designed for low voltage, high frequency operation. It significantly reduces the transient switching noise and power dissipation when compared to conventional CMOS drivers. The nominal value of the channel impedance is 50Ω. The pull up and pull down resistors provide matching channel termination. The combination of the differential driver and the output network determines the voltage swing on the channel. The output clock is specified at the measurement point indicated in Figure 6 on page 8 and Figure 7 on page 8.

Signal Waveforms

A physical signal that appears at the pins of the device is deemed valid or invalid depending on its voltage and timing relations with other signals. This section defines the voltage and timing waveforms for the input and output pins of the CY2213. The Device Characteristics tables list the specifications for the device parameters that are defined here.

Input and Output voltage waveforms are defined as shown in Figure 9. Rise and fall times are defined as the 20% and 80% measurement points of $V_{OHmin} – V_{OLmax}$.

The device parameters are defined in Table 3. Figure 10 on page 10 shows the definition of long term duty cycle, which is simply the CLK waveform high time divided by the cycle time (defined at the crossing point). Long term duty cycle is the average over many (>10,000) cycles. DC is defined as the Output Clock Long Term Duty Cycle.

Table 3. Definition of Device Parameters

Parameter	Definition
V_{OH}, V_{OL}	Clock output high and low voltages
V_{IH}, V_{IL}	V_{DD} LVCMOS input high and low voltages
t_{CR}, t_{CF}	Clock output rise and fall times

Figure 9. Voltage Waveforms

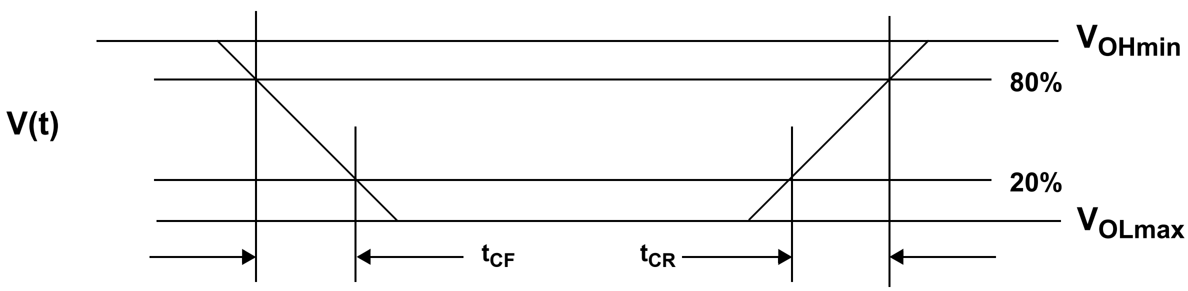
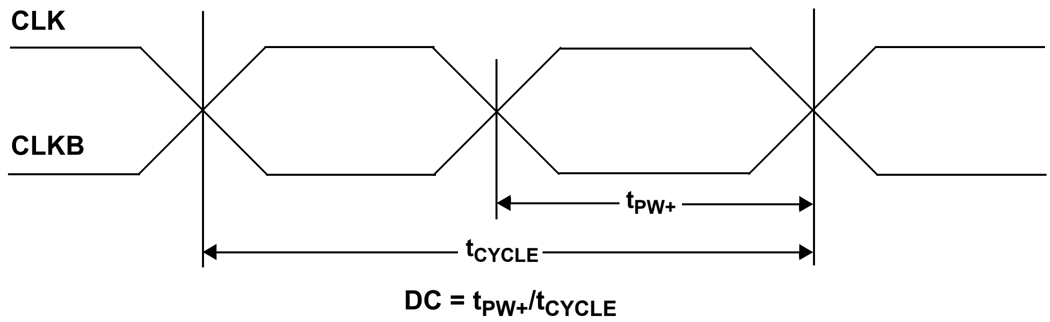


Figure 10. Duty Cycle Jitter



Jitter

This section defines the specifications that relate to timing uncertainty (or jitter) of the input and output waveforms. Figure 11 shows the definition of period jitter with respect to the falling edge of the CLK signal. Period jitter is the difference between the minimum and maximum cycle times over many cycles (typically 12,800 cycles at 400 MHz). Equal requirements apply for rising edges of the CLK signal. t_{JP} is defined as the output period jitter.

Figure 12 shows the definition of cycle-to-cycle jitter with respect to the falling edge of the CLK signal. Cycle-to-cycle jitter is the difference between cycle times of adjacent cycles over many cycles (typically 12,800 cycles at 400 MHz). Equal requirements apply for rising edges of the CLK signal. t_{JC} is defined as the Clock Output Cycle-to-cycle Jitter.

Figure 13 on page 11 shows the definition of cycle-to-cycle duty cycle error. Cycle-to-cycle duty cycle error is defined as the difference between high-times of adjacent cycles over many cycles (typically 12,800 cycles at 400 MHz). Equal requirements apply to the low-times. $t_{DC,ERR}$ is defined as the Clock Output Cycle-to-cycle Duty Cycle Error.

Figure 14 on page 11 shows the definition of long-term jitter error. Long term jitter is defined as the accumulated timing error over many cycles (typically 12,800 cycles at 400 MHz). It applies to both rising and falling edges. t_{JLT} is defined as the long term jitter.

Figure 11. Period Jitter

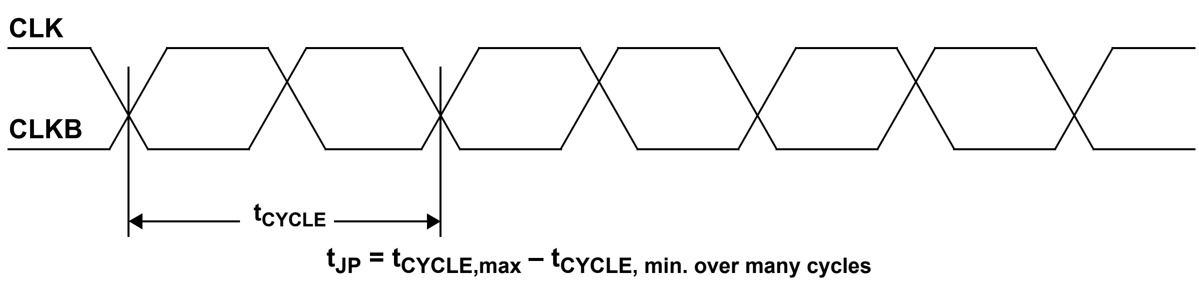


Figure 12. Cycle-to-cycle Jitter

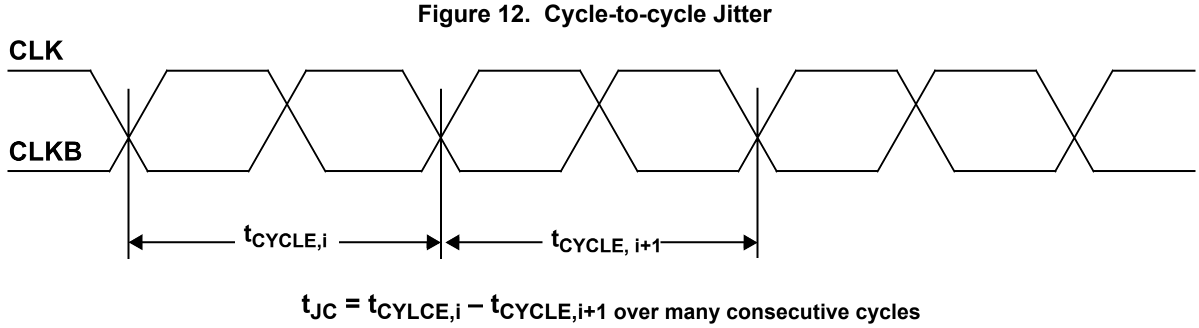


Figure 13. Cycle-to-cycle Duty Cycle Error

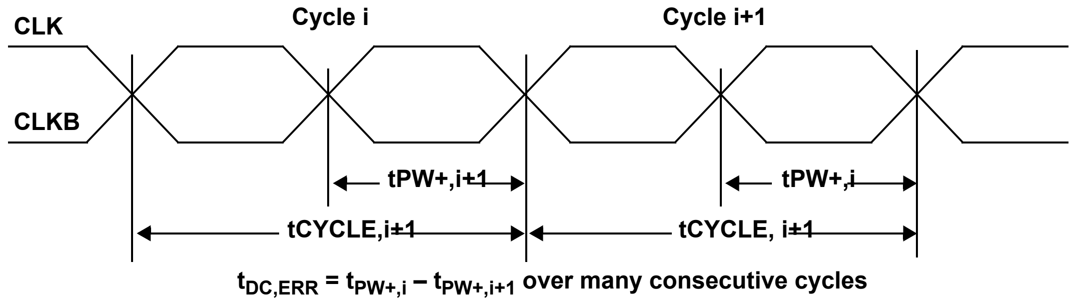
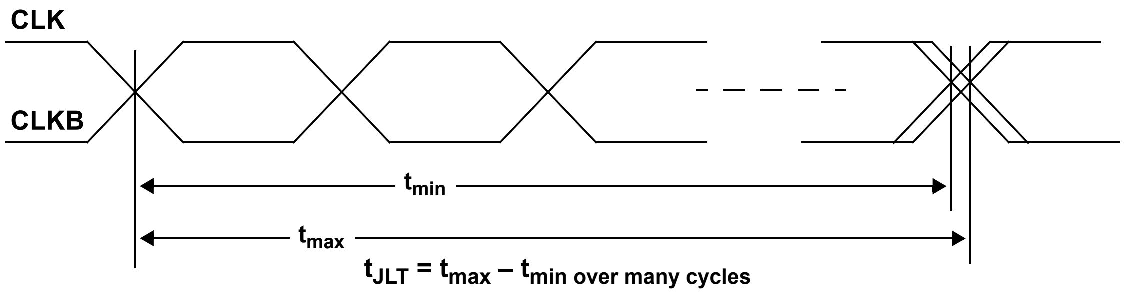


Figure 14. Long-term Jitter



Ordering Information

Ordering Code	Package Type	Operating Range	Operating Voltage
CY2213ZXC-1	16-pin TSSOP	Commercial, to 400 MHz	3.3 V
CY2213ZXC-1T	16-pin TSSOP – Tape and Reel	Commercial, to 400 MHz	3.3 V

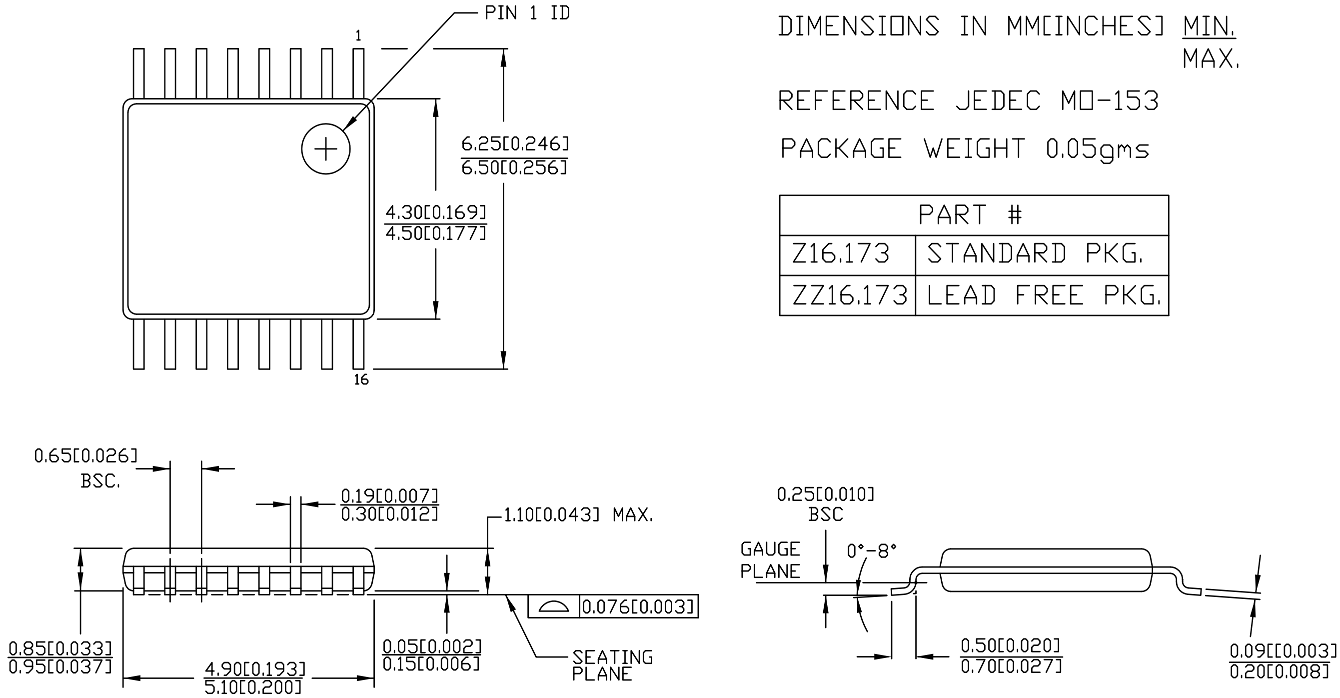
Ordering Code Definitions

CY 2213 Z X C - 1 X

- X = blank or T
  blank = Tube; T = Tape and Reel
- Fixed
- Temperature Range: C = Commercial
- Pb-free
- Package Type:
  Z = 16-pin TSSOP
- Part Identifier
- Company ID: CY = Cypress

Package Diagrams

Figure 15. 16-pin TSSOP (4.40 mm Body) Z16.173/ZZ16.173 Package Outline, 51-85091



51-85091 *E

Acronyms

Acronym	Description
CMOS	complementary metal-oxide semiconductor
DC	duty cycle
EMI	electromagnetic interference
LVCMOS	low voltage complementary metal-oxide semiconductor
LVPECL	low voltage pseudo (positive) emitter coupled logic
OE	output enable
PECL	pseudo (positive) emitter coupled logic
PLL	phase locked loop
TSSOP	thin-shrink small outline package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kΩ	kilohm
MHz	megahertz
ms	millisecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
V	volt

Document History Page

Document Title: CY2213, High Frequency Programmable PECL Clock Generator Document Number: 38-07263				
Rev.	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	113090	02/06/02	DSG	Change from Spec number: 38-01100 to 38-07263
*A	113512	05/24/02	CKN	Added PLL Block Diagram (Figure 5) and PLL frequency equation
*B	121882	12/14/02	RBI	Power up requirements added to Operating Conditions
*C	123215	12/19/02	LJN	Previous revision was released with incorrect *A numbering in footer; *A should have been *B (and was changed accordingly)
*D	124012	03/05/03	CKN	Added -2 to data sheet; edited line 3 of Benefits
*E	126557	05/27/03	RGL	Added 200 MHz Jitter Spec. Added optional output termination
*F	2738056	07/14/09	CXQ	Obsolete document.
*G	2742301	07/22/09	CXQ	Undo obsolete document. Removed all references to obsolete -2 option. Changed Ordering Information entry to Pb-free CY2213ZXC-1 and -1T. Revised the version of Package Drawing from 51-85091 ** to 51-85091 *A.
*H	3709157	08/10/2012	PURU	Added Ordering Code Definitions. Updated Package Diagrams (spec 51-85091 (Changed revision from *A to *D)). Added Acronyms and Units of Measure. Updated in new template.
*I	4575273	11/20/2014	PURU	Added related documentation hyperlink in page 1. Updated Package Diagrams.
*J	4888407	08/18/2015	XHT	Sunset review, no change
*K	5992889	12/13/2017	AESATMP8	Updated logo and Copyright.

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