

12 Channel Constant Current LED Driver IC



BD18377EFV-M

●General Description

The BD18377EFV-M is a serial input controlled constant-current LED driver with 10V output rating. 6 bit current calibration is available for each output while a global PWM performs dimming on all outputs simultaneously. The BD18377EFV-M is able to perform diagnostic (open / short load / temperature) checks to detect LED failure and over temperature on chip. The settings of all internal registers can be read out to verify written information at any time.

●Key Specifications

■ Input voltage range:	3.0V to 5.5V
■ Output voltage range:	0.5V to 10V
■ Output Current range/channel:	15mA to 50mA
■ Output Current accuracy at 30mA:	3.5% (Typ.)
■ Min PWM ON Time:	5μS
■ Maximum circuit current:	5mA
■ Maximum clock frequency:	1250KHz
■ Operating temperature range:	-40°C to +105°C

●Features

- Constant current output of up to 50mA per output channel.
- 4-line Serial Control + Enable Signal.
- PWM dimming 0.1-100% global.
- 6 Bit LED brightness adjustment on each channel.
- Diagnostic output on LED OPEN and SHORT for each channel.
- Over Temperature Protection and thermal Feedback.
- Read-back of all register settings.
- Outputs may be connected in parallel to achieve more than 50mA into the load.
- Slew limited switching reduces conducted and radiated Noise (EMI).
- Daisy chain compatible with BD18377EFV-M and/or BD8377EFV-M (12ch LED driver IC).
- AEC-Q100 qualified.

●Package

HTSSOP-B20

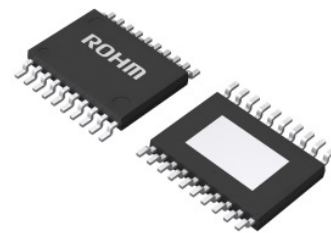
 W(Typ.) x D(Typ.) x H(Max.)
 6.50mm x 6.40mm x 1.00mm


Figure 1. HTSSOP-B20 Package

●Applications

- Automotive illumination
- Consumer electronics illumination

● Typical Application Diagram

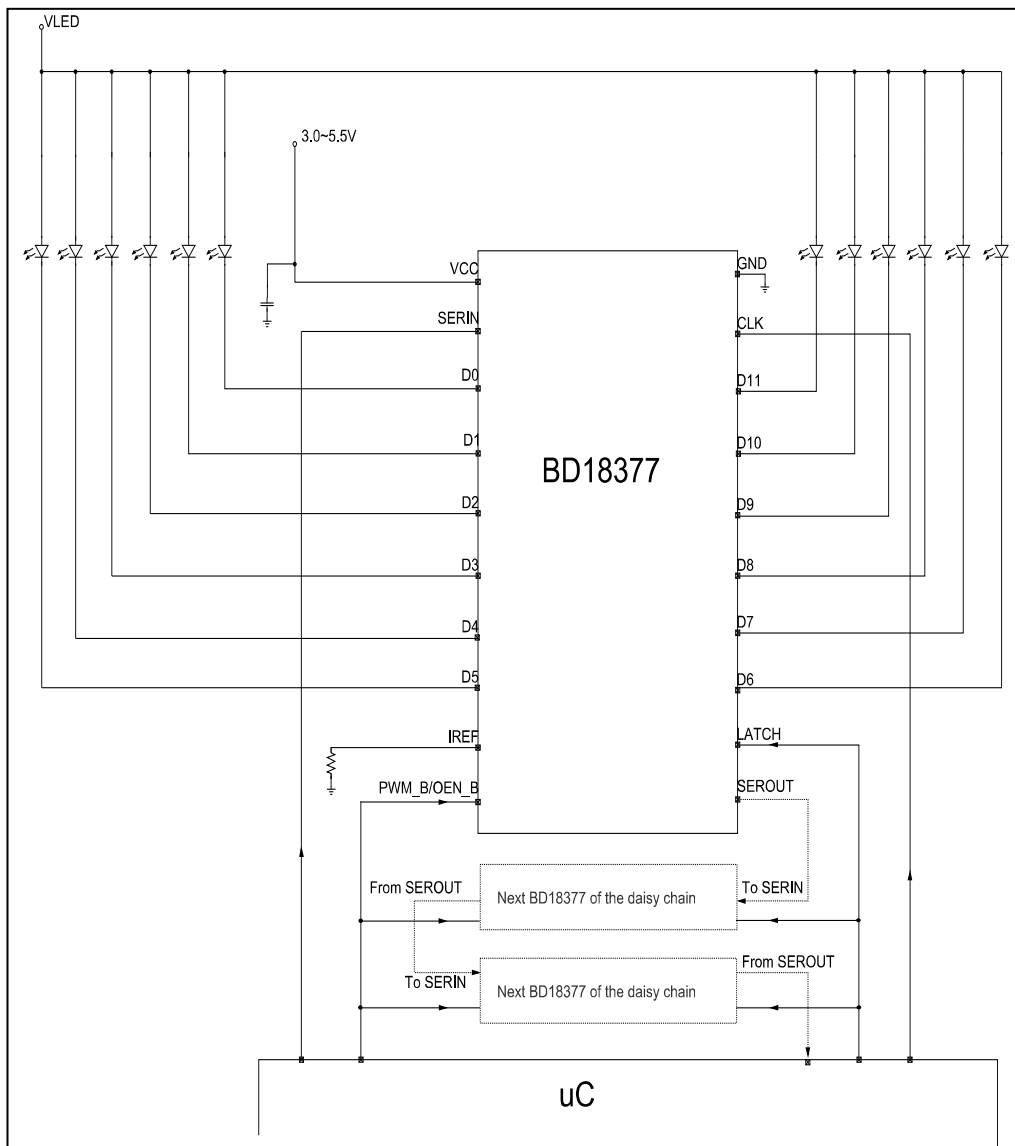


Figure 2. Application diagram for BD18377EFV-M

● Pin Configuration

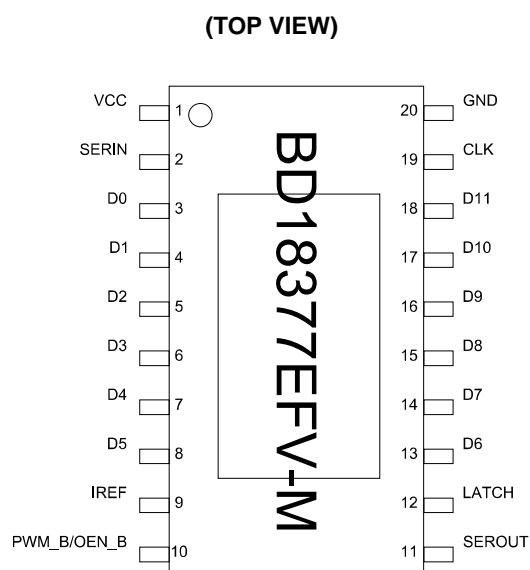


Figure 3. Pin configuration

● Pin Description

Pin Number	Terminal name	Function
1	VCC	Power supply voltage input terminal
2	SERIN	Serial data input terminal
3	D0	Output terminal 0
4	D1	Output terminal 1
5	D2	Output terminal 2
6	D3	Output terminal 3
7	D4	Output terminal 4
8	D5	Output terminal 5
9	IREF	Set nominal output current via external resistor
10	PWM_B/OEN_B	PWM dimming/output enable (active low)
11	SEROUT	Serial data output terminal
12	LATCH	Latch signal input terminal
13	D6	Output terminal 6
14	D7	Output terminal 7
15	D8	Output terminal 8
16	D9	Output terminal 9
17	D10	Output terminal 10
18	D11	Output terminal 11
19	CLK	Serial communication clock
20	GND	GND terminal

●Block Diagram

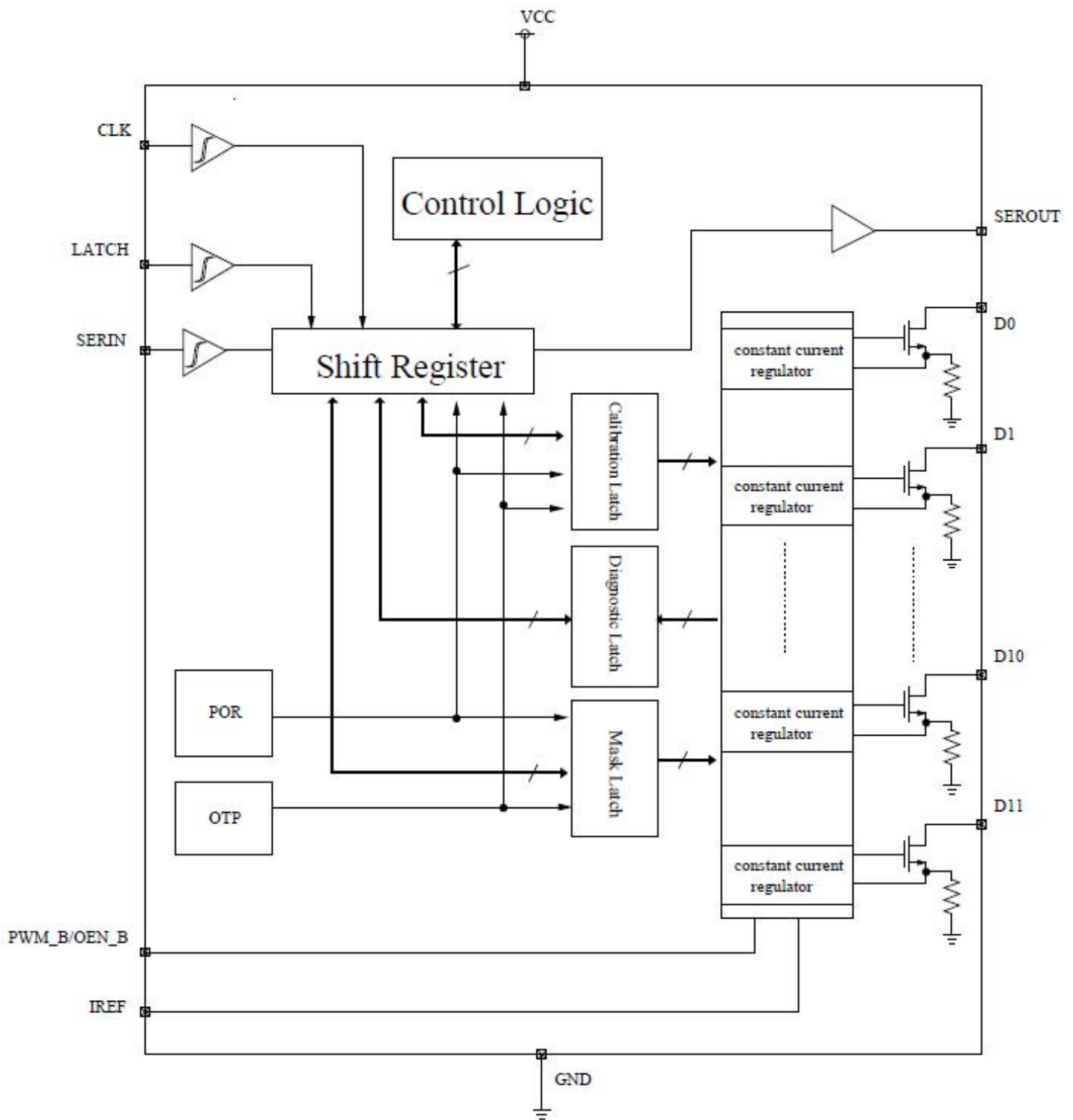


Figure 4. Block Diagram of BD18377EFV-M

● Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7	V
Output Voltage (Pin No: 3~8, 13~18)	V_{Dmax}	10	V
Input Voltage (Pin No: 2, 9, 10, 12, 19)	V_{IN}	-0.3 to V_{CC}	V
Operating Temperature Range	T_{OPR}	-40 to +105	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C
Junction Temperature	T_{Jmax}	150	°C
Drive Current	I_{Dmax}	60	mA
Electrostatic-Discharge Capability Human Body Model	ESDHBM	2000	V
Electrostatic-Discharge Capability Machine Model	ESDMM	200	V

● Recommended Operating Ratings ($T_a = 25^{\circ}\text{C}$)

Item	Symbol	Standard Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	3.0	-	5.5	V
Drive Current at 100% brightness	I_D	15	30	50	mA

●Electrical Characteristic(s)

(Unless otherwise specified, Ta=-40~105°C V_{CC}=3.0~5.5V)

Item	Symbol	Standard Value			Unit	Conditions
		Min	Typ	Max		
[Output D0~D11] (Pin No: 3~8, 13~18)						
Output current accuracy ¹	RDIO (Relative)	-	-	9.8 4.7 7	%	Ta = 25°C V _{CC} = 3.3V Calibration = 63 I _D = 15 mA I _D = 30 mA I _D = 50 mA
Output current accuracy absolute, Device to Device ²	AD2DIO (Absolute)	-4.2 -1.7 -2.5	-	4.0 1.6 2.1	%	Ta = 25°C V _{CC} = 3.3V Calibration = 63 I _D = 15 mA I _D = 30 mA I _D = 50 mA
Output current accuracy relative, Channel to Channel ²	RC2CDIO (Relative)	-8.8 -2.3 -4.0	-	8.9 2.5 4.3	%	Ta = 25°C V _{CC} = 3.3V Calibration = 63 I _D = 15 mA I _D = 30 mA I _D = 50 mA
Output current temperature shift	DTIO	-	-	1.5	%	V _{CC} =3.0V I _D = 30 mA Calibration = 63
Output current supply voltage shift	DVIO	-	-	1.76	%	Ta = 25°C I _D = 30 mA Calibration = 63 V _{CC} = 3.0V-3.6V/4.5V-5.5V
Output leakage Current	I _{DLeak}	-	-	0.1	uA	V _D =10V Ta=25°C
Minimum output voltage level	V _{Dmin}	-	0.44 0.40	0.65 0.51	V	V _{CC} =3.3V V _{CC} =5V
Dynamic settling time of I _D	ST	0.3	0.5	2	us	From 10% to 90% of I _D max.
Ton error ³	RT	-1	-	0	us	
Delay time PWM_B to I _D	DT1	-	0.26	-	us	From PWM_B=10%V _{CC} to I _D =10%I _{Dmax}
[Logic input] (Pin No: 2, 10, 12, 19)						
High going threshold voltage	V _{TH}	V _{CC} x 0.35	-	V _{CC} x 0.45	V	
Low going threshold voltage	V _{TL}	V _{CC} x 0.25	-	V _{CC} x 0.35	V	
Hysteresis width	V _{HYS}	-	0.1 x V _{CC}	-	V	
Serial clock frequency	f _{CLK}	-	-	1250	kHz	
PWM ON Time ^{4,5}	t _{ON}	5	-	-	us	Minimum requirement for OPEN/SHORT detection.
Input leakage current	I _{INLeak}	-	-	1	uA	For pins 2,10,12,19
[Logic output] (Pin No: 11)						
Output Voltage high	VOH	0.9 x V _{CC}	0.95 x V _{CC}	1 x V _{CC}	V	I _{SEROUT} =-4mA
Output voltage Low	VOL	0	0.05 x V _{CC}	0.1 x V _{CC}	V	I _{SEROUT} =4mA

¹ This is duplicate information with respect to AD2DIO and RC2CDIO.

² This parameter is guaranteed by design.

³ Δt between t_{RISE} and t_{FALL} of I_D relative to the pulse width of PWM.

⁴ Please note that the PWM signal is active LOW therefore, the t_{ON} time denotes the period when the signal is at LOW level.

⁵ This period is derived from a PWM frequency of 200Hz and a minimum duty cycle of 0.1%.

Item	Symbol	Standard Value			Unit	Conditions
		Min	Typ	Max		
[DEVICE]						
Circuit Current	I_{CC}	-	-	5.0	mA	Serial Data Input, $f_{CLK}=1.25\text{MHz}$, SEROUT=OPEN,
Under voltage lock out	UVLO	2.4	-	2.7	V	
Minimum glitch Reject ^{2,6}	t_{glitch_reject}	-	3	-	us	For OPEN / SHORT detection.
SHORT detection threshold	V_{SCth}	3.9	-	4.3	V	PWM_B="LOW" AND channel is enabled
SHORT detection bypass current	I_{SC}	5	6.3	10	uA	Channel is enabled, $V_D \leq 4.3\text{V}$.
OPEN detection threshold	V_{OCth}	110	-	390	mV	PWM_B="LOW", channel is enabled
Reference Voltage	V_{REF}	1.1	1.2	1.23	V	R_{EXT} connected to I_{REF} pin.
Temperature monitoring accuracy	T_{MON}	-	± 10	-	%	At 125°C and 150°C
Temperature hysteresis ²	T_{hyst}	-	10	-	°C	At 125°C and 150°C

⁶ An OPEN or SHORT that lasts for less than this time will be rejected.

● Typical Performance Curves

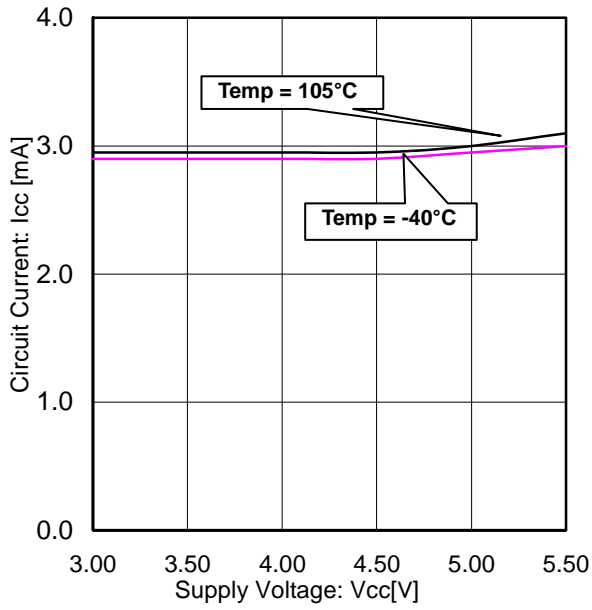


Figure 5. I_{CC} vs. V_{CC} over Temp

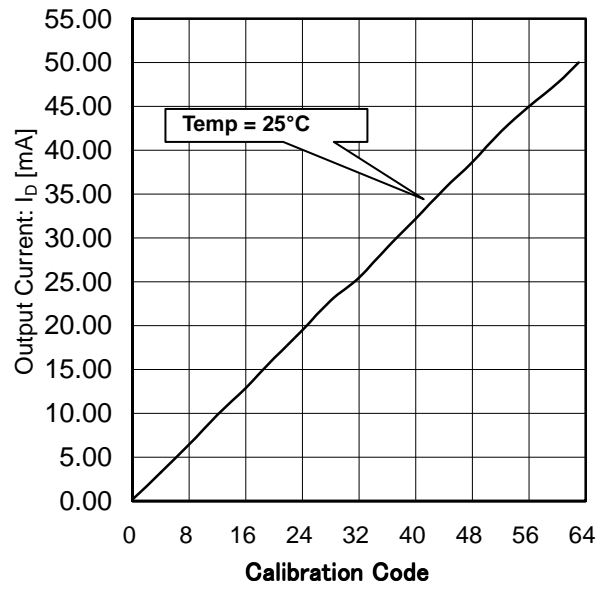


Figure 6. I_b vs. Cal over at V_{CC} = 5.0V

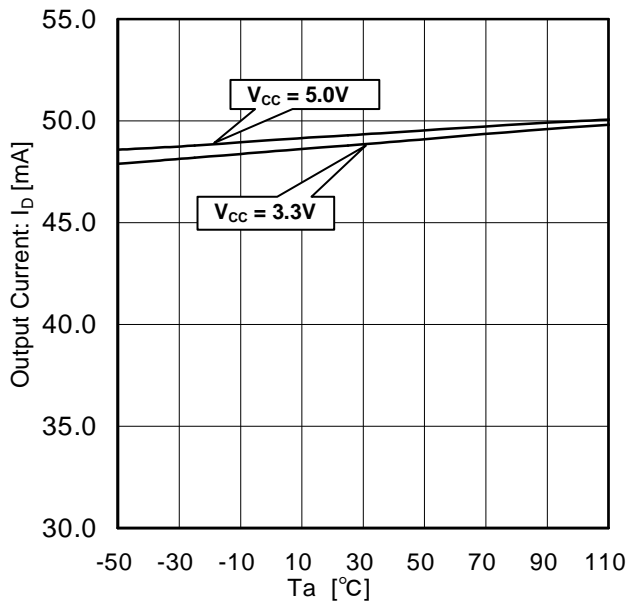


Figure 7. I_b Vs Temp over V_{CC}

● Functional Description

Constant current driver block

The BD18377EFV-M uses a constant current output driver with a provision for dot calibration per channel. The constant current I_D is derived from referring an internal reference voltage over the external resistor R_{EXT} , see Equation 1. Reference current. The external resistor is chosen to set a reference current I_{REF} , in the range of 30~100uA. In operating conditions the resistor value is in the range of 12k-40kΩ. The maximum output current I_{Dmax} is 500 x I_{REF} , see Equation 2. The external resistor value, the 6 bit current calibration (CAL) and output current relate as follows: see Equation 3.

$$I_{REF} = \frac{V_{REF}}{R_{EXT}}$$

Equation 1. Reference current

$$I_{Dmax} = I_{REF} \cdot 500$$

Equation 2. Maximum output current

$$I_D = \frac{I_{Dmax} \cdot (CAL + 1)}{64}$$

Equation 3. Output current as function of CAL value

$$I_{LED} = I_D + I_{SC}, \text{ where } I_{SC} \leq \frac{V_D}{430k\Omega}$$

Equation 4. Total LED current.

Finally the total LED current, including the offset current due to the SHORT detection is shown in Equation 4. Note that the short detection current flows at all times when the channel is enabled.

For example in case of a maximum output current of 20mA R_{EXT} shall be 30kΩ.

See **Figure 8** the global reference current, I_{REF} , is mirrored into the channel current to generate a local reference voltage. The error amplifier A1 forces the voltage across the LED current sense resistor to match the local reference voltage. The output device is scaled to give 6 bit output range. Thus a factor I_{Dmax}/I_D can be achieved in the range from 0 to 63 in 64 steps. The output devices driving analog current amplitude are timed by the global PWM.

The active drivers have a low leakage current to keep the LED in firm OFF condition when the channel is not active. To ensure low leakage current ($I_{DL,leak}$), the gate voltage of the output transistors will be pulled low during MASK = LOW or PWM_B = HIGH or when the device is not required by the CAL setting.

When there is an open load, half open load or a weak battery supply, the channel will be unable to sink enough current. In this case the output of error amplifier A1 will latch to maximum voltage pulling the output voltage V_D below V_{OCth} . This is detected by comparator A2 as an OPEN event. There is a glitch reject filter that will reject any OPEN that is $< t_{glitch_reject}$.

The voltage V_D at pin D_N (**Figure 8**) is divided by a high ohmic voltage divider and compared to a reference voltage in order to detect the short circuit. When comparator A3 detects a voltage at pin $D_n > V_{SCth}$ this indicates a LED SHORT circuit condition. SHORT detection requires a minimum PWM ON time $> t_{ON}$. This is because the glitch reject filter will reject any SHORT that is $< t_{glitch_reject}$. The same circuit is used for both OPEN and SHORT rejection and therefore the period is the same.

Both the OPEN and SHORT detection circuits are disconnected during PWM_B = "HIGH" or MASK = LOW, but the SHORT detection bypass current will flow when MASK = HIGH.

The status of OPEN, SHORT for each channel can be read out from the OPEN / SHORT registers using the command [READ OPEN] and [READ SHORT].

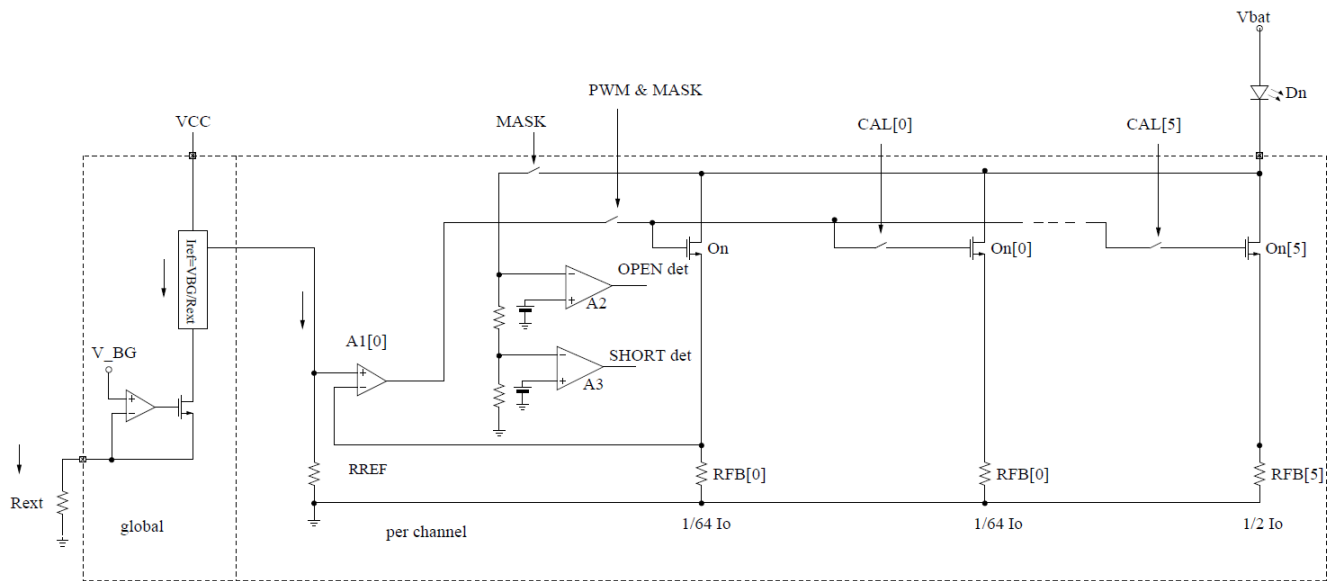


Figure 8. Block diagram of global V_{REF} and per-channel regulation loop

Protection Circuitry

Types of POR

In the BD18377 a POR event can occur for one of three reasons:

- Low supply voltage which will occur due to either startup or UVLO.
- When the die temperature exceeds 150°C
- When the controller sends a command

These three situations are discussed below.

POR at Startup or UVLO

At startup, which is defined here as first application of supply voltage V_{CC} , or when $V_{CC} < UVLO$ (UVLO refers to Under Voltage Lock Out), a POR event (Power ON Reset) will occur. The expected behavior is shown in **Table 1**.

In this case the analog circuits are UNDEFINED and therefore the reported status of the diagnostics registers (TSD150, TSD125, SHORT_FLAG, OPEN_FLAG, SHORT and OPEN) is UNDEFINED. It is **mandatory** to use the command [SOFTWARE RESET].

During RESET:

- The device cannot receive data
- The SEROUT is held active LOW, so the device cannot transmit data

Therefore communication between the controller and the device is lost during a POR. Any data transmitted during this period will be lost. Since SEROUT is held low, the controller must send, and receive, any command that is NOT 0000 to confirm communication is active.

The state machine inside the digital is undefined and the device will recognize the first two bits it receives as "00". It is therefore recommended to send a dummy byte or a dummy command at startup to put the device into a known state before beginning of programming.

When the POR is released, the MASK, CAL, MASK LOCK, CAL LOCK and SHORT_MASK registers will have their default values as shown in **Table 1**. These values will put the device into a safe state.

The POR flag in the STATUS register is set HIGH, so the event is visible to the controller on the next [READ STATUS] command. The POR flag can be reset by the command [RESET_POR].

Table 1. Default registers values

Register		STARTUP / UVLO	TSD150	SOFTWARE	
CALIBRATION<5:0>		<000000>	<000000>	<000000>	
MASK<11:0>		<000000000000>	<000000000000>	<000000000000>	
STATUS Register	0	TSD125	UNDEFINED.	<1>	depends upon Die temp
	1	TSD150	UNDEFINED.	<1>	depends upon Die temp
	2	CALIBRATION LOCK	<0>	<0>	<0>
	3	MASK LOCK	<0>	<0>	<0>
	4	ANY-SHORT-FLAG	UNDEFINED.		
	5	ANY-OPEN-FLAG	UNDEFINED.		
	6	POR-FLAG	<1>	<1>	<1>
SHORT MASK<11:0>		<111111111111>	<111111111111>	<111111111111>	
SHORT<11:0>		UNDEFINED.			
OPEN<11:0>		UNDEFINED.			
COMMUNICATION INTERRUPT?		YES	YES	NO	
DIAGNOSTIC RESET?		MANDATORY	RECOMMENDED	AUTOMATIC	
RELEASE CONDITION		$V_{CC} > UVLO$ threshold	Die Temp < 150°C	end of command	

When the controller detects an unexpected POR flag it is recommended to start a defined start up sequence. Check for OTP anywhere else. Degrees Celsius

POR (due to TSD)

A POR event (Power ON Reset) can occur due to die temperature over 150°C (TSD150). This is referred to as TSD150 (Thermal Shut Down at 150°C). The conditions are as shown in **Table 1**. If the die temperature is > 150°C, the TSD150 and POR flag will be set HIGH.

The channel diagnostics (OPEN and SHORT) will be UNDEFINED.

The TSD125, TSD150 and POR flags are held unchanged until cleared explicitly by command [RESET STATUS]. This is to ensure that a POR due to temperature is always visible to the controller. The circuit will then report the current die temperature.

After a POR due to TSD150, the delay until POR release will depend upon the time required for the die temperature to drop below 150°C.

The device monitors its own die temperature and stores it internally (see **Table 2**). When the die temperature exceeds 125°C the TSD125 bit will set high. This bit can be read by the controller. In this case the controller can take steps to reduce power dissipation such as to reduce PWM duty, reduce CAL settings or MASK channels to prevent thermal shutdown. At temperatures between 125°C and 150°C there is no limitation or change to the functionality of BD18377EFV-M.

Table 2. Coding of temperature monitoring

Name	TDS150	TSD125	Comment
Bit	STATUS<1>	STATUS<0>	
	0	0	Die temperature < 125°C
	0	1	125°C < die temperature < 150°C
	1	0	reserved
	1	1	OTP active, die temperature > 150°C

The accuracy of temperature monitoring is T_{MON} , while the variation at 125°C threshold is correlated to the one at 150°C. The hysteresis is T_{hyst} .

De-activation of shutdown at TSD150

The following commands disable the shutdown at TSD150:

Hex	Bit		
[F832]		1111 1000 0011 0010	[UNLOCK]
[FD04]		1111 1101 0000 0100	[TSD SHUTDOWN]

In this setting the TSD150 flag can be set but no shutdown will occur.

- This setting is reset by POR, and must be set again AFTER any POR event.
- It is recommended that when detecting TSD125 the controller should immediately take steps to reduce power dissipation to avoid damage.
- **When TSD150 is detected it is mandatory to take action to reduce power dissipation to avoid damage because the device may continue to heat up and has no self-protection.**
- The first command [F832] unlocks the register for ONE command only. This command must be followed by the correct TSD_SHUTDOWN command [FC04].

This setting can be used to maintain communication continuity during a TSD150 in a daisy chain application.

POR (due to command [SOFTWARE RESET])

The controller can send a command [SOFTWARE RESET]. The command is executed on the latch edge. The command [SOFTWARE RESET] also executes the command [STATUS RESET]. Communication between the controller and the device is not lost due to a POR command. The POR flag in the STATUS register is set HIGH.

The channel diagnostics (OPEN and SHORT) will be UNDEFINED.

LED Short Detection

A SHORT is detected when voltage V_D at the output pin rises above V_{SCth} for a period greater than t_{glitch_reject} . This time is short enough to allow SHORT detection at minimum t_{ON} . This voltage is based upon the assumption of a LED forward voltage drop below V_{LED} ($5V \pm 4\%$). If a higher V_{LED} or more than one LED per channel is used this SHORT detection threshold is inappropriate and can be either ignored by the controller or can be MASK'ed for ANY-SHORT detection. This functionality is therefore application dependent. The SHORT flag for the channel will be always set when V_D at the output pin rises above V_{SCth} . It is only ANY-SHORT flag for which the shorts can be masked. The SHORT detection bypass current, I_{SC} , is flowing whenever the channel is enabled (independent of PWM), and will cause a maximum output current offset of about 10 A, and is given by Equation 5. Current offset when short detection active:

$$I_{SC} \leq \frac{V_D}{R_{SHORT\ det}}, \text{ when } R_{SHORT\ det} \geq 430k\Omega$$

Equation 5. Current offset when short detection active

After a detected LED SHORT the corresponding bit of the SHORT detection register and the ANY_SHORT bit (unless MASKed) will remain high until it is cleared by the controller.

LED Open Detection

When the channel cannot achieve the programmed output current I_o value, the error amplifier output voltage will rise to maximum forcing the output device fully ON, pulling V_D low. This indicates an open load, a half open load or a weak battery supply. An OPEN is detected when voltage V_D at the output pin falls below V_{OCth} for a period greater than t_{glitch_reject} . This time is short enough to allow OPEN detection at minimum t_{ON} .

In this architecture it is not possible to distinguish between a true open circuit and the situation when there is not enough headroom on V_{LED} to drive the required LED forward voltage. Therefore on a low V_{LED} , LEDs with sufficient forward voltage will always be reported as "OPEN".

After a LED open has been detected the corresponding bit of the OPEN detection register and ANY_OPEN flag remain high until it is cleared by the controller.

Dimming

Figure 9. Illustration of Calibration and dimming of Output Current describes the relation between calibration and dimming. The maximum current, I_{Dmax} , is set by the reference resistor, R_{EXT} . Setting the calibration bits will change the value of the switched current in the corresponding channel whilst controlling the PWM_B/OEN_B input will modulate the current in all active channels in the time domain.

PWM is fully independent of the clock signal.

In the example below, D0 and D1 have been calibrated below the maximum current set by R_{EXT} while D1 has been set to less output current than D0. At the same time, brightness of both channels is set by the global PWM_B/OEN_B pin. The independence between the value of the switched current and the switching duty cycle ensures that calibration changes will not influence the dimming curve or cause any harmonic distortion. Output to input linearity is ensured by equal rising and falling propagation delays.

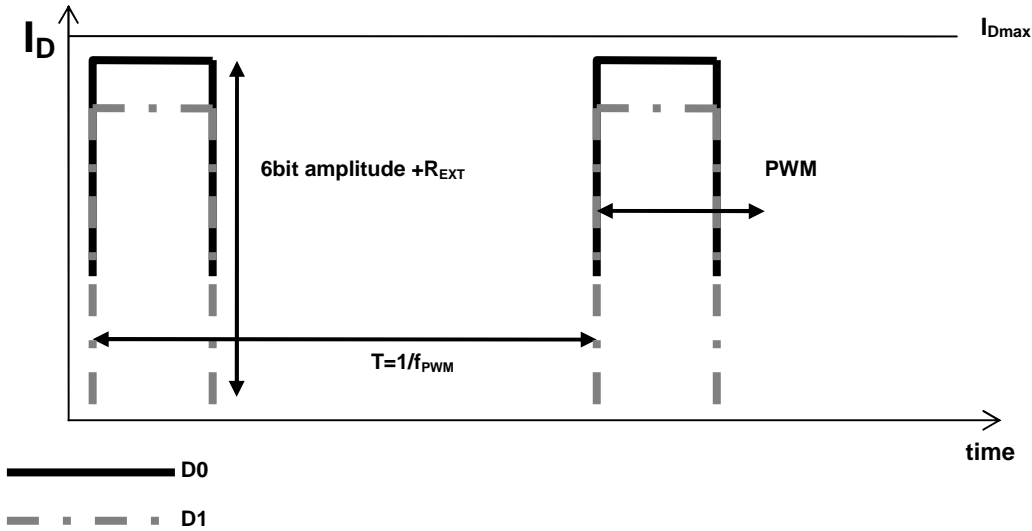


Figure 9. Illustration of Calibration and dimming of Output Current

Serial Communication

The serial port is used to write data to, read diagnostic status from and configure settings of the IC by transferring the input data to the desired address. During normal operation a 4-bit serial address and 12-bit serial data is written into the 16-bit shift register. The shift register advances on CLK rising edges, converting the 16 most recent inputs to parallel signals on the LATCH rising edge. In order to provide extended functionality there are two addresses where 4 bits of the serial data are interpreted as sub addresses. These sub addresses access functions instead of registers.

At a rising edge on the LATCH input addresses and sub-addresses are interpreted by a decoder which controls data transfer between shift- and storage registers. Depending on the address valid data is conveyed from or to the appropriate latch or a command is interpreted.

When a read address is latched data is read out from a storage register and shifted out of SEROUT to the microcontroller or daisy chained BD18377EFV-M. Since for each address the BD18377EFV-M shifts out a fixed amount of data at the end of a write/read cycle it is possible to send different address codes to each IC in a daisy chain.

The content of calibration, mask, short mask and diagnostic data can be read on SEROUT pin.

During the exchange of information the LED outputs do not flicker or dim.

Register Map

Table 3. Address Codes and Description

Address <15:12>	Sub Address <11:8>	Data		Name
		<7:4>	<3:0>	
0	CAL1<5:0>		CAL0<5:0>	WRITE CAL1/CAL0
1	CAL3<5:0>		CAL2<5:0>	WRITE CAL3/CAL2
2	CAL5<5:0>		CAL4<5:0>	WRITE CAL5/CAL4
3	CAL7<5:0>		CAL6<5:0>	WRITE CAL7/CAL6
4	CAL9<5:0>		CAL8<5:0>	WRITE CAL9/CAL8
5	CAL11<5:0>		CAL10<5:0>	WRITE CAL11/CAL10
6	MASK<11:8>	MASK<7:4>	MASK<3:0>	WRITE MASK
7	0	X	X	LOCK CAL
7	1	X	X	UNLOCK CAL
7	2	X	X	LOCK MASK
7	3	X	X	UNLOCK MASK
7	4	X	X	RESET POR
7	5	X	X	RESET STATUS
7	6	S_MASK<7:4>	S_MASK<3:0>	WRITE SHORT_MASK 7:0
7	7	X	S_MASK<11:8>	WRITE SHORT_MASK 11:8
7	8	X	X	SOFTWARE POR
7	9	X	X	RESERVED
7	A	X	X	Unused
7	B	X	X	Unused
7	C	X	X	Unused
7	D	X	X	Unused
7	E	X	X	Unused
7	F	X	X	Unused
8	X	X	X	READ CAL0/CAL1
9	X	X	X	READ CAL2/CAL3
A	X	X	X	READ CAL4/CAL5
B	X	X	X	READ CAL6/CAL7
C	X	X	X	READ CAL8/CAL9
D	X	X	X	READ CAL10/CAL11
E	X	X	X	READ MASK
F	0	X	X	READ STATUS Flags
F	1	X	X	Unused
F	2	X	X	READ SHORT 7:0
F	3	X	X	READ SHORT 11:8
F	4	X	X	READ OPEN 7:0
F	5	X	X	READ OPEN 11:8
F	6	X	X	READ SHORT_MASK 7:0
F	7	X	X	READ SHORT_MASK 11:8
F	8	X	X	RESERVED
F	9	X	X	Unused
F	A	X	X	Unused
F	B	X	X	Unused
F	C	X	X	Unused
F	D	X	X	Unused
F	E	X	X	Unused
F	F	X	X	Unused

Table 4. Communication address overview

Addr	INPUT												OUTPUT												
	Sub-address/ Data				Data								Addr	Sub-address/ Data				Data							
HEX	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0		HEX	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1
0	x	x	x	x	x	x	x	x	x	x	x	x	u	u	u	u	u	u	u	u	u	u	u	u	
1	x	x	x	x	x	x	x	x	x	x	x	x	u	u	u	u	u	u	u	u	u	u	u	u	
2	x	x	x	x	x	x	x	x	x	x	x	x	u	u	u	u	u	u	u	u	u	u	u	u	
3	x	x	x	x	x	x	x	x	x	x	x	x	u	u	u	u	u	u	u	u	u	u	u	u	
4	x	x	x	x	x	x	x	x	x	x	x	x	u	u	u	u	u	u	u	u	u	u	u	u	
5	x	x	x	x	x	x	x	x	x	x	x	x	u	u	u	u	u	u	u	u	u	u	u	u	
6	x	x	x	x	x	x	x	x	x	x	x	x	u	u	u	u	u	u	u	u	u	u	u	u	
7	0	0	0	0	dc	dc	dc	dc	dc	dc	dc	dc	u	u	u	u	u	u	u	u	u	u	u	u	
7	0	0	0	1	dc	dc	dc	dc	dc	dc	dc	dc	u	u	u	u	u	u	u	u	u	u	u	u	
7	0	0	1	0	dc	dc	dc	dc	dc	dc	dc	dc	u	u	u	u	u	u	u	u	u	u	u	u	
7	0	0	1	1	dc	dc	dc	dc	dc	dc	dc	dc	u	u	u	u	u	u	u	u	u	u	u	u	
7	0	1	0	0	dc	dc	dc	dc	dc	dc	dc	dc	u	u	u	u	u	u	u	u	u	u	u	u	
7	0	1	0	1	dc	dc	dc	dc	dc	dc	dc	dc	u	u	u	u	u	u	u	u	u	u	u	u	
7	0	1	1	0	x	x	x	x	x	x	x	x	u	u	u	u	u	u	u	u	u	u	u	u	
7	0	1	1	1	dc	dc	dc	dc	x	x	x	x	u	u	u	u	u	u	u	u	u	u	u	u	
7	1	0	0	0	dc	dc	dc	dc	dc	dc	dc	dc	u	u	u	u	u	u	u	u	u	u	u	u	
7	1	0	0	1	Reserved																				
7	1	0	1	0	Unused																				
7	1	0	1	1	Unused																				
7	1	1	0	0	Unused																				
7	1	1	0	1	Unused																				
7	1	1	1	0	Unused																				
7	1	1	1	1	Unused																				
8	dc	dc	dc	dc	dc	dc	dc	dc	dc	dc	dc	dc	u	x	x	x	x	x	x	x	x	x	x	x	
9	dc	dc	dc	dc	dc	dc	dc	dc	dc	dc	dc	dc	u	x	x	x	x	x	x	x	x	x	x	x	
A	dc	dc	dc	dc	dc	dc	dc	dc	dc	dc	dc	dc	u	x	x	x	x	x	x	x	x	x	x	x	
B	dc	dc	dc	dc	dc	dc	dc	dc	dc	dc	dc	dc	u	x	x	x	x	x	x	x	x	x	x	x	
C	dc	dc	dc	dc	dc	dc	dc	dc	dc	dc	dc	dc	u	x	x	x	x	x	x	x	x	x	x	x	
D	dc	dc	dc	dc	dc	dc	dc	dc	dc	dc	dc	dc	u	x	x	x	x	x	x	x	x	x	x	x	
E	dc	dc	dc	dc	dc	dc	dc	dc	dc	dc	dc	dc	u	x	x	x	x	x	x	x	x	x	x	x	
F	0	0	0	0	dc	dc	dc	dc	dc	dc	dc	dc	u	u	u	u	u	x	x	x	x	x	x	x	
F	0	0	0	1	Unused																				
F	0	0	1	0	dc	dc	dc	dc	dc	dc	dc	dc	u	u	u	u	u	x	x	x	x	x	x	x	
F	0	0	1	1	dc	dc	dc	dc	dc	dc	dc	dc	u	u	u	u	u	u	x	x	x	x	x	x	
F	0	1	0	0	dc	dc	dc	dc	dc	dc	dc	dc	u	u	u	u	u	x	x	x	x	x	x	x	
F	0	1	0	1	dc	dc	dc	dc	dc	dc	dc	dc	u	u	u	u	u	u	x	x	x	x	x	x	
F	0	1	1	0	dc	dc	dc	dc	dc	dc	dc	dc	u	u	u	u	u	x	x	x	x	x	x	x	
F	0	1	1	1	dc	dc	dc	dc	dc	dc	dc	dc	u	u	u	u	u	u	u	x	x	x	x	x	
F	1	0	0	0	Reserved																				
F	1	0	0	1	Unused																				
F	1	0	1	0	Unused																				
F	1	0	1	1	Unused																				
F	1	1	0	0	Unused																				
F	1	1	0	1	Unused																				
F	1	1	1	0	Unused																				
F	1	1	1	1	Unused																				

Legend of Table 3 and Table 4

X: Any kind of data.

dc: don't care.

U: unchanged; address and data which is shifted in and out is the same.

Reserved: these commands are potentially used for manufacturing purposes and should not be accessed.

Unused: these commands are not used and could be used for dummy commands.

Table 3 gives an overview about valid address codes. An overflow output is available on SEROUT allowing for daisy chaining more devices.

Description of Commands

Command [WRITE_CALxy] is used to set the calibration of each output during operation. The first 6 bits of the shift register are used for calibration of channels with even numbering whilst the last 6 calibrate the odd channels. For example [WRITE CAL5/CAL4] sets the calibration for channel 4 and 5. Command [READ CALxy] is used to read back the data to ensure it was received correctly.

The mask register which enables/disables the outputs is accessed through command [WRITE MASK]. Command [READ MASK] is used to read back the data to ensure it was received correctly.

The write access to calibration and mask register may be locked using command [LOCK CAL] and [LOCK MASK]. When any data is written during lock there will be no change in the content of the register. This is protecting these most important registers from invalid data during for example unexpected rising edges on the LATCH pin. The lock registers enable denial of access to the mask and calibration registers. The access to calibration and mask register may be unlocked using commands [UNLOCK CAL] and [UNLOCK MASK].

The detection of shorts in the ANY_SHORT register from a given channel may be masked by the command [WRITE SHORT_MASK]⁷. When it is known that the chosen application circuit implementation may lead to inadvertently incorrect SHORT detections in a channel, the SHORT MASK prevents that channel from changing the ANY_SHORT register. However the SHORT detection of individual channels is still active and still can be read by the controller. There is no similar functionality for OPEN detection. The status of SHORT_MASK may be read by the command [READ SHORT_MASK]⁷.

The diagnostic data is accessed via the command [READ STATUS]. See structure of this register is shown in **Table 5. Content of STATUS data**. The POR register flag may be reset by the controller via command [RESET POR].

Table 5. Content of STATUS data

NAME	STATUS	DATA
TSD125	0	Die temperature >125°C (1 = over temp)
TSD150	1	Die temperature >150°C (1 = over temp)
CAL_LOCK	2	CALIBRATION LOCK (1 = locked)
MASK_LOCK	3	MASK LOCK (1 = locked)
ANY_SHORT_FLAG	4	At least one short detected at any output (1 = short detected)
ANY_OPEN_FLAG	5	At least one open detected at any output (1 = open detected)
POR	6	POR flag (1 = POR detected)
x	7	Unused

All of the other bits in the STATUS registers (TSD150, TSD125, CAL_LOCK, MASK_LOCK, ANY_SHORT_FLAG, and ANY_OPEN_FLAG) and channel diagnostic registers (OPEN and SHORT) are reset by command [RESET STATUS].

The detection of shorts in any channel may be read by the command [READ SHORT]⁷. This command reads the status of the SHORT registers. If a SHORT is detected in a channel, the SHORT register flag is maintained until [RESET STATUS]. The next [READ SHORT] will report the actual status of the channel.

The detection of open in any channel may be read by the command [READ OPEN]⁷. If an OPEN is detected in a channel, the OPEN register flag is maintained until [RESET STATUS]. The next [READ OPEN] will report the actual status of the channel.

The controller can initiate a software POR using command [SOFTWARE POR]. This returns the registers to default status without interrupting communication. This also implements a [RESET STATUS] command.

⁷ These commands are spilt into two parts to access all 12 bits.

Timing Diagrams

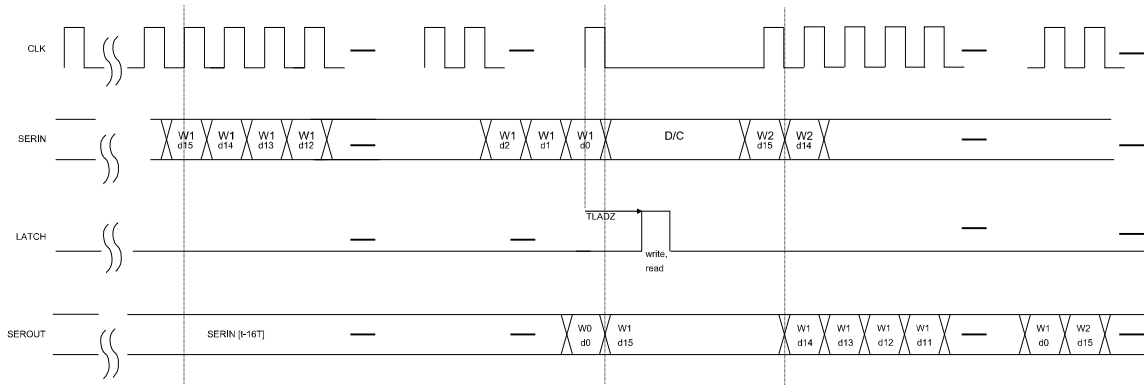
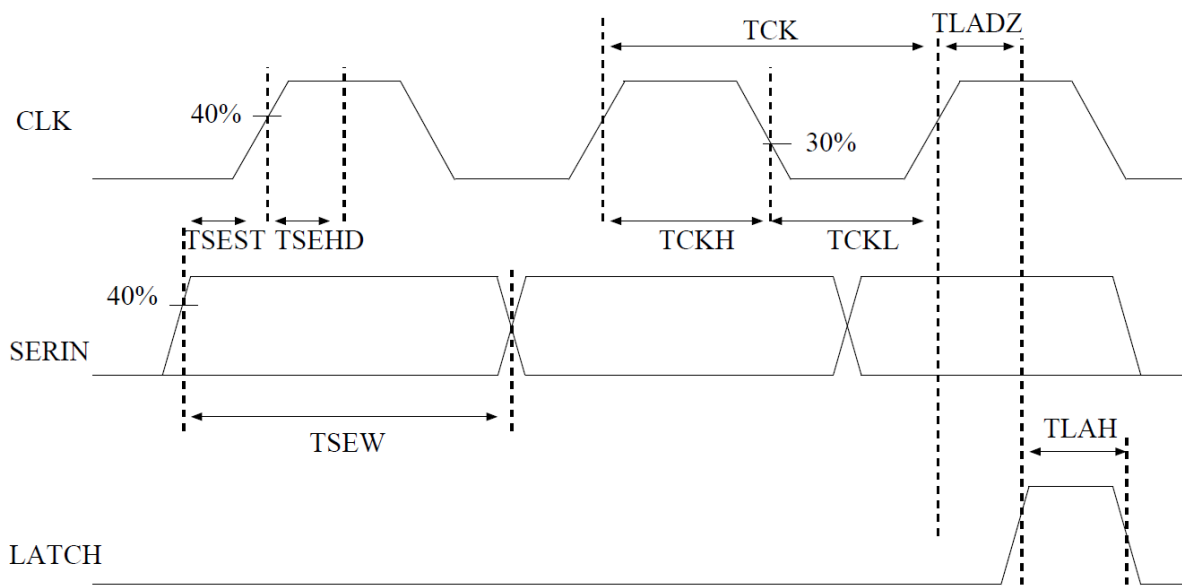


Figure 10. Write/access data for typical use case

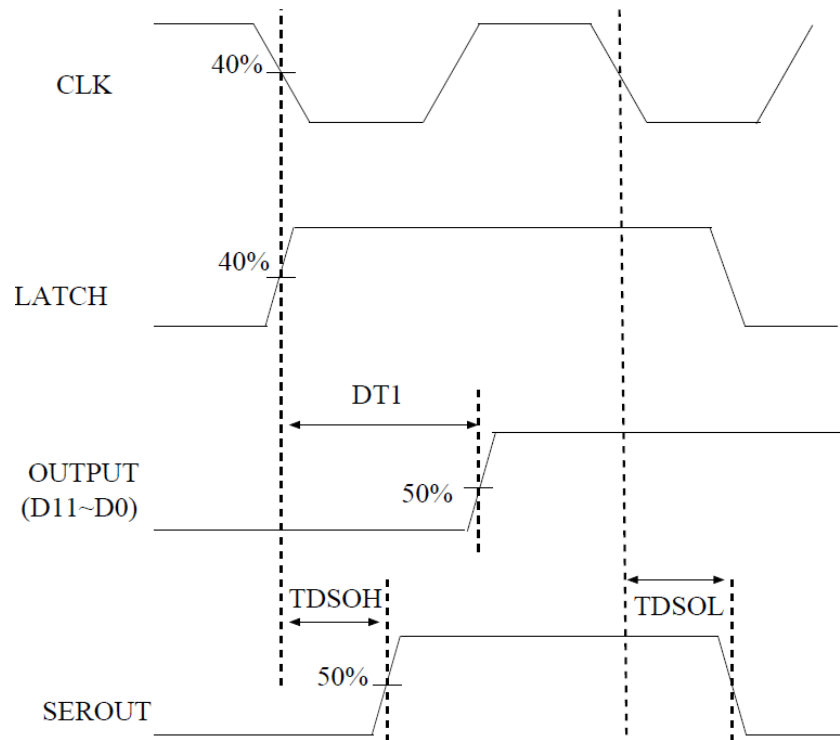


INPUT SIGNAL's TIMING RULE (Ta=-40~105°C VCC=3.0~5.5V)

Parameter	Symbol	Min	Unit
CLK period	TCK	800	ns
CLK high pulse width	TCKH	300	ns
CLK low pulse width	TCKL	300	ns
SERIN high and low pulse width	TSEW	780	ns
SERIN setup time prior to CLK rise	TSEST	150	ns
SERIN hold time after CLK rise	TSEHD	150	ns
LATCH high pulse time	TLAH	380	ns
LAST CLK rise to LATCH rise	TLADZ	200	ns

Figure 11. Input signals timing diagram showing absolute minimal timing

The timings in **Figure 11** are valid for a 1.25MHz clock signal. The input High Going threshold voltage (V_{TH}) is $0.4 V_{CC}$ on the rising edge and (V_{TH}) $0.3 V_{CC}$ on the falling edge for all digital pins. See electrical characteristics on page 6.



OUTPUT SIGNAL's DELAY TIME (Ta=-40~105°C VCC=3.0~5.5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
LATCH switching delay	TDLAH	-	-	3000	ns	
SEROUT propagation delay time(L→H)	TDSOH	-	-	1000	ns	
SEROUT propagation delay(H→L)	TDSOL	-	-	3000	ns	

Figure 12. Output signal's delay time

● Start-up sequence

After POR the digital registers are RESET. All outputs are off, the calibration register is set to have minimum LED brightness while diagnostic registers are pulled to zero. By default mask and calibration register are unlocked for writing and POR flag is "high" (see **Table 1. Default registers values**). This is described in the POR description above.

At startup the state machine inside the digital core of the BD18377 is in an undefined state. It requires two clock pulses to put the state machine into a defined state. The first two bits in the command sent to the controller will be recognized as "00". For this reason it is necessary to send either a dummy byte or a dummy command to put the device into a known state before sending other commands.

It is recommended to send a dummy byte since this will get latched out of the device without effect. If sending a dummy command it is recommended to send the commands 00xx, 10xx, 20xx or 30xx because these commands will not be changed and will have no effect until the MASK command is sent.

The recommended sequence to start-up is as follows:

- Send a dummy byte or command (**mandatory**)
- Read the diagnostics [READ STATUS].
- Read the diagnostics [READ STATUS] again. Receive the first command sent.
- The controller should compare the sent and received data. There are two possible results:
 - If the command address sent and received is equal communication is successful.
 - If the command received is 0000, there is an active POR event in the daisy chain and communication is corrupted.
- Clear the POR flag [RESET POR].
- Clear the diagnostic flags [RESET STATUS].
- Writes calibration data of all channels which are used in the application [WRITE CAL].
- Read back the calibration data for verification [READ CAL].
- Lock calibration data [LOCK CAL].
- If the application requires masking the short detection in the STATUS, the SHORTMASK is set [WRITE SHORT_MASK].
- If used the SHORT_MASK is read back for verification [READ SHORT_MASK].
- MASK data is written [WRITE MASK].
- Read back the MASK registers for verification [READ MASK].
- Set PWM to active.
- Use the command [READ SHORT] to confirm that none of the LEDs are shorted.
- Use the command [READ OPEN] to confirm that none of the LEDs are open circuit.
- If there is no fault, lock MASK registers [LOCK MASK].
- If there is a fault verify that it is persistent by the command [RESET STATUS] and then [READ STATUS].
- Clear all diagnostics at the end of the start-up sequence [RESET STATUS].
- Adjust PWM duty cycle for dimming if required.

● Post software POR Start-up sequence

In the full start-up sequence after a software POR [SOFTWARE POR] the controller:

- Read the diagnostics to confirm no pre exiting fault [READ STATUS].
- Clear the POR flag [RESET POR].
- If needed clear the diagnostics to confirm no persistent fault [RESET STATUS].
- Writes calibration data of all channels which are used in the application [WRITE CAL].
- Read back the calibration data for verification [READ CAL].
- Lock calibration data [LOCK CAL].
- If the application requires masking the short detection of STATUS, the SHORTMASK is set [WRITE SHORT_MASK].
- If used the SHORT_MASK is read back for verification [READ SHORT_MASK].
- MASK data is written [WRITE MASK].
- Read back the MASK registers for verification [READ MASK].
- Set PWM to active.
- Use the command [READ SHORT] to confirm that none of the LEDs are shorted.
- Use the command [READ OPEN] to confirm that none of the LEDs are open circuit.
- If there is no fault, lock MASK registers [LOCK MASK].
- If there is a fault verify that it is persistent by the command [RESET STATUS] and then [READ STATUS].
- Clear all diagnostics at the end of the start-up sequence [RESET STATUS].
- Adjust PWM duty cycle for dimming if required.

●Power dissipation

The maximum current specification per output $I_{D,max} = 50mA$. However when all channels are sinking this maximum the total power dissipation exceeds the value set by the package limit. The power dissipation can be estimated using Equation 6. Maximum power dissipation. In case of high current and high voltage it is possible to exceed the maximum power dissipation even at a single channel. Because these situations do not occur often the current limit per channel is set higher such that the flexibility of the system is improved.

It is recommended to connect the LEDs to a 5V supply voltage (V_{LED}) for an optimal SHORT detection and thermal performance. If the LEDs are connected to a higher voltage care should be taken to ensure proper short detect functionality and the power dissipation will increase. LED series resistors (R_D) may be added to reduce the voltage drop over the IC output. These resistors are an optional safeguard against exceeding the dissipation limit of BD18377. The maximum power rating of the BD18377EFV-M can be read from **Figure 13**.

$$P_{diss,max} > \sum_{i=0}^{11} (V_{LED} - V_{f,i} - I_{out,i} \cdot R_{D,i}) \cdot I_{out,i} \cdot \frac{T_{ON}}{T_{PWM}}$$

$$= \sum_{i=0}^{11} (V_{D,i} \cdot I_{o_i}) \cdot \frac{T_{ON}}{T_{PWM}}$$

Equation 6. Maximum power dissipation

- $P_{diss,max}$: Maximum power dissipation of the package
- V_{LED} : Supply voltage of LEDs.
- V_f : LED forward voltage
- R_D : Optional series resistance.
- T_{PWM} : Period of PWM
- T_{ON} : ON time (duty) of PWM

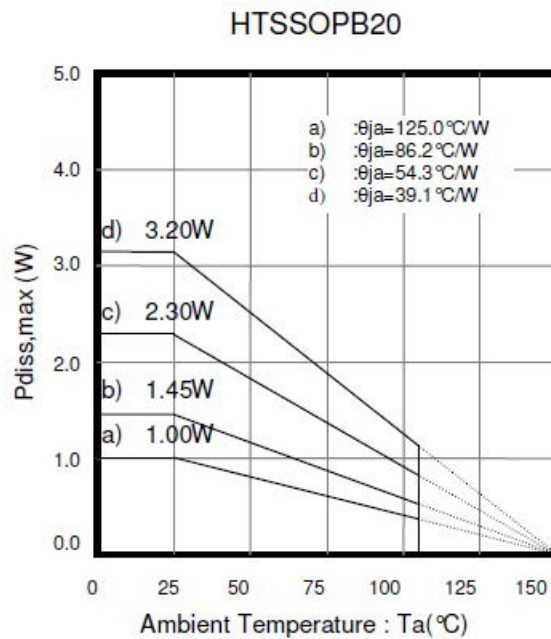


Figure 13. Maximum power dissipation of HTSSOPB20

- Measuring equipment: TH-156(Kuwano Electric)
- PCB size: 70mm x 70mm x 1.6mm
- PCB material: Glass epoxy FR4 CS3355
- Copper thickness: 18um
- For temperatures above 105°C Pdiss, max was measured but is not ensured
- : 1Layer PCB
- : 2Layer PCB(reverse copper area 15mm x 15mm)
- : 2Layer PCB(reverse copper area 70mm x 70mm)
- : 4Layer PCB(reverse copper area 70mm x 70mm)

● Input/output equivalent circuit

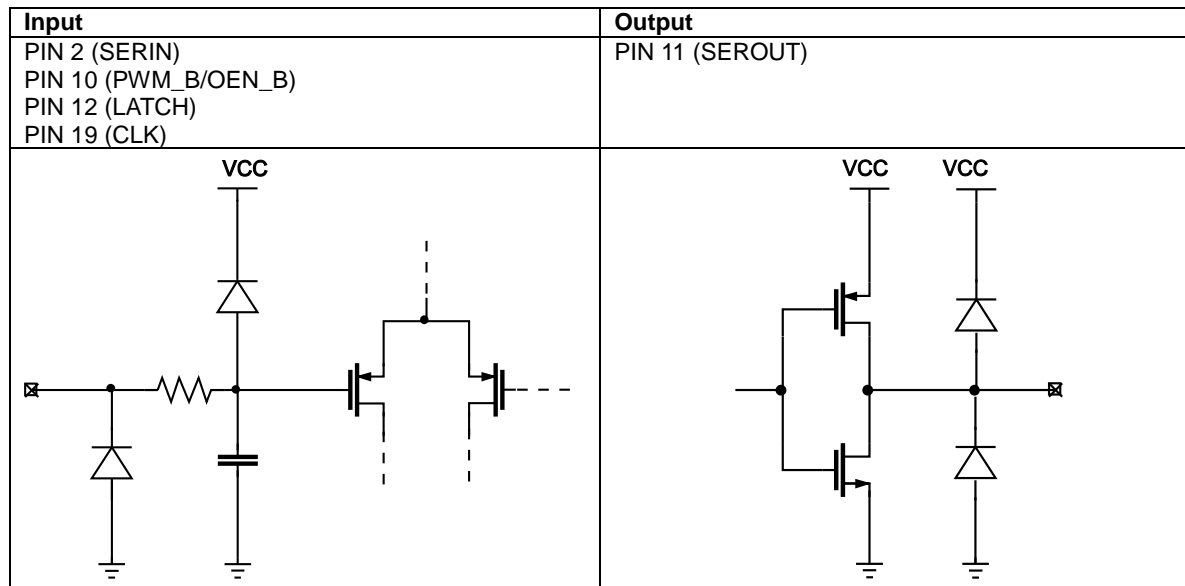


Figure 14. Input/output equivalent circuit

The digital inputs are CMOS inputs. They are not internally connected to pull-up or pull-down resistors such that even in a daisy chain they can be driven from a controller without delivering significant current.

●Operating Notes

1. Absolute maximum ratings
Use of the IC in excess of absolute maximum ratings (such as the input voltage or operating temperature range) may result in damage to the IC. Assumptions should not be made regarding the state of the IC (e.g., short mode or open mode) when such damage is suffered. If operational values are expected to exceed the maximum ratings for the device, consider adding protective circuitry (such as fuses) to eliminate the risk of damaging the IC.
2. GND potential
Ensure that the GND pin is held at the minimum potential in all operating conditions.
3. Thermal Design
Use a thermal design that allows for a sufficient margin for power dissipation (Pd) under actual operating conditions.
4. Inter-pin shorts and mounting errors
Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pins caused by poor soldering or foreign objects may result in damage to the IC.
5. Operation in strong electromagnetic fields
Exercise caution when using the IC in the presence of strong electromagnetic fields as doing so may cause the IC to malfunction.
6. Testing on application boards
When testing the IC on an application board, connecting a capacitor directly to a low-impedance pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from a jig or fixture during the evaluation process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.
7. Ground wiring patterns
When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground potential within the application in order to avoid variations in the small-signal ground caused by large currents. Also ensure that the GND traces of external components do not cause variations on GND voltage.
8. IC input pins and parasitic elements
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. PN junctions are formed at the intersection of these P layers with the N layers of other elements, creating parasitic diodes and/or transistors. For example (refer to the figure below):

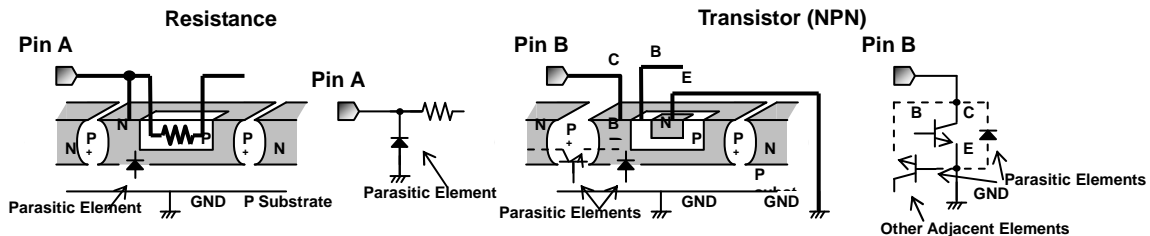


Figure 15. Example of IC Structure

- When GND > Pin A and GND > Pin B, the PN junction operates as a parasitic diode
- When GND > Pin B, the PN junction operates as a parasitic transistor

Parasitic diodes occur inevitably in the structure of the IC, and the operation of these parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

9. Over-current protection circuits
An over-current protection circuit (designed according to the output current) is integrated into the IC to prevent damage in the event of load shorting. This protection circuit is effective in preventing damage due to sudden and unexpected overloads on the output. However, the IC should not be used in applications where operation of the OCP function is anticipated or assumed
10. Thermal shutdown circuit (TSD)
This IC also incorporates a built-in TSD circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power

dissipation limits, the rise in the chip's junction temperature T_j will trigger the TSD circuit, shutting off all output power elements. The circuit automatically resets itself once the junction temperature T_j drops down to normal operating temperatures. The TSD protection will only engage when the IC's absolute maximum ratings have been exceeded; therefore, application designs should never attempt to purposely make use of the TSD function.

Status of this document

The English version of this document is formal specification. A customer may use the translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document formal version takes priority.

● Ordering Information

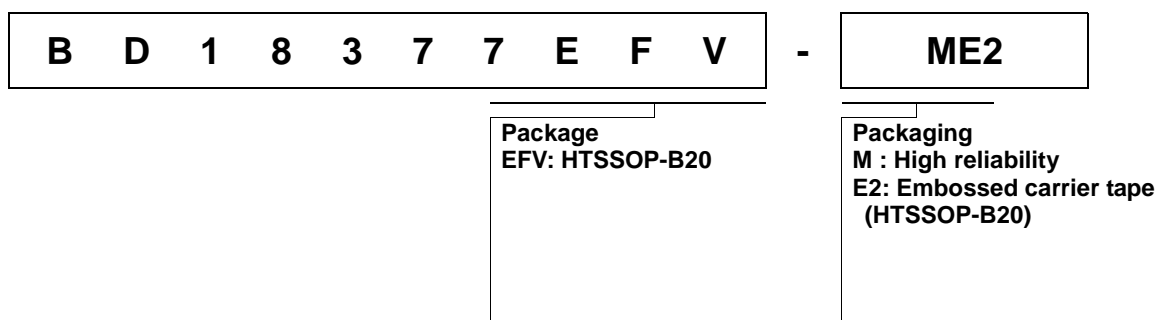


Figure 16. Ordering Information

● Physical Dimensions, Tape And Reel Information for HTSSOP-B20

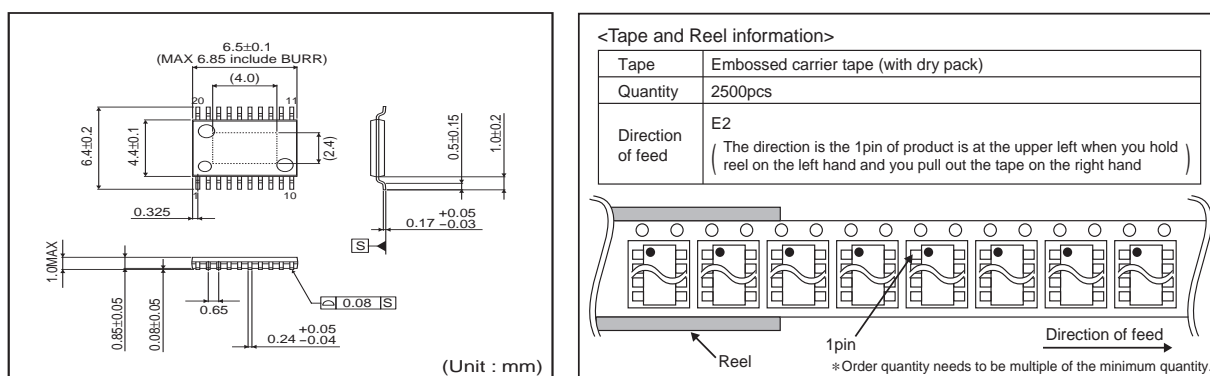


Figure 17. Tape and Reel Information for HTSSOP-B20

● Marking Diagram

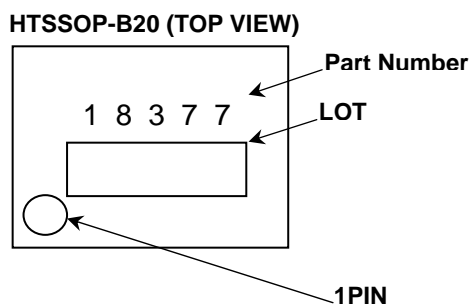


Figure 18. Marking Diagram

●Revision History

S. No.	Change	Date	Ver.	Author
1	First Version	June 31, 2012	Rev. 001	R. Kaushik D. James
2	Convergence with Rohm datasheet standard.	August 14, 2012	Rev. 002	R. Spee D. James
3	Updated Fig8 to correctly show the relation between PWM , Mask & Diagnostics	Sept 19, 2012	Rev. 003	R. Kaushik
4	Corrected the formatting of curves in Fig 5 & 6. Included -M in ordering information. Output current supply voltage shift better explained in Electrical Characteristics table.	Oct 01, 2012	Rev. 004	R. Kaushik

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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