



DDR SDRAM Module 256Mbyte (32Mx72bit), based on 16Mx8, 4Banks, 4K Ref., 184Pin-DIMM with PLL & Register Part No. HDD32M72D18RPW

GENERAL DESCRIPTION

The HDD32M72D18RPW is a 64M x 72 bit Double Data Rate(DDR) Synchronous Dynamic RAM high-density memory module. The module consists of eighteen CMOS 16M x 8 bit with 4banks DDR SDRAMs in 66pin TSOP-II 400mil packages and 2K EEPROM in 8-pin TSSOP package on a 184-pin glass-epoxy. Four 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each DDR SDRAM. The HDD32M72D18RPW is a DIMM(Dual in line Memory Module) .Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allows the same device to be useful for a variety of high bandwidth, high performance memory system applications. All module components may be powered from a single 2.5V DC power supply and all inputs and outputs are SSTL_2 compatible.

FEATURES

- Part Identification

HDD32M72B18RPW – 10A : 100MHz (CL=2)

HDD32M72B18RPW – 13A : 133MHz (CL=2)

HDD32M72B18RPW – 13B : 133MHz (CL=2.5)

- 256MB(32Mx72) registered DDR DIMM based on 16Mx8 DDR SDRSM
- 2.5V $\pm$ 0.2V VDD and VDDQ power supply
- Auto & self refresh capability (4K Cycles / 64ms)
- All input and output are compatible with SSTL_2 interface
- Data(DQ), Data strobes and write masks latched on the rising and falling edges of the clock
- All Addresses and control inputs except Data(DQ), Data strobes and Data masks latched on the rising edges of the clock
- MRS cycle with address key programs
 - Latency (Access from column address) : 2, 2.5
 - Burst length : 2, 4, 8
 - Data scramble : Sequential & Interleave
- Data(DQ), Data strobes and write masks latched on the rising and falling edges of the clock
- All Addresses and control inputs except Data(DQ), Data strobes and Data masks latched on the rising edges of the clock
- The used device is 4M x 8bit x 4Banks DDR SDRAM

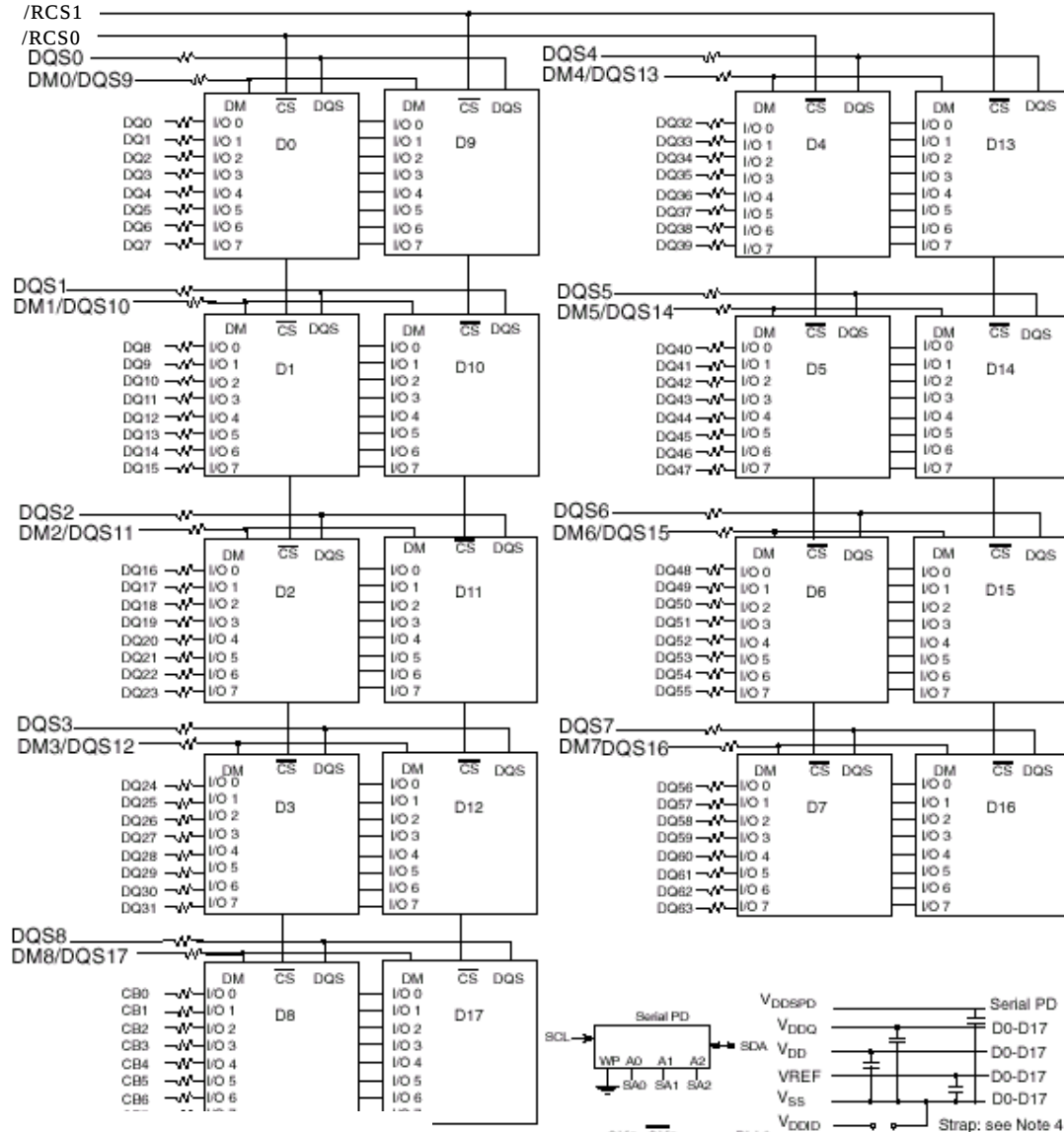
PIN ASSIGNMENT

PIN	Front	PIN	Back	PIN	Frontl	PIN	Back	PIN	Front	PIN	Back
1	VREF	32	A5	62	VDDQ	93	Vss	124	Vss	154	/RAS
2	DQ0	33	DQ24	63	/WE	94	DQ4	125	A6	155	DQ45
3	Vss	34	Vss	64	DQ41	95	DQ5	126	DQ28	156	VDDQ
4	DQ1	35	DQ25	65	/CAS	96	VDDQ	127	DQ29	157	/CS0
5	DQS0	36	DQS3	66	Vss	97	DM0	128	VDDQ	158	/CS1
6	DQ2	37	A4	67	DQS5	98	DQ6	129	DM3	159	DM5
7	VDD	38	VDD	68	DQ42	99	DQ7	130	A3	160	Vss
8	DQ3	39	DQ26	69	DQ43	100	Vss	131	DQ30	161	DQ46
9	NC	40	DQ27	70	VDD	101	NC	132	Vss	162	DQ47
10	/RESET	41	A2	71	* /CS2	102	NC	133	DQ31	163	* /CS3
11	Vss	42	Vss	72	DQ48	103	*A13	134	CB4	164	VDDQ
12	DQ8	43	A1	73	DQ49	104	VDDQ	135	CB5	165	DQ52
13	DQ9	44	CB0	74	Vss	105	DQ12	136	VDDQ	166	DQ53
14	DQS1	45	CB1	75	* CK2	106	DQ13	137	CK0	167	NC
15	VDDQ	46	VDD	76	* /CK2	107	DM1	138	/CK0	168	VDD
16	* CK1	47	DQS8	77	VDDQ	108	VDD	139	Vss	169	DM6
17	* /CK1	48	A0	78	DQS6	109	DQ14	140	DM8	170	DQ54
18	Vss	49	CB2	79	DQ50	110	DQ15	141	A10	171	DQ55
19	DQ10	50	Vss	80	DQ51	111	CKE1	142	CB6	172	VDDQ
20	DQ11	51	CB3	81	Vss	112	VDDQ	143	VDDQ	173	NC
21	CKE0	52	BA1	82	VDDID	113	* BA2	144	CB7	174	DQ60
22	VDDQ	KEY		83	DQ56	114	DQ20	KEY		175	DQ61
23	DQ16	53	DQ32	84	DQ57	115	*A12	145	Vss	176	Vss
24	DQ17	54	VDDQ	85	VDD	116	Vss	146	DQ36	177	DM7
25	DQS2	55	DQ33	86	DQS7	117	DQ21	147	DQ37	178	DQ62
26	Vss	56	DQS4	87	DQ58	118	A11	148	VDD	179	DQ63
27	A9	57	DQ34	88	DQ59	119	DM2	149	DM4	180	VDDQ
28	DQ18	58	Vss	89	Vss	120	VDD	150	DQ38	181	SA0
29	A7	59	BA0	90	NC	121	DQ22	151	DQ39	182	SA1
30	VDDQ	60	DQ35	91	SDA	122	A8	152	Vss	183	SA2
31	DQ19	61	DQ40	92	SCL	123	DQ23	153	DQ44	184	VDDSPD

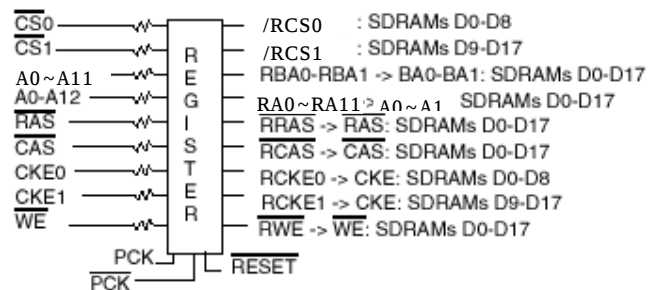
*These pins should be NC in the system which does not support SPD

PIN	PIN DESCRIPTION	PIN	PIN DESCRIPTION
A0~A11	Address input	VDD	Power supply(2.5V)
BA0~BA1	Bank Select Address	VDDQ	Power supply for DQs(2.5V)
DQ0~DQ63	Data input/output	VREF	Power supply for reference
CB0~CB7	Check Bit	VDDSPD	Serial EEPROM Power supply(3.3)
DQS0~DQS8	Data Strobe input/output	VSS	Ground
DM0~DM8	Data-in Mask	SA0~SA2	Address in EEPROM
CK0~/CK0	Clock input	SDA	Serial data I/O
CKE0~CKE1	Clock enable input	SCL	Serial clock
/CS0~/CS1	Chip Select input	VDDID	VDD identification flag
/RAS	Row Address strobe	NC	No connection
/CAS	Column Address strobe		

FUNCTIONAL BLOCK DIAGRAM



* Wire per Clock Loading Table/Wiring Diagrams



Notes:

1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ/DQS resistors should be 22 Ohms.
4. VDDID strap connections
(for memory device VDD, VDDQ):
STRAP OUT (OPEN): VDD = VDDQ
STRAP IN (VSS): VDD ≠ VDDQ.
5. RS0 and RS1 alternate between the back and front sides of the DIMM.
6. Address and control resistors should be 22 Ohms.

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CK, /CK	Clock	CK and CK are differential clock inputs. All address and control input signals are sam-pled on the positive edge of CK and negative edge of CK. Output (read) data is referenced to both edges of CK. Internal clock signals are derived from CK/CK.
CKE	Clock Enable	CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN(row ACTIVE in any bank). CKE is synchronous for all functions except for disabling outputs, which is achieved asynchronously. Input buffers, excluding CK, CK and CKE are disabled during power-down and self refresh modes, providing low standby power. CKE will recognizean LVCMOS LOW level prior to VREF being stable on power-up.
/CS	Chip Select	CS enables(registered LOW) and disables(registered HIGH) the command decoder. All commands are masked when CS is registered HIGH. CS provides for external bank selection on systems with multiple banks. CS is considered part of the command code.
A0 ~ A11	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	Bank select address	BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRE-CHARGE command is being applied.
/RAS	Row address strobe	Latches row addresses on the positive going edge of the CLK with /RAS low. Enables row access & precharge.
/CAS	Column address strobe	Latches column addresses on the positive going edge of the CLK with /CAS low. Enables column access.
/WE	Write enable	Enables write operation and row precharge. Latches data in starting from /CAS, /WE active.
DQS0~8	Data Strobe	Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data.
DM0~8	Input Data Mask	DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. DM pins include dummy loading internally, to matches the DQ and DQS load-ing.
DQ0 ~ 63	Data input/output	Data inputs/outputs are multiplexed on the same pins.
CB0~CB7	Check Bit	Check Bit Input/Output pins
VDDQ	Supply	DQ Power Supply : +2.5V $\pm$ 0.2V.
VDD	Supply	Power Supply : +2.5V $\pm$ 0.2V (device specific).
VSS	Supply	DQ Ground.
VREF	Supply	SSTL_2 reference voltage.
VDDSPD	Supply	Serial EEPROM Power Supply : 3.3v
VDDID		VDD identification Flag

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNTE
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}	-1.0 ~ 3.6	V
Voltage on V_{DDQ} supply relative to Vss	V_{DDQ}	-0.5 ~ 3.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	18	W
Short circuit current	I_{OS}	50	mA

Notes: Operation at above absolute maximum rating can adversely affect device reliability

DC OPERATING CONDITIONS

(Recommended operating conditions (Voltage referenced to Vss = 0V, $T_A = 0$ to 70°C))

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTE
Supply Voltage	V_{DD}	2.3	2.7	V	
I/O Supply Voltage	V_{DDQ}	2.3	2.7	V	
I/O Reference Voltage	V_{REF}	$V_{DDQ}/2 - 50mA$	$V_{DDQ}/2 + 50mA$	V	1
I/O Termination Voltage(system)	V_{TT}	$V_{REF} - 0.04$	$V_{REF} + 0.04$	V	2
Input High Voltage	$V_{IH} (DC)$	$V_{REF} + 0.15$	$V_{REF} + 0.3$	V	4
Input Low Voltage	$V_{IL} (DC)$	-0.3	$V_{REF} - 0.15$	V	4
Input Voltage Level, CK and /CK inputs	$V_{IN} (DC)$	-0.3	$V_{DDQ} + 0.3$	V	
Input Differential Voltage, CK and /CK inputs	$V_{ID} (DC)$	0.3	$V_{DDQ} + 0.6$	V	3
Input crossing point Voltage, CK and /CK inputs	$V_{IX} (DC)$	1.15	1.35	V	5
Input leakage current	I_{LI}	-2	2	uA	
Output leakage current	I_{OZ}	-5	5	uA	
Output High current ($V_{OUT} = 1.95V$)	I_{OH}	-16.8		mA	
Output Low current ($V_{OUT} = 0.35V$)	I_{OL}	16.8		mA	

Notes :

1. Includes $\pm 25mV$ margin for DC offset on V_{REF} , and a combined total of $\pm 50mV$ margin for all AC noise and DC offset on V_{REF} , bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on V_{REF} and internal DRAM noise coupled to V_{REF} , both of which may result in V_{REF} noise. V_{REF} should be de-coupled with an inductance of $\leq 3nH$.
2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} , and must track variations in the DC level of V_{REF} .
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
4. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a V_{REF} envelop that has been bandwidth limited to 200MHz.
5. The value of V_{IX} is expected to equal $0.5 \cdot V_{DDQ}$ of the transmitting device and must track variations in the dc level of the same.
6. These characteristics obey the SSTL-2 class II standards.

CAPACITANCE ($V_{DD} = \text{min to max}$, $V_{DDQ} = 2.5V \text{ to } 2.7V$, $T_A = 25^\circ C$, $f = 100MHz$)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Input capacitance(A0~A12, BA0~BA1, /RAS, /CAS,/WE)	C_{IN1}	-	12	pF
Input capacitance(CKE0,CKE1)	C_{IN2}	-	12	pF
Input capacitance(/CS0,/CS1)	C_{IN3}	-	11	pF
Input capacitance(CK0~/CK1)	C_{IN4}	-	12	pF
Input capacitance(DM0~DM8)	C_{IN5}	-	16	pF
Data & DQS input/output capacitance (DQ0 ~ DQ63, DQS0~DQS8)	C_{OUT1}	-	16	pF
Data input/output capacitance (CB0~CB7))	C_{OUT2}	-	16	pF

DC CHARACTERISTICS(RECOMMENDED OPERATING CONDITION UNLESS OTHERWISE NOTED, $V_{DD} = 2.5V$, $T = 25^\circ C$)

pARAMETER	Symbo I	TEST Condition	version			Unit
			-10A	-13A	-13B	
Operating current (One bank active-Precharge)	I_{DD0}	$t_{RC} \geq t_{RC}(\text{min})$, $t_{CK}=100MHz$ for DDR200,133MHz for DDR266A & DDR266B DQ,DM and DQS inputs changing twice per clock cycle Address and control inputs changing once per clock cycle	1299	1425	1425	mA
Operating current (One bank Operation)	I_{DD1}	One bank open, BL=4,Reads-Refer to the following page for detailed test condition	1479	1605	1605	mA
Precharge power-Down standby current	I_{DD2P}	All banks idle, power-down mode $CKE \leq V_{IL}(\text{max})$, $t_{CK}=100MHz$ for DDR200,133MHz for DDR266A & DDR266B $V_{IN} = V_{REF}$ for DQ,DQS and DM	696	736.5	736.5	mA
Precharge Floating standby current	I_{DD2F}	$/CS \geq V_{IH}(\text{min})$, All banks idle $CKE \geq V_{IH}(\text{min})$, $t_{CK}=100MHz$ for DDR200,133MHz for DDR266A & DDR266B Address and control inputs changing once per clock cycle $V_{IN} = V_{REF}$ for DQ,DQS and DM	831	885	885	mA
Precharge Quiet Standby current	I_{DD2Q}	$/CS \geq V_{IH}(\text{min})$, All banks idle $CKE \geq V_{IH}(\text{min})$, $t_{CK}=100MHz$ for DDR200,133MHz for DDR266A & DDR266B Address and other control inputs stable with keeping $\geq V_{IH}(\text{min})$ or $\leq V_{IL}(\text{max})$ $V_{IN} = V_{REF}$ for DQ,DQS and DM	786	822	822	
Active power-down Mode standby current	I_{DD3P}	One bank active; power-down mode; $CKE \leq V_{IL}(\text{max})$, $t_{CK}=100MHz$ for DDR200,133MHz for DDR266A & DDR266B $V_{IN} = V_{REF}$ for DQ,DQS and DM.	939	975	975	mA
Active standby current	I_{DD3N}	$CS\# \geq V_{IH}(\text{min})$, $CKE \geq V_{IH}(\text{min})$ one bank active, active – precharge, $t_{RC}=t_{RAS\text{max}}$ $t_{CK} = 100MHz$ for DDR200, 133Mhz for DDR266A & DDR266B, DQ, DQS and DM inputs changing twice per clock cycle Address and other control inputs changing once per clock cycle	1038	1110	1110	mA

Operating current (burst read)	I_{DD4R}	BL = 2, reads, continuous burst One bank open, Address and control inputs changing once per clock cycle, $I_{OUT} = 0mA$	1839	2055	2055	mA
Operating current (Burst write)	I_{DD4W}	BL = 2, write, continuous burst One bank open, Address and control inputs changing once per clock cycle	1839	2100	2100	mA
Auto refresh current	I_{DD5}	$t_{RC} = t_{RFC}(\min) - 8 \cdot t_{CK}$ for DDR200 at 100Mhz, $10 \cdot t_{CK}$ for DDR266A & DDR266B at 133Mhz, distributed refresh	2019	2415	2415	mA
Self refresh current	Normal	$CKE \leq 0.2V$, External clock should be on $t_{CK} = 100Mhz$ for DDR200, 133Mhz for DDR266A & DDR266B	336	336	336	mA
	Low Power		318	318	318	
Operating current (Four bank operation)	I_{DD7A}	Four bank interleaving with BL=4 -Refer to the following page for detailed test condition	2919	3315	3315	mA

Notes: Operation at above absolute maximum rating can adversely affect device reliability

AC OPERATING CONDITIONS

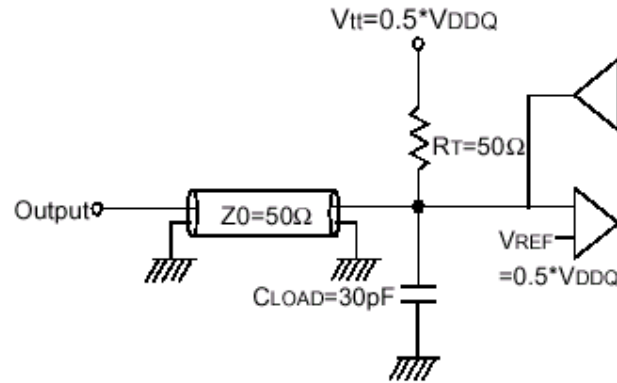
PARAMETER	STMBOL	MIN	MAX	UNIT	NOTE
Input High (Logic 1) Voltage, DQ, DQS and DM signals	$V_{IH} (AC)$	$V_{REF} + 0.31$			3
Input Low (Logic 0) Voltage, DQ, DQS and DM signals.	$V_{IL} (AC)$		$V_{REF} - 0.31$	V	3
Input Differential Voltage, CK and CK inputs	$V_{ID} (AC)$	0.7	$V_{DDQ} + 0.6$	V	1
Input Crossing Point Voltage, CK and CK inputs	$V_{IX} (AC)$	$0.5 \cdot V_{DDQ} - 0.2$	$0.5 \cdot V_{DDQ} + 0.2$	V	2

Notes:

1. V_{ID} is the magnitude of the difference between the input level on CK and the input on CK.
2. The value of V_{IX} is expected to equal $0.5 \cdot V_{DDQ}$ of the transmitting device and must track variations in the DC level of the same
3. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. the AC and DC input specifications are refation to a Vref envelope that has been bandwidth limited 20MHz.

AC OPERATING TEST CONDITIONS

PARAMETER	VALUE	UNIT	NOTE
Input reference voltage for Clock	$0.5 \cdot V_{DDQ}$	V	
Input signal maximum peak swing	1.5	V	
Input signal minimum slew rate	1.0	V	
Input Levels(V_{IH}/V_{IL})	$V_{REF} + 0.35/V_{REF}$	V	
Input timing measurement reference level	V_{REF}	V	
Output timing measurement reference level	V_{TT}	V	
Output load condition	See Load Circuit	V	



(Fig. 1) Output Load Circuit (SSTL_2)

AC CHARACTERISTICS (These AC characteristics were tested on the Component)

PARAMETER		SYMBOL	DDR200		DDR266A		DDR266B		UNIT	NOTE
			-10A		-13A		-13B			
			MIN	MAX	MIN	MAX	MIN	MAX		
Row cycle time		t _{RC}	70		65		65		ns	1
Refresh row cycle time		t _{RFC}	80		75		75		ns	1,2
Row active time		t _{RAS}	48	120K	45	120K	45	120K	ns	1,2
/RAS to /CAS delay		t _{RCD}	20		20		20		ns	3
Row precharge time		t _{RP}	20		20		20		ns	3
Row active to Row active delay		t _{RRD}	15		15		15		ns	3
Write recovery time		t _{WR}	2		2		2		t _{CK}	3
Last data in to Read command		t _{CDLR}	1		1		1		t _{CK}	2
Col. address to Col. address delay		t _{CCD}	1		1		1		t _{CK}	
Clock cycle time	CL=2.0	t _{CK}	10	12	7.5	12	10	12	ns	
	CL=2.5			12	7.5	12	7.5	12	ns	
Clock high level width		t _{CH}	0.45	0.55	0.45	0.55	0.45	0.55	t _{CK}	
Clock low level width		t _{CL}	0.45	0.55	0.45	0.55	0.45	0.55	t _{CK}	
DQS-out access time from CK/CK		t _{DQSCK}	-0.8	+0.8	-0.75	+0.75	-0.75	+0.75	ns	
Output data access time from CK/CK		t _{AC}	-0.8	+0.8	-0.75	+0.75	-0.75	+0.75	ns	
Data strobe edge to ouput data edge		t _{DQSQ}	-	+0.6	-	+0.5	-	+0.5	ns	
Read Preamble		t _{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	t _{CK}	
Read Postamble		t _{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	t _{CK}	
Data out high impedance time from CK- /CK		t _{HZQ}	-0.8	+0.8	-0.75	+0.75	-0.75	+0.75	ns	2

CK to valid DQS-in	t_{DQSS}	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
DQS-in setup time	t_{WPRES}	0		0		0		ns	3
DQS-in hold time	t_{WPREH}	0.25		0.25		0.25		t_{CK}	
DQS-in falling edge to CK rising-setup time	t_{DSS}	0.2		0.2		0.2		t_{CK}	
DQS-in falling edge to CK rising hold time	t_{DSH}	0.2		0.2		0.2		t_{CK}	
DQS-in high level width	t_{DQSH}	0.35		0.35		0.35		t_{CK}	
DQS-in low level width	t_{DQSL}	0.35		0.35		0.35		t_{CK}	
DQS-in cycle time	t_{DSC}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	
Address and Control Input setup time	t_{IS}	1.1		0.9		0.9		ns	
Address and Control Input hold time	t_{IH}	1.1		0.9		0.9		ns	
Mode register set cycle time	t_{MRD}	16		15		15		ns	
DQ & DM setup time to DQS	t_{DS}	0.6		0.5		0.5		ns	
DQ & DM hold time to DQS	t_{DH}	0.6		0.5		0.5		ns	
DQ & DM input pulse width	t_{DIPW}	2		1.75		1.75		ns	
Power down exit time	t_{PDEX}	10		10		10		ns	
Exit self refresh to write command	t_{XSW}	116		95				ns	
Exit self refresh to bank active command	t_{XSA}	80		75		75		ns	
Exit self refresh to read command	t_{XSR}	200		200		200		Cycle	
Refresh interval time	T_{REF}	7.8		7.8		7.8		us	1
Output DQS valid window	T_{QH}	0.35		0.35		0.35		t_{CK}	
DQS write postamble time	T_{WPST}	0.25		0.25		0.25		t_{CK}	4

Notes :

1. Maximum burst refresh of 8.
2. t_{HZQ} transitions occurs in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving.
3. The specific requirement is that DQS be valid(High-Low) on or before this CK edge. The case shown(DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on t_{DQSS} .
4. The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.

SIMPLIFIED TRUTH TABLE

COMMAND			CK E n-1	CK E n	/CS	/RAS	/CAS	/WE	DM	BA 0,1	A10/ AP	A11,A12 A9~A0	NOTE
Register	Extended MRS		H	X	L	L	L	L	X	OP code			1,2
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column Address (A0 ~A9)	4
	Auto precharge enable										H		4
Write & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column Address (A0 ~ A9)	4
	Auto precharge enable							L			H		4,6
Burst Stop			H	X	L	H	H	L	X	X			7
Precharg e	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		5
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Precharge power down mode		Entry	H	L	X	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DM			H	X					V	X			8
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

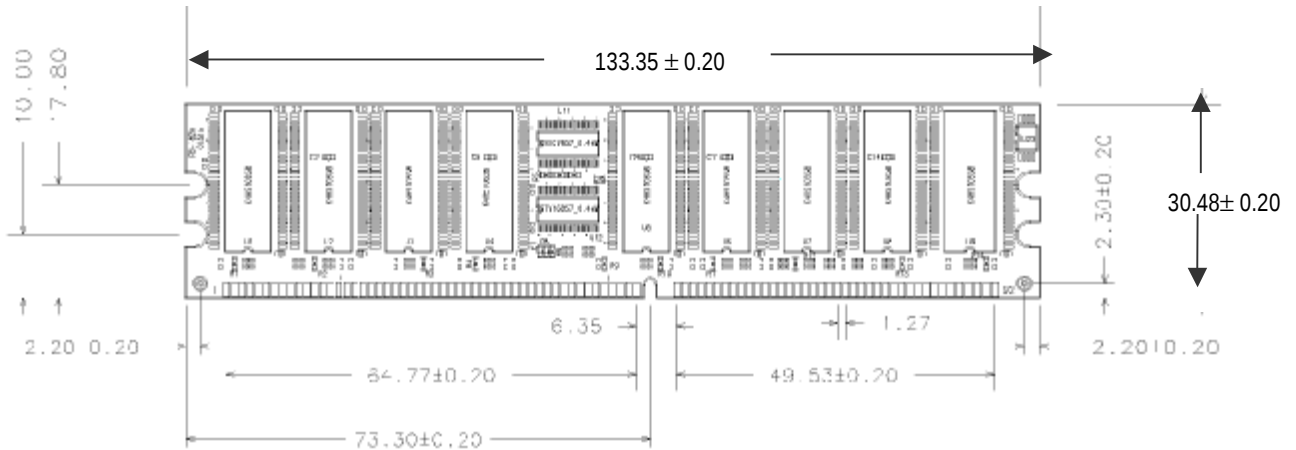
Notes :

- OP Code : Operand code
A0 ~ A12 & BA0 ~ BA1 : Program keys. (@ MRS)
- MRS can be issued only at all banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.
- Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
- BA0 ~ BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.
- During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.
- Burst stop command is valid at every burst length.
- DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges
(Write DM latency is 0)

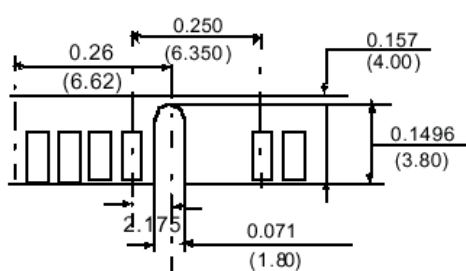
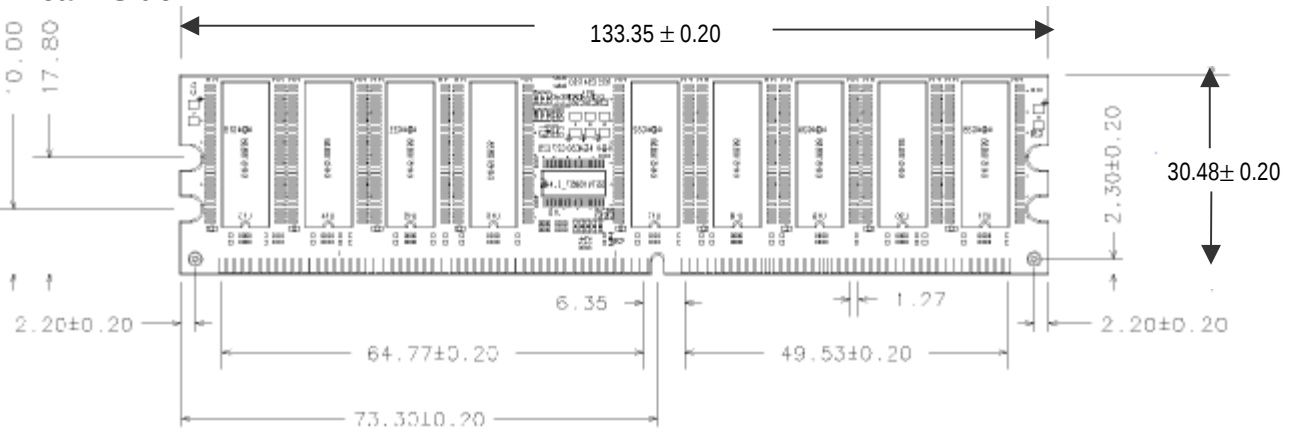
PACKAGING INFORMATION

Unit : mm

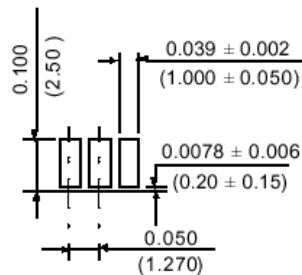
< Front -Side >



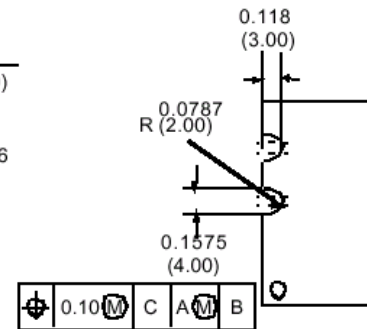
< Rear -Side >



Detail A



Detail B

*** PCB 두께 : 1.27 ± 0.08 mm

ORDERING INFORMATION

Part Number	Density	Org.	Package	Ref.	Vcc	MODE	MAX.frq
HDD32M72B18RWP-10A	256MByte	32M x 72	184PIN DIMM	4K	2.5V	DDR	100MHz/CL2
HDD32M72B18RW-13A	256MByte	32M x 72	184PIN DIMM	4K	2.5V	DDR	100MHz/CL2
HDD32M72B18RW-13B	256MByte	32M x 72	184PIN DIMM	4K	2.5V	DDR	100MHz/CL2

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru

moschip.ru_4

moschip.ru_6

moschip.ru_9