



FDP4D5N10C / FDPF4D5N10C

N-Channel Shielded Gate PowerTrench® MOSFET

100 V, 128 A, 4.5 mΩ

Features

- Max $r_{DS(on)}$ = 4.5 mΩ at $V_{GS} = 10$ V, $I_D = 100$ A
- Extremely Low Reverse Recovery Charge, Q_{rr}
- 100% UIL Tested
- RoHS Compliant

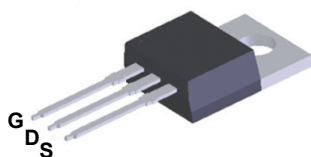


General Description

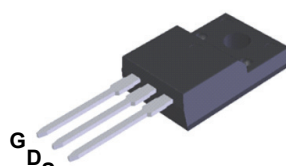
This N-Channel MV MOSFET is produced using ON Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized to minimize on-state resistance and yet maintain superior switching performance with best in class soft body diode.

Applications

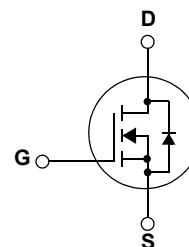
- Synchronous Rectification for ATX / Server / Telecom PSU
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter



TO-220



TO-220F



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Ratings		Units
		FDP4D5N10C	FDPF4D5N10C	
V_{DS}	Drain to Source Voltage	100	100	V
V_{GS}	Gate to Source Voltage	±20	±20	V
I_D	Drain Current -Continuous $T_C = 25^\circ\text{C}$ (Note 3)	128*	128*	A
	-Continuous $T_C = 100^\circ\text{C}$ (Note 3)	91	91	
	-Pulsed (Note 1)	512	512	
E_{AS}	Single Pulse Avalanche Energy (Note 2)	486		mJ
P_D	Power Dissipation $T_C = 25^\circ\text{C}$	150	37.5	W
	Power Dissipation $T_A = 25^\circ\text{C}$	2.4	2.4	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +175	-55 to +175	$^\circ\text{C}$

* Drain current limited by maximum junction temperature. Package limitation current is 120A.

Thermal Characteristics

Symbol	Parameter	FDP4D5N10C	FDPF4D5N10C	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.0	4.0	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	62.5	

Package Marking and Ordering Information

Device Marking	Device	Package	Packing Mode	Quantity
FDP4D5N10C	FDP4D5N10C	TO-220	Tube	50 units
FDPF4D5N10C	FDPF4D5N10C	TO-220F	Tube	50 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C		53		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 80\ \text{V}$, $T_J = 150^\circ\text{C}$			500	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}$, $V_{DS} = 0\ \text{V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 310\ \mu\text{A}$	2.0	3.2	4.0	V
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}$, $I_D = 100\ \text{A}$		4.0	4.5	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 5\ \text{V}$, $I_D = 100\ \text{A}$		134		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 50\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$		3615	5065	pF
C_{oss}	Output Capacitance			2330	3265	pF
C_{rss}	Reverse Transfer Capacitance			18	35	pF
R_g	Gate Resistance		0.1	1.1	2.2	Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\ \text{V}$, $I_D = 100\ \text{A}$, $V_{GS} = 10\ \text{V}$, $R_{GEN} = 6\ \Omega$		29	47	ns
t_r	Rise Time			49	79	ns
$t_{d(off)}$	Turn-Off Delay Time			41	66	ns
t_f	Fall Time			13	24	ns
Q_g	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $10\ \text{V}$	$V_{DD} = 50\ \text{V}$, $I_D = 100\ \text{A}$	48	68	nC
Q_{gs}	Gate to Source Gate Charge			19		nC
Q_{gd}	Gate to Drain "Miller" Charge			9		nC
Q_{oss}	Output Charge	$V_{DD} = 50\ \text{V}$, $V_{GS} = 0\ \text{V}$		150		nC

Drain-Source Diode Characteristic

I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	128	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	512	A
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}$, $I_S = 100\ \text{A}$		1.0	1.3	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\ \text{V}$, $V_{DD} = 50\ \text{V}$, $I_F = 100\ \text{A}$, $dI_F/dt = 100\ \text{A}/\mu\text{s}$		82	132	ns
Q_{rr}	Reverse Recovery Charge			106	170	nC
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\ \text{V}$, $V_{DD} = 50\ \text{V}$, $I_F = 100\ \text{A}$, $dI_F/dt = 300\ \text{A}/\mu\text{s}$		71	114	ns
Q_{rr}	Reverse Recovery Charge			258	413	nC

Notes:

1. Pulsed I_D please refer to Figure "Forward Bias Safe Operating Area" for more details.
2. E_{AS} of 486 mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 3\ \text{mH}$, $I_{AS} = 18\ \text{A}$, $V_{DD} = 100\ \text{V}$, $V_{GS} = 10\ \text{V}$. 100% test at $L = 0.1\ \text{mH}$, $I_{AS} = 58\ \text{A}$.
3. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

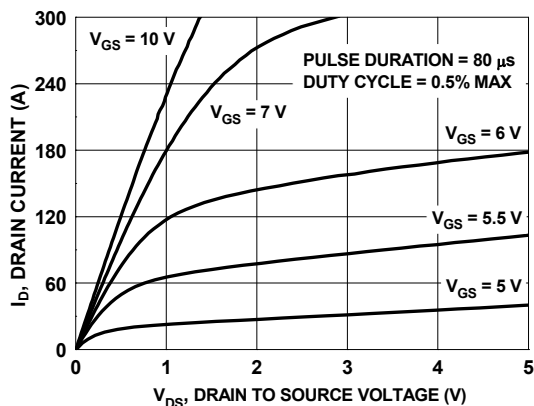


Figure 1. On Region Characteristics

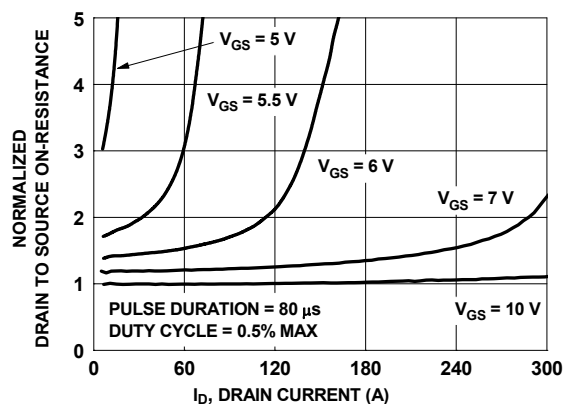


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

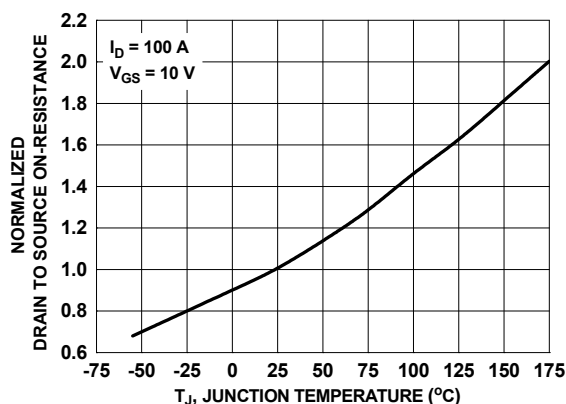


Figure 3. Normalized On Resistance vs. Junction Temperature

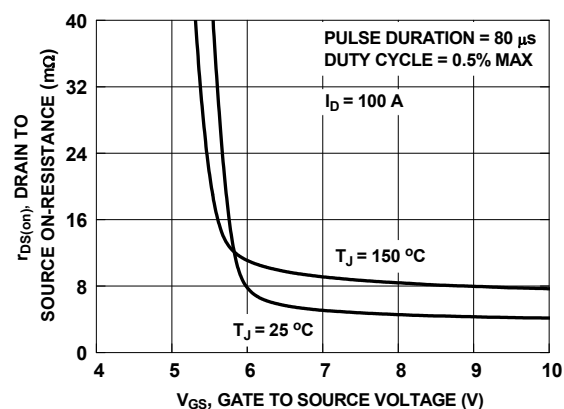


Figure 4. On-Resistance vs. Gate to Source Voltage

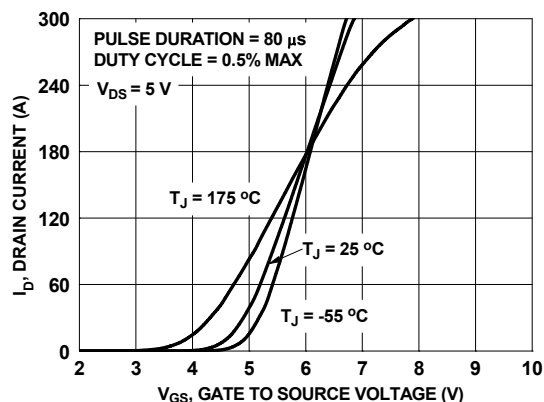


Figure 5. Transfer Characteristics

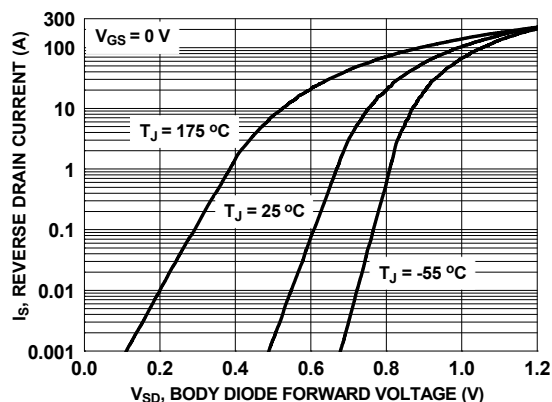


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted.

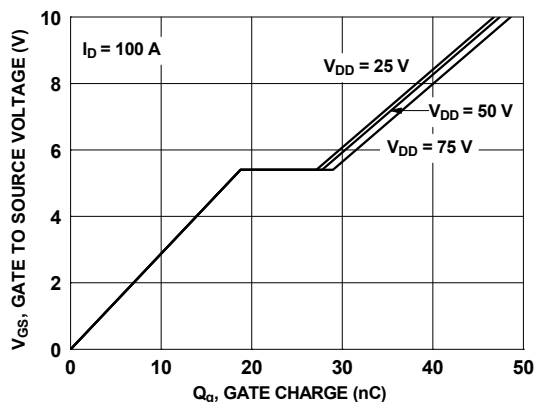


Figure 7. Gate Charge Characteristics

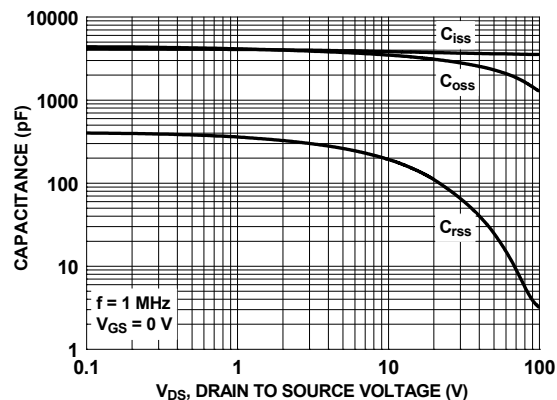


Figure 8. Capacitance vs. Drain to Source Voltage

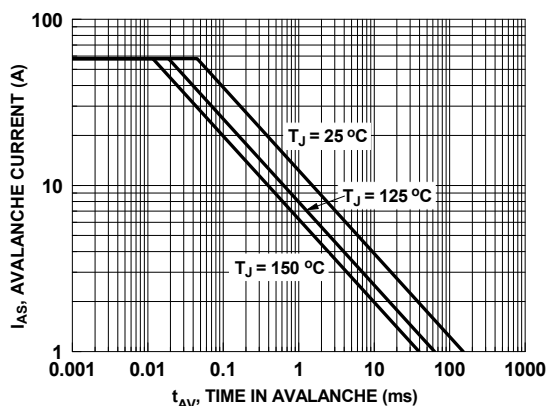


Figure 9. Unclamped Inductive Switching Capability

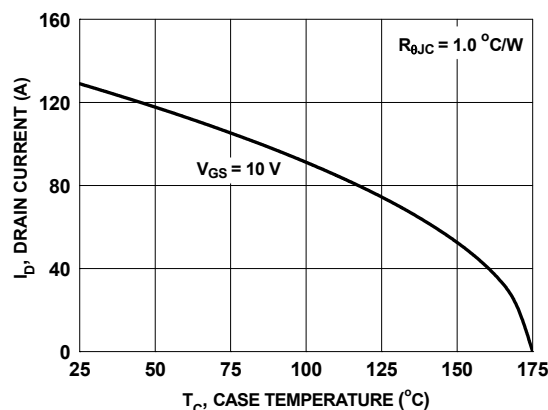


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

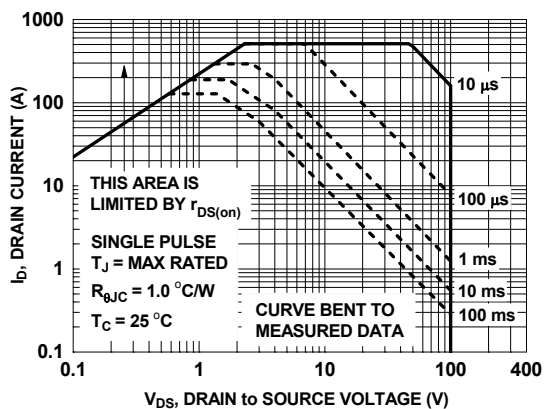


Figure 11. Forward Bias Safe Operating Area for FDP4D5N10C

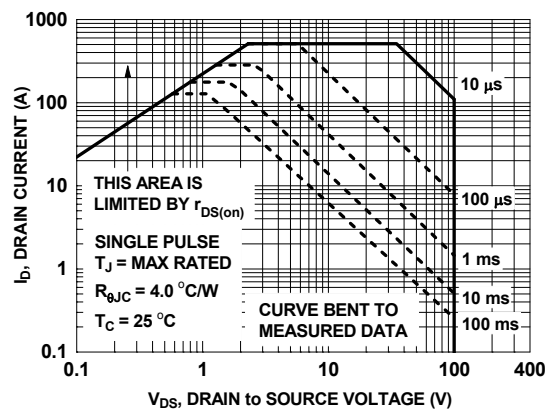


Figure 12. Forward Bias Safe Operating Area for FDPF4D5N10C

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

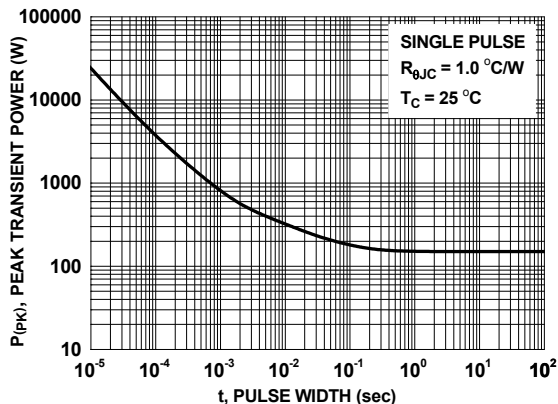


Figure 13. Single Pulse Maximum Power Dissipation for FDP4D5N10C

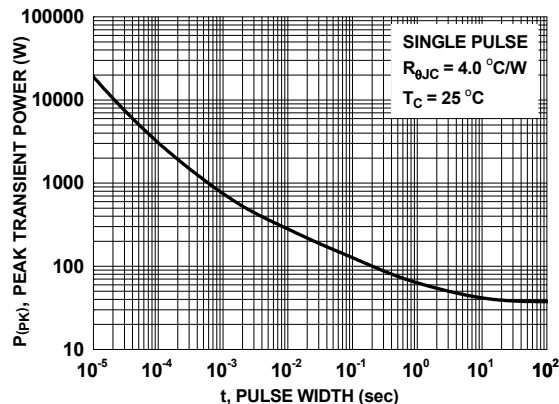


Figure 14. Single Pulse Maximum Power Dissipation for FDPF4D5N10C

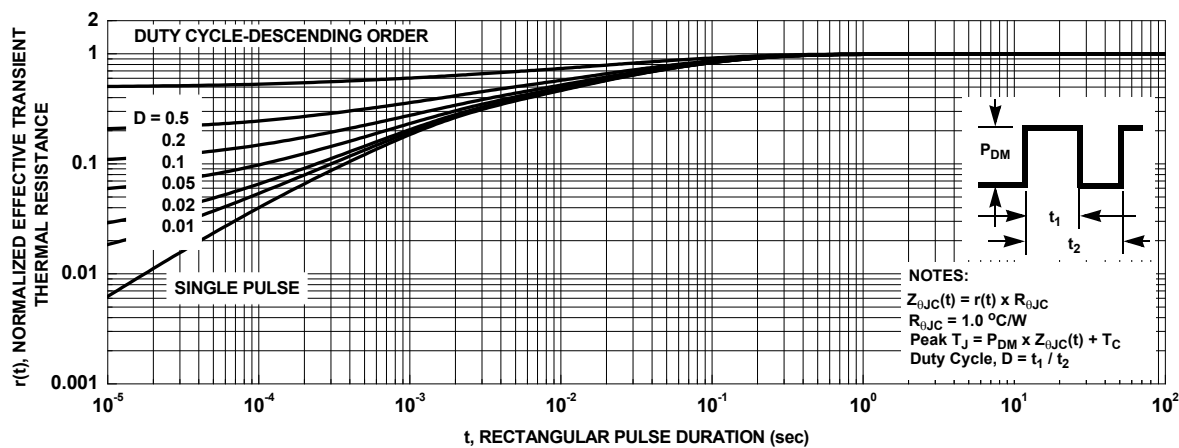


Figure 15. Junction-to-Case Transient Thermal Response Curve for FDP4D5N10C

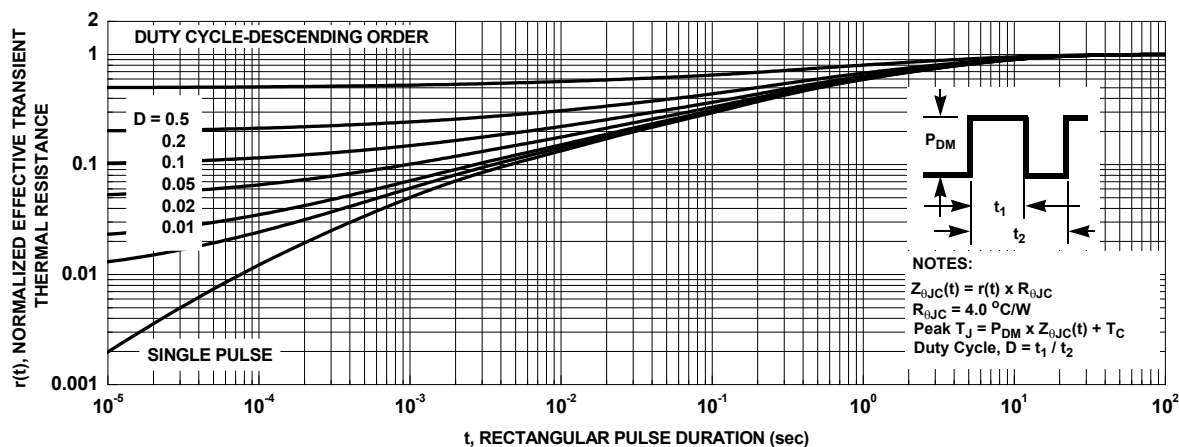
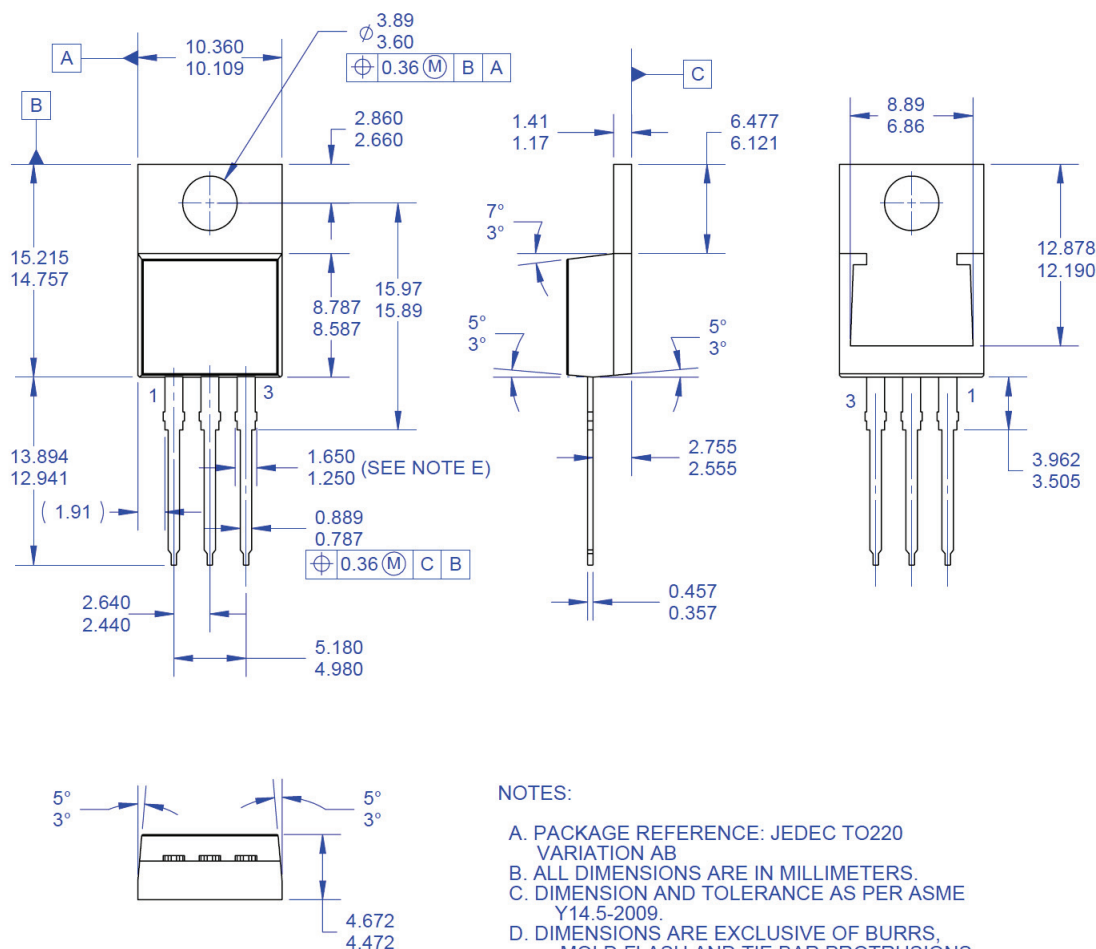


Figure 16. Junction-to-Case Transient Thermal Response Curve for FDPF4D5N10C

Dimensional Outline and Pad Layout



NOTES:

- A. PACKAGE REFERENCE: JEDEC TO220 VARIATION AB
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSION AND TOLERANCE AS PER ASME Y14.5-2009.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. MAX WIDTH FOR F102 DEVICE = 1.35mm.
- F. DRAWING FILE NAME: TO220T03REV4.
- G. FAIRCHILD SEMICONDUCTOR.

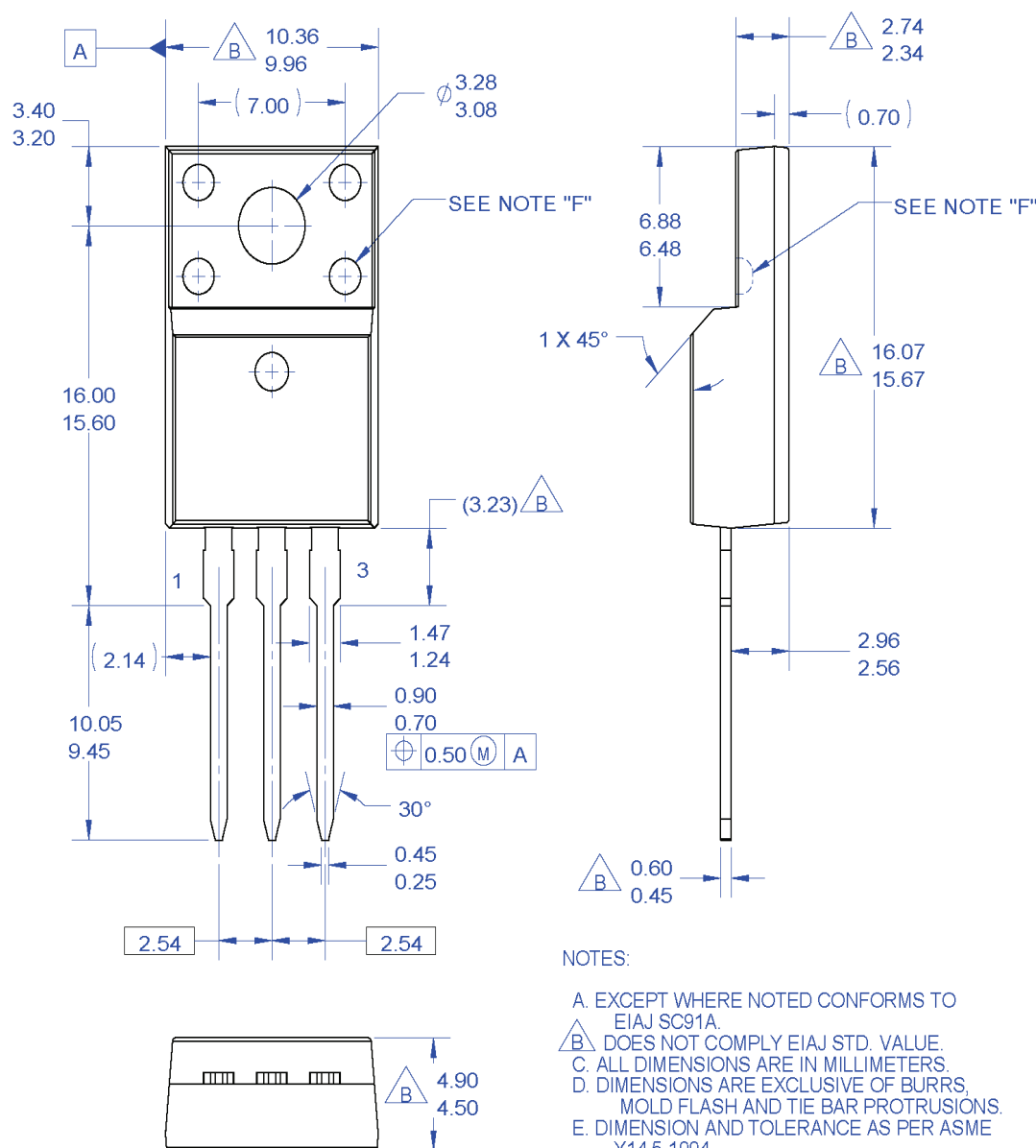
TO-220, Molded, 3-Lead, Jedec Variation AB (Delta)

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Dimensional Outline and Pad Layout



TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead

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