# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

# 74HC/HCT40103
## 8-bit synchronous binary down counter

Product specification
Supersedes data of December 1990
File under Integrated Circuits, IC06

1998 Jul 08

Philips Semiconductors

PHILIPS

# 8-bit synchronous binary down counter 74HC/HCT40103

## FEATURES

- Cascadable
- Synchronous or asynchronous preset
- Output capability: standard
- $I_{CC}$ category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT40103 are high-speed Si-gate CMOS devices and are pin compatible with the “40103” of the “4000B” series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT40103 consist each of an 8-bit synchronous down counter with a single output which is active when the internal count is zero. The “40103” contains a single 8-bit binary counter and has control inputs for enabling or disabling the clock (CP), for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the terminal count output ($\overline{TC}$) are active-LOW logic.

In normal operation, the counter is decremented by one count on each positive-going transition of the clock (CP).

Counting is inhibited when the terminal enable input ($\overline{TE}$) is HIGH. The terminal count output ($\overline{TC}$) goes LOW when the count reaches zero if $\overline{TE}$ is LOW, and remains LOW for one full clock period.

When the synchronous preset enable input ($\overline{PE}$) is LOW, data at the jam input ($P_0$ to $P_7$) is clocked into the counter on the next positive-going clock transition regardless of the state of $\overline{TE}$. When the asynchronous preset enable input ($\overline{PL}$) is LOW, data at the jam input ($P_0$ to $P_7$) is asynchronously forced into the counter regardless of the state of $\overline{PE}$, $\overline{TE}$, or CP. The jam inputs ($P_0$ to $P_7$) represent a single 8-bit binary word.

When the master reset input ($\overline{MR}$) is LOW, the counter is asynchronously cleared to its maximum count (decimal 255) regardless of the state of any other input. The precedence relationship between control inputs is indicated in the function table.

If all control inputs except $\overline{TE}$ are HIGH at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 256 clock pulses long.
The “40103” may be cascaded using the $\overline{TE}$ input and the $\overline{TC}$ output, in either a synchronous or ripple mode.

## QUICK REFERENCE DATA

GND = 0 V; $T_{amb}$ = 25 °C; $t_r = t_f$ = 6 ns

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|---|---|---|---|---|---|
| | | | HC | HCT | |
| $t_{PHL}/ t_{PLH}$ | propagation delay CP to $\overline{TC}$ | $C_L$ = 15 pF; $V_{CC}$ = 5 V | 30 | 30 | ns |
| $f_{max}$ | maximum clock frequency | | 32 | 31 | MHz |
| $C_I$ | input capacitance | | 3.5 | 3.5 | pF |
| $C_{PD}$ | power dissipation capacitance per package | notes 1 and 2 | 24 | 27 | pF |

**Notes**

1. $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   $f_i$ = input frequency in MHz

   $f_o$ = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   $C_L$ = output load capacitance in pF

   $V_{CC}$ = supply voltage in V

2. For HC the condition is $V_I$ = GND to $V_{CC}$
   For HCT the condition is $V_I$ = GND to $V_{CC}$ – 1.5 V

## ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|---|---|---|---|
| | NAME | DESCRIPTION | VERSION |
| 74HC40103N; 74HCT40103N | DIP16 | plastic dual in-line package; 16 leads (300 mil); long body | SOT38-1 |
| 74HC40103D; 74HCT40103D | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| 74HC40103DB; 74HCT40103DB | SSOP16 | plastic shrink small outline package; 16 leads; body width 5.3 mm | SOT338-1 |
| 74HC40103PW; | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |

## PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| 1 | CP | clock input (LOW-to-HIGH, edge-triggered) |
| 2 | $\overline{MR}$ | asynchronous master reset input (active LOW) |
| 3 | $\overline{TE}$ | terminal enable input |
| 4, 5, 6, 7, 10, 11, 12, 13 | $P_0$ to $P_7$ | jam inputs |
| 8 | GND | ground (0 V) |
| 9 | $\overline{PL}$ | asynchronous preset enable input (active LOW) |
| 14 | $\overline{TC}$ | terminal count output (active LOW) |
| 15 | $\overline{PE}$ | synchronous preset enable input (active LOW) |
| 16 | $V_{CC}$ | positive supply voltage |

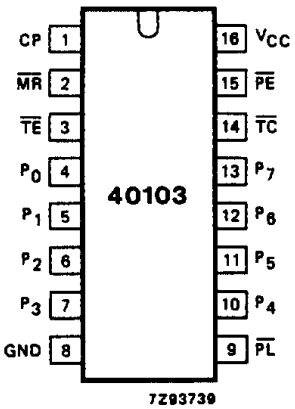



Fig.1 Pin configuration.

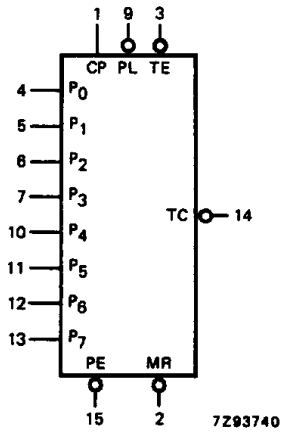



Fig.2 Logic symbol.

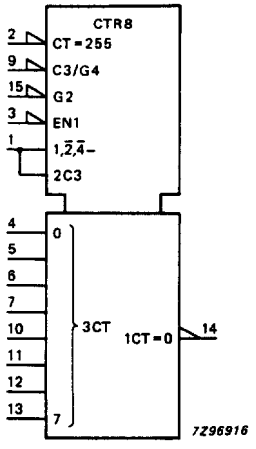



Fig.3 IEC logic symbol.

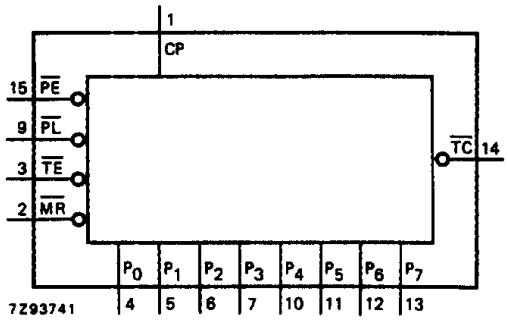



Fig.4 Functional diagram.

**FUNCTION TABLE**

| CONTROL INPUTS | | | | PRESET MODE | ACTION |
|---|---|---|---|---|---|
| $\overline{MR}$ | $\overline{PL}$ | $\overline{PE}$ | $\overline{TE}$ | | |
| H | H | H | H | synchronous | inhibit counter |
| H | H | H | L | | count down |
| H | H | L | X | | preset on next LOW-to HIGH clock transition |
| H | L | X | X | asynchronous | preset asynchronously |
| L | X | X | X | | clear to maximum count |

**Note**

1. Clock connected to CP.
   Synchronous operation: changes occur on the LOW-to-HIGH CP transition.
   Jam inputs: MSD = $P_7$, LSD = $P_0$.
   H = HIGH voltage level
   L = LOW voltage level
   X = don't care

**APPLICATIONS**

- Divide-by-n counters
- Programmable timers
- Interrupt timers
- Cycle/program counters

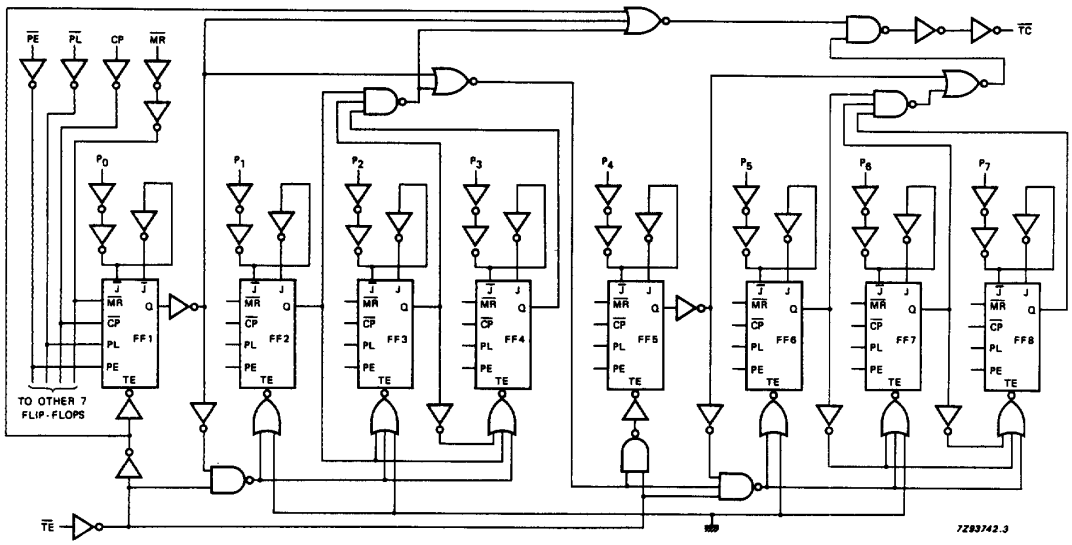



Fig.5 Logic diagram.

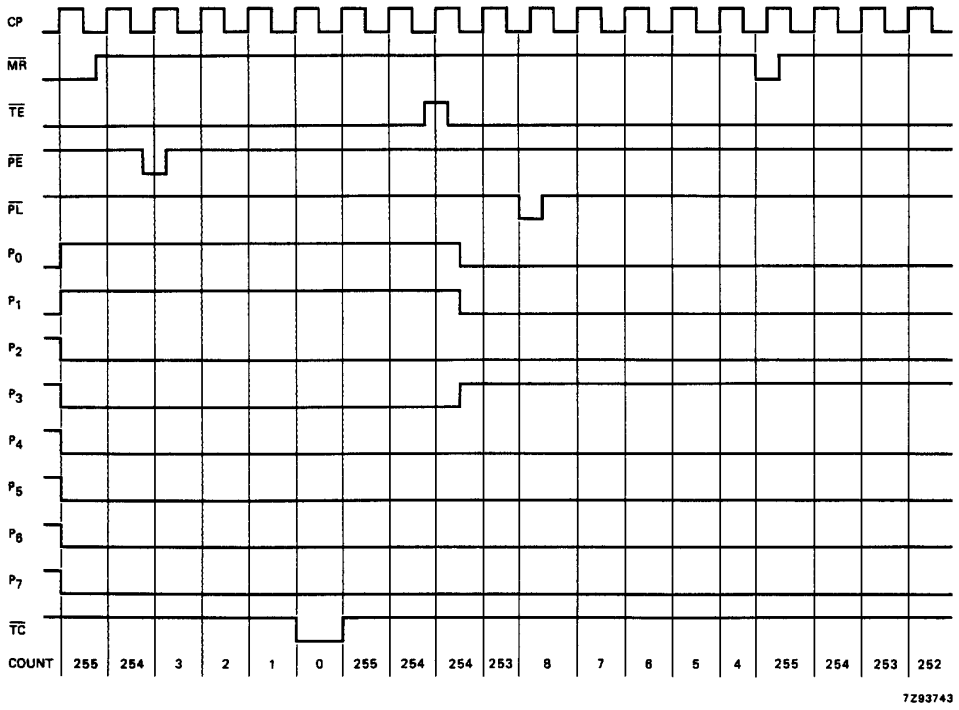



Fig.6 Timing diagram.

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
$I_{CC}$ category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; $C_L$ = 50 pF

| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HC | | | | | | | | $V_{CC}$ (V) | WAVEFORMS |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| $t_{PHL}/ t_{PLH}$ | propagation delay CP to $\overline{TC}$ | | 96 | 300 | | 375 | | 450 | ns | 2.0 | Fig.7 |
| | | | 35 | 60 | | 75 | | 90 | | 4.5 | |
| | | | 28 | 51 | | 64 | | 77 | | 6.0 | |
| $t_{PHL}/ t_{PLH}$ | propagation delay $\overline{TE}$ to $\overline{TC}$ | | 50 | 175 | | 220 | | 265 | ns | 2.0 | Fig.8 |
| | | | 18 | 35 | | 44 | | 53 | | 4.5 | |
| | | | 14 | 30 | | 37 | | 45 | | 6.0 | |
| $t_{PHL}/ t_{PLH}$ | propagation delay $\overline{PL}$ to $\overline{TC}$ | | 102 | 315 | | 395 | | 475 | ns | 2.0 | Fig.9 |
| | | | 37 | 63 | | 79 | | 95 | | 4.5 | |
| | | | 30 | 53 | | 40 | | 81 | | 6.0 | |
| $t_{PHL}$ | propagation delay $\overline{MR}$ to $\overline{TC}$ | | 83 | 275 | | 345 | | 415 | ns | 2.0 | Fig.9 |
| | | | 30 | 55 | | 69 | | 83 | | 4.5 | |
| | | | 24 | 47 | | 59 | | 71 | | 6.0 | |
| $t_{THL}/ t_{TLH}$ | output transition time | | 19 | 75 | | 95 | | 110 | ns | 2.0 | Figs 7 and 8 |
| | | | 7 | 15 | | 19 | | 22 | | 4.5 | |
| | | | 6 | 13 | | 16 | | 19 | | 6.0 | |
| $t_W$ | clock pulse width HIGH or LOW | 165 | 22 | | 205 | | 250 | | ns | 2.0 | Fig.7 |
| | | 33 | 8 | | 41 | | 50 | | | 4.5 | |
| | | 28 | 6 | | 35 | | 43 | | | 6.0 | |
| $t_W$ | master reset pulse width LOW | 125 | 39 | | 155 | | 190 | | ns | 2.0 | Fig.9 |
| | | 25 | 14 | | 31 | | 38 | | | 4.5 | |
| | | 21 | 11 | | 26 | | 32 | | | 6.0 | |
| $t_W$ | preset enable pulse width $\overline{PL}$; LOW | 125 | 33 | | 155 | | 190 | | ns | 2.0 | Fig.9 |
| | | 25 | 12 | | 31 | | 38 | | | 4.5 | |
| | | 21 | 10 | | 26 | | 32 | | | 6.0 | |
| $t_{rem}$ | removal time $\overline{MR}$ to CP or $\overline{PL}$ to CP | 50 | 14 | | 65 | | 75 | | ns | 2.0 | Fig.10 |
| | | 10 | 5 | | 13 | | 15 | | | 4.5 | |
| | | 9 | 4 | | 11 | | 13 | | | 6.0 | |
| $t_{su}$ | set-up time $\overline{PE}$ to CP | 75 | 22 | | 95 | | 110 | | ns | 2.0 | Fig.11 |
| | | 15 | 8 | | 19 | | 22 | | | 4.5 | |
| | | 13 | 6 | | 16 | | 19 | | | 6.0 | |

| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HC | | | | | | | | $V_{CC}$ (V) | WAVEFORMS |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| $t_{su}$ | set-up time $\overline{TE}$ to CP | 150 | 44 | | 190 | | 225 | | ns | 2.0 | Fig.11 |
| | | 30 | 16 | | 38 | | 45 | | | 4.5 | |
| | | 26 | 13 | | 33 | | 38 | | | 6.0 | |
| $t_{su}$ | set-up time $P_n$ to CP | 75 | 22 | | 95 | | 110 | | ns | 2.0 | Fig.12 |
| | | 15 | 8 | | 19 | | 22 | | | 4.5 | |
| | | 13 | 6 | | 16 | | 19 | | | 6.0 | |
| $t_h$ | hold time $\overline{PE}$ to CP | 0 | −14 | | 0 | | 0 | | ns | 2.0 | Fig.11 |
| | | 0 | −5 | | 0 | | 0 | | | 4.5 | |
| | | 0 | −4 | | 0 | | 0 | | | 6.0 | |
| $t_h$ | hold time $\overline{TE}$ to CP | 0 | −30 | | 0 | | 0 | | ns | 2.0 | Fig.11 |
| | | 0 | −11 | | 0 | | 0 | | | 4.5 | |
| | | 0 | −9 | | 0 | | 0 | | | 6.0 | |
| $t_h$ | hold time $P_n$ to CP | 0 | −17 | | 0 | | 0 | | ns | 2.0 | Fig.12 |
| | | 0 | −6 | | 0 | | 0 | | | 4.5 | |
| | | 0 | −5 | | 0 | | 0 | | | 6.0 | |
| $f_{max}$ | maximum clock pulse frequency | 3.0 | 10 | | 2.4 | | 2.0 | | MHz | 2.0 | Fig.7 |
| | | 15 | 29 | | 12 | | 10 | | | 4.5 | |
| | | 18 | 35 | | 14 | | 12 | | | 6.0 | |

### DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
$I_{CC}$ category: MSI

#### Note to HCT types

The value of additional quiescent supply current ($\Delta I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\Delta I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT | UNIT LOAD COEFFICIENT |
|---|---|
| CP, $\overline{PE}$ | 1.50 |
| $\overline{MR}$ | 1.00 |
| $\overline{TE}$ | 0.80 |
| $\overline{PL}$ | 0.35 |
| $P_n$ | 0.25 |

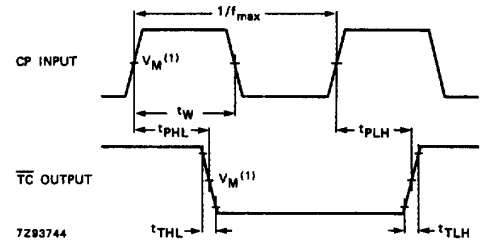
### AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; $C_L$ = 50 pF

| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HCT | | | | | | | | $V_{CC}$ (V) | WAVEFORMS |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| $t_{PHL}/ t_{PLH}$ | propagation delay CP to $\overline{TC}$ | | 35 | 60 | | 75 | | 90 | ns | 4.5 | Fig.7 |
| $t_{PHL}/ t_{PLH}$ | propagation delay $\overline{TE}$ to $\overline{TC}$ | | 23 | 40 | | 50 | | 60 | ns | 4.5 | Fig.8 |
| $t_{PHL}/ t_{PLH}$ | propagation delay $\overline{PL}$ to $\overline{TC}$ | | 44 | 75 | | 94 | | 112 | ns | 4.5 | Fig.9 |
| $t_{PHL}$ | propagation delay $\overline{MR}$ to $\overline{TC}$ | | 29 | 55 | | 69 | | 83 | ns | 4.5 | Fig.9 |
| $t_{THL}/ t_{TLH}$ | output transition time | | 7 | 15 | | 19 | | 22 | ns | 4.5 | Figs. 7 and 8 |
| $t_W$ | clock pulse width HIGH or LOW | 33 | 10 | | 41 | | 50 | | ns | 4.5 | Fig.7 |
| $t_W$ | master reset pulse width LOW | 30 | 16 | | 38 | | 45 | | ns | 4.5 | Fig.9 |
| $t_W$ | preset enable pulse width $\overline{PL}$; LOW | 38 | 22 | | 48 | | 57 | | ns | 4.5 | Fig.9 |
| $t_{rem}$ | removal time $\overline{MR}$ to CP or $\overline{PL}$ to CP | 10 | 1 | | 13 | | 15 | | ns | 4.5 | Fig.10 |
| $t_{su}$ | set-up time $\overline{PE}$ to CP | 20 | 11 | | 25 | | 30 | | ns | 4.5 | Fig.11 |
| $t_{su}$ | set-up time $\overline{TE}$ to CP | 40 | 20 | | 50 | | 60 | | ns | 4.5 | Fig.11 |

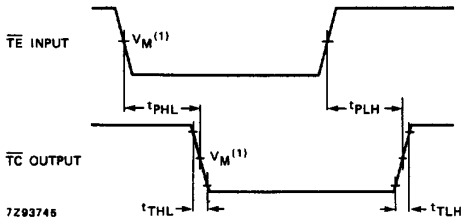
| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HCT | | | | | | | | $V_{CC}$ (V) | WAVEFORMS |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| $t_{su}$ | set-up time $P_n$ to CP | 20 | 11 | | 25 | | 30 | | ns | 4.5 | Fig.12 |
| $t_h$ | hold time $\overline{PE}$ to CP | 2 | –3 | | 2 | | 2 | | ns | 4.5 | Fig.11 |
| $t_h$ | hold time $\overline{TE}$ to CP | 0 | –10 | | 0 | | 0 | | ns | 4.5 | Fig.11 |
| $t_h$ | hold time $P_n$ to CP | 0 | –5 | | 0 | | 0 | | ns | 4.5 | Fig.12 |
| $f_{max}$ | maximum clock pulse frequency | 15 | 28 | | 12 | | 10 | | MHz | 4.5 | Fig.7 |

## AC WAVEFORMS



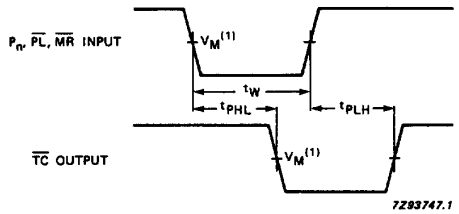

(1) HC : $V_M$ = 50%; $V_I$ = GND to $V_{CC}$.
HCT: $V_M$ = 1.3 V; $V_I$ = GND to 3 V.

Fig.7 Waveforms showing the clock input (CP) to $\overline{TC}$ propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.



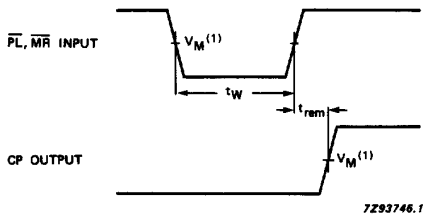

(1) HC : $V_M$ = 50%; $V_I$ = GND to $V_{CC}$.
HCT: $V_M$ = 1.3 V; $V_I$ = GND to 3 V.

Fig.8 Waveforms showing the $\overline{TE}$ to $\overline{TC}$ propagation delays.



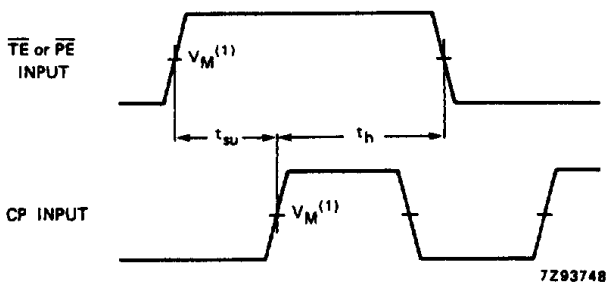

(1) HC : $V_M$ = 50%; $V_I$ = GND to $V_{CC}$.
HCT: $V_M$ = 1.3 V; $V_I$ = GND to 3 V.

Fig.9 Waveforms showing $\overline{PL}$, $\overline{MR}$, $P_n$ to $\overline{TC}$ propagation delays.



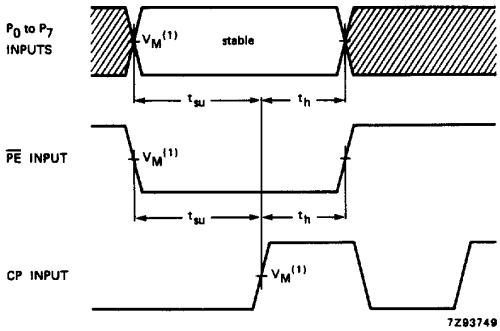

(1) HC : $V_M$ = 50%; $V_I$ = GND to $V_{CC}$.
HCT: $V_M$ = 1.3 V; $V_I$ = GND to 3 V.

Fig.10 Waveforms showing removal time for $\overline{MR}$ and $\overline{PL}$.




(1) HC : $V_M$ = 50%; $V_I$ = GND to $V_{CC}$.
HCT: $V_M$ = 1.3 V; $V_I$ = GND to 3 V.

Fig.11 Waveforms showing hold and set-up times for $\overline{MR}$ or $\overline{PE}$ to CP.




The shaded areas indicate when the input is permitted to change for predictable output performance.

(1) HC : $V_M$ = 50%; $V_I$ = GND to $V_{CC}$.
HCT: $V_M$ = 1.3 V; $V_I$ = GND to 3 V.

Fig.12 Waveforms showing hold and set-up times for $P_n$, $\overline{PE}$ to CP.

## APPLICATION INFORMATION

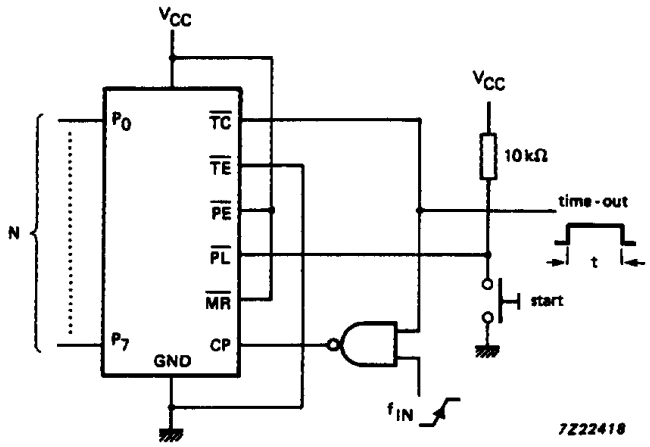



Fig.13 Programmable timer.

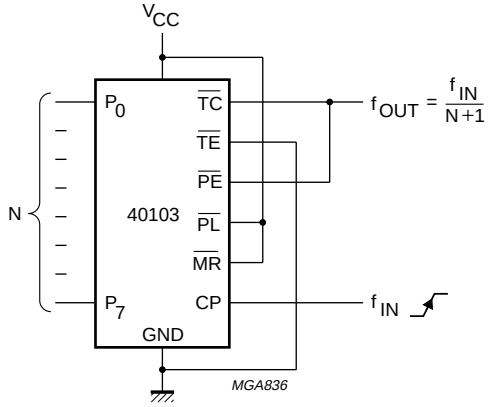
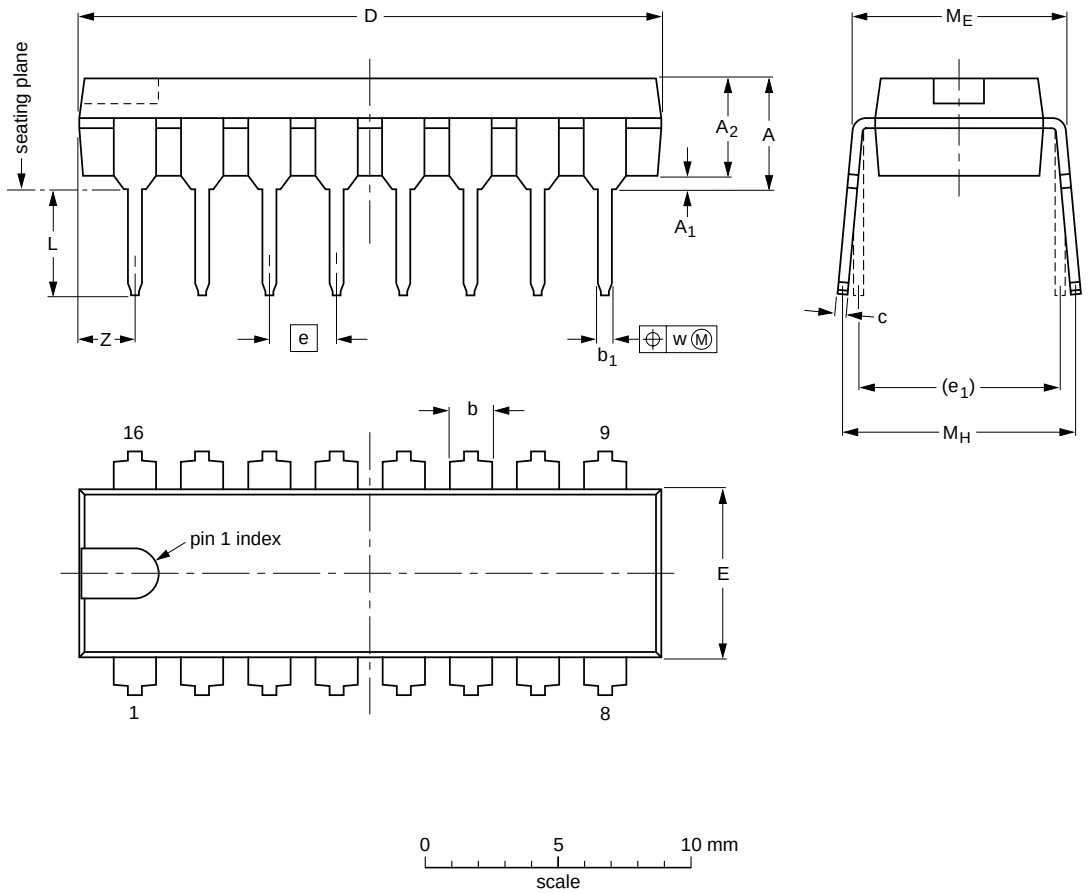



Fig.14 Divide-by-N counter.

## PACKAGE OUTLINES

**DIP16: plastic dual in-line package; 16 leads (300 mil); long body** **SOT38-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

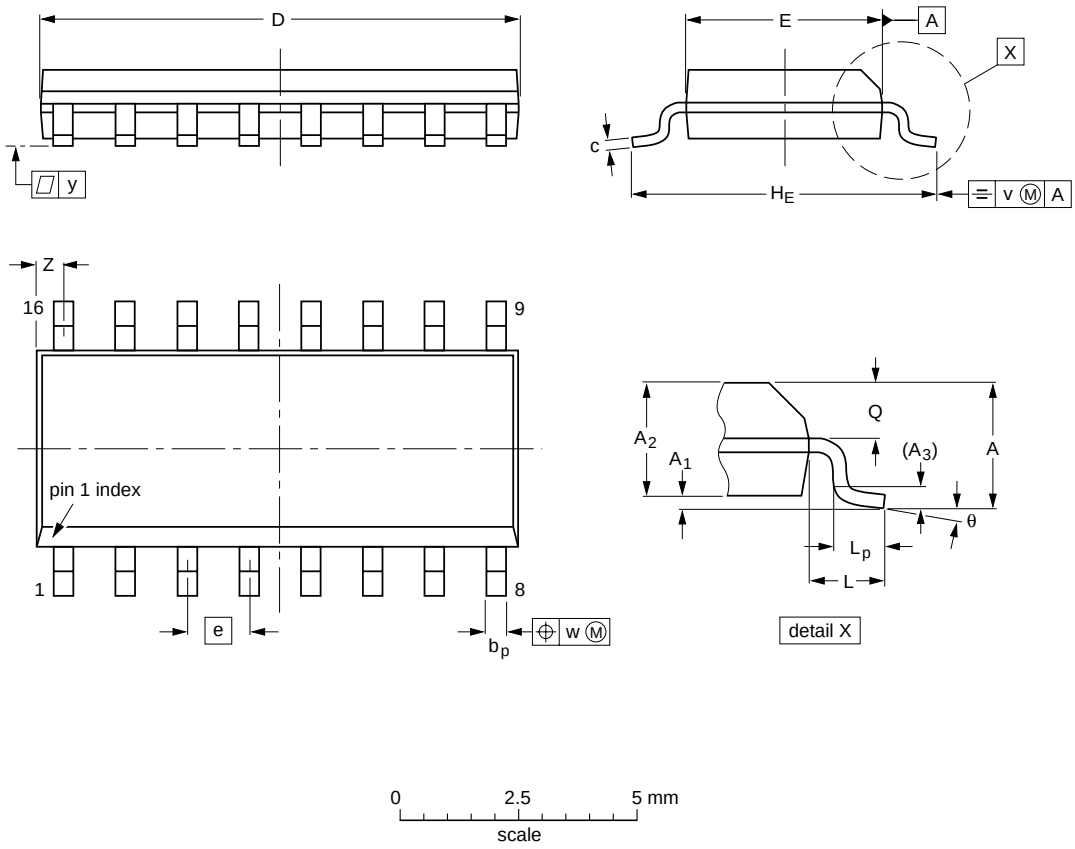
| UNIT | A max. | $A_1$ min. | $A_2$ max. | b | $b_1$ | c | D (1) | E (1) | e | $e_1$ | L | $M_E$ | $M_H$ | w | Z (1) max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.7 | 0.51 | 3.7 | 1.40<br>1.14 | 0.53<br>0.38 | 0.32<br>0.23 | 21.8<br>21.4 | 6.48<br>6.20 | 2.54 | 7.62 | 3.9<br>3.4 | 8.25<br>7.80 | 9.5<br>8.3 | 0.254 | 2.2 |
| inches | 0.19 | 0.020 | 0.15 | 0.055<br>0.045 | 0.021<br>0.015 | 0.013<br>0.009 | 0.86<br>0.84 | 0.26<br>0.24 | 0.10 | 0.30 | 0.15<br>0.13 | 0.32<br>0.31 | 0.37<br>0.33 | 0.01 | 0.087 |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT38-1 | 050G09 | MO-001AE | | | | ~~92-10-02~~<br>95-01-19 |

**SO16: plastic small outline package; 16 leads; body width 3.9 mm** **SOT109-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

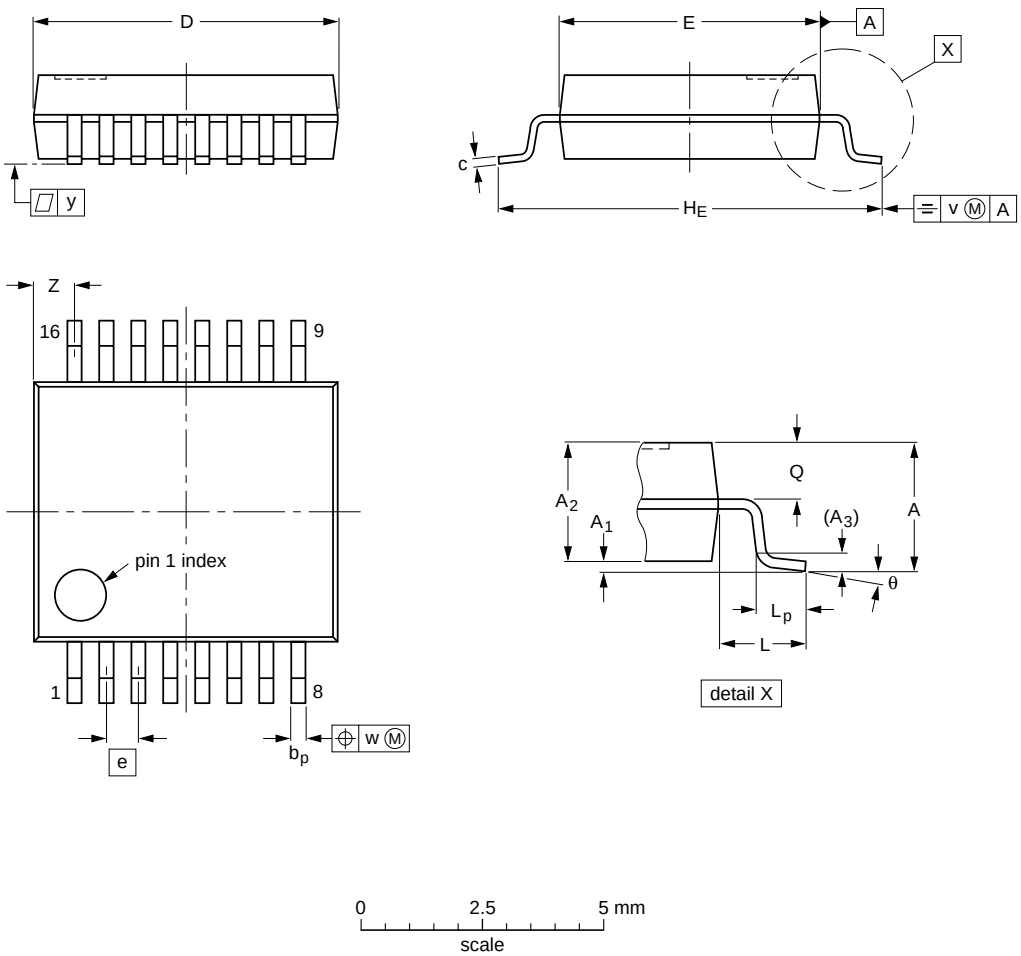
| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 10.0<br>9.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.39<br>0.38 | 0.16<br>0.15 | 0.050 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.020 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT109-1 | 076E07S | MS-012AC | | | | ~~95-01-23~~<br>97-05-22 |

**SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm** **SOT338-1**




**DIMENSIONS (mm are the original dimensions)**

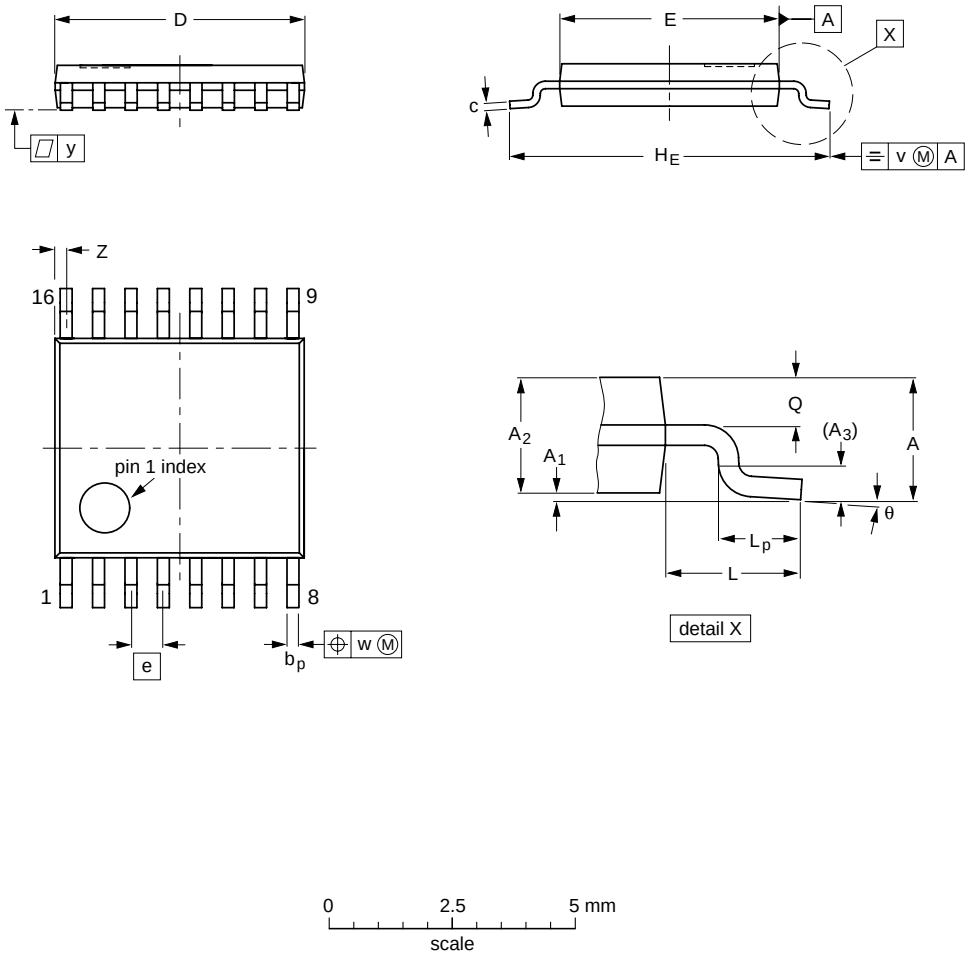
| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.0 | 0.21<br>0.05 | 1.80<br>1.65 | 0.25 | 0.38<br>0.25 | 0.20<br>0.09 | 6.4<br>6.0 | 5.4<br>5.2 | 0.65 | 7.9<br>7.6 | 1.25 | 1.03<br>0.63 | 0.9<br>0.7 | 0.2 | 0.13 | 0.1 | 1.00<br>0.55 | $8^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT338-1 | | MO-150AC | | | | ~~94-01-14~~<br>95-02-04 |

**TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm** **SOT403-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.10 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 5.1<br>4.9 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1.0 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.40<br>0.06 | $8^o$<br>$0^o$ |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT403-1 | | MO-153 | | | | ~~94-07-12~~<br>95-04-04 |

## SOLDERING

### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

### DIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

### SO, SSOP and TSSOP

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO, SSOP and TSSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method.

Typical reflow temperatures range from 215 to 250 °C. Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering can be used for all SO packages. Wave soldering is **not** recommended for SSOP and TSSOP packages, because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering is used - **and cannot be avoided for SSOP and TSSOP packages** - the following conditions must be observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.

**Even with these conditions:**

- **Only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).**
- **Do not consider wave soldering TSSOP packages with 48 leads or more, that is TSSOP48 (SOT362-1) and TSSOP56 (SOT364-1).**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally- opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## DEFINITIONS

| **Data sheet status** | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| **Limiting values** | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| **Application information** | |
| Where application information is given, it is advisory and does not form part of the specification. | |

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