Digital Sound Processors for FPD TVs

28bit Audio DSP with Built-in 2ch ADC, 6ch DAC and ASRC

BD9406KS2

No.12083EAT01

●General Description

This LSI is the digital sound processor which made the use digital signal processing for FPD TVs.
DSP of ROHM original is used for the TV sound processor unit, and it excels in cost performance.
The asynchronous sampling rate converter is built in the digital input one line. The audio AD converter is built in the analog input one line. The audio DA converters are built in the output three lines.

●Features

■ Digital Signal Processor unit

Word length:	28bit (Data RAM)
The fastest machine Cycle:	40.7ns (512fs, fs=48kHz)
Multiplier:	28x24 → 52 bit
Adder:	28+28 → 28bit
Data RAM:	256x28bit
Coefficient RAM:	128x24bit
Sampling Frequency:	fs=48kHz
Master Clock:	512fs (24.576Mhz, fs=48kHz)

■ Digital Signal Input (Stereo 4 lines): 16/20/24bit (I^2S, Left-Justified, Right-Justified)
Digital Signal Output (Stereo 4 lines): 16/20/24bit (I^2S, Left-Justified, Right-Justified, S/PDIF)

■ Asynchronous Sampling Rate Converter (Stereo 1 line): 32kHz/44.1kHz → 48kHz

■ Audio ADC: Stereo Input 1 line
20bit 64 x Over-sampling sigma delta ADC
S/N: 90dB
THD+N: 0.02% (Sine-wave 1kHz, -0.5dB)
Digital HPF (fc=1Hz)

■ Audio DAC: Stereo Output 2 lines
24bit 8x Over-sampling digital filter + 1bit sigma delta DAC
S/N: 96dB
THD+N: 0.005% (Sine-wave 1kHz, 0dB)

■ Audio 16bit DAC: Stereo Output 1 line
24bit 8x Over-sampling digital filter + Audio 16bit DAC
S/N: 90dB
THD+N: 0.03% (Sine-wave 1kHz, 0dB)

■ The sound signal processing function for FPD TVs
Pre-scaler, Channel Mixer, Pseudo Stereo, Surround, P^2Bass, SAS,12-band parametric EQ, Master Volume, L/R Balance, Compression, Post-scaler, Output Signal Clipper
(P^2Bass and SAS are ROHM's own sound effect functions.)

●Applications

Flat Panel TVs (LCD, Plasma)

●Absolute Maximum Ratings (Ta=25℃)

Item	Symbol	Rating	Unit
Power Supply Voltage	V_{DD}	4.5	V
Power Dissipation	P_d	950 (※1)	mW
Operating Temperature Range	T_{opr}	-40～+85	℃
Storage Temperature Range	T_{stg}	-55～+125	℃

*1 Use of this processor at Ta=25℃ and over is subject to reduction of 9.5mW per 1 .

*2Operation is not guaranteed.

●Recommendation Operating range (Ta=-40～+85℃)

Item	Symbol	Rating	Unit
Power Supply Voltage	V_{DD}	3.0～3.6	V

*1This product is not designed for protection against radioactive rays.

●Electrical Characteristics (Digital system)

V_{DD}=3.3V (Unless otherwise specified Ta=25℃)

Item		Symbol	Limit			Unit	Conditions	Relevant Pins
			Min.	Typ.	Max.			
Input Voltage	H-level Voltage	V_{IH}	2.3	-	-	V		*1
	L-level Voltage	V_{IL}	-	-	1.0	V		*1
Hysteresis Input Voltage	H-level Voltage	V_{IH}	2.5	-	-	V		*2,3,4
	L-level Voltage	V_{IL}	-	-	0.8	V		*2,3,4
Input Current		I_I	-	-	±1	μA	V_{IN}=0～3.3V	*1,2
Input L Current to Pull-up Resistor		I_{IL}	-150	-100	-50	μA	V_{IN}=0V	*3
Input H Current to Pull-down Resistor		I_{IH}	35	70	105	μA	V_{IN}=3.3V	*4
Output Voltage	H-level Voltage	V_{OH}	2.75	-	-	V	I_O=-0.6mA	*5
	L-level Voltage	V_{OL}	-	-	0.55	V	I_O=0.6mA	*5

Relevant Pins

*1 CMOS input pin
XI (pin 60)

*2 CMOS hysteresis input pin
MODE (pin 2), SCANTEST (pin 3), SDA (pin 4), SCL (pin 5)

*3 CMOS hysteresis input pin with built-in pull-up resistance
RESETB (pin 8), DATAI1 (pin 52), BCKI1 (pin 53), LRCKI1 (pin 54), DATAI2 (pin 55), BCKI2 (pin 56), LRCKI2 (pin 57), DATAI3 (pin 58), BCKI3 (pin 63), LRCKI3 (pin 64), DATAI4 (pin 65), BCKI4 (pin 66), LRCKI4 (pin 67), AMCLKI1 (pin 68), AMCLKI2 (pin 69), AMCLKI3 (pin 75), AMCLKI4S (pin 76)

*4 CMOS input pin with built-in pull-down resistance
I2CADR1 (pin 6), I2CADR2 (pin 7)

*5 CMOS output pin
SDA (pin 4), ERROR (pin 39), DATAOC (pin 42), BCKOC (pin 43), LRCKOC (pin 44), DATAOB (pin 45), BCKOB (pin 46), LRCKOB (pin 47), DATAOA (pin 48), BCKOA (pin 49), LRCKOA (pin 50), XO (pin 61), AMCLKI4S (pin 76), AMCLKOA (pin 77), AMCLKOB (pin 78), AMCLKOC (pin 79)

●Electrical Characteristics (Analog system)

V_{DD}=3.3V (Unless otherwise specified Ta=25℃, R_L=10kΩ, Standard $V_{C)}$

Item	Symbol	Standard Values			Unit	Applicable Pins/Conditions
		Min.	Typ.	Max.		
Total						
Circuit Current	I_Q	-	60	90	mA	DVDDIO1,DVDDIO2,DVDDIO3,DVDDREG, DVDDPLL,AVDDAD1,ADVDDAD2, AVDDDA1,AVDDDAR2,AVDDDAL2, AVDDDAR3,AVDDDAL3
Regulator						
Output Voltage	V_{REG}	-	1.5	-	V	I_O=100mA
PLL_ASRC						
Lock Frequency (8 times frequency multiplier)	F_{LK8}	-	24.576	-	MHz	BCK=3.072MHz (fs=48kHz)
Sigma-delta audio ADC						
Maximum Input Amplitude	V_{IMAX}	-	-	0.7	Vrms	
Distortion rate(THD+N)	THD_{AD}	-	0.02	0.05	%	1kHz, -0.5dB
S/N	S/N_{AD}	-	90	-	dB	AIN=0.7Vrms,1kHz,A-weighted
Input Impedance	R_I	42	60	78	kΩ	
Sigma-delta audio DAC						
Maximum Output Amplitude	V_{OMAX}	0.63	0.75	0.86	Vrms	
Distortion rate(THD+N)	THD_{DA}	-	0.005	0.03	%	0dB,1kHz
S/N	S/N_{DA}	-	96	-	dB	0dB,1kHz,A-weighted
16bit DAC Section						
Maximum Output Amplitude	V_{OMAX}	0.65	0.77	0.88	Vrms	
Distortion rate(THD+N)	THD_{DA}	-	0.03	-	%	0dB,1kHz
S/N	S/N_{DA}	-	90	-	dB	0dB,1kHz,A-weighted

●Block diagram

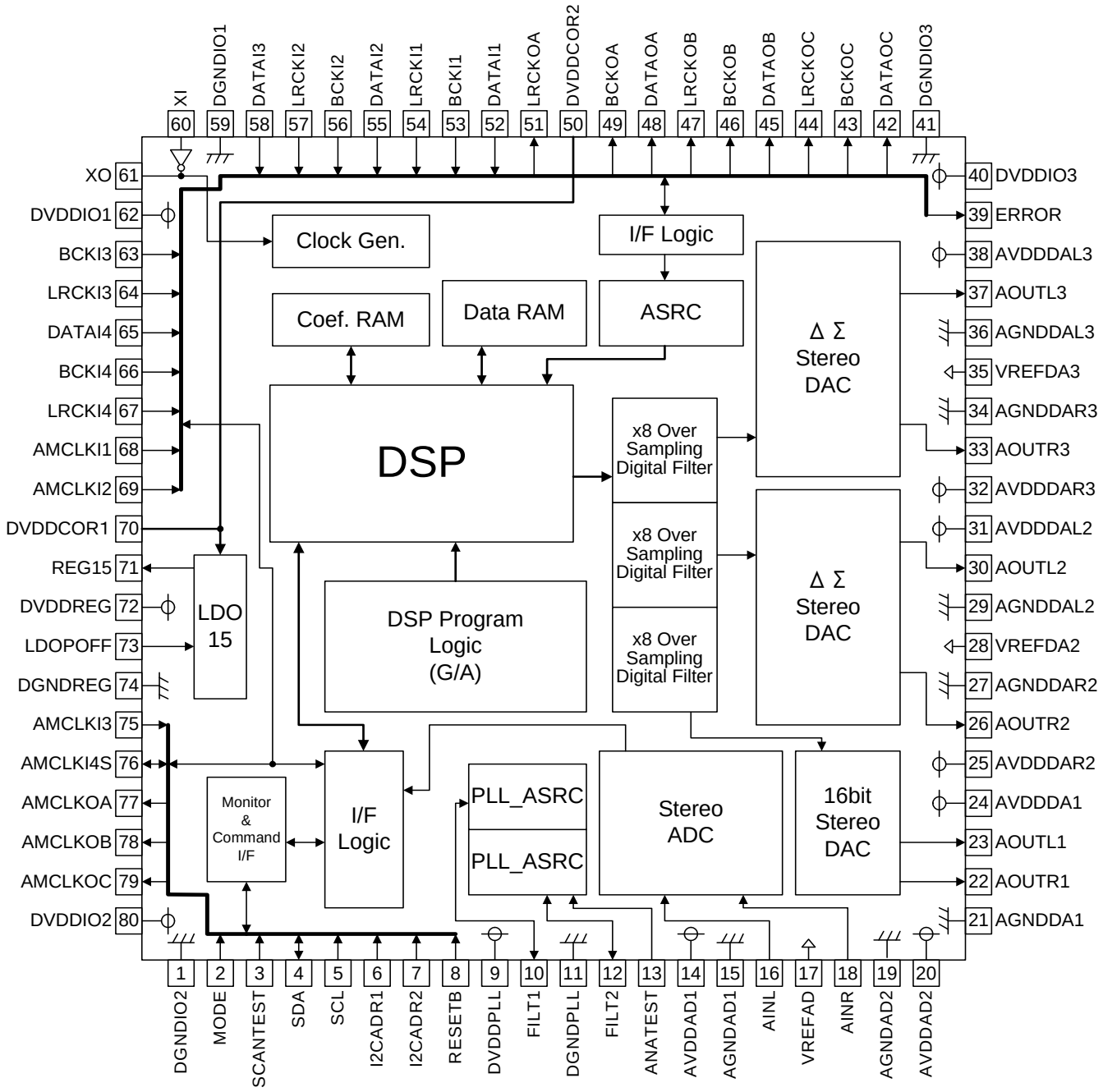
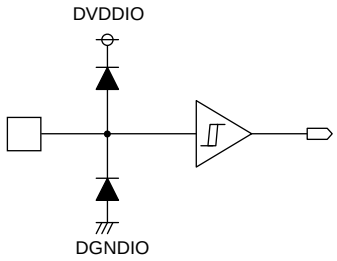
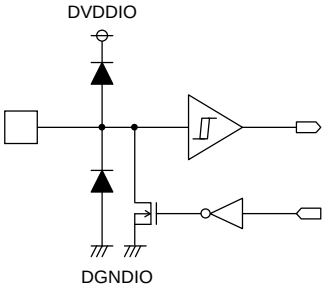
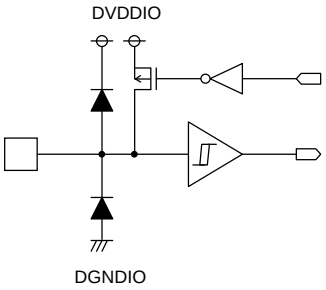
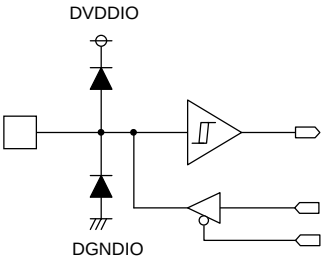
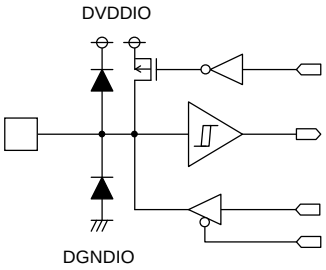
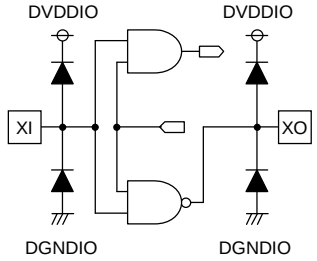


Fig.2 Block diagram

●Pin Description(s)

No.	Name	Description of terminals	Type
1	DGNDIO2	Digital I/O GND2	—
2	MODE	Test mode select pin	A
3	SCANTEST	Digital test mode select pin	A
4	SDA	I^2C data I/O pin	D
5	SCL	I^2C transfer clock input pin	D
6	I2CADR1	I^2C slave address select pin 1	B
7	I2CADR2	I^2C slave address select pin 2	B
8	RESETB	“L” -> Reset condition	C
9	DVDDPLL	PLL power supply	—
10	FILT1	PLL_ASRC filter connect terminal 1	G
11	DGNDPLL	PLL GND	—
12	FILT2	PLL_ASRC filter connect terminal 2	G
13	ANATEST	Analog test mode select pin	G
14	AVDDAD1	Audio ADC power supply 1	—
15	AGNDAD1	Audio ADC GND 1	—
16	AINL	Analog signal Lch input pin	G
17	VREFAD	ADC reference voltage pin	G
18	AINR	Analog signal Rch input pin	G
19	AGNDAD2	Audio ADC GND 2	—
20	AVDDAD2	Audio ADC power supply 2	—
21	AGNDDA1	Audio DAC GND 1	—
22	AOUTR1	Audio DAC Rch output pin 1	G
23	AOUTL1	Audio DAC Lch output pin 1	G
24	AVDDDA1	Audio DAC power supply 1	—
25	AVDDDAR2	Audio DAC Rch power supply 2	—
26	AOUTR2	Audio DAC Rch output pin 2	G
27	AGNDDAR2	Audio DAC Rch GND 2	—
28	VREFDA2	DAC reference voltage 2	G
29	AGNDDAL2	Audio DAC Lch GND 2	—
30	AOUTL2	Audio DAC Lch output pin 2	G
31	AVDDDAL2	Audio DAC Lch power supply 2	—
32	AVDDDAR3	Audio DAC Rch power supply 3	—
33	AOUTR3	Audio DAC Rch output pin3	G
34	AGNDDAR3	Audio DAC Rch GND 3	—
35	VREFDA3	DAC reference voltage 3	G
36	AGNDDAL3	Audio DAC Lch GND 3	—
37	AOUTL3	Audio DAC Lch output pin 3	G
38	AVDDDAL3	Audio DAC Lch power supply 3	—
39	ERROR	Sampling frequency input error pin	D
40	DVDDIO3	Digital I/O power supply 3	—
41	DGNDIO3	Digital I/O GND 3	—
42	DATAOC	I^2S audio data output C	D
43	BCKOC	I^2S audio bit transfer clock output C	D
44	LRCKOC	I^2S audio LR sampling clock output C	D
45	DATAOB	I^2S audio data output B	D
46	BCKOB	I^2S audio bit transfer clock output B	D
47	LRCKOB	I^2S audio LR sampling clock output B	D
48	DATAOA	I^2S audio data output A	D
49	BCKOA	I^2S audio bit transfer clock output A	D
50	DVDDCOR2	Connects with REG15 Pin	—
51	LRCKOA	I^2S audio LR sampling clock output A	D
52	DATAI1	I^2S audio data input 1	E
53	BCKI1	I^2S audio bit transfer clock input 1	E
54	LRCKI1	I^2S audio LR sampling clock input 1	E
55	DATAI2	I^2S audio data input 2	E
56	BCKI2	I^2S audio bit transfer clock input 2	E
57	LRCKI2	I^2S audio LR sampling clock input 2	E
58	DATAI3	I^2S audio data input 3	E
59	DGNDIO1	Digital I/O GND1	—
60	XI	X’tal connecting (input) terminal	F
61	XO	X’tal connecting terminal	F
62	DVDDIO1	Digital I/O power supply 1	—
63	BCKI3	I^2S audio bit transfer clock input 3	E
64	LRCKI3	I^2S audio LR sampling clock input 3	E
65	DATAI4	I^2S audio data input 4	E
66	BCKI4	I^2S audio bit transfer clock input 4	E
67	LRCKI4	I^2S audio LR sampling clock input 4	E
68	AMCLKI1	I^2S synchronous clock input 1	E
69	AMCLKI2	I^2S synchronous clock input 2	E
70	DVDDCOR1	Connects with REG15 Pin	—
71	REG15	Built in regulator voltage output	G
72	DVDDREG	Power supply for built in regulator	—
73	LDOPOFF	Power off signal input for regulator	G
74	DGNDREG	GND for built in regulator	—
75	AMCLKI3	I^2S synchronous clock input 3	E
76	AMCLKI4S	I^2S synchronous clock Input 4 or S/PDIF output	E
77	AMCLKOA	I^2S synchronous clock output A	D
78	AMCLKOB	I^2S synchronous clock output B	D
79	AMCLKOC	I^2S synchronous clock output C	D
80	DVDDIO2	Digital I/O power supply 2	—

● **Pin Equivalent Circuit Diagrams**

A	B	C
		
D	**E**	**F**
		
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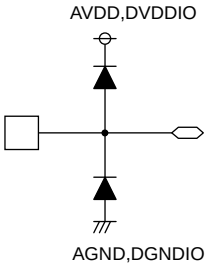
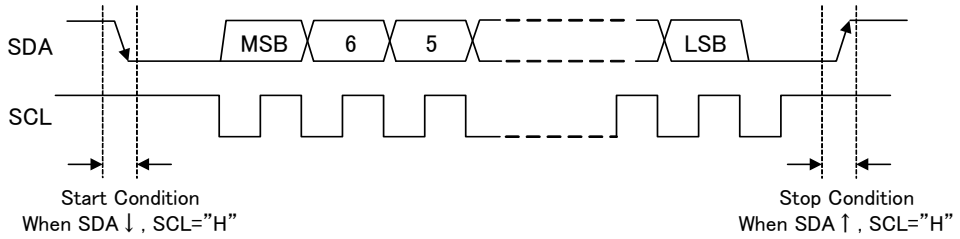
		

1. Command Interface

BU9406KS2 uses the I^2C bus format for the command interface with the host CPU.
With BU9406KS2, in addition to write mode, read mode read-out is possible with many registers.
BU9406KS2 assigns a 1-byte select address in addition to the slave address and performs write-in and read-out.
The I^2C bus slave mode format is as follows:

	MSB LSB		MSB LSB		MSB LSB		
S	Slave Address	A	Select Address	A	Data	A	P

S: Start Condition
Slave Address: Adds either a read mode (H") or write mode (L") bit to the slave address (7bit) configured by I2CADR1 and I2CADR2, sending a total of 8 bits of data. (MSB first)
A: Acknowledge An acknowledge bit is added on to each bit of data transmitted.
When data transmission is being done correctly, "L" is transmitted.
"H" transmission means there was no acknowledge.
Select Address: BU9406KS2 uses a 1-byte select address. (MSB first)
Data: Data byte, transmitted data (MSB first)
P: Stop condition



1-1. Data Write-In

S	Slave Address	A	Select Address	A	Data	A	P

: Master to Slave : Slave to Master

MSB LSB

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	0	0

Slave Address Configuration for BU9406KS2

Pin Configuration		Write Mode
I2CADR2	I2CADR1	Slave Address
0	0	80h
0	1	82h
1	0	84h
1	1	86h

S	Slave Address	A	Select Address	A	Data	A	Data	A	Data	A	P
(Ex.)	80h		20h		00h		00h		00h		

: Master to Slave : Slave to Master

Write-in Procedure

Step	Clock	Master	Slave(BU9406KS2)	Note
1		Start Condition		
2	7	Slave Address		&h80 (&h82, &h84, &h86)
3	1	R/W (0)		
4	1		Acknowledge	
5	8	Select Address		Write-in target register: 8bit
6	1		Acknowledge	
7	8	Data		8bit write-in data
8	1		Acknowledge	
9		Stop Condition		

○When transmitting continuous data, the auto-increment function moves the select address up by one.
Repeat steps 7 and 8.

1-2. Data Read-out

During read-out, the corresponding read-out address is first written into the &hD0 address register (&h20h in the example). In the following stream, the data is read out after the slave address. Do not return an acknowledge after completing the reception.

S	Slave Address	A	Request Address	A	Select Address	A	P
(ex.)	80h		D0h		20h		

S	Slave Address	A	Data 1	A	Data 2	A		A	Data N	Ā	P
(ex.)	81h		**h		**h				**h		

: Master to Slave, : Slave to Master, A: With acknowledge, Ā: Without acknowledge

Read-out Procedure

Step	Clock	Master	Slave(BU9406KS2)	Note
1		Start Condition		
2	7	Slave Address		&h80 (&h82, &h84, &h86)
3	1	R/W (0)		
4	1		Acknowledge	
5	8	Request Address		I^2C read-out address &hD0
6	1		Acknowledge	
7	8	Select Address		Read-out target register: 8bit
8	1		Acknowledge	
9	1	Stop Condition		
10	1	Start Condition		
11	7	Slave Address		&h81 (&h82, &h85, &h87)
12	1	R/W (1)		
13	1		Acknowledge	
14	8		Data	8bit read-out data
15	1	Acknowledge		
16		**Stop Condition**		

○When transmitting continuous data, the auto-increment function moves up the select address by one.
Repeat steps 14 and 15.

1-3. Control Signal Specifications

○ Electrical Characteristics and Timing for Bus Line and I/O Stage

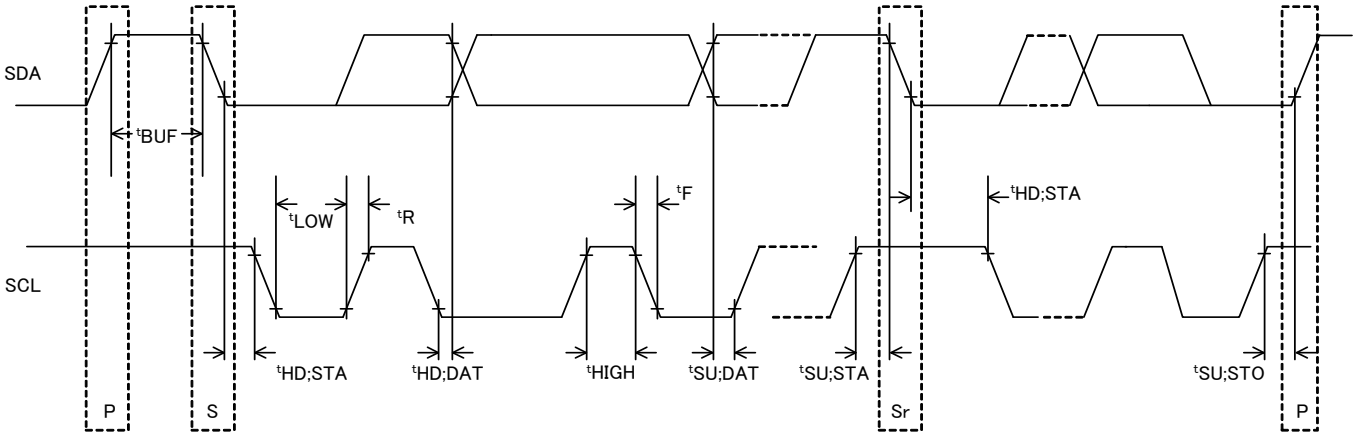


Fig.1-1: Timing Chart

Chart 1-1: SDA and SCL Bus Line Characteristics (Unless specified, Ta=25℃ and V_{DD}=3.3V)

Parameters		Symbol	High-Speed Mode		Unit
			Min.	Max.	
1	SCL clock frequency	fSCL	0	400	kHz
2	Bus free time between “stop” condition and “start” condition	t_{BUF}	1.3	—	μS
3	Hold time (re-transmit) “start” condition. After this period, the first clock pulse is generated.	$t_{HD;STA}$	0.6	—	μS
4	SCL clock LOW state hold time	t_{LOW}	1.3	—	μS
5	SCL clock HIGH state hold time	t_{HIGH}	0.6	—	μS
6	Re-transmit set-up time of “start” condition	$t_{SU;STA}$	0.6	—	μS
7	Data hold time	$t_{HD;DAT}$	0[1)]	—	μS
8	Data setup time	$t_{SU;DAT}$	100	—	ns
9	SDA and SCL signal stand-up time	t_R	20+Cb	300	ns
10	SDA and SCL signal stand-down time	t_F	20+Cb	300	ns
11	Set-up time for “stop” condition	$t_{SU;STO}$	0.6	—	μS
12	Each bus line’s capacitive load	Cb	—	400	pF

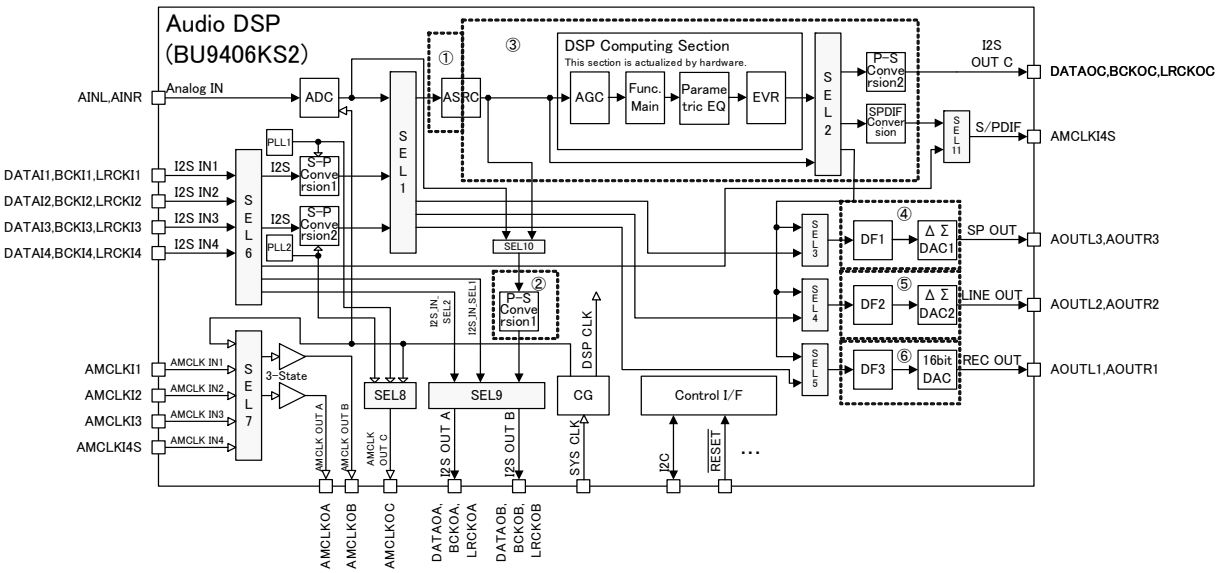
The values above correspond with $V_{IH\ min}$ and $V_{IL\ max}$ levels.

1) Because the transmission device exceeds the undefined domain of the SCL fall edge, it is necessary to internally provide a minimum 300ns
hold time for the SDA signal (of $V_{IH\ min}$ of SCL signal).

The characteristics above are logical values for design; guarantees in the form of delivery inspections are not offered.
In the event of a problem, comprehensive consultation and support will be provided.

2. Data and Clock Switching

Below is the in/output system diagram for BU9406KS2.



BU9406KS2 has a 4-line digital stereo input, 1-line analog stereo input, 4-line digital stereo output and 3-line analog stereo output.

The digital data input to the DSP computing section is first changed to fs=48kHz data at the ASRC (asynchronous sampling rate converter).

DSP computing section output is changed to either I^2S format digital output, S/PDIF format digital serial output or analog output.

2-1. ASRC Input Selection (SEL1)

Default = 0

Select Address	Value	Operation Description
&h03 [5 : 4]	0	Inputs analog signals converted to digital data
	1	Inputs via S-P conversion 1 (refer to &h05[5:4])
	2	Inputs via S-P conversion 2 (refer to &h05[1:0])

S-P conversions 1 and 2 convert I^2C format serial data to 24bit parallel data.

2-2. DF1 Input Selection (SEL1, SEL2, SEL3)

Default = 0

Select Address	Value	Operation Description
&h03 [2 : 0]	0	Inputs analog signals converted to digital data
	1	Inputs via S-P conversion 1 (refer to &h05[5:4])
	2	Inputs via S-P conversion 2 (refer to &h05[1:0])
	3	Inputs data before DSP processing
	4	Inputs data after DSP processing

2-3. DF2 Input Selection (SEL1, SEL2, SEL4)

Default = 0

Select Address	Value	Operation Description
&h04 [6 : 4]	0	Inputs analog signals converted to digital data
	1	Inputs via S-P conversion 1 (refer to &h05[5:4])
	2	Inputs via S-P conversion 2 (refer to &h05[1:0])
	3	Inputs data before DSP processing
	4	Inputs data after DSP processing

2-4. DF3 Input Selection (SEL1, SEL2, SEL5)

Default = 0

Select Address	Value	Operation Description
&h04 [2 : 0]	0	Inputs analog signals converted to digital data
	1	Inputs via S-P conversion 1 (refer to &h05[5:4])
	2	Inputs via S-P conversion 2 (refer to &h05[1:0])
	3	Inputs data before DSP processing
	4	Inputs data after DSP processing

2-5. S-P Conversion 1 Input Selection (SEL6)

Default = 0

Select Address	Value	Operation Description
&h05 [5 : 4]	0	Inputs data from I2S_IN1
	1	Inputs data from I2S_IN2
	2	Inputs data from I2S_IN3
	3	Inputs data from I2S_IN4

2-6. S-P Conversion 2 Input Selection (SEL6)

Default = 0

Select Address	Value	Operation Description
&h05 [1 : 0]	0	Inputs data from I2S_IN1
	1	Inputs data from I2S_IN2
	2	Inputs data from I2S_IN3
	3	Inputs data from I2S_IN4

2-7. Clock Output Selection (SEL&) to AMCLKOA Pin

Default = 0

Select Address	Value	Operation Description
&h06 [6 : 4]	0	Outputs Hi-z
	1	Outputs 256fs (12.288MHz) clock used in DSP
	2	Outputs clock from AMCLK_IN1
	3	Outputs clock from AMCLK_IN2
	4	Outputs clock from AMCLK_IN3
	5	Outputs clock from AMCLK_IN4

2-8. Clock Output Selection to AMCLKOB Pin (SEL7)

Default = 0

Select Address	Value	Operation Description
&h06 [2 : 0]	0	Outputs Hi-z
	1	Outputs 256fs (12.288MHz) clock used in DSP
	2	Outputs clock from AMCLK_IN1
	3	Outputs clock from AMCLK_IN2
	4	Outputs clock from AMCLK_IN3
	5	Outputs clock from AMCLK_IN4

2-9. Clock Output Selection to AMCLKOC Pin (SEL8)

Default = 0

Select Address	Value	Operation Description
&h07 [5 : 4]	0	Outputs 256fs (12.288MHz) clock used in DSP
	1	Outputs 256fs clock extracted by S-P conversion 1 PLL1
	2	Outputs 256fs clock extracted by S-P conversion 2 PLL2

2-10. Output Selection to DATAOA Pin (SEL6, SEL9)

Default = 0

Select Address	Value	Operation Description
&h08 [6 : 4]	0	Outputs data from I2S_IN1
	1	Outputs data from I2S_IN2
	2	Outputs data from I2S_IN3
	3	Outputs data from I2S_IN4
	4	Outputs data from P-S conversion 1 (refer to &h09[7])

P-S conversion 1 converts 24bit parallel data to I^2C format serial data.

2-11. Output Selection to DATAOB Pin (SEL6, SEL9)

Default = 0

Select Address	Value	Operation Description
&h08 [2 : 0]	0	Outputs data from I2S_IN1
	1	Outputs data from I2S_IN2
	2	Outputs data from I2S_IN3
	3	Outputs data from I2S_IN4
	4	Outputs data from P-S conversion 1 (refer to &h09[7])

2-12. Output Selection to DATAOC Pin (SEL2)

Default = 0

Select Address	Value	Operation Description
&h09 [4]	0	Inputs data before DSP processing
	1	Outputs data after DSP processing

2-13. Input Selection to P-S Conversion 1 (SEL10)

Default = 0

Select Address	Value	Operation Description
&h09 [7]	0	Outputs data from AD conversion
	1	Outputs data after conversion to fs=48kHz at ASRC

2-15. Output Selection When Configuring AMCLK4S Pin to S/PDIF Output (SEL2, SEL6, SEL11)

Default = 0

Select Address	Value	Operation Description
&h09 [2 : 0]	0	Inputs data before DSP processing
	1	Outputs data after DSP processing
	2	Outputs data from I2S_IN1 (Only output data in S/PDIF format)
	3	Outputs data from I2S_IN2 (Only output data in S/PDIF format)
	4	Outputs data from I2S_IN3 (Only output data in S/PDIF format)
	5	Outputs data from I2S_IN4 (Only output data in S/PDIF format)

2-16. AMCLK4S Pin In/Output Switching (SEL2)

Default = 0

Select Address	Value	Operation Description
&h09 [3]	0	Clock input
	1	S/PDIF data output (refer to &h11, &h12 and &h13)

There are three types of system clocks used by the DSP or DF+DAC sections of BU9406KS2.
One is the 24.576MHz (512fs) system clock from the XI pin, and the other two are 512fs clocks generated by PLL1 andPLL2 from the input clocks BCKI1~3.

2-17. System Clock Selection of ASRC Input Section (used for up-sampling) (Dotted line ①)

Default = 0

Select Address	Value	Operation Description
&h0A [7 : 6]	0	24.576MHz (512fs) system clock from XI pin
	1	512fs clock extracted from S-P conversion 1 PLL1
	2	512fs clock extracted from S-P conversion 2 PLL2

2-18. System Clock Selection for ASRC Output Section (used for down-sampling), P-S Conversion 2 and S/PDIF Output (Dotted line ③)

Default = 0

Select Address	Value	Operation Description
&h0A [1 : 0]	0	24.576MHz (512fs) system clock from XI pin
	1	512fs clock extracted from S-P conversion 1 PLL1
	2	512fs clock extracted from S-P conversion 2 PLL2

2-19. System Clock Selection for P-S Conversion 1 (Dotted line ②)

Default = 0

Select Address	Value	Operation Description
&h0A [5 : 4]	0	24.576MHz (512fs) system clock from XI pin
	1	512fs clock extracted from S-P conversion 1 PLL1
	2	512fs clock extracted from S-P conversion 2 PLL2

2-20. System Clock Selection of DF1 and ΔΣDAC 1 (Dotted line ④)

Default = 0

Select Address	Value	Operation Description
&h0B[7 : 6]	0	24.576MHz (512fs) system clock from XI pin
	1	512fs clock extracted from S-P conversion 1 PLL1
	2	512fs clock extracted from S-P conversion 2 PLL2

2-21. System Clock Selection of DF2 and ΔΣDAC2 (Dotted line ⑤)

Default = 0

Select Address	Value	Operation Description
&h0B[5 : 4]	0	24.576MHz (512fs) system clock from XI pin
	1	512fs clock extracted from S-P conversion 1 PLL1
	2	512fs clock extracted from S-P conversion 2 PLL2

2-22. System Clock Selection of DF3 and 16bit DAC (Dotted line ⑥)

Default = 0

Select Address	Value	Operation Description
&h0B[3 : 2]	0	24.576MHz (512fs) system clock from XI pin
	1	512fs clock extracted from S-P conversion 1 PLL1
	2	512fs clock extracted from S-P conversion 2 PLL2

3. S-P Conversion 1 and S-P Conversion 2

BU9406KS2 has two built-in serial-parallel conversion circuits. (S-P Conversion 1 and S-P Conversion 2)

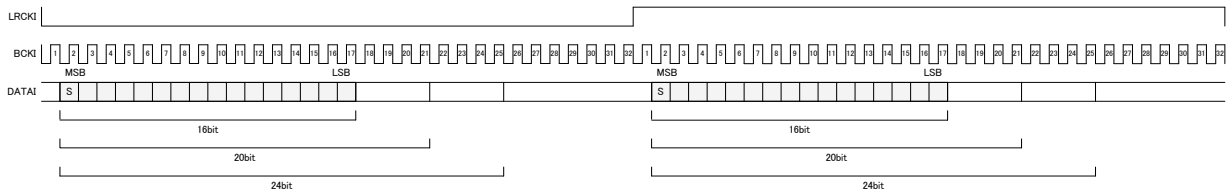
S-P conversions 1 and 2 are blocks which receive 3-line serial input audio data from pins and convert it to parallel data.

Input from DATAI1, BCKI1 and LRCKI1 (pins 52,53 and 54), DATAI2, BCKI2 and LRCKI2 (pins 55, 56, and 57), DATAI3, BCKI3 and LRCKI3 (pins 58, 63 and 64), and DATAI4, BCKI4 and LRCKI4 (pins 65, 66 and 67) are selected.

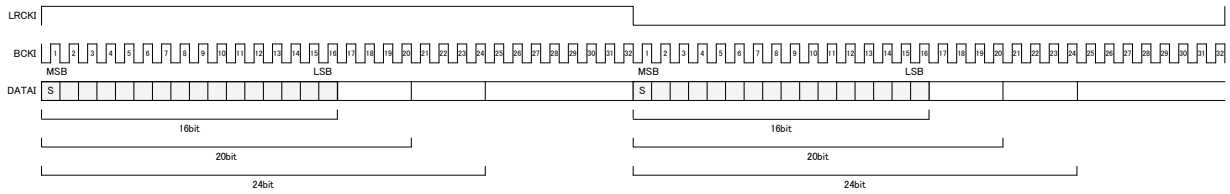
The three input formats are IIS, left-justified and right-justified. The bit clock frequency may be selected from either 64fs or 48fs, but when 48fs is selected, the input format is always right-justified. 16bit, 20bit and 24bit output may be selected for each format.

Below are the timing charts for each transfer format.

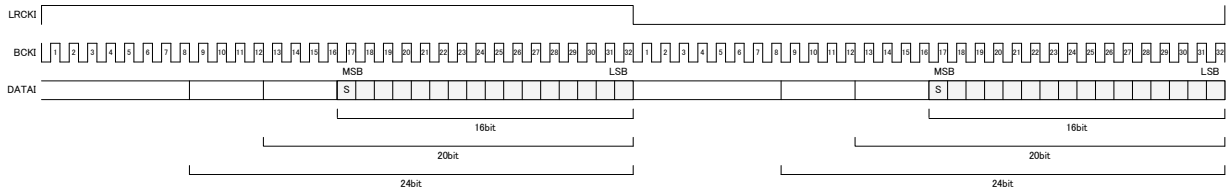
IIS Format



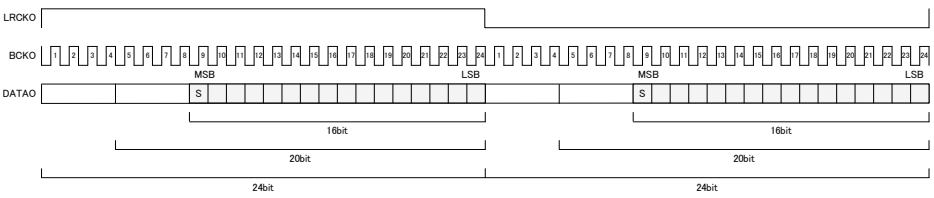
Left-Justified Format



Right-Justified Format



48fs



3-1. Input Selection for S-P Conversions 1 and 2

Default = 0

Select Address	Value	Operation Description
S-P Conversion 1 &h05[5:4] S-P Conversion 2 &h05[1:0]	0	Input data from I2S_IN1
	1	Input data from I2S_IN2
	2	Input data from I2S_IN3
	3	Input data from I2S_IN4

3-2. Bit Clock Frequency Configuration for 3-line Serial Input

Default = 0

Select Address	Value	Operation Description
S-P Conversion 1 &h0C [4]	0	64fs format
S-P Conversion 2 &h0D [4]	1	48fs format

3-3. Format Configuration for 3-line Serial Input

Default = 0

Select Address	Value	Operation Description
S-P Conversion 1 &h0C[3:2] S-P Conversion 2 &h0D[3:2]	0	IIS format
	1	Left-justified format
	2	Right-justified format

3-4. Data Bit Width Configuration for 3-line Serial Input

Default = 0

Select Address	Value	Operation Description
S-P Conversion 1 &h0C[1:0] S-P Conversion 2 &h0D[1:0]	0	16 bit
	1	20 bit
	2	24 bit

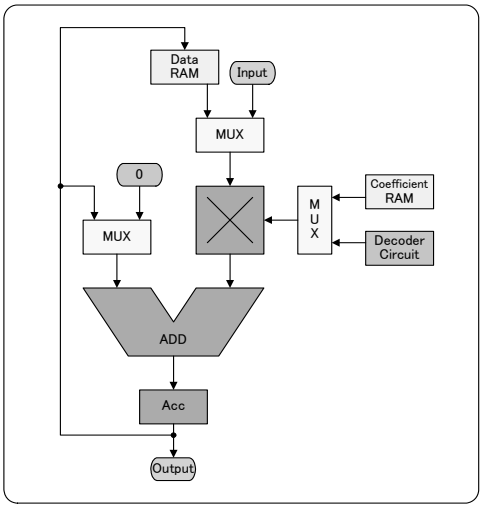
4. Digital Sound Processing (DSP)

BU9406KS2's digital sound processing (DSP) section is constructed with specific hardware optimal for FPD TVs.
BU9406KS2 uses this special DSP to perform the following processes:

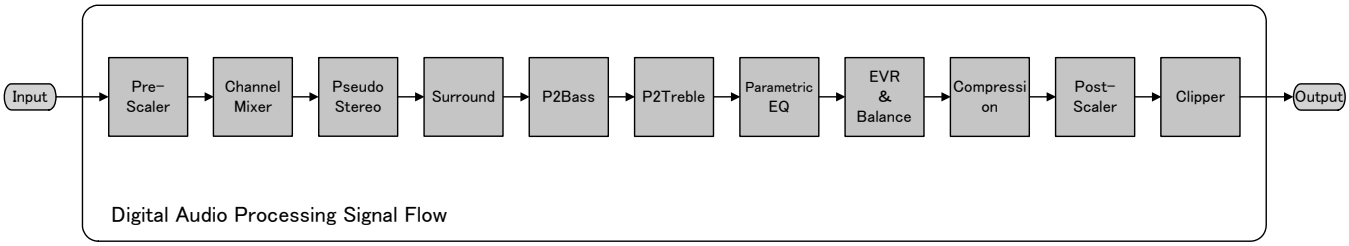
Pre-scaler, Channel Mixer, Pseudo-Stereo, Surround, P^2Bass, P^2Treble, Parametric Equalizer,
EVR & Balance, Compression, Post-scaler, Clipper

4-1. Overview and Signal Flow of DSP Section

Word length:	28 bit (DATA RAM)
Machine Cycle:	40.7ns (512fs, fs=48kHz)
Multiplier:	28×24 → 52 bit
Adder:	28+28 → 28 bit
Data RAM:	256×28 bit
Coefficient RAM:	128×24 bit
Sampling Frequency:fs=48kHz	
Master Clock:	512fs (24.576MHz, fs=48kHz)



16bit and 24bit digital signals are input to the DSP, but there is an overflow margin of +4bit (+24dB) on the top side.
For processes that exceed this range, there is a clipping process within the DSP.



4-2. Pre-Scaler

When the digital signals are input to the sound DSP the level may be full-scale input, causing overflow from surround or equalizer treatment, so the pre-scaler adjusts the input gain.
Analog signals are changed to digital values with the A/D converter, and the gain can be adjusted with the pre-scaler even when the input level is low.
The adjustment range can be configured in 2dB increments from +16dB to -44dB.

Default = 00

Select Address	Operation Description
&h20 [4 : 0]	

Command Value	Gain	Command Value	Gain	Command Value	Gain	Command Value	Gain
00	0dB	08	−16dB	10	−32dB	18	+16dB
01	−2dB	09	−18dB	11	−34dB	19	+14dB
02	−4dB	0A	−20dB	12	−36dB	1A	+12dB
03	−6dB	0B	−22dB	13	−38dB	1B	+10dB
04	−8dB	0C	−24dB	14	−40dB	1C	+8dB
05	−10dB	0D	−26dB	15	−42dB	1D	+6dB
06	−12dB	0E	−28dB	16	−44dB	1E	+4dB
07	−14dB	0F	−30dB	17	−∞	1F	+2dB

4-3. Channel Mixer

Performs the mixing configuration of the left and right channel sounds of digital signals input to the sound DSP.
Stereo signals can be changed to monaural here.

Mixes DSP Lch input data.

Default = 0

Select Address	Value	Operation Description
&h2A [7 : 6]	0	Inputs Lch data
	1	Inputs (Lch+Rch)/2 data
	2	Inputs (Lch+Rch)/2 data
	3	Inputs Rch data

Mixes DSP Rch input data.

Default = 0

Select Address	Value	Operation Description
&h2A [5 : 4]	0	Inputs Rch data
	1	Inputs (Lch+Rch)/2 data
	2	Inputs (Lch+Rch)/2 data
	3	Inputs Lch data

4-4. Pseudo-Stereo 2

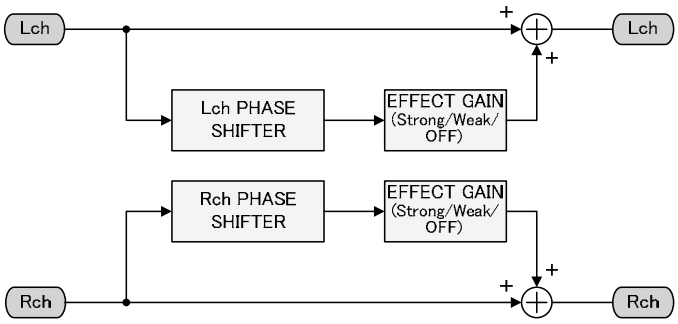
Recreates stereo feel in monaural sound through signal treatment.
The quality of this pseudo-stereo treatment is higher than that of the pseudo-stereo of “5-5 Surround and Pseudo-Stereo 1”.

Selection of Pseudo-Stereo 2 Filter Effect

Default = 0

Select Address	Value	Operation Description
&h71 [1 : 0]	0	Pseudo-stereo OFF
	1	Effect configured to “weak”
	2	Effect configured to “strong”

Sound is further enhanced when used together with surround (&h70[7]=1).

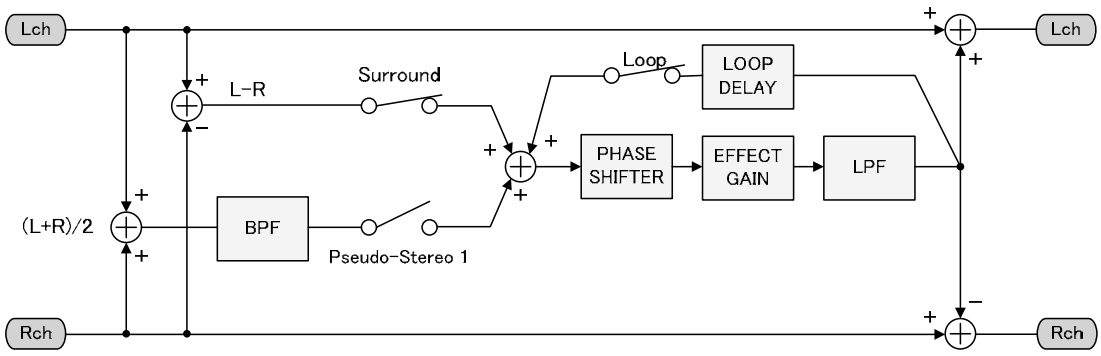


4-5. Surround (Matrix Surround 3D) and Pseudo-Stereo 1

Actualizes surround sound with a vast sweet spot, which allows longer viewing with less fatigue.

Recreates natural mid- and high-range sound, actualizing sound field that does not take away from the stability of the vocal.

Using the loop function simulates extra steps of the phase shifter.



Turning Surround Function ON/OFF

Default = 0

Select Address	Value	Operation Description
&h70 [7]	0	Turns surround effect OFF
	1	Turns surround effect ON

Turning Pseudo-Stereo Function 1 ON/OFF (Different function from 5-4 pseudo-stereo 2)

Default = 0

Select Address	Value	Operation Description
&h70 [6]	0	Turns pseudo-stereo effect OFF
	1	Turns pseudo-stereo effect ON

Loop Usage Configuration

Default = 0

Select Address	Value	Operation Description
&h70 [5]	0	Loop OFF
	1	Loop ON

Delay Length Configuration in Loop use

Default = 0

Select Address	Value	Operation Description
&h71 [7 : 6]	0	1 sample
	1	64 samples
	2	128 samples
	3	255 samples

Surround Gain Configuration

Default = 0

Select Address	Operation Description
&h70 [3 : 0]	

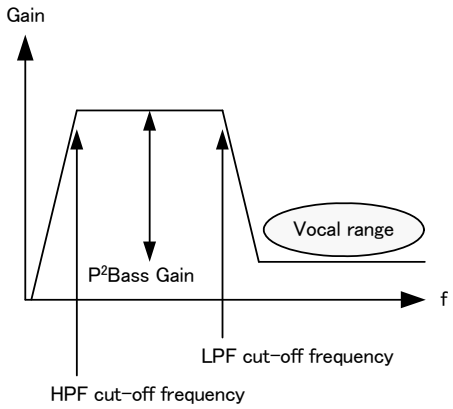
Command Value	Gain	Command Value	Gain
0	0dB	8	−8dB
1	−1dB	9	−9dB
2	−2dB	A	−10dB
3	−3dB	B	−11dB
4	−4dB	C	−12dB
5	−5dB	D	−13dB
6	−6dB	E	−14dB
7	−7dB	F	−15dB

Simultaneous use of surround (Matrix Surround 3D) and pseudo-stereo 1 will not produce optimal results.

4-6. P^{2}Bass (Perfect Pure Bass: Deep Bass Equalizer)

The deep bass equalizer recreates dynamic bass and realistic sound, even with FPD TVs which have limited speaker enclosure.

It actualizes clear, heavy bass with low distortion. Rich and natural bass is obtained, and the vocal range is not affected even when with bass boost.



Turning P^{2}Bass Function ON/OFF

Default = 0

Select Address	Value	Operation Description
&h72 [7]	0	P^{2}Bass function OFF
	1	P^{2}Bass function ON

P^{2}Bass HPF Cut-off Frequency Configuration

Default = 0

Select Address	Value	Operation Description
&h72 [3 : 2]	0	60Hz
	1	80Hz
	2	100Hz
	3	120Hz

P^{2}Bass LPF Cut-off Frequency Configuration

Default = 0

Select Address	Value	Operation Description
&h72 [1 : 0]	0	120Hz
	1	160Hz
	2	200Hz
	3	240Hz

P^{2}Bass Deep Bass Gain Configuration

Default = 0

Select Address	Operation Description
&h73 [6 : 4]	

Command Value	Gain	Command Value	Gain
0	+6dB	4	+10dB
1	+7dB	5	+11dB
2	+8dB	6	+12dB
3	+9dB	7	+13dB

4-7. P²Treble (Perfect Pure Treble: Mid-/High-range equalizer)

Actualizes clear, crisp and extensive sound.
With sets which have speakers placed near the bottom, the effect will allow the sound to feel “lifted”.

Turning P²Treble Function ON/OFF

Default = 0

Select Address	Value	Operation Description
&h72 [6]	0	SAS function OFF
	1	SAS function ON

P²Treble Mid-/High-Range Gain Configuration

Default = 0

Select Address	Operation Description
&h73 [3 : 0]	

Command Value	Gain	Command Value	Gain
0	+1dB	8	+9dB
1	+2dB	9	+10dB
2	+3dB	A	+11dB
3	+4dB	B	+12dB
4	+5dB	C	+13dB
5	+6dB	D	+14dB
6	+7dB	E	+15dB
7	+8dB		

4-8. Parametric Equalizer

BU9406KS2 has a 2-channel, 12-band parametric equalizer. This is used either to control bass and treble or as an equalizer to improve the frequency characteristics of speakers.

Data Width: 28 bit
Coefficient:: 24 bit (-4~+4)

The first 5 bands configure common coefficients for both Lch and Rch. They are used chiefly to control tone.
The latter 7 bands are used as independent parametric equalizers for Lch and Rch.
There is a built-in soft transition function to change the audio characteristics while sound is being played back.
The configuration diagrams of Lch and Rch parametric equalizers are on the following page.

Collective Load of Coefficients to Coefficient RAM

Default = 0

Select Address	Value	Operation Description
&h40 [7]	0	Load stop
	1	Load start

Monitor for State of Parametric Equalizer (for read-out)

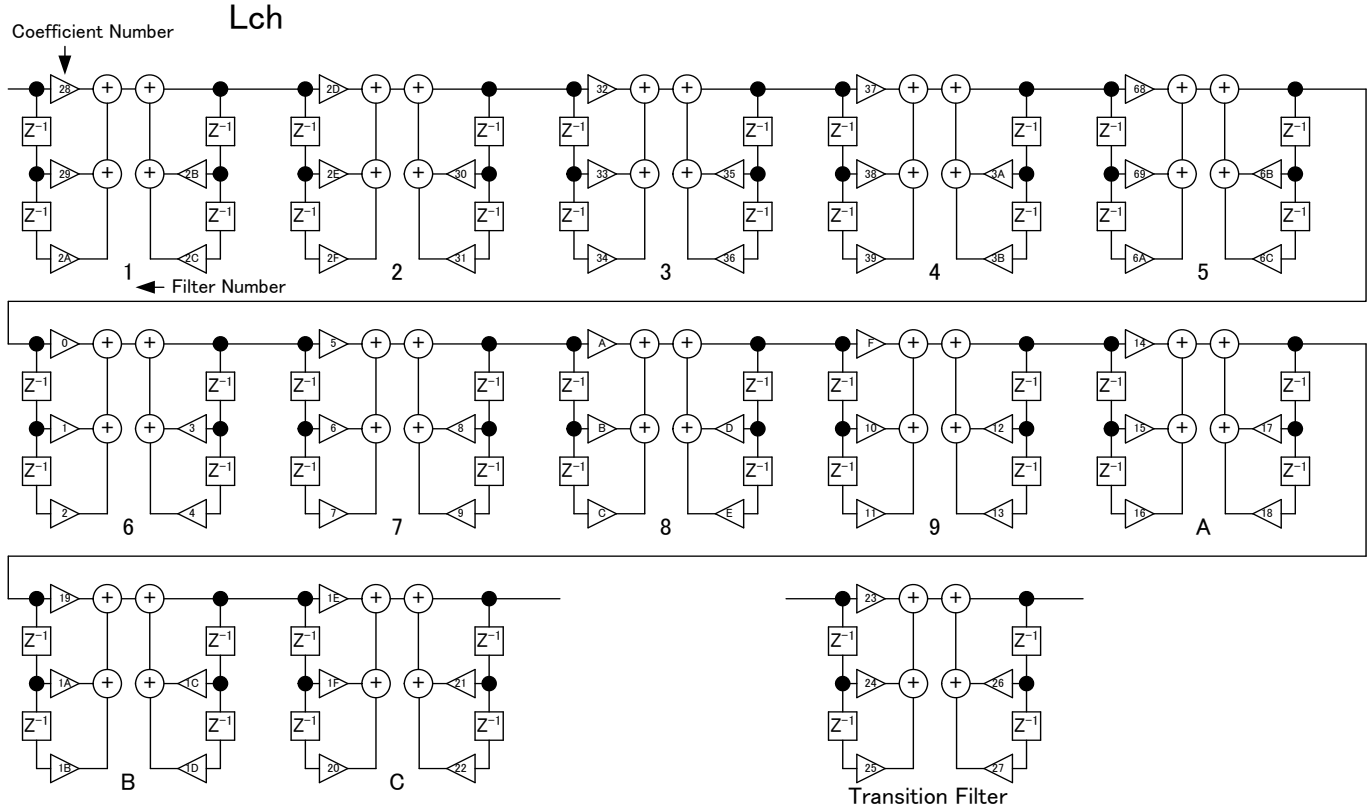
Select Address	Definition	State
&h46 [7]	BUSY signal monitor during coefficient transition	Displays “H” during transition
&h46 [6]	BUSY monitor during coefficient load	Displays “H” during load

Time Configuration for Soft Transition Completion

Default = 0

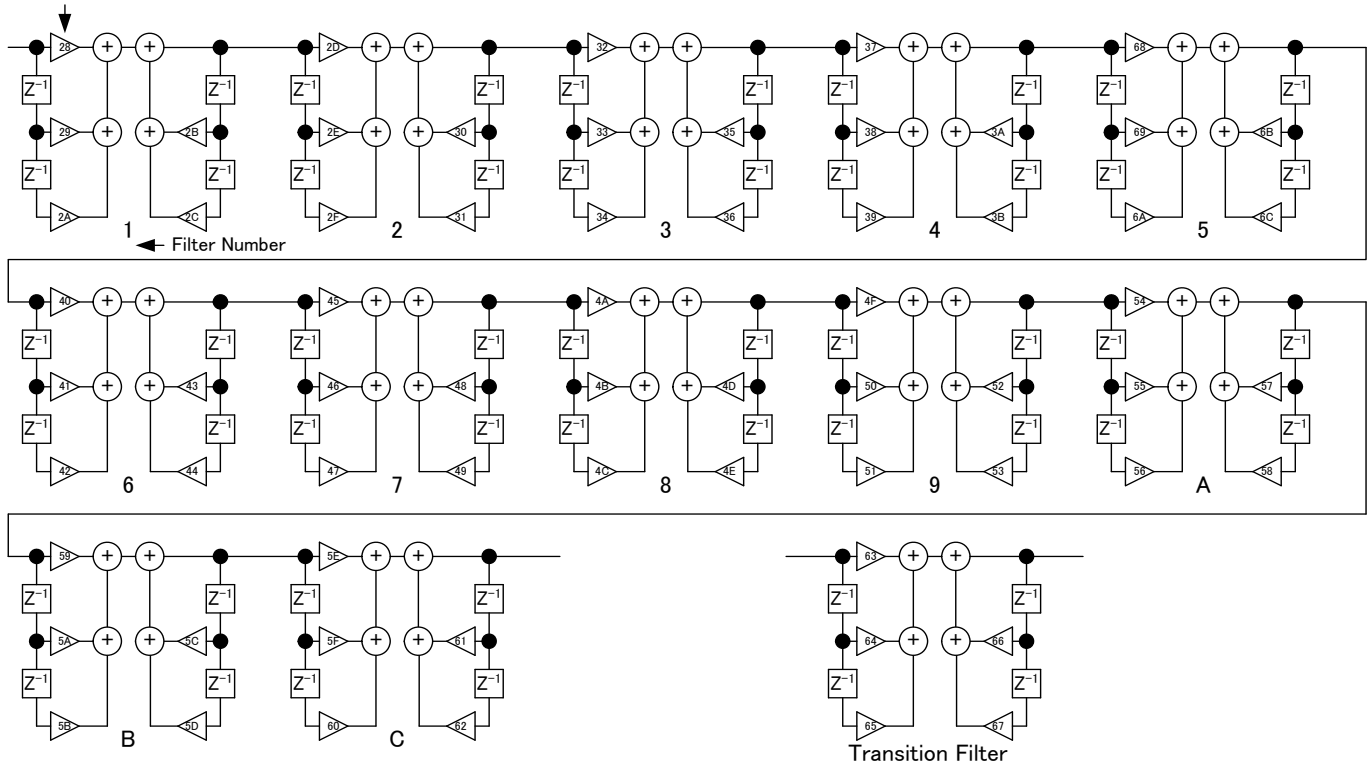
Select Address	Value	Operation Description
&h45 [5 : 4]	0	21.3ms （1024fs）
	1	42.6ms （2048fs）
	2	10.6ms （512fs）
	3	5.3ms （256fs）

Lch



※Coefficient Numbers and Filter Numbers are hexadecimal

Rch(Latter 7 bands and transition filter coefficients differ from Lch)



※Coefficient Number and Filter Numbers are hexadecimal

4-8-1. Parametric EQ Coefficient Configuration Method

① Set &h40[7] to “L”.
② Configure the address (7bits) of the coefficient number to be converted at &h41[6:0].
Configure the data (24bits) at &h42[7:0], &h43[7:0] and &h44[7:0].
③ Set &h40[7] to “H”. Data can be collectively written into the coefficient RAM of the appointed coefficient numbers.
④ The write-in to the coefficient RAM completes when &h46[6] is read out and confirmed to be “L”, or after a 20μs wait.
Afterwards, set &h40[7] to “L”.
⑤ With coefficients, h7FFFFF (maximum value) refers to +4-1LSB and h800000 (minimum value) refers to -4. In addition, h200000 refers to +1, h00000 refers to 0, and hE00000 refers to -1.

4-8-2. Soft Transition Usage Method During Coefficient Switching of Parametric EQ

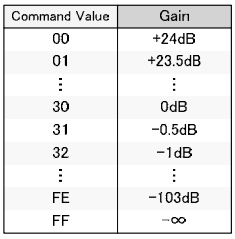
① Configure the transition time at &h45[5:4].
② New coefficients are set to the transition filters of two channels. To transit the first 5 bands (same coefficients for both channels), the same coefficients must be set to the transition filters of both channels.
③ Set the filter number to transit at &h45[3:0]. Transition begins.
④ seni_busy (signal read out at &h46[7]) becomes “H”, and turns to “L” when transition is complete.
⑤ 0 must be set to &h45[3:0] when transition is complete, finishing the soft transition operation.

4-9. EVR (Electrical Volume) and Balance

The volume can be selected in 0.5dB increments from +24dB to -103dB.
Soft transition is performed when volume is changed. It takes approximately 21ms to go from 0dB to mute.
The balance can be decreased in 1dB increments from the volume configuration value. Soft transition is performed at switch.

Volume Configuration

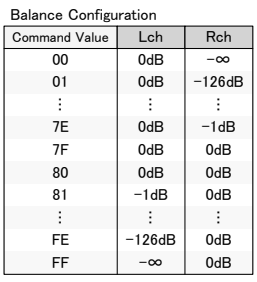
Default = 00h

Select Address	Operation Description
&h24 [7 : 0]	

Command Value	Gain
00	+24dB
01	+23.5dB
⋮	⋮
30	0dB
31	−0.5dB
32	−1dB
⋮	⋮
FE	−103dB
FF	−∞

L/R Balance Configuration

Default = 80h

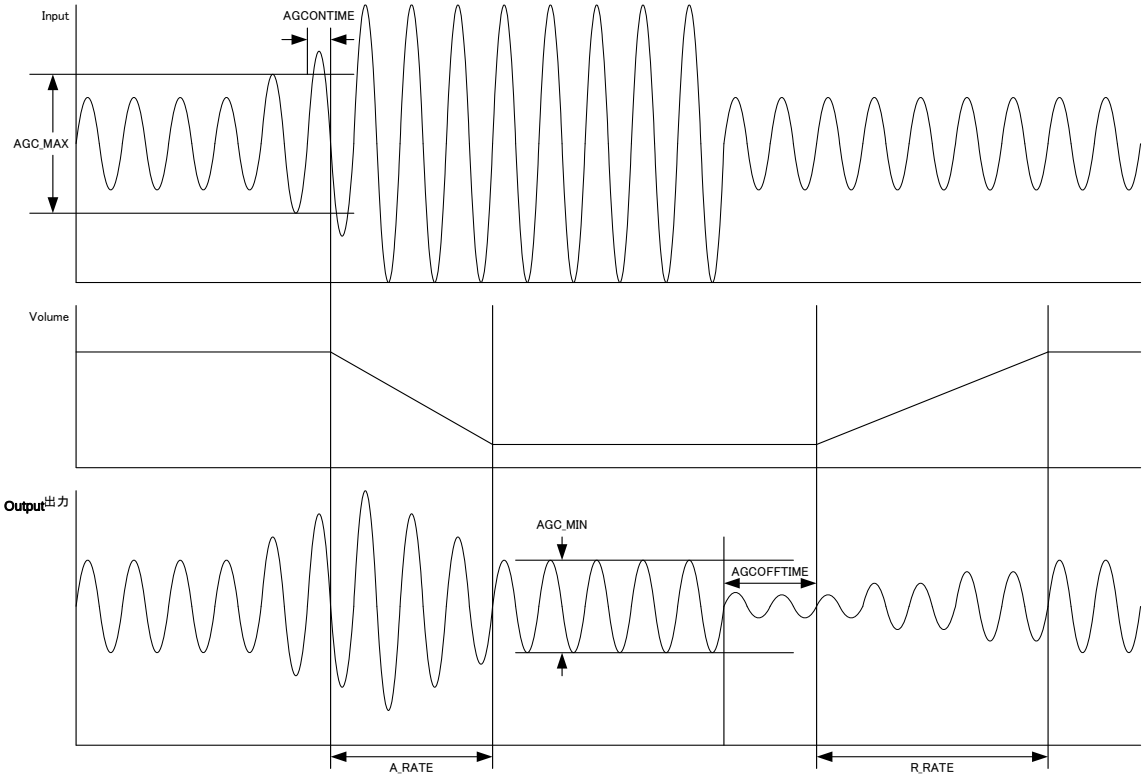
Select Address	Operation Description
&h25 [7 : 0]	

Balance Configuration

Command Value	Lch	Rch
00	0dB	−∞
01	0dB	−126dB
⋮	⋮	⋮
7E	0dB	−1dB
7F	0dB	0dB
80	0dB	0dB
81	−1dB	0dB
⋮	⋮	⋮
FE	−126dB	0dB
FF	−∞	0dB

4-10. Compression

This function automatically adjusts the volume when sound suddenly increases, such as with explosion sounds in TV commercials or movies, in order to prevent shocking the listener.



&h21[7] should be set to “H” when the compression function is used.

Default = 0

Select Address	Value	Operation Description
&h21 [7]	0	Compression function OFF
	1	Compression function ON

AGC_MAX is the input level configuration for turning compression ON. It is configured at &h21[6:4].

Default = 0

Select Address	Operation Description
&h26 [6 : 4]	

Command Value	Gain	Command Value	Gain
0	0dB	4	−12dB
1	−3dB	5	−18dB
2	−6dB	6	−24dB
3	−9dB	7	−30dB

When the time and input level configured at AGCONTIME exceeds AGC_MAX, compression is turned ON.
AGCONTIME is configured at &h22[6:4].

Default = 0

Select Address	Operation Description
&h22 [6 : 4]	

Command Value	Time	Command Value	Time
0	0.5ms	4	3ms
1	1ms	5	4ms
2	1.5ms	6	5ms
3	2ms	7	6ms

A_RATE is the configuration for the speed of volume decrease. It is configured at &h23[6:4].

Default = 0

Select Address	Operation Description
&h23 [6 : 4]	

Command Value	a_rate Time	Command Value	a_rate Time
0	1ms	4	5ms
1	2ms	5	10ms
2	3ms	6	20ms
3	4ms	7	40ms

AGC_MIN is the configuration for level output when compression is turned ON. It is configured at &h21[2:0].

Default = 0

Select Address	Operation Description
&h21 [2 : 0]	

Command Value	Gain	Command Value	Gain
0	0dB	4	−12dB
1	−3dB	5	−18dB
2	−6dB	6	−24dB
3	−9dB	7	−30dB

When the time and output level configured at AGCOFFTIME goes under AGC_MIN, compression turns OFF.
AGCOFFTIME is configured at &h22[2:0].

Default = 0

Select Address	Operation Description
&h22 [2 : 0]	

Command Value	Time	Command Value	Time
0	50ms	4	300ms
1	100ms	5	400ms
2	150ms	6	500ms
3	200ms	7	600ms

R_RATE is the configuration of the speed of volume increase. It is configured at &h23[3:0].

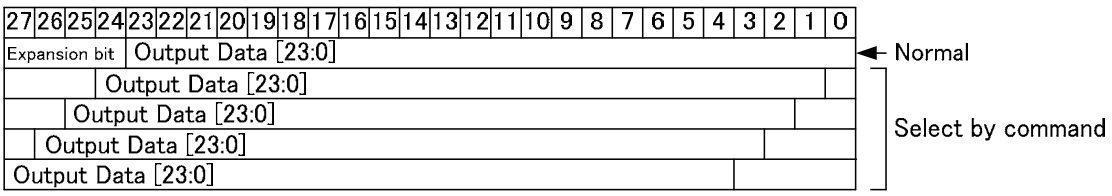
Default = 0h

Select Address	Operation Description
&h23 [3 : 0]	

Command Value	r_rate Time	Command Value	r_rate Time
0	0.25s	8	3s
1	0.5s	9	4s
2	0.75s	A	5s
3	1s	B	6s
4	1.25s	C	7s
5	1.5s	D	8s
6	2s	E	9s
7	2.5s	F	10s

4-11. Post-Scaler

When outputting 28bit-wide data computed by the DSP, the first 4 bits that were added on at input as overflow margin are removed before the output; however, if the post-scaler is used when the DSP performs a variety of calculations and adjusts the level for output, the level adjustments are made simpler.

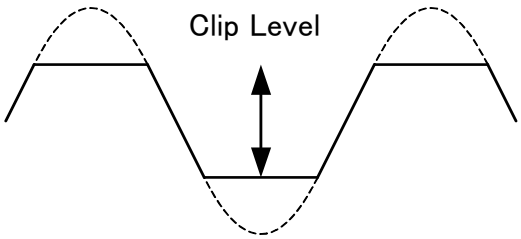


Default = 0

Select Address	Value	Operation Description
&h26 [2 : 0]	0	0dB (removes top 4 bits added on at input)
	1	-6dB
	2	-12dB
	3	-18dB
	4	-24dB

4-12. Clipper

The rated output (actual maximum output) of a TV is measured when the combined distortion (THD+N) is at 10%. The clipper function allows the user to clip the output amplitude freely, for example to get a rated output of 10W or 5W using an amplifier with 15W output.



Set &h27[7] to “H” when using the clipper function.

Default = 0

Select Address	Value	Operation Description
&h27 [7]	0	Clipper function OFF
	1	Clipper function ON

The clip level is configured at the upper 8 bits &h28[7:0] and lower 8 bits &h29[7:0].
Decreasing the configured value decreases the clip level.

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	◀Maximum Positive Value
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	◀Minimum Negative Value
0	clip_level[15:0]																0	0	0	0	0	0	0	◀ Positive Clip Level
1	~clip_level[15:0]																1	1	1	1	1	1	1	◀ Negative Clip Level

Negative clip level configures the opposite data of positive clip level.
(Note) The clipper function must be used when DSP output is output to DF1, DF2 or DF3.

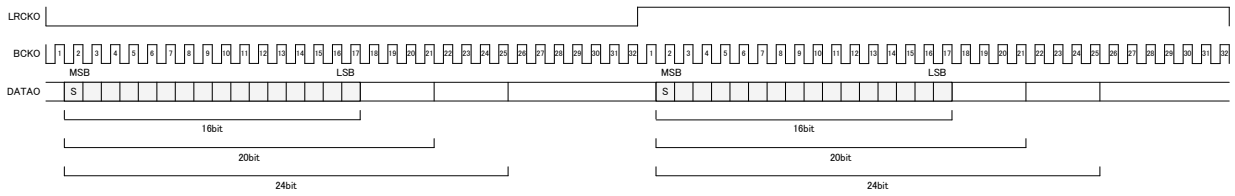
5. P-S Conversion 1 and P-S Conversion 2

BU9406KS2 has two built-in parallel-serial conversion circuits (P-S Conversion 1 and P-S Conversion 2). P-S conversion 1 converts the output from the AD converter or ASRC to 3-line serial data before sending it from DATAOA, BCKOA and LRCKOA (pins 48, 49 and 51) or DATAOB, BCKOB and LRCKOB (pins 45, 46 and 47). (Refer to &h08[6:4] and &h08[2:0]) P-S conversion 2 converts the ASRC or DSP output into 3-line serial data before transmitting it from DATAOC, BCKOC and LRCKOC (pins 42, 43 and 44).

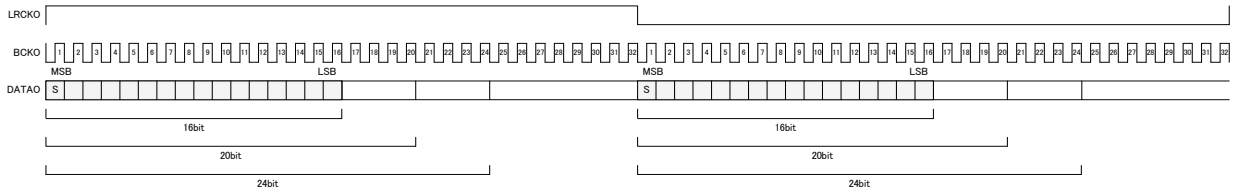
The system clock for P-S conversion 1 is configured at &h0A[5:4], however, when outputting an AD converter, SYSCLK should be selected. When outputting ASRC, the same selection should be made as with &h0A[1:0].

The three output formats are IIS, left-justified and right-justified. 16bit, 20bit and 24bit output can be selected for each format.
The timing charts for each transfer format are as follows:

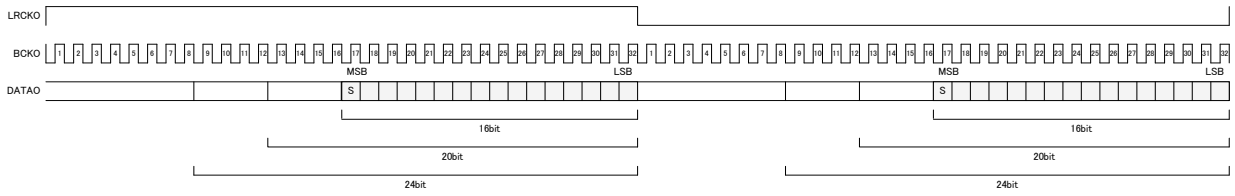
IIS Format



Left-Justified Format



Right-Justified Format



5-1. P-S Conversion 1 Output Selection

Default = 0

Select Address	Value	Operation Description
&h09 [7]	0	Outputs AD converter data
	1	Outputs data after ASRC

5-2. P-S Conversion 2 Output Selection

Default = 0

Select Address	Value	Operation Description
&h09 [4]	0	Outputs data after ASRC (before DSP processing)
	1	Outputs data after DSP processing

5-3. P-S Conversion 1 System Clock Selection

Default = 0

Select Address	Value	Operation Description
&h0A [5 : 4]	0	SYSCLK (512fs)
	1	PLL1_512fs
	2	PLL2_512fs

5-4. 3-line Serial Output Format Configuration

Default = 0

Select Address	Value	Operation Description
P-S Conversion 1 &h0E[3:2]	0	IIS format
P-S Conversion 2 &h0F[3:2]	1	Left-justified format
	2	Right-justified format

5-5. 3-line Serial Output Data Bit Width Configuration

Default = 0

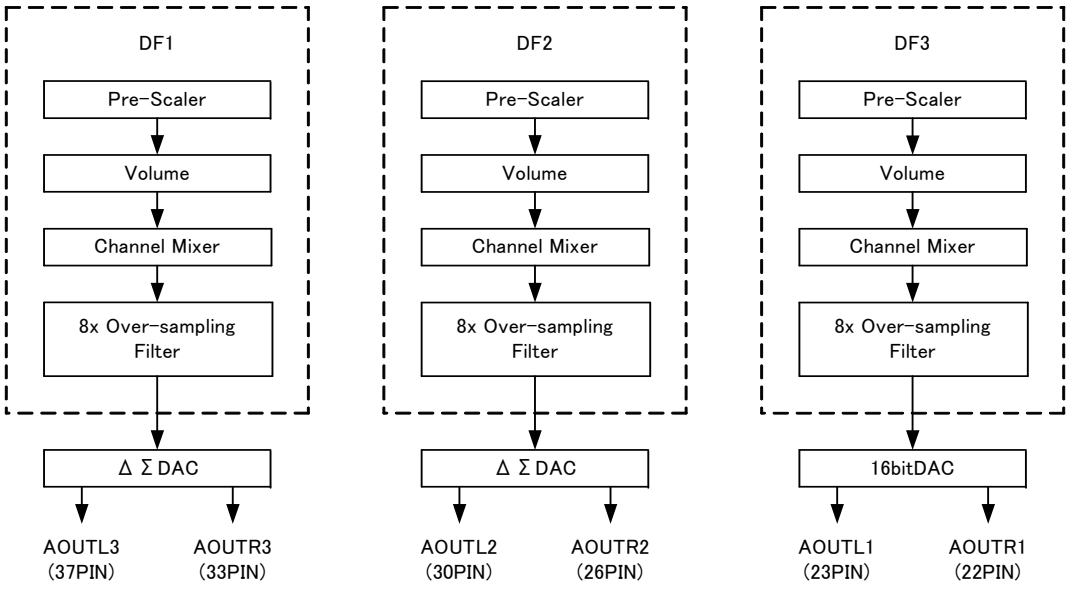
Select Address	Value	Operation Description
P-S Conversion 1 &h0C[1:0]	0	16 bit
P-S Conversion 2 &h0D[1:0]	1	20 bit
	2	24 bit

6. 8x Over-Sampling Digital Filter (DF)

In each BU9406KS2 audio analog signal output DAC, an 8x over-sampling digital filter is inserted into the previous step of the DAC input.

In addition to filter calculations, this block also performs pre-scaler, volume and Lch/Rch mix functions.

BU9406KS2's DF+DAC configurations are as follows:



6-1. Pre-Scaler Function

The signal levels are adjusted in order to bring out the audio DAC performance.

For DF1, refer to &h80[7:0] and &h81[7:0]. The default value is h4000.

For DF2, refer to &h83[7:0] and &h84[7:0]. The default value is h4000.

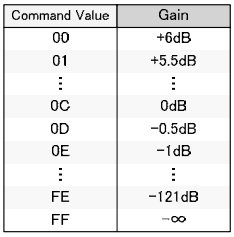
For DF3, refer to &h86[7:0] and &h87[7:0]. The default value is h4000.

6-2. Volume Function

The volume value can be configured in 0.5dB increments from +6dB to -121dB.

To change the volume value, coefficient soft transition takes place. The transition time from 0dB to mute is approximately 21ms.

Default = 0Ch

Select Address	Operation Description
DF1 &h82 [7 : 0] DF2 &h85 [7 : 0] DF3 &h88 [7 : 0]	

Calculation format: (12-command value)x0.5dB

6-3. Channel Mixer

Performs mixing configuration of left and right channel sounds of digital signals input to the DAC.

Stereo signals are converted to monaural here.

Mixes DAC Lch input data.

Default = 0

Select Address	Value	Operation Description
DF1 &h2A [3 : 2] DF2 &h2B [7 : 6] DF3 &h2B [3 : 2]	0	Inputs Lch data
	1	Inputs (Lch+Rch)/2 data
	2	Inputs (Lch+Rch)/2 data
	3	Inputs Rch data

Mixes DAC Rch input data.

Default = 0

Select Address	Value	Operation Description
DF1 &h2A [1 : 0] DF2 &h2B [5 : 4] DF2 &h2B [1 : 0]	0	Inputs Rch data
	1	Inputs (Lch+Rch)/2 data
	2	Inputs (Lch+Rch)/2 data
	3	Inputs Lch data

7. Commands Transmitted after Reset Release

(1) The following commands must be transmitted after reset release, including after power supply stand-up.

0. Turn power on.

↓

○Wait approximately 1ms until oscillation is stable. (The time to stabilization should be adjusted according to the pendulum product.)

↓

1 Reset release

↓

○Wait approximately 500us until RAM initialization is complete.

↓

2. &h01[7] = 0: The internal RAM is cleared, resulting in usable state.

↓

3. &hF1[2] = 0: Signals from the analog block are connected to the digital block.

↓

4. &hF5[5:4] = 0: Configure PLL clock to regular use state. (&hF5=00)

↓

5. &hF6[7:0] = AAh: Performs phase focusing of the clock output from PLL.

↓

6. Configure the default value (24'h200000) to parametric equalizer coefficient b0 (refer to (2) for procedure).

↓

○Wait approximately 10ms until PLL is stable.

↓

7. Configuration of other registers.

（2） 6. Procedure to configure default value (24'h200000) to parametric equalizer coefficient b0

6-1. &h42[7:0] = 20h : Configure 20h to bit [23:16] of 24bit coefficient to be loaded.

↓

6-2. &h41[7:0] = **h : Appoint coefficient address. (i.e.) Configure 28h to b0 of filter number 1.

↓

6-3. &h40[7] = 1 : Begin coefficient load.

↓

○Wait approximately 20us

↓

6-4. &h40[7] = 0 : Stop coefficient load.

Repeat steps 6-2 through 6-4 19 times, each time changing the filter coefficient b0 address.

N0.	&h41[7:0] = **h	Parametric Equalizer Filter Numbers
1	28h	Filter Number 1 (Lch/Rch common coefficient b0)
2	2Dh	Filter Number 2 (Lch/Rch common coefficient b0)
3	32h	Filter Number 3 (Lch/Rch common coefficient b0)
4	37h	Filter Number 4 (Lch/Rch common coefficient b0)
5	68h	Filter Number 5 (Lch/Rch common coefficient b0)
6	00h	Filter Number 6 (Lch coefficient b0)
7	05h	Filter Number 7 (Lch coefficient b0)
8	0Ah	Filter Number 8 (Lch coefficient b0)
9	0Fh	Filter Number 9 (Lch coefficient b0)
10	14h	Filter Number A (Lch coefficient b0)
11	19h	Filter Number B (Lch coefficient b0)
12	1Eh	Filter Number C (Lch coefficient b0)
13	40h	Filter Number 6 (Rch coefficient b0)
14	45h	Filter Number 7 (Rch coefficient b0)
15	4Ah	Filter Number 8 (Rch coefficient b0)
16	4Fh	Filter Number 9 (Rch coefficient b0)
17	54h	Filter Number A (Rch coefficient b0)
18	59h	Filter Number B (Rch coefficient b0)
19	5Eh	Filter Number C (Rch coefficient b0)

●Operational Notes

(1) ABSOLUTE MAXIMUM RATINGS

Permanent device damage may occur and break mode (open or short) can not be specified if power supply, operating temperature, and those of ABSOLUTE MAXIMUM RATINGS are exceeded. If such a special condition is expected, components for safety such as fuse must be used.

(2) Power Supply

Power and Ground line must be designed as low impedance in the PCB. Print patterns if digital power supply and analog power supply must be separated even if these have same voltage level. Print patterns for ground must be designed as same as power supply. These considerations avoid analog circuits from the digital circuit noise. All pair of power supply and ground must have their own de-coupling capacitor. Those capacitor should be checked about their specification, etc. (nominal electrolytic capacitor degrades its capacity at low temperature) and choose the constant of an electrolytic capacitor.

(3) Functionality in the strong electro-magnetic field

Malfunction may occur if in the strong electro-magnetic field.

(4) Input terminals

All LSI contain parasitic components. Some are junctions which normally reverse bias. When these junctions forward bias, currents flows on unwanted path, malfunction or device damage may occur. To prevent this, all input terminal voltage must be between ground and power supply, or in the range of guaranteed value in the Electrical characteristics. And no voltage should be supplied to all input terminal when power is not supplied.

●Ordering Information

B	U	9	4	0	6	K	S	2	

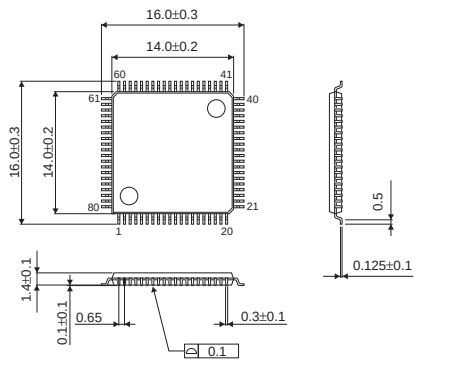
Part Number

Package
KS2: SQFP-T80C

Packaging and forming specification
None: Tray, Tube

●Physical Dimension Tape and Reel Information

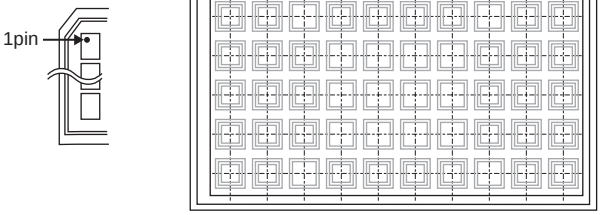
SQFP-T80C



(Unit : mm)

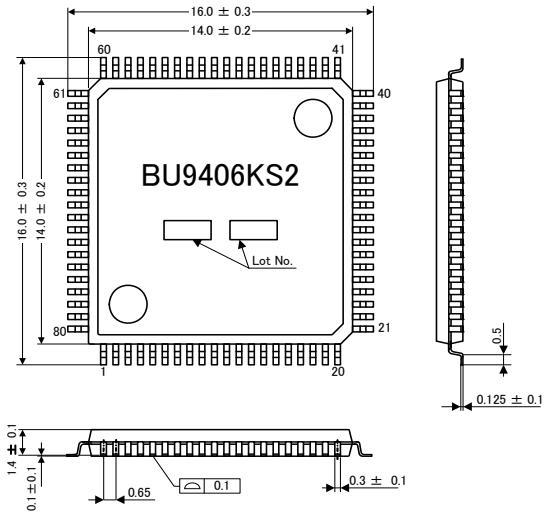
<Tape and Reel information>

Container	Tray (with dry pack)
Quantity	500pcs
Direction of feed	Direction of product is fixed in a tray



∗Order quantity needs to be multiple of the minimum quantity.

●Marking Diagram(s)(TOP VIEW)



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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
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   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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   [d] the Products are exposed to high Electrostatic

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