

R5011ANX

Silicon N-channel MOSFET

- 1) Low on-resistance.
- 2) Fast switching speed.
- 3) Gate-source voltage (V_{GS}) guaranteed to be $\pm 30V$.
- 4) Drive circuits can be simple.
- 5) Parallel use is easy.

Technical drawing of the TO-220FM transistor package showing front and side views with dimensions in millimeters.

Front View Dimensions:

- Top width: 10.0
- Top hole diameter: $\phi 3.2$
- Overall height: 15.0
- Height to mounting tab: 12.0
- Mounting tab height: 8.0
- Base width: 2.5
- Collector width: 1.3
- Emitter width: 1.2
- Base to collector spacing: 2.54
- Collector to emitter spacing: 2.54
- Mounting tab thickness: 0.8

Side View Dimensions:

- Mounting tab thickness: 4.5
- Mounting tab width: 2.8
- Base thickness: 0.75
- Collector thickness: 2.6

Legend:

- (1) Base
- (2) Collector
- (3) Emitter

Switching

Type	Package	Bulk
	Code	—
	Basic ordering unit (pieces)	500
R5011ANX		○

(1) Gate
(2) Drain
(3) Source

*1 Body Diode

Parameter		Symbol	Limits	Unit
Drain-source voltage		V _{DSS}	500	V
Gate-source voltage		V _{GSS}	±30	V
Drain current	Continuous	I _D *3	±11	A
	Pulsed	I _{DP} *1	±44	A
Source current (Body Diode)	Continuous	I _S *3	11	A
	Pulsed	I _{SP} *1	44	A
Avalanche Current		I _{AS} *2	5.5	A
Avalanche Energy		E _{AS} *2	8.1	mJ
Total power dissipation (Tc=25°C)		P _D	50	W
Channel temperature		T _{ch}	150	°C
Range of storage temperature		T _{stg}	-55 to +150	°C

*3 Limited only by maximum temperature allowed

Transistors

●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to case	Rth(ch-c)	2.5	°C/W

●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I _{GSS}	–	–	±100	nA	V _{GS} =±30V, V _{DS} =0V
Drain-source breakdown voltage	V _{(BR)DSS}	500	–	–	V	I _D =1mA, V _{GS} =0V
Zero gate voltage drain current	I _{DSS}	–	–	100	μA	V _{DS} =500V, V _{GS} =0V
Gate threshold voltage	V _{GS(th)}	2.5	–	4.5	V	V _{DS} =10V, I _D =1mA
Static drain-source on-state resistance	R _{DS(on)} [*]	–	0.38	0.5	Ω	I _D =5.5A, V _{GS} =10V
Forward transfer admittance	Y _{fs} [*]	3.5	–	–	S	I _D =5.5A, V _{DS} =10V
Input capacitance	C _{iss}	–	1000	–	pF	V _{DS} =25V
Output capacitance	C _{oss}	–	400	–	pF	V _{GS} =0V
Reverse transfer capacitance	C _{rss}	–	35	–	pF	f=1MHz
Turn-on delay time	t _{d(on)} [*]	–	26	–	ns	I _D =5.5A, V _{DD} ≒250V
Rise time	t _r [*]	–	28	–	ns	V _{GS} =10V
Turn-off delay time	t _{d(off)} [*]	–	75	–	ns	R _L =45.5Ω
Fall time	t _f [*]	–	30	–	ns	R _G =10Ω
Total gate charge	Q _g [*]	–	30	–	nC	V _{DD} ≒250V
Gate-source charge	Q _{gs} [*]	–	7	–	nC	I _D =11A
Gate-drain charge	Q _{gd} [*]	–	12	–	nC	V _{GS} =10V R _L =22.7Ω / R _G =10Ω

* Pulsed

●Body diode characteristics (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V _{SD} [*]	–	–	1.5	V	I _S = 11A, V _{GS} =0V

* Pulsed

Transistors

●Electrical characteristic curves

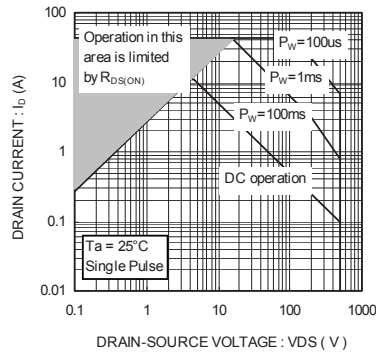


Fig.1 Maximum Safe Operating Area

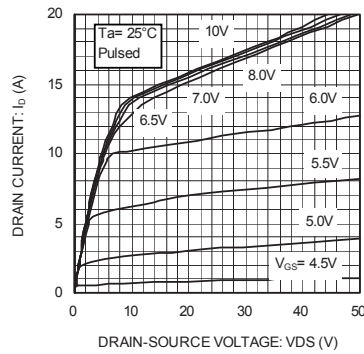


Fig.2 Typical Output Characteristics(I)

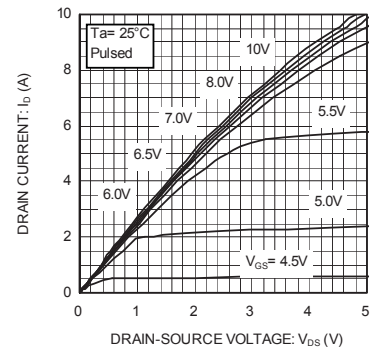


Fig.3 Typical Output Characteristics(II)

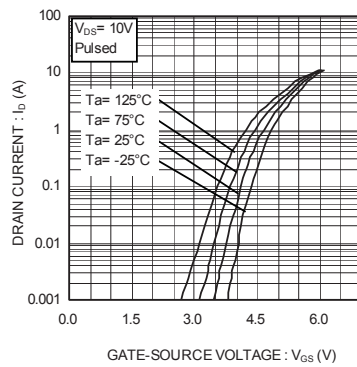


Fig.4 Typical Transfer Characteristics

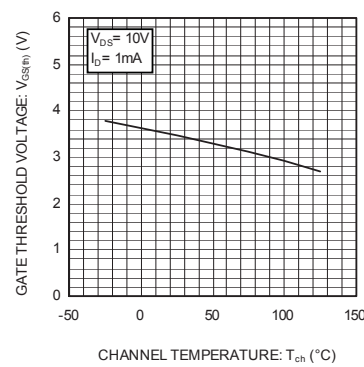


Fig.5 Gate Threshold Voltage vs. Channel Temperature

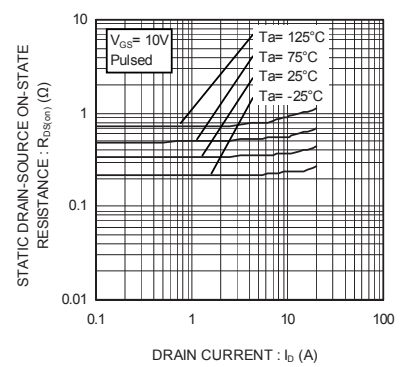


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current

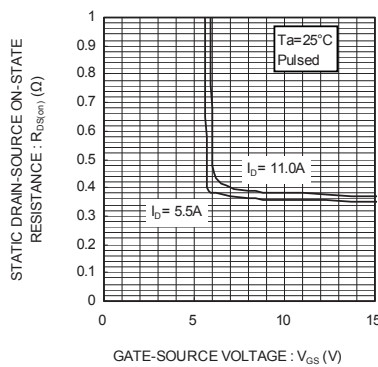


Fig.7 Static Drain-Source On-State Resistance vs. Gate Source Voltage

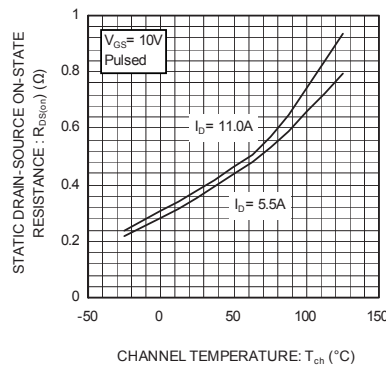


Fig.8 Static Drain-Source On-State Resistance vs. Channel Temperature

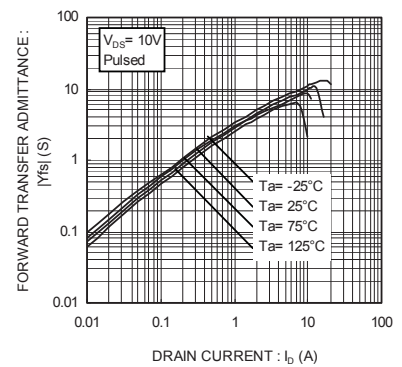


Fig.9 Forward Transfer Admittance vs. Drain Current

Transistors

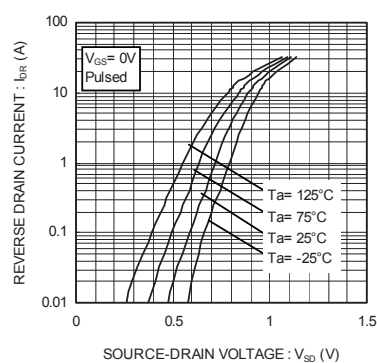


Fig. 10 Reverse Drain Current vs. Source-Drain Voltage

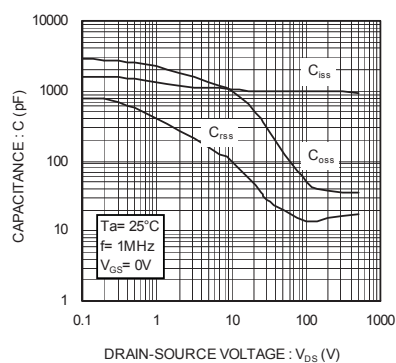


Fig. 11 Typical Capacitance vs. Drain-Source Voltage

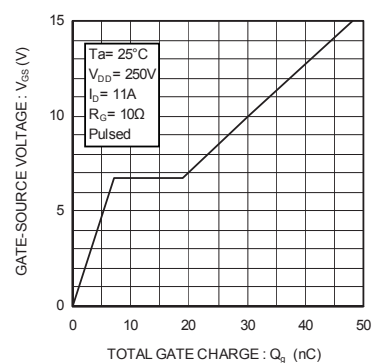


Fig. 12 Dynamic Input Characteristics

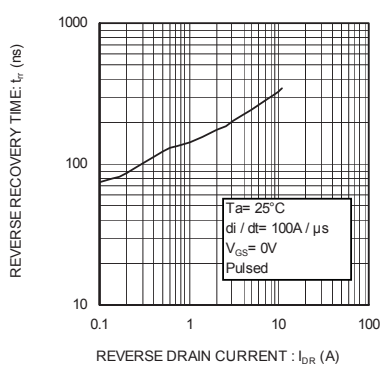


Fig. 13 Reverse Recovery Time vs. Reverse Drain Current

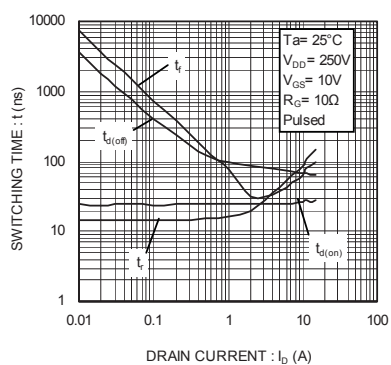


Fig. 14 Switching Characteristics

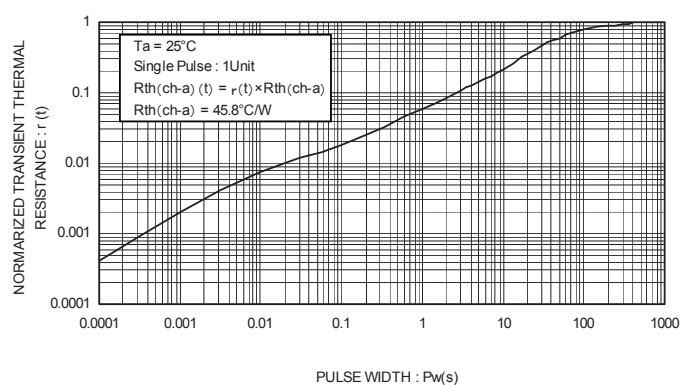


Fig. 15 Normalized Transient Thermal Resistance vs. Pulse Width

Transistors

●Switching characteristics measurement circuit

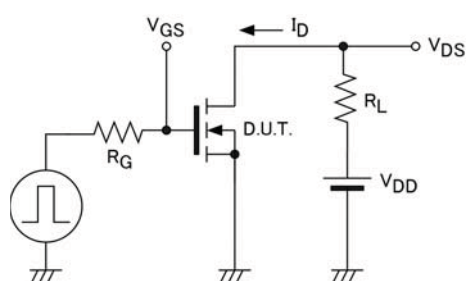


Fig.1-1 Switching Time Measurement Circuit

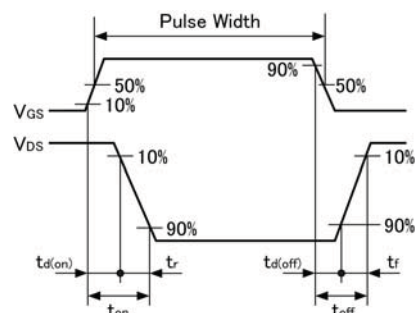


Fig.1-2 Switching Waveforms

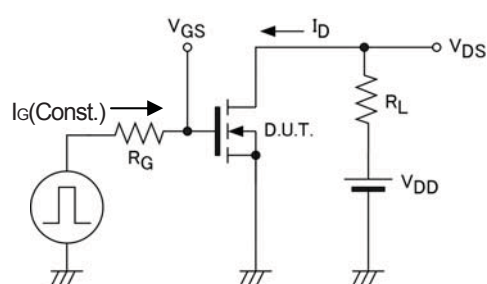


Fig.2-1 Gate Charge Measurement Circuit

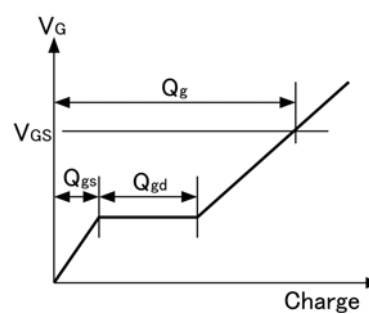


Fig.2-2 Gate Charge Waveform

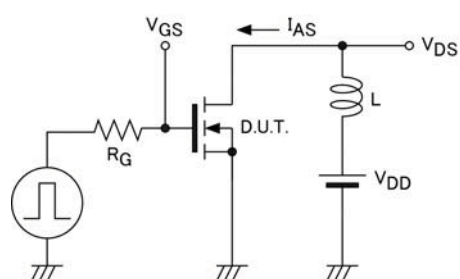


Fig.3-1 Avalanche Measurement Circuit

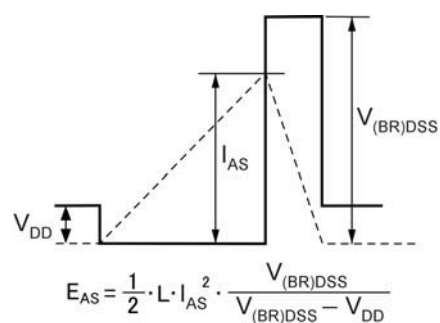


Fig.3-2 Avalanche Waveform

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