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May 2015

FDPC5030SG

PowerTrench® Power Clip 30V Asymmetric Dual N-Channel MOSFET

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 5.0 m Ω at V_{GS} = 10 V, I_D = 17 A
- Max $r_{DS(on)}$ = 6.5 m Ω at V_{GS} = 4.5 V, I_D = 14 A

Q2: N-Channel

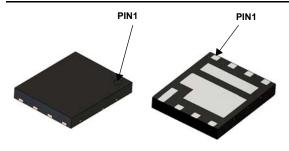
- Max $r_{DS(on)}$ = 2.4 m Ω at V_{GS} = 10 V, I_D = 25 A
- Max $r_{DS(on)}$ = 3.0 m Ω at V_{GS} = 4.5 V, I_D = 22 A
- Low Inductance Packaging Shortens Rise/Fall Times, Resulting in Lower Switching Losses
- MOSFET Integration Enables Optimum Layout for Lower Circuit Inductance and Reduced Switch Node Ringing
- RoHS Compliant

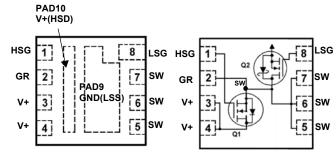
General Description

This device includes two specialized N-Channel MOSFETs in a dual package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFETTM (Q2) have been designed to provide optimal power efficiency.

Applications

- Computing
- Communications
- General Purpose Point of Load





Ton	Power Clin 5X6	Bottom

Pin	Name	Description	Pin	Name	Description	Pin	Name	Description
1	HSG	High Side Gate	3,4,10	V+(HSD)	High Side Drain	8	LSG	Low Side Gate
2	GR	Gate Return	5,6,7	SW	Switching Node, Low Side Drain	9	GND(LSS)	Low Side Source

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted.

Symbol	Parameter		Q1	Q2	Units
V _{DS}	Drain to Source Voltage		30	30	V
V _{GS}	Gate to Source Voltage		±20	±12	V
	Drain Current -Continuous	T _C = 25 °C (Note 5)	56	84	
	-Continuous	T _C = 100 °C (Note 5)	35	53	
ID	-Continuous	T _A = 25 °C	17 ^{Note1a}	25 ^{Note1b}	A
	-Pulsed	T _A = 25 °C (Note 4)	227	503	
E _{AS}	Single Pulse Avalanche Energy	(Note 3)	54	96	mJ
	Power Dissipation for Single Operation	T _C = 25 °C		25	
P_{D}	Power Dissipation for Single Operation	T _A = 25 °C		2.3 ^{Note1b}	W
	Power Dissipation for Single Operation	T _A = 25 °C	1.0 ^{Note1c}	1.1 ^{Note1d}	
T _J , T _{STG}	Operating and Storage Junction Temperature Range		-55 to	+150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	5.6	4.9	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	60 ^{Note1a}	55 ^{Note1b}	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	130 ^{Note1c}	120 ^{Note1d}	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDPC5030SG	FDPC5030SG	Power Clip 56	13 "	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted.

Symbol	Parameter	Test Conditions	Type	Min	Тур	Max	Units
Off Chara	acteristics						
D\/	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	Q1	30			V
BV_{DSS}	Drain to Source Breakdown voltage	$I_D = 1 \text{ mA}, V_{GS} = 0 \text{ V}$	Q2	30			V
ΔBV _{DSS}	Breakdown Voltage Temperature	I _D = 250 μA, referenced to 25 °C	Q1		15		mV/°C
ΔT_{J}	Coefficient	I_D = 10 mA, referenced to 25 °C	Q2		16		IIIV/ C
ı	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V	Q1			1	μΑ
I _{DSS}	Zero Gate voltage Drain Current	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$	Q2			500	μΑ
1	Gate to Source Leakage Current,	V _{GS} = 20 V, V _{DS} = 0 V V _{GS} = 12 V, V _{DS} = 0 V	Q1			100	nA
I _{GSS}	Forward	$V_{GS} = 12 \text{ V}, V_{DS} = 0 \text{ V}$	Q2			100	nA

On Characteristics

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$ $V_{GS} = V_{DS}, I_D = 1 mA$	Q1 Q2	1.0 1.0	1.7 1.6	3.0 3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C I_D = 10 mA, referenced to 25 °C	Q1 Q2		-5 -3		mV/°C
-	Drain to Source On Resistance	V _{GS} = 10V, I _D = 17 A V _{GS} = 4.5 V, I _D = 14 A V _{GS} = 10 V, I _D = 17 A,T _J =125 °C	Q1		4.1 5.4 5.7	5.0 6.5 7.0	mΩ
r _{DS(on)}	Drain to Source On Resistance	V _{GS} = 10V, I _D = 25 A V _{GS} = 4.5 V, I _D = 22 A V _{GS} = 10 V, I _D = 25 A ,T _J =125 °C	Q2		1.9 2.4 2.7	2.4 3.0 3.4	1115.2
9 _{FS}	Forward Transconductance	$V_{DS} = 5 \text{ V}, I_{D} = 17 \text{ A}$ $V_{DS} = 5 \text{ V}, I_{D} = 25 \text{ A}$	Q1 Q2		93 139		S

Dynamic Characteristics

C _{iss}	Input Capacitance	Q1:	Q1 Q2		1224 2730	1715 3825	pF
C _{oss}	Output Capacitance	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHZ}$ $Q2:$	Q1 Q2		397 801	560 1125	pF
C _{rss}	Reverse Transfer Capacitance	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHZ}$	Q1 Q2		42 72	60 100	pF
R _g	Gate Resistance		Q1 Q2	0.1 0.1	0.5 1.1	1.5 2.2	Ω

Switching Characteristics

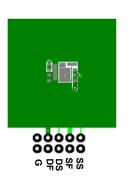
t _{d(on)}	Turn-On Delay Time			Q1 Q2	8 10	16 19	ns
t _r	Rise Time	Q1: V _{DD} = 15 V, I _D = 17	7 A, R _{GEN} = 6 Ω	Q1 Q2	2	10 10	ns
t _{d(off)}	Turn-Off Delay Time	Q2:	5 A Rosu = 6 O	Q1 Q2	18 30	33 48	ns
t _f	Fall Time	VDD - 13 V, 10 - 20	V_{DD} = 15 V, I_D = 25 A, R_{GEN} = 6 Ω		2	10 10	ns
Qg	Total Gate Charge	V _{GS} = 0 V to 10 V	Q1	Q1 Q2	17 39	24 55	nC
Qg	Total Gate Charge	V _{GS} = 0 V to 4.5 V		Q1 Q2	8 18	11 26	nC
Q _{gs}	Gate to Source Gate Charge		Q2 V _{DD} = 15 V, I _D	Q1 Q2	3.1 6.1		nC
Q _{gd}	Gate to Drain "Miller" Charge		= 25 A	Q1 Q2	2.0 4.3		nC

Electrical Characteristics T_J = 25 °C unless otherwise noted.

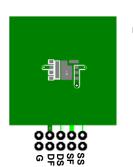
Symbol	Parameter	Test Conditions	Type	Min	Тур	Max	Units
Drain-Sou	rce Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 17 \text{ A}$ (Note 2) $V_{GS} = 0 \text{ V}, I_S = 25 \text{ A}$ (Note 2)	Q1		8.0	1.2	V
V SD	Source to Drain Blode I of Ward Voltage	$V_{GS} = 0 \text{ V}, I_S = 25 \text{ A}$ (Note 2)	Q2		8.0	1.2	V
+	Reverse Recovery Time	Q1	Q1		23	37	ns
۲rr	Reverse Recovery Time	I _F = 17 A, di/dt = 100 A/μs	Q2		27	44	115
0	Reverse Recovery Charge	Q2	Q1		8	16	nC
Q_{rr}	Reverse Recovery Charge	$I_F = 25 \text{ A}, \text{ di/dt} = 230 \text{ A/}\mu\text{s}$	Q2		31	50	110

Notes:

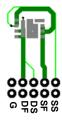
 $1.R_{\theta JA} \text{ is determined with the device mounted on a 1 in}^2 \text{ pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material, } R_{\theta CA} \text{ is determined by the user's board design.}$



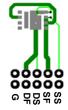
a. 60 °C/W when mounted on a 1 in² pad of 2 oz copper



b. 55 °C/W when mounted on a 1 in² pad of 2 oz copper



c. 130 °C/W when mounted on a minimum pad of 2 oz copper



d. 120 °C/W when mounted on a minimum pad of 2 oz copper

- 2 Pulse Test: Pulse Width < 300 $\mu\text{s},$ Duty cycle < 2.0%.
- 3. Q1 :E_{AS} of 54 mJ is based on starting T_J = 25 o C; L = 3 mH, I_{AS} = 6 A, V_{DD} = 30 V, V_{GS} = 10 V. 100% tested at L = 0.1 mH, I_{AS} = 20 A. Q2: E_{AS} of 96 mJ is based on starting T_J = 25 o C; L = 3 mH, I_{AS} = 8 A, V_{DD} = 30 V, V_{GS} = 10 V. 100% tested at L = 0.1 mH, I_{AS} = 27 A.
- 4. Pulsed Id refer to Fig.11 and Fig.24 SOA curve for more details.
- 5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted.

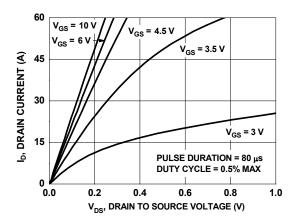


Figure 1. On Region Characteristics

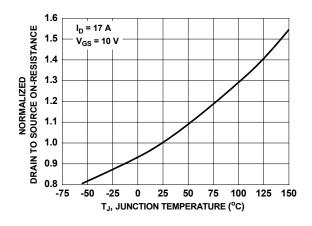


Figure 3. Normalized On Resistance vs. Junction Temperature

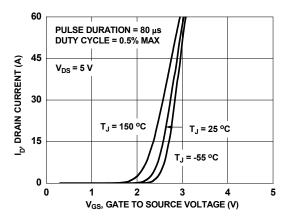


Figure 5. Transfer Characteristics

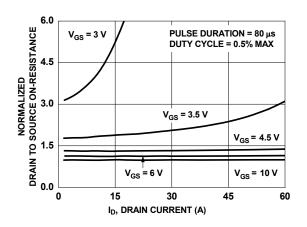


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

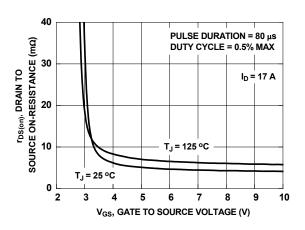


Figure 4. On-Resistance vs. Gate to Source Voltage

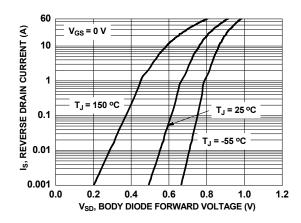


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted.

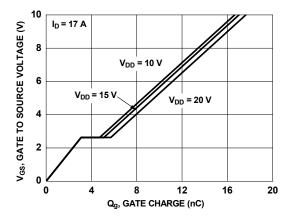


Figure 7. Gate Charge Characteristics

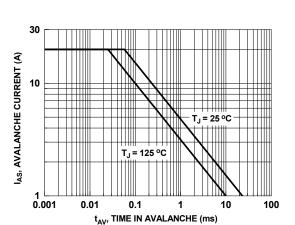


Figure 9. Unclamped Inductive Switching Capability

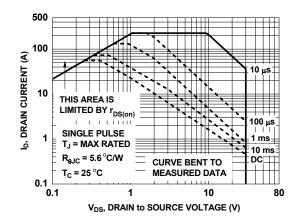


Figure 11. Forward Bias Safe Operating Area

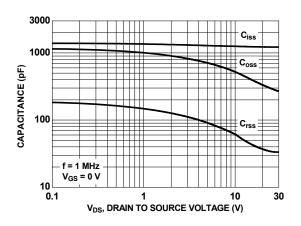


Figure 8. Capacitance vs. Drain to Source Voltage

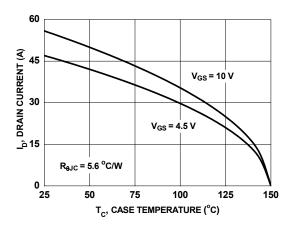


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

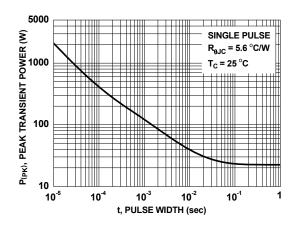


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted.

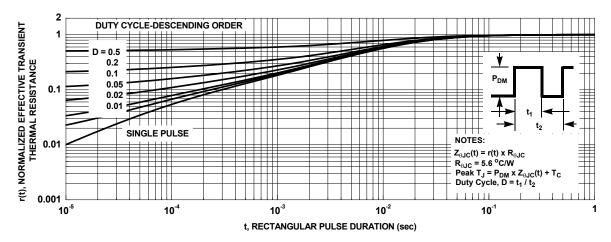


Figure 13. Junction-to-Case Transient Thermal Response Curve

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unless otherwise noted.

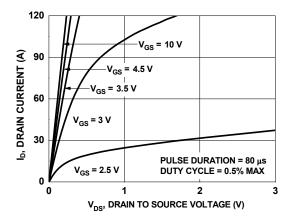


Figure 14. On-Region Characteristics

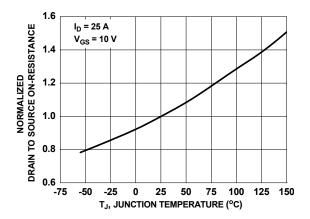


Figure 16. Normalized On-Resistance vs. Junction Temperature

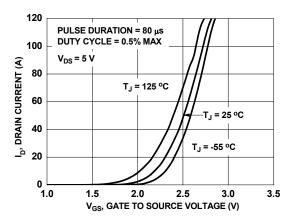


Figure 18. Transfer Characteristics

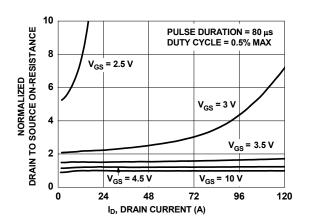


Figure 15. Normalized on-Resistance vs. Drain Current and Gate Voltage

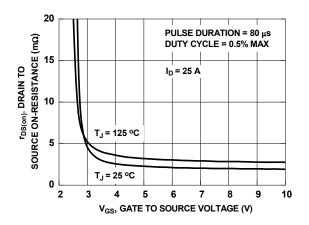


Figure 17. On-Resistance vs. Gate to Source Voltage

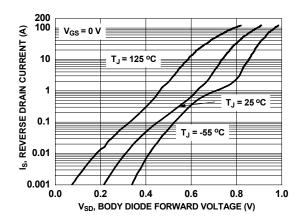


Figure 19. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics (Q2 N-Channel) T_{.I} = 25°C unless otherwise noted.

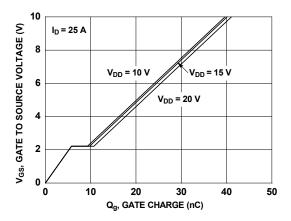


Figure 20. Gate Charge Characteristics

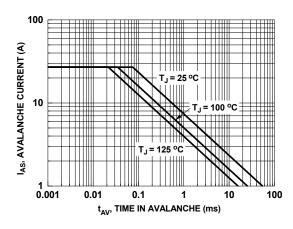


Figure 22. Unclamped Inductive Switching Capability

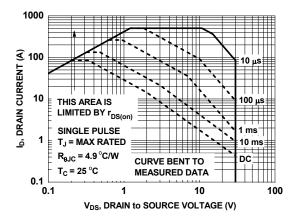


Figure 24. Forward Bias Safe Operating Area

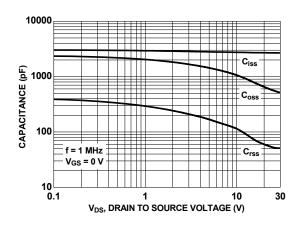


Figure 21. Capacitance vs. Drain to Source Voltage

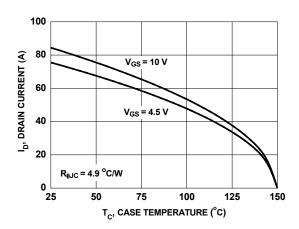


Figure 23. Maximum Continuous Drain Current vs. Case Temperature

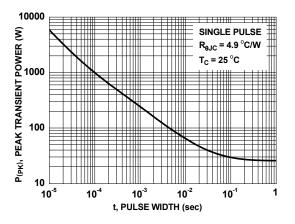


Figure 25. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unless otherwise noted.

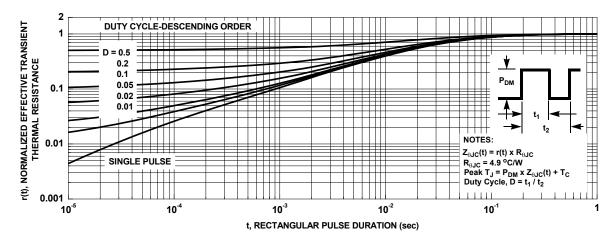


Figure 26. Junction-to-Case Transient Thermal Response Curve

Typical Characteristics (continued)

SyncFETTM Schottky Body Diode Characteristics

Fairchild's SyncFETTM process embeds a Schottky diode in parallel with PowerTrench[®] MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDPC5030SG.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

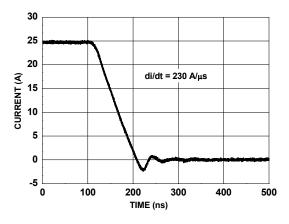


Figure 27. FDPC5030SG SyncFETTM Body Diode Reverse Recovery Characteristic

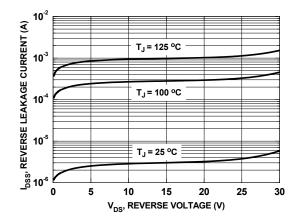
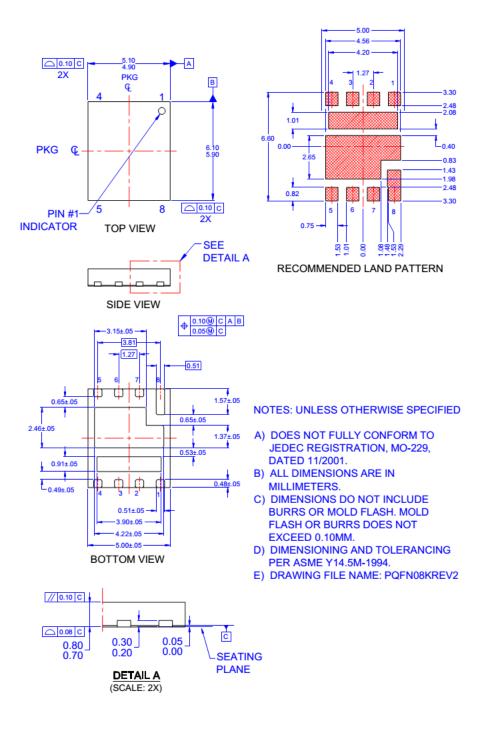


Figure 28. SyncFETTM Body Diode Reverse Leakage vs. Drain-Source Voltage

Dimensional Outline and Pad Layout



Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.





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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
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