EVALUATION KIT AVAILABLE

MAX16833/MAX16833B–MAX16833D

High-Voltage HB LED Drivers with Integrated High-Side Current Sense

General Description

The MAX16833/MAX16833B–MAX16833D are peak current-mode-controlled LED drivers for boost, buck-boost, SEPIC, flyback, and high-side buck topologies. A dimming driver designed to drive an external p-channel in series with the LED string provides wide-range dimming control. This feature provides extremely fast PWM current switching to the LEDs with no transient overvoltage or undervoltage conditions. In addition to PWM dimming, the ICs provide analog dimming using a DC input at ICTRL. The ICs sense the LED current at the high side of the LED string.

A single resistor from RT/SYNC to ground sets the switching frequency from 100kHz to 1MHz, while an external clock signal capacitively coupled to RT/SYNC allows the ICs to synchronize to an external clock. In the MAX16833/MAX16833C, the switching frequency can be dithered for spread-spectrum applications. The MAX16833B/MAX16833D instead provide a 1.64V reference voltage with a 2% tolerance.

The ICs operate over a wide 5V to 65V supply range and include a 3A sink/source gate driver for driving a power MOSFET in high-power LED driver applications. Additional features include a fault-indicator output ($\overline{FLT}$) for short or overtemperature conditions and an overvoltage-protection sense input (OVP) for overvoltage protection. High-side current sensing combined with a p-channel dimming MOSFET allow the positive terminal of the LED string to be shorted to the positive input terminal or to the negative input terminal without any damage. This is a unique feature of the ICs.

Applications

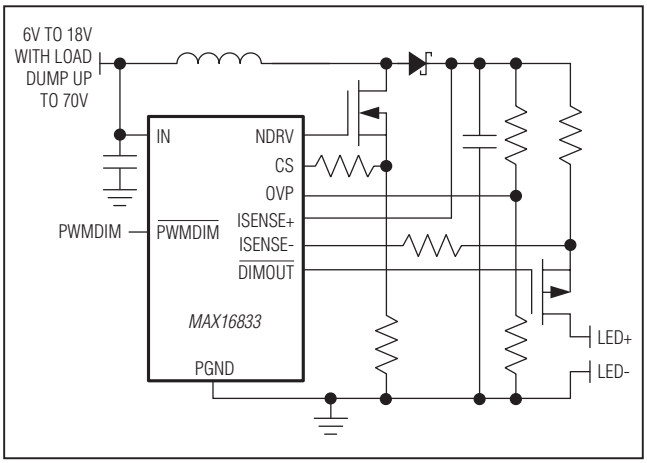
Automotive Exterior Lighting:
- High-Beam/Low-Beam/Signal/Position Lights
- Daytime Running Lights (DRLs)
- Fog Light and Adaptive Front Light Assemblies

Commercial, Industrial, and Architectural Lighting

Features

- **Boost, SEPIC, and Buck-Boost Single-Channel LED Drivers**
- **+5V to +65V Wide Input Voltage Range with a Maximum 65V Boost Output**
- **Integrated High-Side Current-Sense Amplifier**
- **ICTRL Pin for Analog Dimming**
- **Integrated High-Side pMOS Dimming MOSFET Driver (Allows Single-Wire Connection to LEDs)**
- **Programmable Operating Frequency (100kHz to 1MHz) with Synchronization Capability**
- **Frequency Dithering for Spread-Spectrum Applications (MAX16833/MAX16833C)**
- **2% Accurate 1.64V Reference (MAX16833B/MAX16833D)**
- **Full-Scale, High-Side, Current-Sense Voltage of 200mV**
- **Short-Circuit, Overvoltage, and Thermal Protection**
- **Fault Indicator Output**
- **-40°C to +125°C Operating Temperature Range**
- **Thermally Enhanced 5mm x 4.4mm, 16-Pin TSSOP Package with Exposed Pad**

Simplified Operating Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	FUNCTIONALITY	MAX DUTY CYCLE (%)
MAX16833AUE+	-40°C to +125°C	16 TSSOP-EP*	Frequency Dithering	88.5
MAX16833AUE/V+	-40°C to +125°C	16 TSSOP-EP*	Frequency Dithering	88.5

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
/V denotes an automotive qualified part.

Ordering Information continued at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-5187; Rev 5; 4/13

ABSOLUTE MAXIMUM RATINGS

IN to PGND ..... -0.3V to +70V
ISENSE+, ISENSE-, $\overline{DIMOUT}$ to PGND ..... -0.3V to +80V
$\overline{DIMOUT}$ to ISENSE+ .....-9V to +0.3V
ISENSE- to ISENSE+ .....-0.6V to +0.3V
PGND to SGND .....-0.3V to +0.3V
V_{CC} to PGND .....-0.3V to +9V
NDRV to PGND ..... -0.3V to (V_{CC} + 0.3V)
OVP, PWMDIM, COMP, LFRAMP, REF, ICTRL, RT/SYNC, $\overline{FLT}$ to SGND .....-0.3V to +6.0V
CS to PGND .....-0.3V to +6.0V
Continuous Current on IN 100mA
Peak Current on NDRV ..... ±3A
Continuous Current on NDRV ..... ±100mA
Short-Circuit Duration on V_{CC} .....Continuous
Continuous Power Dissipation (T_A = +70°C)
16-Pin TSSOP (derate 26.1mW/°C above +70°C) 2089mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

16 TSSOP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....38.3°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....3°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, R_{RT} = 12.4kΩ, C_{IN} = C_{VCC} = 1µF, C_{LFRAMP}/C_{REF} = 0.1µF, NDRV = COMP = $\overline{DIMOUT}$ = PWMDIM = $\overline{FLT}$ = unconnected, V_{OVP} = V_{CS} = V_{PGND} = V_{SGND} = 0V, $V_{ISENSE+}$ = $V_{ISENSE-}$ = 45V, V_{ICTRL} = 1.40V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM SPECIFICATIONS						
Operational Supply Voltage	V_{IN}		5		65	V
Supply Current	I_{INQ}	PWMDIM = 0, no switching		1.5	2.5	mA
		Switching		2.5	4	
Undervoltage Lockout (UVLO)	$UVLOR_{IN}$	V_{IN} rising	4.2	4.55	4.85	V
	$UVLOF_{IN}$	V_{IN} falling, I_{VCC} = 35mA	4.05	4.3	4.65	
UVLO Hysteresis				250		mV
Startup Delay	t_{START_DELAY}	During power-up		410		µs
UVLO Falling Delay	t_{FALL_DELAY}	During power-down		3.3		µs
V_{CC} LDO REGULATOR						
Regulator Output Voltage	V_{CC}	0.1mA ≤ I_{VCC} ≤ 50mA, 9V ≤ V_{IN} ≤ 14V	6.75	6.95	7.15	V
		14V ≤ V_{IN} ≤ 65V, I_{VCC} = 10mA				
Dropout Voltage	V_{DOVCC}	I_{VCC} = 50mA, V_{IN} = 5V		0.15	0.35	V
Short-Circuit Current	I_{MAXVCC}	V_{CC} = 0V, V_{IN} = 5V	55	100	150	mA
OSCILLATOR (RT/SYNC)						
Switching Frequency Range	f_{SW}		100		1000	kHz
Bias Voltage at RT/SYNC	V_{RT}			1		V
Maximum Duty Cycle	D_{MAX}	V_{CS} = 0V; MAX16833/MAX16833B only	87.5	88.5	89.5	%
		V_{CS} = 0V; MAX16833C/MAX16833D only	93	94	95	
Oscillator Frequency Accuracy			-5		+5	%

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V, R_{RT} = 12.4kΩ, C_{IN} = C_{VCC} = 1µF, C_{LFRAMP}/C_{REF} = 0.1µF, NDRV = COMP = $\overline{DIMOUT}$ = PWMDIM = $\overline{FLT}$ = unconnected, V_{OVP} = V_{CS} = V_{PGND} = V_{SGND} = 0V, $V_{ISENSE+}$ = $V_{ISENSE-}$ = 45V, V_{ICTRL} = 1.40V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Synchronization Logic-High Input	$V_{IH-SYNC}$	VRT rising	3.8			V
Synchronization Frequency Range	f_{SYNCIN}		1.1f_{SW}		1.7f_{SW}	
SLOPE COMPENSATION						
Slope Compensation Current-Ramp Height	I_{SLOPE}	Ramp peak current added to CS input per switching cycle	46	50	54	µA
DITHERING RAMP GENERATOR (LFRAMP) (MAX16833/MAX16833C only)						
Charging Current		V_{LFRAMP} = 0V	80	100	120	µA
Discharging Current		V_{LFRAMP} = 2.2V	80	100	120	µA
Comparator High Trip Threshold				2		V
Comparator Low Trip Threshold				V_{RT}		V
REFERENCE OUTPUT (REF) (MAX16833B/MAX16833D only)						
Reference Output Voltage	V_{REF}	I_{REF} = 0 to 80µA	1.604	1.636	1.669	V
ANALOG DIMMING (ICTRL)						
Input-Bias Current	IB_{ICTRL}	V_{ICTRL} = 0.62V	0	35	200	nA
LED CURRENT-SENSE AMPLIFIER						
ISENSE+ Input-Bias Current	$IB_{ISENSE+}$	$V_{ISENSE+}$ = 65V, $V_{ISENSE-}$ = 64.8V	200	400	700	µA
ISENSE+ Input-Bias Current with DIM Low	$IB_{ISENSE+OFF}$	$V_{ISENSE+}$ = 48V, $V_{ISENSE-}$ = 48V, PWMDIM = 0		200		µA
ISENSE- Input-Bias Current	$IB_{ISENSE-}$	$V_{ISENSE+}$ = 65V, $V_{ISENSE-}$ = 64.8V	2	5	8	µA
Voltage Gain				6.15		V/V
Current-Sense Voltage	V_{SENSE}	V_{ICTRL} = 1.4V	195	199	203	mV
		V_{ICTRL} = 0.616V		100		
		V_{ICTRL} = 0.2465V	38.4	40	41.4	
Bandwidth	BW	AV_{DC} - 3dB		5		MHz
COMP						
Transconductance	GM_{COMP}		2100	3500	4900	µS
Open-Loop DC Gain	AV_{OTA}			75		dB
COMP Input Leakage	I_{LCOMP}		-300		+300	nA
COMP Sink Current	I_{SINK}		100	400	700	µA
COMP Source Current	I_{SOURCE}		100	400	700	µA
PWM COMPARATOR						
Input Offset Voltage	V_{OS-PWM}			2		V
Leading-Edge Blanking				50		ns
Propagation Delay to NDRV	$t_{ON(MIN)}$	Includes leading-edge blanking time with 10mV overdrive	55	80	110	ns
CS LIMIT COMPARATOR						
Current-Limit Threshold	V_{CS_LIMIT}		406	418	430	mV
CS Limit-Comparator Propagation Delay to NDRV	t_{CS_PROP}	10mV overdrive (excluding leading-edge blanking time)		30		ns
Leading-Edge Blanking				50		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V, R_{RT} = 12.4kΩ, C_{IN} = C_{VCC} = 1µF, C_{LFRAMP}/C_{REF} = 0.1µF, NDRV = COMP = $\overline{DIMOUT}$ = PWMDIM = $\overline{FLT}$ = unconnected, V_{OVP} = V_{CS} = V_{PGND} = V_{SGND} = 0V, $V_{ISENSE+}$ = $V_{ISENSE-}$ = 45V, V_{ICTRL} = 1.40V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GATE DRIVER (NDRV)						
Peak Pullup Current	I_{NDRVPU}	V_{CC} = 7V, V_{NDRV} = 0V		3		A
Peak Pulldown Current	I_{NDRVPD}	V_{CC} = 7V, V_{NDRV} = 7V		3		A
Rise Time	t_r	C_{NDRV} = 10nF		30		ns
Fall Time	t_f	C_{NDRV} = 10nF		30		ns
R_{DSON} Pulldown nMOS	R_{NDRVON}	V_{COMP} = 0V, I_{SINK} = 100mA	0.25	0.6	1.1	Ω
PWM DIMMING (PWMDIM)						
ON Threshold	V_{PWMON}		1.19	1.225	1.26	V
Hysteresis	V_{PWMHY}			70		mV
Pullup Resistance	R_{PWMPU}		1.7	3	4.5	MΩ
PWMDIM to LED Turn-Off Time		PWMDIM falling edge to rising edge on $\overline{DIMOUT}$, $C_{\overline{DIMOUT}}$ = 7nF		2		µs
PWMDIM to LED Turn-On Time		PWMDIM rising edge to falling edge on $\overline{DIMOUT}$, $C_{\overline{DIMOUT}}$ = 7nF		3		µs
pMOS GATE DRIVER ($\overline{DIMOUT}$)						
Peak Pullup Current	$I_{DIMOUTPU}$	V_{PWMDIM} = 0V, $V_{ISENSE+}$ - $V_{\overline{DIMOUT}}$ = 7V	25	50	80	mA
Peak Pulldown Current	$I_{DIMOUTPD}$	$V_{ISENSE+}$ - $V_{\overline{DIMOUT}}$ = 0V	10	25	45	mA
$\overline{DIMOUT}$ Low Voltage with Respect to $V_{ISENSE+}$			-8.7	-7.4	-6.3	V
OVERVOLTAGE PROTECTION (OVP)						
Threshold	V_{OVPOFF}	V_{OVP} rising	1.19	1.225	1.26	V
Hysteresis	V_{OVPHY}			70		mV
Input Leakage	I_{LOVP}	V_{OVP} = 1.235V	-300		+300	nA
SHORT-CIRCUIT HICCUP MODE						
Short-Circuit Threshold	$V_{SHORT-HIC}$	($V_{ISENSE+}$ - $V_{ISENSE-}$) rising	285	298	310	mV
Hiccup Time	t_{HICCUP}			8192		Clock Cycles
Delay in Short-Circuit Hiccup Activation				1		µs
BUCK-BOOST SHORT-CIRCUIT DETECT						
Buck-Boost Short-Circuit Threshold	$V_{SHORT-BB}$	($V_{ISENSE+}$ - V_{IN}) falling, V_{IN} = 12V	1.15	1.55	1.9	V
Delay in $\overline{FLT}$ Assertion from Buck-Boost Short-Circuit Condition	$t_{DEL-BB-SHRT}$	Counter increments only when V_{PWMDIM} > V_{PWMON}		8192		Clock Cycles
Delay in $\overline{FLT}$ Deassertion After Buck-Boost Short Circuit is Removed (Consecutive Clock-Cycle Count)		Counter increments only when V_{PWMDIM} > V_{PWMON}		8192		Clock Cycles

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V, R_{RT} = 12.4kΩ, C_{IN} = C_{VCC} = 1µF, C_{LFRAMP}/C_{REF} = 0.1µF, NDRV = COMP = $\overline{DIMOUT}$ = PWMDIM = $\overline{FLT}$ = unconnected, V_{OVP} = V_{CS} = V_{PGND} = V_{SGND} = 0V, $V_{ISENSE+}$ = $V_{ISENSE-}$ = 45V, V_{ICTRL} = 1.40V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

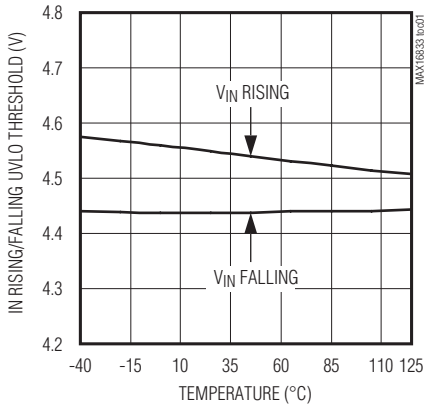
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OPEN-DRAIN FAULT ($\overline{FLT}$)						
Output Voltage Low	$V_{OL-\overline{FLT}}$	V_{IN} = 4.75V, V_{OVP} = 2V, and I_{SINK} = 5mA		40	200	mV
Output Leakage Current		$V_{\overline{FLT}}$ = 5V			1	µA
THERMAL SHUTDOWN						
Thermal-Shutdown Temperature		Temperature rising		+160		°C
Thermal-Shutdown Hysteresis				10		°C

Note 2: All devices are 100% tested at T_A = +25°C. Limits over temperature are guaranteed by design.

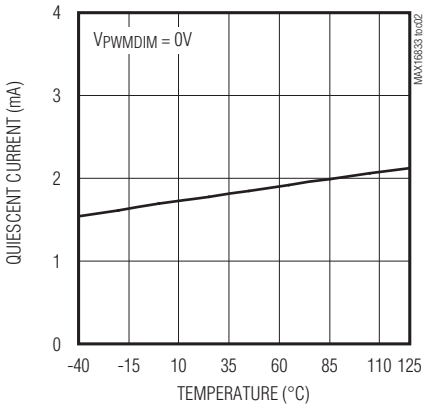
Typical Operating Characteristics

(V_{IN} = +12V, C_{VIN} = C_{VCC} = 1µF, C_{LFRAMP}/C_{REF} = 0.1µF, T_A = +25°C, unless otherwise noted.)

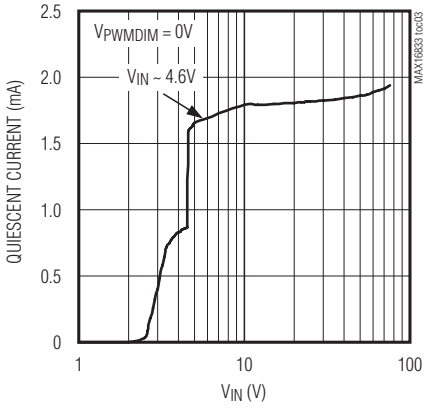
IN RISING/FALLING UVLO THRESHOLD vs. TEMPERATURE



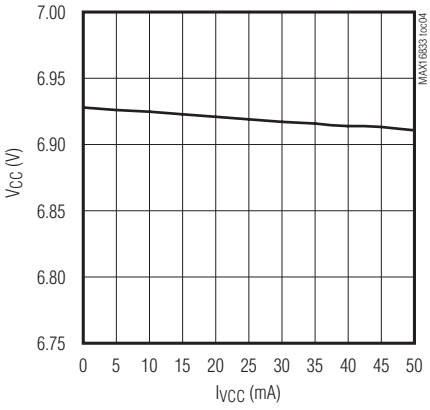
QUIESCENT CURRENT vs. TEMPERATURE



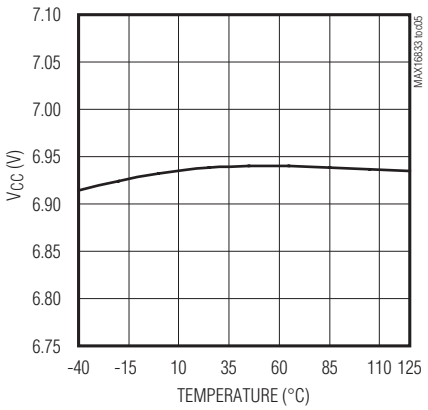
QUIESCENT CURRENT vs. V_{IN}



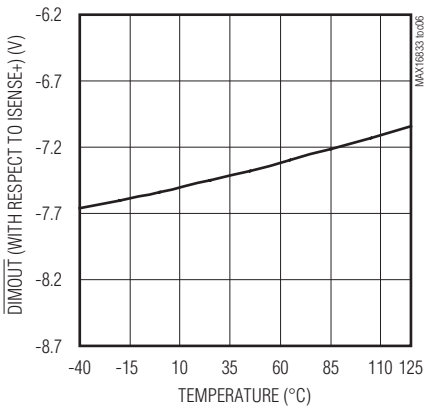
V_{CC} vs. I_{VCC}



V_{CC} vs. TEMPERATURE



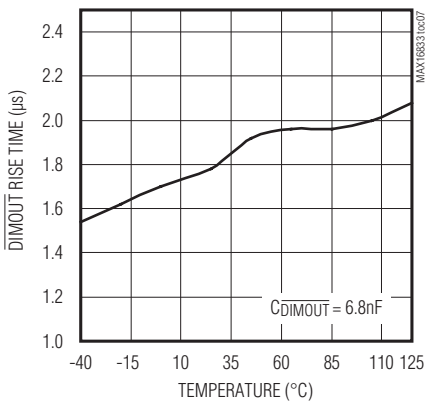
$\overline{DIMOUT}$ (WITH RESPECT TO ISENSE+) vs. TEMPERATURE



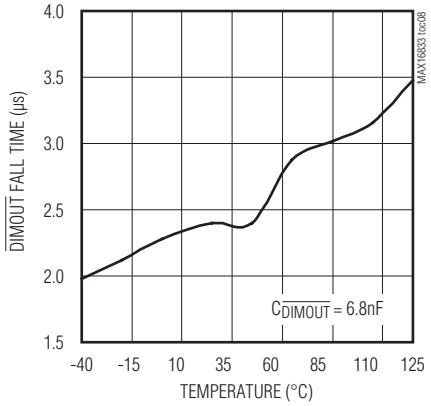
Typical Operating Characteristics (continued)

(V_{IN} = +12V, C_{VIN} = C_{VCC} = 1µF, C_{LFRAMP}/C_{REF} = 0.1µF, T_A = +25°C, unless otherwise noted.)

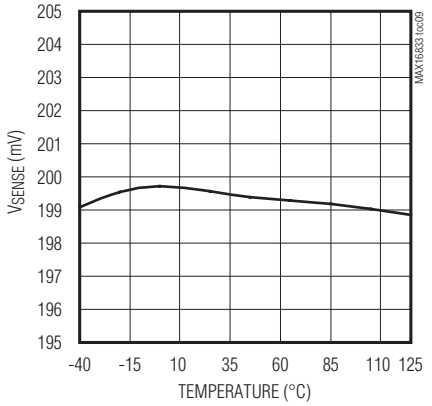
$\overline{DIMOUT}$ RISE TIME vs. TEMPERATURE



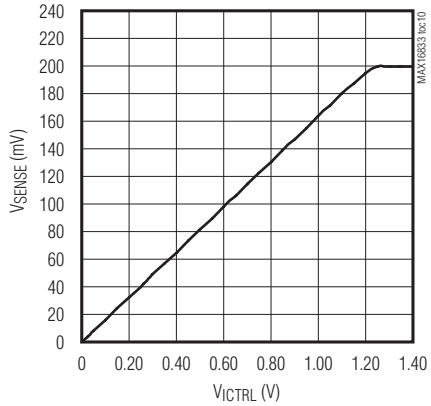
$\overline{DIMOUT}$ FALL TIME vs. TEMPERATURE



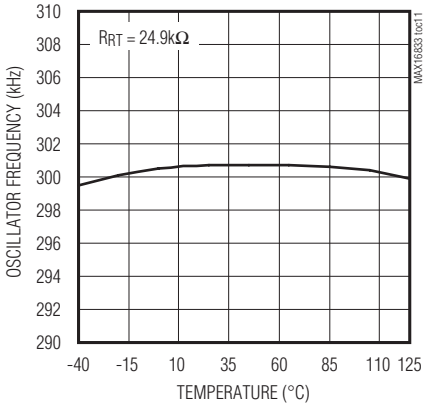
V_{SENSE} vs. TEMPERATURE



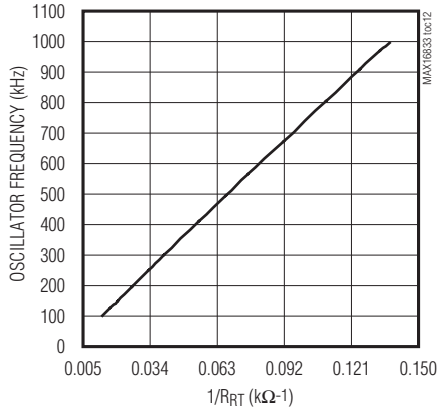
V_{SENSE} vs. V_{ICTRL}



OSCILLATOR FREQUENCY vs. TEMPERATURE (MAX16833/MAX16833B ONLY)



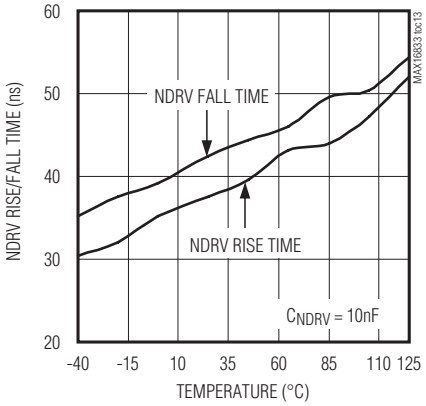
OSCILLATOR FREQUENCY vs. 1/R_{RT} CONDUCTANCE (MAX16833/MAX16833B ONLY)



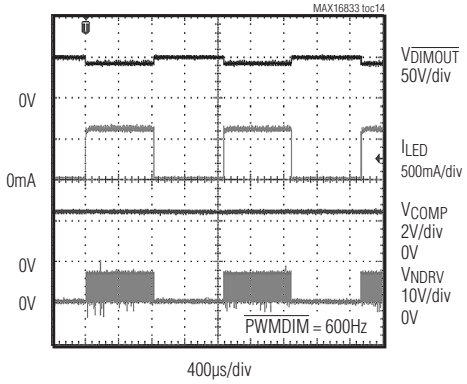
Typical Operating Characteristics (continued)

(V_{IN} = +12V, C_{VIN} = C_{VCC} = 1µF, C_{LFRAMP}/C_{REF} = 0.1µF, T_A = +25°C, unless otherwise noted.)

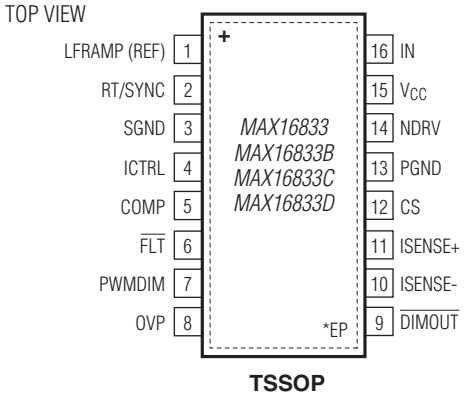
NDRV RISE/FALL TIME vs. TEMPERATURE



600Hz DIMMING OPERATION



Pin Configuration



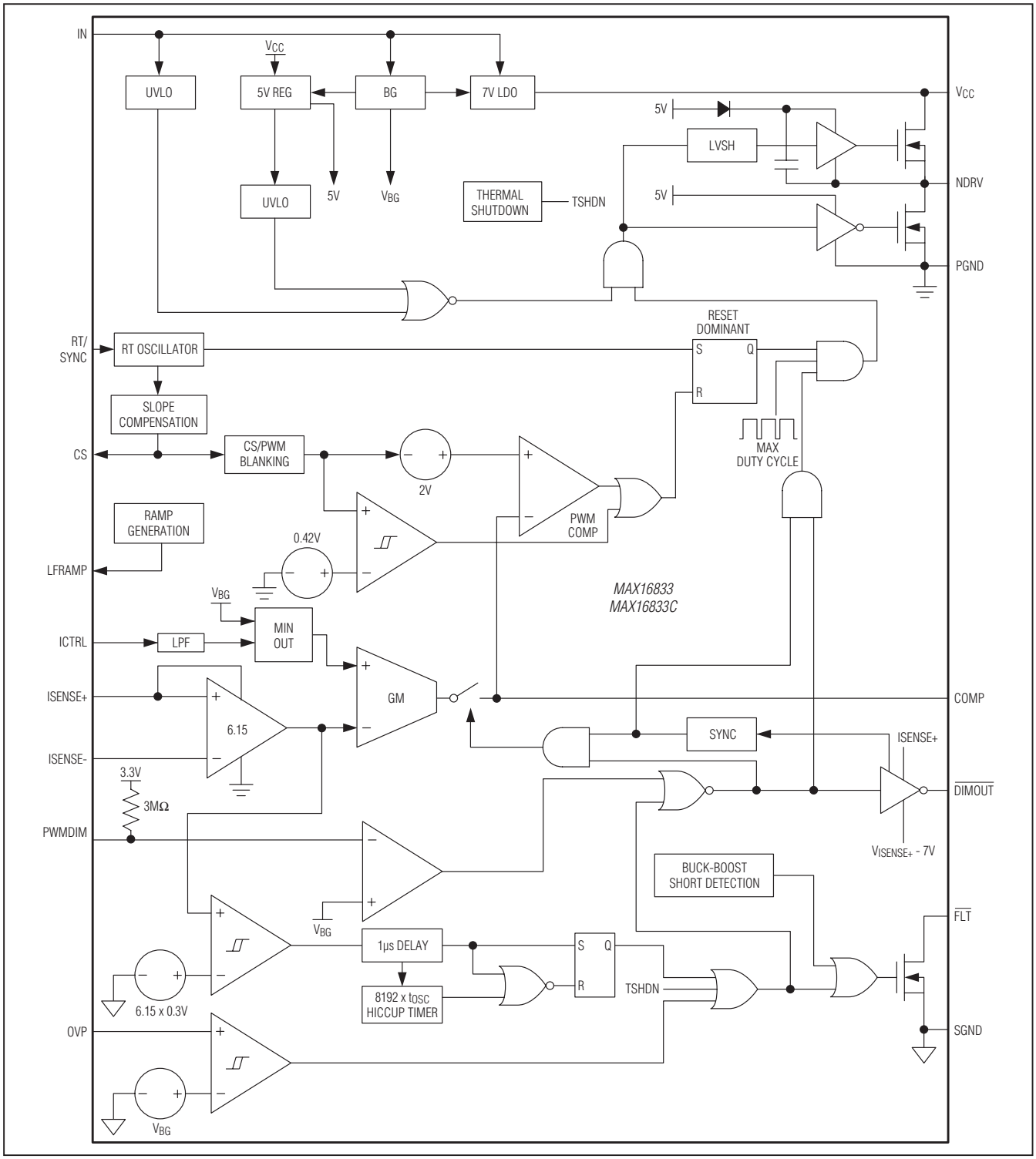
TSSOP

*EP = EXPOSED PAD.
( ) FOR MAX16833B/MAX16833D ONLY.

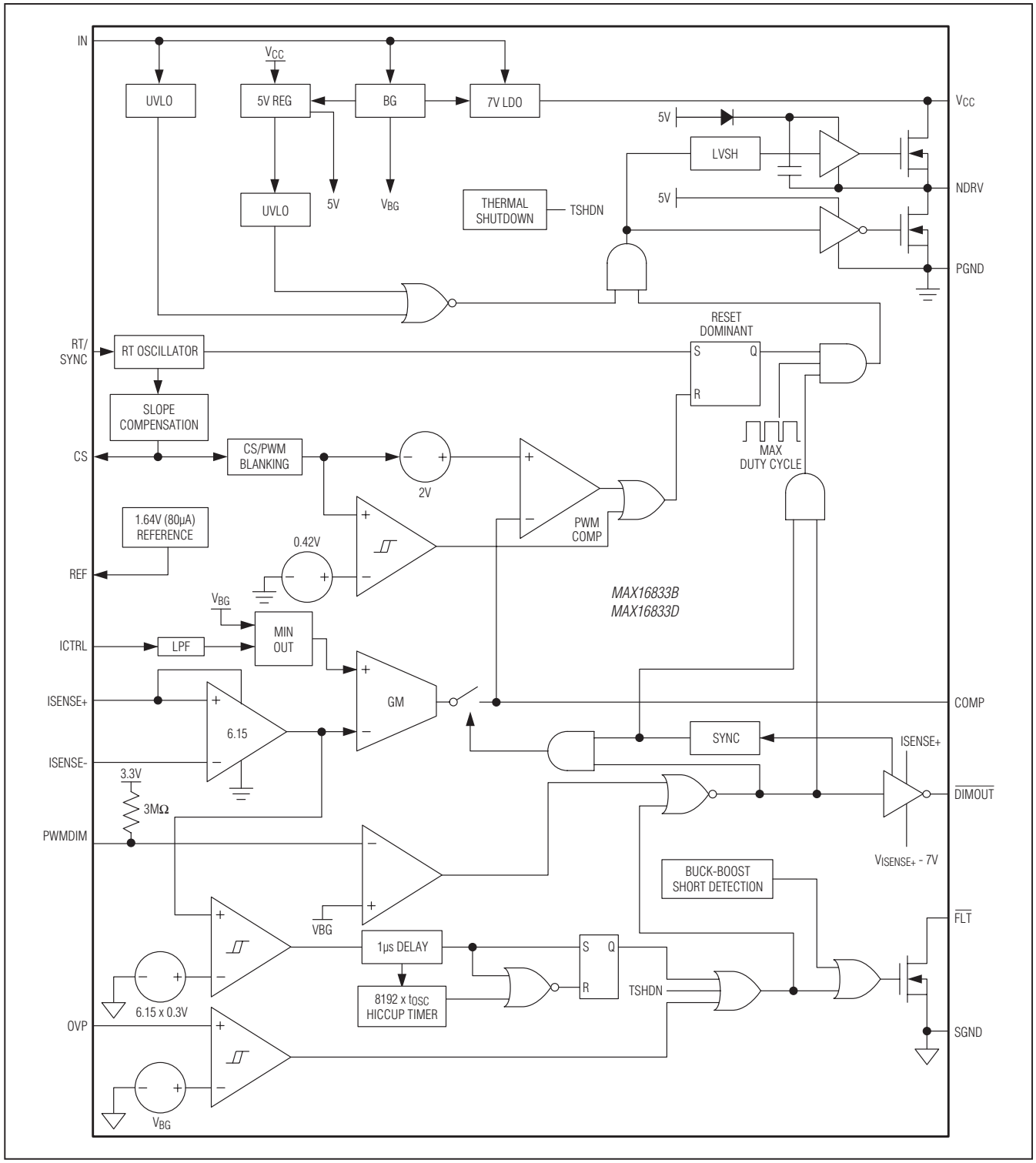
Pin Description

PIN	NAME	FUNCTION
1	LFRAMP (MAX16833/ MAX16833C)	Low-Frequency Ramp Output. Connect a capacitor from LFRAMP to ground to program the ramp frequency, or connect to SGND if not used. A resistor can be connected between LFRAMP and RT/SYNC to dither the PWM switching frequency to achieve spread spectrum.
	REF (MAX16833B/ MAX16833D)	1.64V Reference Output. Connect a 1µF ceramic capacitor from REF to SGND to provide a stable reference voltage. Connect a resistive divider from REF to ICTRL for analog dimming.
2	RT/SYNC	PWM Switching Frequency Programming Input. Connect a resistor (R_{RT}) from RT/SYNC to SGND to set the internal clock frequency. Frequency = (7.350 x 10^9)/R_{RT} for the MAX16833/MAX16833B. Frequency = (6.929 x10^9)/R_{RT} for the MAX16833C/MAX16833D. An external pulse can be applied to RT/SYNC through a coupling capacitor to synchronize the internal clock to the external pulse frequency. The parasitic capacitance on RT/SYNC should be minimized.
3	SGND	Signal Ground
4	ICTRL	Analog Dimming-Control Input. The voltage at ICTRL sets the LED current level when V_{ICTRL} < 1.2V. For V_{ICTRL} > 1.4V, the internal reference sets the LED current.
5	COMP	Compensation Network Connection. For proper compensation, connect a suitable RC network from COMP to ground.
6	$\overline{FLT}$	Active-Low, Open-Drain Fault Indicator Output. See the *Fault Indicator ($\overline{FLT}$)* section.
7	PWMDIM	PWM Dimming Input. When PWMDIM is pulled low, $\overline{DIMOUT}$ is pulled high and PWM switching is disabled. PWMDIM has an internal pullup resistor, defaulting to a high state when left unconnected.
8	OVP	LED String Overvoltage-Protection Input. Connect a resistive divider between ISENSE+, OVP, and SGND. When the voltage on OVP exceeds 1.23V, a fast-acting comparator immediately stops PWM switching. This comparator has a hysteresis of 70mV.
9	$\overline{DIMOUT}$	Active-Low External Dimming p-Channel MOSFET Gate Driver
10	ISENSE-	Negative LED Current-Sense Input. A 100Ω resistor is recommended to be connected between ISENSE- and the negative terminal of the LED current-sense resistor. This preserves the absolute maximum rating of the ISENSE- pin during LED short circuit.
11	ISENSE+	Positive LED Current-Sense Input. The voltage between ISENSE+ and ISENSE- is proportionally regulated to the lesser of V_{ICTRL} or 1.23V.
12	CS	Switching Regulator Current-Sense Input. Add a resistor from CS to switching MOSFET current-sense resistor terminal for programming slope compensation.
13	PGND	Power Ground
14	NDRV	External n-channel MOSFET Gate-Driver Output
15	V_{CC}	7V Low-Dropout Voltage Regulator Output. Bypass V_{CC} to PGND with a 1µF (min) ceramic capacitor.
16	IN	Positive Power-Supply Input. Bypass IN to PGND with at least a 1µF ceramic capacitor.
—	EP	Exposed Pad. Connect EP to the ground plane for heatsinking. Do not use EP as the only electrical connection to ground.

MAX16833/MAX16833C Functional Diagram



MAX16833B/MAX16833D Functional Diagram



Detailed Description

The MAX16833/MAX16833B–MAX16833D are peak current-mode-controlled LED drivers for boost, buck-boost, SEPIC, flyback, and high-side buck topologies. A low-side gate driver capable of sinking and sourcing 3A can drive a power MOSFET in the 100kHz to 1MHz frequency range. Constant-frequency peak current-mode control is used to control the duty cycle of the PWM controller that drives the power MOSFET. Externally programmable slope compensation prevents subharmonic oscillations for duty cycles exceeding 50% when the inductor is operating in continuous conduction mode. Most of the power for the internal control circuitry inside the ICs is provided from an internal 5V regulator. The gate drive for the low-side switching MOSFET is provided by a separate V_{CC} regulator. A dimming driver designed to drive an external p-channel in series with the LED string provides wide-range dimming control. This dimming driver is powered by a separate unconnected reference -7V regulator. This feature provides extremely fast PWM current switching to the LEDs with no transient overvoltage or undervoltage conditions. In addition to PWM dimming, the ICs provide analog dimming using a DC input at the ICTRL input.

A single resistor from RT/SYNC to ground sets the switching frequency from 100kHz to 1MHz, while an external clock signal capacitively coupled to RT/SYNC allows the ICs to synchronize to an external clock. The switching frequency can be dithered for spread-spectrum applications by connecting the LFRAMP output to RT/SYNC through an external resistor in the MAX16833/MAX16833C. In the MAX16833B/MAX16833D, the LFRAMP output is replaced by a REF output, which provides a regulated 1.64V, 2% accurate reference that can be used with a resistive divider from REF to ICTRL to set the LED current. The maximum current from the REF output cannot exceed 80µA.

Additional features include a fault-indicator output ($\overline{FLT}$) for short, overvoltage, or overtemperature conditions and an overvoltage-protection (OVP) sense input for overvoltage protection. In case of LED string short, for a buck-boost configuration, the short-circuit current is equal to the programmed LED current. In the case of boost configuration, the ICs enter hiccup mode with automatic recovery from short circuit.

UVLO

The ICs feature undervoltage lockout (UVLO) using the positive power-supply input (IN). The ICs are enabled when V_{IN} exceeds the 4.6V (typ) threshold and are disabled when V_{IN} drops below the 4.35V (typ) threshold. The UVLO is internally fixed and cannot be adjusted. There is a startup delay of 300µs (typ) + 64 switching clock cycles on power-up after the UVLO threshold is crossed. There is a 3.3µs delay on power-down on the falling edge of the UVLO.

Dimming MOSFET Driver ($\overline{DIMOUT}$)

The ICs require an external p-channel MOSFET for PWM dimming. For normal operation, connect the gate of the MOSFET to the output of the dimming driver ($\overline{DIMOUT}$). The dimming driver can sink up to 25mA or source up to 50mA of peak current for fast charging and discharging of the p-MOSFET gate. When the PWMDIM signal is high, this driver pulls the p-MOSFET gate to 7V below the ISENSE+ pin to completely turn on the p-channel dimming MOSFET.

n-Channel MOSFET Switch Driver (NDRV)

The ICs drive an external n-channel switching MOSFET. NDRV swings between V_{CC} and PGND. NDRV can sink/source 3A of peak current, allowing the ICs to switch MOSFETs in high-power applications. The average current demanded from the supply to drive the external MOSFET depends on the total gate charge (Q_G) and the operating frequency of the converter, f_{SW}. Use the following equation to calculate the driver supply current I_{NDRV} required for the switching MOSFET:

$$I_{NDRV} = Q_G \times f_{SW}$$

Pulse-Dimming Input (PWMDIM)

The ICs offer a dimming input (PWMDIM) for pulse-width modulating the output current. PWM dimming can be achieved by driving PWMDIM with a pulsating voltage source. When the voltage at PWMDIM is greater than 1.23V, the PWM dimming p-channel MOSFET turns on and the gate drive to the n-channel switching MOSFET is also enabled. When the voltage on PWMDIM drops 70mV below 1.23V, the PWM dimming MOSFET turns off and the n-channel switching MOSFET is also turned off. The COMP capacitor is also disconnected from the internal transconductance amplifier when PWMDIM is low. When left unconnected, a weak internal pullup resistor sets this input to logic-high.

Analog Dimming (ICTRL)

The ICs offer an analog dimming control input (ICTRL). The voltage at ICTRL sets the LED current level when V_{ICTRL} < 1.2V. The LED current can be linearly adjusted from zero with the voltage on ICTRL. For V_{ICTRL} > 1.4V, an internal reference sets the LED current. The maximum withstand voltage of this input is 5.5V.

Low-Side Linear Regulator (VCC)

The ICs feature a 7V low-side linear regulator (V_{CC}). V_{CC} powers up the switching MOSFET driver with sourcing capability of up to 50mA. Use a 1µF (min) low-ESR ceramic capacitor from V_{CC} to PGND for stable operation. The V_{CC} regulator goes below 7V if the input voltage falls below 7V. The dropout voltage for this regulator at 50mA is 0.2V. This means that for an input voltage of 5V, the V_{CC} voltage is 4.8V. The short-circuit current on the V_{CC} regulator is 100mA (typ). Connect V_{CC} to IN if V_{IN} is always less than 7V.

LED Current-Sense Inputs (ISENSE±)

The differential voltage from ISENSE+ to ISENSE- is fed to an internal current-sense amplifier. This amplified signal is then connected to the negative input of the transconductance error amplifier. The voltage-gain factor of this amplifier is 6.15.

The offset voltage for this amplifier is ≤ 1mV.

Internal Transconductance Error Amplifier

The ICs have a built-in transconductance amplifier used to amplify the error signal inside the feedback loop. When the dimming signal is low, COMP is disconnected from the output of the error amplifier and $\overline{DIMOUT}$ goes high. When the dimming signal is high, the output of the error amplifier is connected to COMP and $\overline{DIMOUT}$ goes low. This enables the compensation capacitor to hold the charge when the dimming signal has turned off the internal switching MOSFET gate drive. To maintain the charge on the compensation capacitor C_{COMP} (C4 in the *Typical Operating Circuits*), the capacitor should be a low-leakage ceramic type. When the internal dimming signal is enabled, the voltage on the compensation capacitor forces the converter into steady state almost instantaneously.

Internal Oscillator (RT/SYNC)

The internal oscillators of the ICs are programmable from 100kHz to 1MHz using a single resistor at RT/SYNC. Use the following formula to calculate the switching frequency:

$$f_{OSC}\ (kHz) = \frac{7350\ (k\Omega)}{R_{RT}(k\Omega)}$$ for the MAX16833/MAX16833B

$$f_{OSC}\ (kHz) = \frac{6929(k\Omega)}{R_{RT}(k\Omega)}$$ for the MAX16833C/MAX16833D

where R_{RT} is the resistor from RT/SYNC to SGND.

Synchronize the oscillator with an external clock by AC-coupling the external clock to the RT/SYNC input. For f_{OSC} between 200kHz and 1MHz, the capacitor used for the AC-coupling should satisfy the following relation:

$$C_{SYNC} \le \frac{9.8624 \times 10^{-6}}{R_{RT}} - 0.144 \times 10^{-9}\ \text{farads}$$

where R_{RT} is in kΩ. For f_{OSC} below 200GHz, C_{SYNC} ≤ 268nF.

The pulse width for the synchronization pulse should satisfy the following relations:

$$\frac{t_{PW}}{t_{CLK}} < \frac{0.5}{V_S} \quad \text{and} \quad \frac{t_{PW}}{t_{CLK}} < \left(1 - \frac{1.05 \times t_{CLK}}{t_{OSC}}\right)$$

$$3.4V < \left(0.8 - \frac{t_{PW}}{t_{CLK}} V_S\right) + V_S < 5V$$

where t_{PW} is the synchronization source pulse width, t_{CLK} is the synchronization clock time period, t_{OSC} is the free-running oscillator time period, and V_S is the synchronization pulse-voltage level.

Ensure that the external clock signal frequency is at least 1.1 x f_{OSC}, where f_{OSC} is the oscillator frequency set by R_{RT}. A typical pulse width of 200ns can be used for proper synchronization of a frequency up to 250kHz. A rising external clock edge (sync) is interpreted as a synchronization input. If the sync signal is lost, the internal oscillator takes control of the switching rate returning the switching frequency to that set by R_{RT}. This maintains output regulation even with intermittent sync signals.

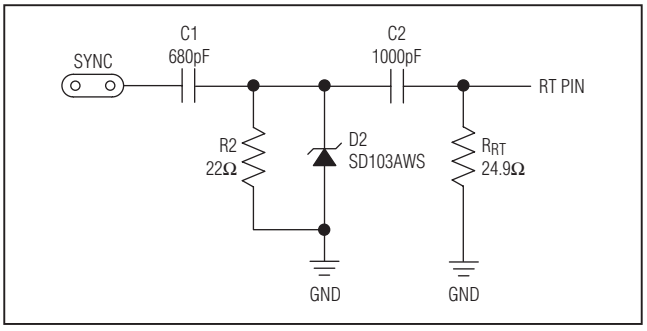


Figure 1. SYNC Circuit

Figure 1 shows the frequency-synchronization circuit suitable for applications where a 5V amplitude pulse with 20% to 80% duty cycle is available as the synchronization source. This circuit can be used for SYNC frequencies in the 100kHz to 1MHz range. C1 and R2 act as a differentiator that reduces the input pulse width to suit the ICs' RT/SYNC input. D2 bypasses the negative current through C1 at the falling edge of the SYNC source to limit the minimum voltage at the RT/SYNC pin. The differentiator output is AC-coupled to the RT/SYNC pin through C2.

The output impedance of the SYNC source should be low enough to drive the current through R2 on the rising edge. The rise/fall times of the SYNC source should be less than 50ns to avoid excessive voltage drop across C1 during the rise time. The amplitude of the SYNC source can be between 4V and 5V. If the SYNC source amplitude is 5V and the rise time is less than 20ns, then the maximum peak voltage at RT/SYNC pin can get close to 6V. Under such conditions, it is desirable to use a resistor in series with C1 to reduce the maximum voltage at the RT/SYNC pin. For proper synchronization, the peak SYNC pulse voltage at RT/SYNC pin should exceed 3.8V.

Frequency Dithering (LFRAMP/MAX16833/MAX16833C)

The MAX16833/MAX16833C feature a low-frequency ramp output. Connect a capacitor from LFRAMP to ground to program the ramp frequency. Connect to SGND if not used. A resistor can be connected between LFRAMP and RT/SYNC to dither the PWM switching frequency to achieve spread spectrum. A lower value resistor provides a larger amount of frequency dithering. The LFRAMP voltage is a triangular waveform between 1V (typ) and 2V (typ). The ramp frequency is given by:

$$f_{LFRAMP}(Hz) = \frac{50\mu A}{C_{LFRAMP}(F)}$$

Voltage-Reference Output (REF/MAX16833B/MAX16833D)

The MAX16833B/MAX16833D have a 2% accurate 1.64V reference voltage on the REF output. Connect a 1µF ceramic capacitor from REF to SGND to provide a stable reference voltage. This reference can supply up to 80µA. This output can drive a resistive divider to the ICTRL input for analog dimming. The resistance from REF to ground should be greater than 20.5kΩ.

Switching MOSFET Current-Sense Input (CS)

CS is part of the current-mode control loop. The switching control uses the voltage on CS, set by R_{CS} (R4 in the *Typical Operating Circuits*) and R_{SLOPE} (R1 in the *Typical Operating Circuits*), to terminate the on pulse width of the switching cycle, thus achieving peak current-mode control. Internal leading-edge blanking of 50ns is provided to prevent premature turn-off of the switching MOSFET in each switching cycle. Resistor R_{CS} is connected between the source of the n-channel switching MOSFET and PGND.

During switching, a current ramp with a slope of 50µA x f_{SW} is sourced from the CS input. This current ramp, along with resistor R_{SLOPE}, programs the amount of slope compensation.

Overvoltage-Protection Input (OVP)

OVP sets the overvoltage-threshold limit across the LEDs. Use a resistive divider between ISENSE+ to OVP and SGND to set the overvoltage-threshold limit. An internal overvoltage-protection comparator senses the differential voltage across OVP and SGND. If the differential voltage is greater than 1.23V, NDRV goes low, $\overline{DIMOUT}$ goes high, and $\overline{FLT}$ asserts. When the differential voltage drops by 70mV, NDRV is enabled, $\overline{DIMOUT}$ goes low, and $\overline{FLT}$ deasserts.

Fault Indicator ($\overline{FLT}$)

The ICs feature an active-low, open-drain fault indicator ($\overline{FLT}$). $\overline{FLT}$ goes low when one of the following conditions occur:

- Overvoltage across the LED string
- Short-circuit condition across the LED string
- Overtemperature condition

$\overline{FLT}$ goes high when the fault condition ends.

Thermal Protection

The ICs feature thermal protection. When the junction temperature exceeds +160°C, the ICs turn off the external power MOSFETs by pulling the NDRV low and $\overline{DIMOUT}$ high. External MOSFETs are enabled again after the junction temperature has cooled by 10°C. This results in a cycled output during continuous thermal-overload conditions. Thermal protection protects the ICs in the event of fault conditions.

Short-Circuit Protection

Boost Configuration

In the boost configuration, if the LED string is shorted it causes the (ISENSE+ to ISENSE-) voltage to exceed 300mV. If this condition occurs for ≥ 1µs, the ICs activates the hiccup timer for 8192 clock cycles during which:

- NDRV goes low and $\overline{DIMOUT}$ goes high.
- The error amplifier is disconnected from COMP.
- $\overline{FLT}$ is pulled to SGND.

After the hiccup time has elapsed, the ICs retry. During this retry period, $\overline{FLT}$ is latched and is reset only if there is no short detected after 20µs of retrying.

Buck-Boost Configuration

In the case of the buck-boost configuration, once an LED string short occurs the behavior is different. The ICs maintain the programmed current across the short. In this case, the short is detected when the voltage between ISENSE+ and IN falls below 1.5V. A buck-boost short fault starts an up counter and $\overline{FLT}$ is asserted only after the counter has reached 8192 clock cycles **consecutively**. If for any reason ($V_{ISENSE+}$ - V_{IN} > 1.5V), the counter starts down counting, resulting in $\overline{FLT}$ being deasserted only after 8192 **consecutive** clock cycles of ($V_{ISENSE+}$ - V_{IN} > 1.5V) condition.

Exposed Pad

The ICs' package features an exposed thermal pad on its underside that should be used as a heatsink. This pad lowers the package's thermal resistance by providing a direct heat-conduction path from the die to the PCB. Connect the exposed pad and GND to the system ground using a large pad or ground plane, or multiple vias to the ground plane layer.

Applications Information

Setting the Overvoltage Threshold

The overvoltage threshold is set by resistors R5 and R11 (see the *Typical Operating Circuits*). The overvoltage circuit in the ICs is activated when the voltage on OVP with respect to GND exceeds 1.23V. Use the following equation to set the desired overvoltage threshold:

$$V_{OV} = 1.23V\ (R5 + R11)/R11$$

Programming the LED Current

Normal sensing of the LED current should be done on the high side where the LED current-sense resistor is connected to the boost output. The other side of the LED current-sense resistor goes to the source of the p-channel dimming MOSFET if PWM dimming is desired. The LED current is programmed using R7. When V_{ICTRL} > 1.23V, the internal reference regulates the voltage across R7 to 200mV:

$$I_{LED} = \frac{200mV}{R7}$$

The LED current can also be programmed using the voltage on ICTRL when V_{ICTRL} < 1.2V (analog dimming). The voltage on ICTRL can be set using a resistive divider from the REF output in the case of the MAX16833B/MAX16833D. The current is given by:

$$I_{LED} = \frac{V_{ICTRL}}{R7 \times 6.15}$$

where:

$$V_{ICTRL} = \frac{V_{REF} \times R8}{(R8 + R9)}$$

where V_{REF} is 1.64V and resistors R8 and R9 are in ohms. At higher LED currents there can be noticeable ripple on the voltage across R7. High-ripple voltages can cause a noticeable difference between the programmed value of the LED current and the measured value of the LED current. To minimize this error, the ripple voltage across R7 should be less than 40mV.

Inductor Selection

Boost Configuration

In the boost converter (see the *Typical Operating Circuits*), the average inductor current varies with the line voltage. The maximum average current occurs at the lowest line voltage. For the boost converter, the average inductor current is equal to the input current. Calculate maximum duty cycle using the following equation:

$$D_{MAX} = \frac{V_{LED} + V_D - V_{INMIN}}{V_{LED} + V_D - V_{FET}}$$

where V_{LED} is the forward voltage of the LED string in volts, V_D is the forward drop of rectifier diode D1 in volts (approximately 0.6V), V_{INMIN} is the minimum input-supply voltage in volts, and V_{FET} is the average drain-to-source voltage of the MOSFET Q1 in volts when it is on. Use an approximate value of 0.2V initially to calculate D_{MAX}. A more accurate value of the maximum duty cycle can be calculated once the power MOSFET is selected based on the maximum inductor current.

Use the following equations to calculate the maximum average inductor current IL_{AVG}, peak-to-peak inductor current ripple ΔI_L, and peak inductor current IL_P in amperes:

$$IL_{AVG} = \frac{I_{LED}}{1 - D_{MAX}}$$

Allowing the peak-to-peak inductor ripple to be ΔI_L, the peak inductor current is given by:

$$IL_P = IL_{AVG} + \frac{\Delta I_L}{2}$$

The inductance value (L) of inductor L1 in henries (H) is calculated as:

$$L = \frac{(V_{INMIN} - V_{FET}) \times D_{MAX}}{f_{SW} \times \Delta I_L}$$

where f_{SW} is the switching frequency in hertz, V_{INMIN} and V_{FET} are in volts, and ΔI_L is in amperes.

Choose an inductor that has a minimum inductance greater than the calculated value. The current rating of the inductor should be higher than IL_P at the operating temperature.

Buck-Boost Configuration

In the buck-boost LED driver (see the *Typical Operating Circuits*), the average inductor current is equal to the input current plus the LED current. Calculate the maximum duty cycle using the following equation:

$$D_{MAX} = \frac{V_{LED} + V_D}{V_{LED} + V_D + V_{INMIN} - V_{FET}}$$

where V_{LED} is the forward voltage of the LED string in volts, V_D is the forward drop of rectifier diode D1 (approximately 0.6V) in volts, V_{INMIN} is the minimum input supply voltage in volts, and V_{FET} is the average drain-to-source voltage of the MOSFET Q1 in volts when it is on. Use an approximate value of 0.2V initially to calculate D_{MAX}. A more accurate value of maximum duty cycle can be calculated once the power MOSFET is selected based on the maximum inductor current.

Use the equations below to calculate the maximum average inductor current IL_{AVG}, peak-to-peak inductor current ripple ΔI_L, and peak inductor current IL_P in amperes:

$$IL_{AVG} = \frac{I_{LED}}{1 - D_{MAX}}$$

Allowing the peak-to-peak inductor ripple to be ΔI_L:

$$IL_P = IL_{AVG} + \frac{\Delta I_L}{2}$$

where IL_P is the peak inductor current.

The inductance value (L) of inductor L1 in henries is calculated as:

$$L = \frac{(V_{INMIN} - V_{FET}) \times D_{MAX}}{f_{SW} \times \Delta I_L}$$

where f_{SW} is the switching frequency in hertz, V_{INMIN} and V_{FET} are in volts, and ΔI_L is in amperes. Choose an inductor that has a minimum inductance greater than the calculated value.

Peak Current-Sense Resistor (R4)

The value of the switch current-sense resistor R4 for the boost and buck-boost configurations is calculated as follows:

$$R4 = \frac{0.418V - V_{SC}}{IL_P}\ \Omega$$

where IL_P is the peak inductor current in amperes and V_{SC} is the peak slope compensation voltage.

Slope Compensation

Slope compensation should be added to converters with peak current-mode control operating in continuous-conduction mode with more than 50% duty cycle to avoid current-loop instability and subharmonic oscillations. The minimum amount of slope compensation that is required for stability is:

V_{SCMIN} = 0.5 (inductor current downslope - inductor current upslope) x R4

In the ICs, the slope-compensating ramp is added to the current-sense signal before it is fed to the PWM comparator. Connect a resistor (R1) from CS to the inductor current-sense resistor terminal to program the amount of slope compensation.

The ICs generate a current ramp with a slope of 50µA/t_{OSC} for slope compensation. The current-ramp signal is forced into the external resistor (R1) connected between CS and the source of the external MOSFET, thereby adding a programmable slope compensating voltage (V_{SCOMP}) at the current-sense input CS. Therefore:

$dV_{SC}/dt = (R1 \times 50\mu A)/t_{OSC}$ in V/s

The minimum value of the slope-compensation voltage that needs to be added to the current-sense signal at peak current and at minimum line voltage is:

$$SC_{MIN} = \frac{(D_{MAX} \times (V_{LED} - 2V_{INMIN}) \times R4)}{2 \times L_{MIN} \times f_{SW}} \text{ (V) Boost}$$

$$SC_{MIN} = \frac{(D_{MAX} \times (V_{LED} - V_{INMIN}) \times R4)}{2 \times L_{MIN} \times f_{SW}} \text{ (V) Buck-boost}$$

where f_{SW} is the switching frequency, D_{MAX} is the maximum duty cycle, which occurs at low line, V_{INMIN} is the minimum input voltage, and L_{MIN} is the minimum value of the selected inductor. For adequate margin, the slope-compensation voltage is multiplied by a factor of 1.5. Therefore, the actual slope-compensation voltage is given by:

$V_{SC} = 1.5SC_{MIN}$

From the previous formulas, it is possible to calculate the value of R4 as:

For boost configuration:

$$R4 = \frac{0.418V}{IL_P + 0.75D_{MAX}\frac{V_{LED} - 2V_{INMIN}}{L_{MIN}f_{SW}}}$$

For buck-boost configuration:

$$R4 = \frac{0.418V}{IL_P + 0.75D_{MAX}\frac{V_{LED} - V_{INMIN}}{L_{MIN}f_{SW}}}$$

The minimum value of the slope-compensation resistor (R1) that should be used to ensure stable operation at minimum input supply voltage can be calculated as:

For boost configuration:

$$R1 = \frac{(V_{LED} - 2V_{INMIN}) \times R4 \times 1.5}{2 \times L_{MIN} \times f_{SW} \times 50\mu A}$$

For buck-boost configuration :

$$R1 = \frac{(V_{LED} - V_{INMIN}) \times R4 \times 1.5}{2 \times L_{MIN} \times f_{SW} \times 50\mu A}$$

where f_{SW} is the switching frequency in hertz, V_{INMIN} is the minimum input voltage in volts, V_{LED} is the LED voltage in volts, D_{MAX} is the maximum duty cycle, IL_P is the peak inductor current in amperes, and L_{MIN} is the minimum value of the selected inductor in henries.

Output Capacitor

The function of the output capacitor is to reduce the output ripple to acceptable levels. The ESR, ESL, and the bulk capacitance of the output capacitor contribute to the output ripple. In most applications, the output ESR and ESL effects can be dramatically reduced by using low-ESR ceramic capacitors. To reduce the ESL and ESR effects, connect multiple ceramic capacitors in parallel to achieve the required bulk capacitance. To minimize audible noise generated by the ceramic capacitors during PWM dimming, it could be necessary to minimize the number of ceramic capacitors on the output. In these cases, an additional electrolytic or tantalum capacitor provides most of the bulk capacitance.

Boost and Buck-Boost Configurations

The calculation of the output capacitance is the same for both boost and buck-boost configurations. The output ripple is caused by the ESR and the bulk capacitance of the output capacitor if the ESL effect is considered negligible. For simplicity, assume that the contributions from ESR and the bulk capacitance are equal, allowing 50% of the ripple for the bulk capacitance. The capacitance is given by:

$$C_{OUT} \geq \frac{I_{LED} \times 2 \times D_{MAX}}{V_{OUTRIPPLE} \times f_{SW}}$$

where I_{LED} is in amperes, C_{OUT} is in farads, f_{SW} is in hertz, and $V_{OUTRIPPLE}$ is in volts. The remaining 50% of allowable ripple is for the ESR of the output capacitor. Based on this, the ESR of the output capacitor is given by:

$$ESR_{COUT} < \frac{V_{OUTRIPPLE}}{(IL_P \times 2)}(\Omega)$$

where IL_P is the peak-inductor current in amperes. Use the equation below to calculate the RMS current rating of the output capacitor:

$$I_{COUT(RMS)} = \sqrt{IL_{AVG}{}^2 D_{MAX}(1 - D_{MAX})}$$

Input Capacitor

The input-filter capacitor bypasses the ripple current drawn by the converter and reduces the amplitude of high-frequency current conducted to the input supply. The ESR, ESL, and the bulk capacitance of the input capacitor contribute to the input ripple. Use a low-ESR input capacitor that can handle the maximum input RMS ripple current from the converter. For the boost configuration, the input current is the same as the inductor current. For buck-boost configuration, the input current is the inductor current minus the LED current. However, for both configurations, the ripple current that the input filter capacitor has to supply is the same as the inductor ripple current with the condition that the output filter capacitor should be connected to ground for buck-boost configuration. This reduces the size of the input capacitor, as the input current is continuous with maximum $\pm\Delta I_L/2$. Neglecting the effect of LED current ripple, the calculation of the input capacitor for boost, as well as buck-boost configurations is the same.

Neglecting the effect of the ESL, the ESR, and the bulk capacitance at the input contribute to the input-voltage ripple. For simplicity, assume that the contributions from the ESR and the bulk capacitance are equal. This allows 50% of the ripple for the bulk capacitance. The capacitance is given by:

$$C_{IN} \geq \frac{\Delta I_L}{4 \times \Delta V_{IN} \times f_{SW}}$$

where ΔI_L is in amperes, C_{IN} is in farads, f_{SW} is in hertz, and ΔV_{IN} is in volts. The remaining 50% of allowable ripple is for the ESR of the input capacitor. Based on this, the ESR of the input capacitor is given by:

$$ESR_{CIN} < \frac{\Delta V_{IN}}{\Delta I_L \times 2}$$

where ΔI_L is in amperes, ESR_{CIN} is in ohms, and ΔV_{IN} is in volts. Use the equation below to calculate the RMS current rating of the input capacitor:

$$I_{CIN}(RMS) = \frac{\Delta I_L}{2\sqrt{3}}$$

Selection of Power Semiconductors

Switching MOSFET

The switching MOSFET (Q1) should have a voltage rating sufficient to withstand the maximum output voltage together with the diode drop of rectifier diode D1 and any possible overshoot due to ringing caused by parasitic inductances and capacitances. Use a MOSFET with a drain-to-source voltage rating higher than that calculated by the following equations.

Boost Configuration

$$V_{DS} = (V_{LED} + V_D) \times 1.2$$

where V_{DS} is the drain-to-source voltage in volts and V_D is the forward drop of rectifier diode D1. The factor of 1.2 provides a 20% safety margin.

Buck-Boost Configuration

$$V_{DS} = (V_{LED} + V_{INMAX} + V_D) \times 1.2$$

where V_{DS} is the drain-to-source voltage in volts and V_D is the forward drop of rectifier diode D1. The factor of 1.2 provides a 20% safety margin.

The RMS current rating of the switching MOSFET Q1 is calculated as follows for boost and buck-boost configurations:

$$I_{DRMS} = 1.3 \times (\sqrt{(IL_{AVG})^2 \times D_{MAX}})$$

where I_{DRMS} is the MOSFET Q1's drain RMS current in amperes.

The MOSFET Q1 dissipates power due to both switching losses, as well as conduction losses. The conduction losses in the MOSFET are calculated as follows:

$$P_{COND} = (IL_{AVG})^2 \times D_{MAX} \times R_{DSON}$$

where R_{DSON} is the on-resistance of Q1 in ohms, P_{COND} is in watts, and IL_{AVG} is in amperes. Use the following equations to calculate the switching losses in the MOSFET.

Boost Configuration

$$P_{SW} = \left(\frac{IL_{AVG} \times V_{LED}^2 \times C_{GD} \times f_{SW}}{2}\right) \times \left(\frac{1}{IG_{ON}} + \frac{1}{IG_{OFF}}\right)$$

Buck-Boost Configuration

$$P_{SW} = \left(\frac{IL_{AVG} \times (V_{LED} + V_{INMAX})^2 \times C_{GD} \times f_{SW}}{2}\right) \times \left(\frac{1}{IG_{ON}} + \frac{1}{IG_{OFF}}\right)$$

where IG_{ON} and IG_{OFF} are the gate currents of the MOSFET Q1 in amperes when it is turned on and turned off, respectively, V_{LED} and V_{INMAX} are in volts, IL_{AVG} is in amperes, f_{SW} is in hertz, and C_{GD} is the gate-to-drain MOSFET capacitance in farads.

Rectifier Diode

Use a Schottky diode as the rectifier (D1) for fast switching and to reduce power dissipation. The selected Schottky diode must have a voltage rating 20% above the maximum converter output voltage. The maximum converter output voltage is V_{LED} in boost configuration and V_{LED} + V_{INMAX} in buck-boost configuration.

The current rating of the diode should be greater than I_D in the following equation:

$$I_D = IL_{AVG} \times (1 - D_{MAX}) \times 1.5$$

Dimming MOSFET

Select a dimming MOSFET (Q2) with continuous current rating at the operating temperature higher than the LED current by 30%. The drain-to-source voltage rating of the dimming MOSFET must be higher than V_{LED} by 20%.

Feedback Compensation

The LED current control loop comprising the switching converter, the LED current amplifier, and the error amplifier should be compensated for stable control of the LED current. The switching converter small-signal transfer function has a right-half-plane (RHP) zero for both boost and buck-boost configurations as the inductor current is in continuous conduction mode. The RHP zero adds a 20dB/decade gain together with a 90-degree phase lag, which is difficult to compensate. The easiest way to avoid this zero is to roll off the loop gain to 0dB at a frequency less than 1/5 the RHP zero frequency with a -20dB/decade slope.

The worst-case RHP zero frequency (f_{ZRHP}) is calculated as follows:

Boost Configuration

$$f_{ZRHP} = \frac{V_{LED} \times (1 - D_{MAX})^2}{2\pi \times L \times I_{LED}}$$

Buck-Boost Configuration

$$f_{ZRHP} = \frac{V_{LED} \times (1 - D_{MAX})^2}{2\pi \times L \times I_{LED} \times D_{MAX}}$$

where f_{ZRHP} is in hertz, V_{LED} is in volts, L is the inductance value of L1 in henries, and I_{LED} is in amperes.

The switching converter small-signal transfer function also has an output pole for both boost and buck-boost configurations. The effective output impedance that determines the output pole frequency together with the output filter capacitance is calculated as follows:

Boost Configuration

$$R_{OUT} = \frac{(R_{LED} + R7) \times V_{LED}}{(R_{LED} + R7) \times I_{LED} + V_{LED}}$$

Buck-Boost Configuration

$$R_{OUT} = \frac{(R_{LED} + R7) \times V_{LED}}{(R_{LED} + R7) \times I_{LED} \times D_{MAX} + V_{LED}}$$

where R_{LED} is the dynamic impedance of the LED string at the operating current in ohms, R7 is the LED current-sense resistor in ohms, V_{LED} is in volts, and I_{LED} is in amperes.

The output pole frequency for both boost and buck-boost configurations is calculated as below:

$$f_{P2} = \frac{1}{2\pi \times C_{OUT} \times R_{OUT}}$$

where f_{P2} is in hertz, C_{OUT} is the output filter capacitance in farads, and R_{OUT} is the effective output impedance in ohms calculated above.

The feedback loop compensation is done by connecting resistor R10 and capacitor C4 in series from the COMP pin to GND. R10 is chosen to set the high-frequency gain of the integrator to set the crossover frequency at $f_{ZRHP}/5$ and C4 is chosen to set the integrator zero frequency to maintain loop stability. For optimum performance, choose the components using the following equations:

$$R10 = \frac{2 \times f_{ZRHP} \times R4}{F_C \times (1 - D_{MAX}) \times R7 \times 6.15 \times GM_{COMP}}$$

The value of C4 can be calculated as below:

$$C4 = \frac{25}{\pi \times R10 \times f_{ZRHP}}$$

where R10 is the compensation resistor in ohms, f_{ZRHP} and f_{P2} are in hertz, R4 is the inductor current-sense resistor in ohms, R7 is the LED current-sense resistor in ohms, factor 6.15 is the gain of the LED current-sense amplifier, and GM_{COMP} is the transconductance of the error amplifier in amps/volts.

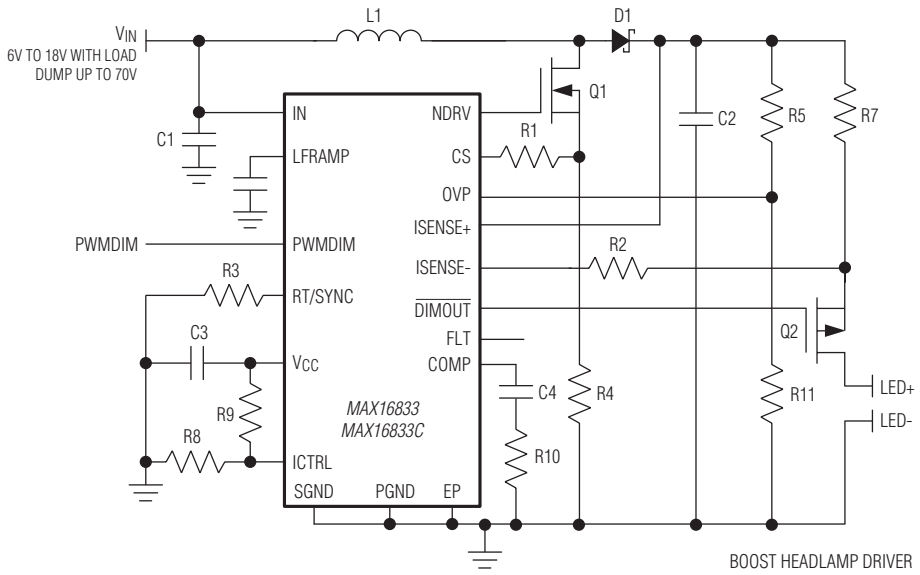
Layout Recommendations

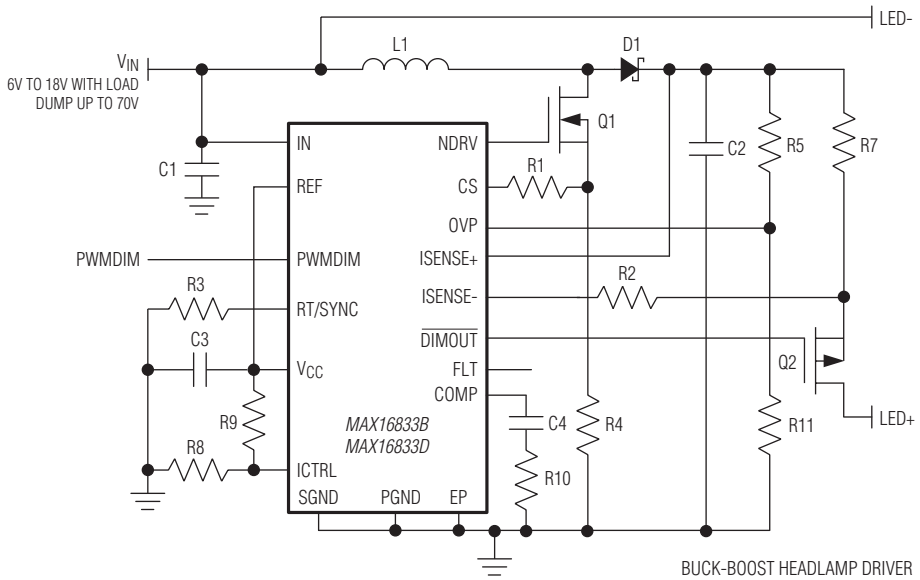
Typically, there are two sources of noise emission in a switching power supply: high di/dt loops and high dV/dt surfaces. For example, traces that carry the drain current often form high di/dt loops. Similarly, the heatsink of the MOSFET connected to the device drain presents a dV/dt source; therefore, minimize the surface area of the heatsink as much as is compatible with the MOSFET power dissipation or shield it. Keep all PCB traces carrying switching currents as short as possible to minimize current loops. Use ground planes for best results.

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity and power dissipation. Follow these guidelines for good PCB layout:

- Use a large contiguous copper plane under the ICs' package. Ensure that all heat-dissipating components have adequate cooling.
- Isolate the power components and high-current paths from the sensitive analog circuitry.
- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. Keep switching loops short such that:
  a) The anode of D1 must be connected very close to the drain of the MOSFET Q1.
  b) The cathode of D1 must be connected very close to C_{OUT}.
  c) C_{OUT} and current-sense resistor R4 must be connected directly to the ground plane.
- Connect PGND and SGND at a single point.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PCBs (2oz vs. 1oz) to enhance full-load efficiency.
- Route high-speed switching nodes away from the sensitive analog areas. Use an internal PCB layer for the PGND and SGND plane as an EMI shield to keep radiated noise away from the device, feedback dividers, and analog bypass capacitors.

Typical Operating Circuits





Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	FUNCTIONALITY	MAX DUTY CYCLE (%)
MAX16833BAUE+	-40°C to +125°C	16 TSSOP-EP*	Reference Voltage Output	88.5
MAX16833BAUE/V+	-40°C to +125°C	16 TSSOP-EP*	Reference Voltage Output	88.5
MAX16833CAUE+	-40°C to +125°C	16 TSSOP-EP*	Frequency Dithering	94
MAX16833CAUE/V+	-40°C to +125°C	16 TSSOP-EP*	Frequency Dithering	94
MAX16833DAUE+	-40°C to +125°C	16 TSSOP-EP*	Reference Voltage Output	94
MAX16833DAUE/V+	-40°C to +125°C	16 TSSOP-EP*	Reference Voltage Output	94

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
/V denotes an automotive qualified part.

Chip Information

PROCESS: BiCMOS-DMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TSSOP-EP	U16E+3	21-0108	90-0120

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/10	Initial release	—
1	11/10	Added MAX16833AUE	1, 21, 22
2	12/10	Added MAX16833C and MAX16833D	22
3	7/11	Added MAX16833E	1–4, 6–14, 20, 21
4	8/12	Removed MAX16833E	1–22
5	4/13	Updated startup delay time and its description	2, 11

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