HIGHLIGHTS

- DPLL1 and DPLL2 can be used on line cards to manage the generation of synchronous port clocks and IEEE 1588 synchronization signals based on multiple system backplane references
- DPLL3 can be used on line cards to select incoming line clocks for use on system backplanes; it can also be used for general purpose timing applications
- APLL1 and APLL2 generate clocks with jitter < 1 ps RMS (12 kHz to 20 MHz) for: 1000BASE-T and 1000BASE-X ports and to generate IEEE 1588 time stamp clocks and 1 pulse per second (PPS) signals
- APLL3 is Voltage Controlled Crystal Oscillator (VCXO) based and generates clocks with jitter <0.3 ps RMS (10 kHz to 20 MHz) for: 10GBASE-R, 10GBASE-W, 40GBASE-R and 100GBASE-R
- Fractional-N input dividers support a wide range of reference frequencies
- DPLLs, APLL1 and APLL2 can be configured from an external EEPROM after reset

FEATURES

- Differential reference inputs (IN1 to IN6) accept clock frequencies between 2 kHz and 650 MHz
- Single ended inputs (IN7 to IN12) accept reference clock frequencies between 2 kHz and 162.5 MHz
- Loss of Signal (LOS) pins (LOS0 to LOS3) can be assigned to any clock reference input
- Reference monitors qualify/disqualify references depending on activity, frequency and LOS pins
- Automatic reference selection state machines select the active reference for each DPLL based on the reference monitors, priority tables, revertive and non-revertive settings and other programmable settings
- Fractional-N input dividers enable the DPLLs to lock to a wide range of reference clock frequencies including: 10/100/1000 Ethernet, 10G/ 40G/100G Ethernet, OTN, SONET/SDH, PDH, TDM, GSM and GNSS frequencies
- Any reference inputs (IN1 to IN12) can be designated as external sync pulse inputs (1 PPS, 2 kHz, 4 kHz or 8 kHz) associated with a selectable reference clock input
- FRSYNC_8K_1PPS and MFRSYNC_2K_1PPS output sync pulses that are aligned with the selected external input sync pulse input and frequency locked to the associated reference clock input
- DPLL1 and DPLL2 can be configured with bandwidths between 18 Hz and 567 Hz
- DPLL1 and DPLL2 lock to input references with frequencies between 2 kHz and 650 MHz
- DPLL3 locks to input references with frequencies between 8 kHz and 650 MHz
- DPLL1 and DPLL2 generate clocks with PDH, TDM, GSM, CPRI/ OBSAI, 10/100/1000 Ethernet and GNSS frequencies; these clocks are directly available on OUT1
- DPLL3 generates N x 8 kHz clocks up to 100 MHz that are output on OUT8 and OUT9
- APLL1, APLL2 and APLL3 can be connected to DPLL1 and DPLL2
- APLL1 and APLL2 generate 10/100/1000 Ethernet, 10G Ethernet, or SONET/SDH frequencies
- APLL3 generates 10G/40G/100G Ethernet, WAN-PHY and LAN-PHY frequencies
- Any of eight common TCXO/OCXO frequencies can be used for the System Clock: 10 MHz, 12.8 MHz, 13 MHz, 19.44 MHz, 20 MHz, 24.576 MHz, 25 MHz or 30.72 MHz
- The I2C slave interface can be used by a host processor to access the control and status registers
- The I2C master interface can automatically load a device configuration from an external EEPROM after reset; APLL3 must be configured via the I2C slave interface
- Differential outputs OUT3 to OUT6 output clocks with frequencies between 1 PPS and 650 MHz
- Differential outputs OUT10 and OUT11 output clocks with frequencies up to 650 MHz
- Single ended outputs OUT1, OUT2, and OUT7 output clocks with frequencies between 1 PPS and 125 MHz
- Single ended outputs OUT8 and OUT9 output clocks N*8kHz multiples up to 100 MHz
- DPLL1 and DPLL2 support independent programmable delays for each of IN1 to IN12; the delay for each input is programmable in steps of 0.61 ns with a range of ~±78 ns
- The input to output phase delay of DPLL1 and DPLL2 is programmable in steps of 0.0745 ps with a total range of ±20 μs
- The clock phase of each of the output dividers for OUT1 to OUT7 is individually programmable in steps of ~200 ps with a total range of +/- 180°
- 1149.1 JTAG Boundary Scan
- 144-pin CABGA green package

APPLICATIONS

- Synchronous clock generation for 10/40G and lower rate, Ethernet, PON OLT and SONET/SDH line card
- Access routers, edge routers, core routers
- Carrier Ethernet switches
- Multi-service access platforms
- PON OLT
- LTE eNodeB

DESCRIPTION

The 82P33741 Port Synchronizer for IEEE 1588 and 10G/40G Synchronous Ethernet provides tools to manage timing references, clock conversion and timing paths for IEEE 1588 and Synchronous Ethernet (SyncE). The device supports up to three independent timing paths for: IEEE 1588 clock generation; SyncE clock generation; and general purpose frequency translation. The device outputs low-jitter clocks that can directly synchronize 100GBASE-R, 40GBASE-R, 10GBASE-R and 10GBASE-W and lower-rate Ethernet interfaces; as well as CPRI/OBSAI, SONET/SDH and PDH interfaces and IEEE 1588 Time Stamp Units (TSUs).

The 82P33741 accepts six differential reference inputs and six single ended reference inputs that can operate at common Ethernet, SONET/SDH and PDH frequencies that range from 2 kHz to 650 MHz. The references are continually monitored for loss of signal and for frequency offset per user programmed thresholds. All of the references are available to all three Digital PLLs (DPLLs). The active reference for each DPLL is determined by forced selection or by automatic selection based on user programmed priorities, locking allowances, reference monitors, and LOS inputs.

The 82P33741 can accept a clock reference and an associated phase locked sync signal as a pair. DPLL1/DPLL2 can lock to the clock reference and align the frame sync and multi-frame sync outputs with the paired sync input. The device allows any of the differential or single ended reference inputs to be configured as sync inputs that can be associated with any of the other differential or single ended reference inputs. The input sync signals can have a frequency of 1 PPS, 2 kHz, 4kHz or 8 kHz. This feature enables DPLL1/DPLL2 to phase align its frame sync and multi-frame sync outputs with a sync input without the need use a low bandwidth setting to lock directly to the sync input.

The DPLLs support three primary operating modes: Free-Run, Locked and Holdover. In Free-Run mode the DPLLs synthesize clocks based on the system clock alone. In Locked mode the DPLLs filter reference clock jitter with the selected bandwidth. In Locked mode, the long-term output frequency accuracy is the same as the long term frequency accuracy of the selected input reference. In Holdover mode, the DPLL uses frequency data acquired while in Locked mode to generate accurate frequencies when input references are not available.

The 82P33741 requires a system clock for its reference monitors and other digital circuitry. The frequency accuracy of the system clock determines the frequency accuracy of the DPLLs in Free-Run mode. The frequency stability of the system clock determines the frequency stability of the DPLLs in Free-Run mode and in Holdover mode; and it affects the wander generation of the DPLLs in Locked mode.

DPLL1 and DPLL2 can be configured with a range of selectable filtering bandwidths from 18 Hz to 567 Hz. DPLL3 is a wideband (BW > 25Hz) frequency translator that can be used, for example, to convert a recovered SyncE clock to a 25MHz backplane clock.

Clocks generated by DPLL1 and DPLL2 can be passed through APLL1 or APLL2 which are LC based jitter attenuating Analog PLLs (APLLs). The output clocks generated by APLL1 and APLL2 are suitable for serial GbE and lower rate interfaces, and for IEEE 1588 time stamps clocks and 1 PPS signals.

Clocks generated by DPLL1 and DPLL2 can be passed through APLL3 which is a voltage controlled crystal oscillator (VCXO) based jitter attenuating APLL. APLL3 can be provisioned with one or two selectable crystal resonators to support up to two base frequencies. The output clocks generated by APLL3 are suitable for serial 10 GbE and lower rate interfaces.

All 82P33741 control and status registers are accessed through an I2C slave microprocessor interface. For configuring the DPLLs, APLL1 and APLL2, the I2C master interface can automatically load a configuration from an external EEPROM after reset. APLL3 must be configured via the I2C slave interface.

FUNCTIONAL BLOCK DIAGRAM

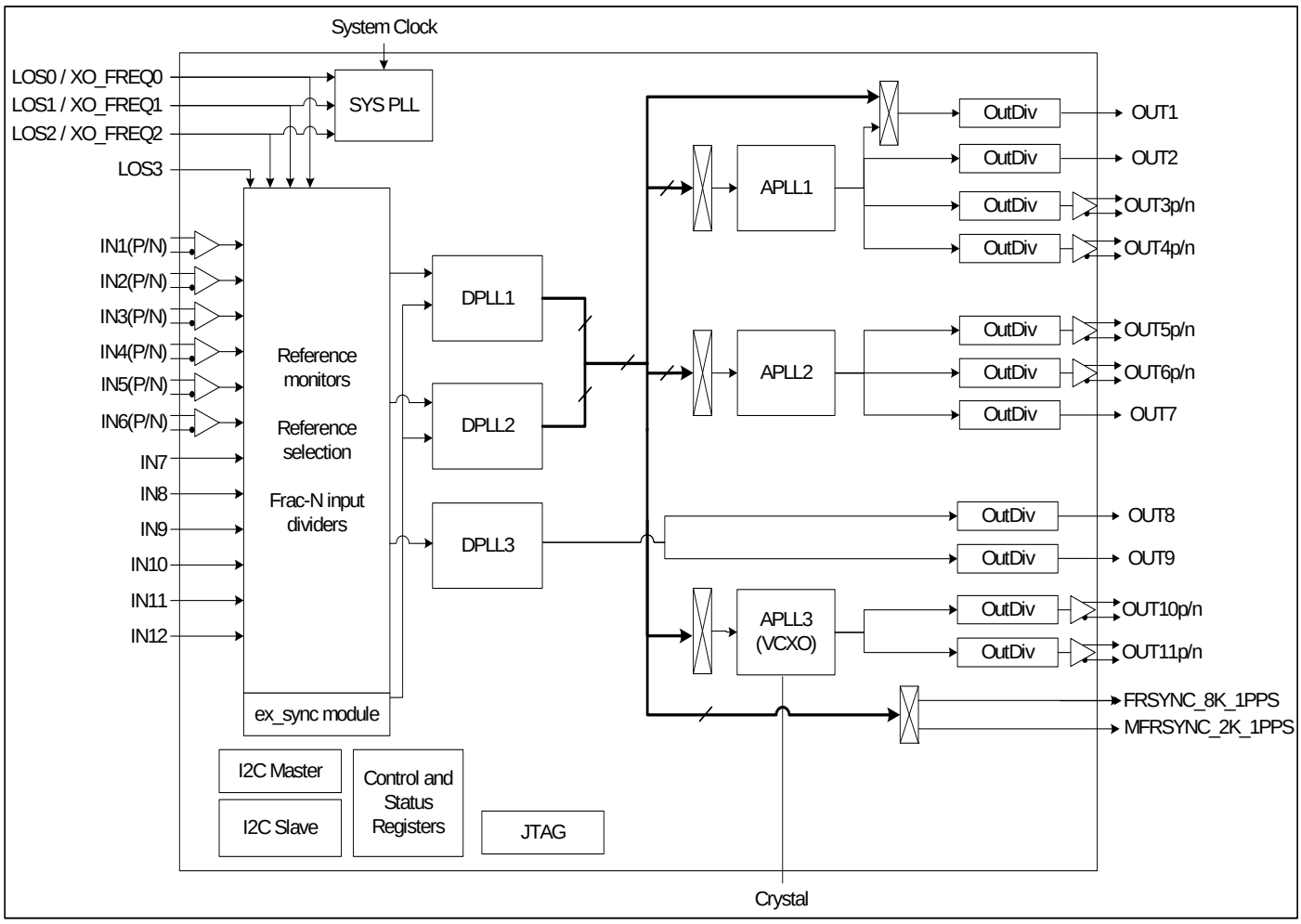

Figure 1. Functional Block Diagram

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1 PIN ASSIGNMENT

	1	2	3	4	5	6	7	8	9	10	11	12	
A	OUT5_POS	OUT5_NEG	OUT6_POS	OUT6_NEG	VDDAO	OUT11_POS	VDDAO	OUT10_POS	CAP2	XTAL2_IN	SONET/SDH/LOS3	XTAL1_IN	A
B	VSSAO	VDDAO	VDDAO	VSSAO	VSSAO	OUT11_NEG	VSSAO	OUT10_NEG	VSSA	XTAL2_OUT	MPU_MODE1/I2CM_SCL	XTAL1_OUT	B
C	VDDA	VSSA	VSS	OUT7	I2C_SDA	VDDA	VDDA	IC	CAP1	IC	MPU_MODE0/I2CM_SDA	MFRSYNC_2K_1PPS	C
D	VSSA	VDDA	VSSCOM	VSSD	VDDD	VSSA	VSSA	CAP3	I2C_AD2	I2C_SCL	OUT9	OUT8	D
E	OSCI	VSSA	IC	VDDDO	I2C_AD1	VDDD0	VSSDO	VSSA	DPLL3_LOCK	IN12	IN11	FRSYNC_8K_1PPS	E
F	TMS	VDDA	VSSA	VSSDO	VSS	VSSD	VDDD	VSSA	VDDA	IN10	IN6_NEG	IN6_POS	F
G	TCK	VDDA	IC	VSS	VSS	VSS	IC	VSS	DPLL2_LOCK	IN9	IN5_NEG	IN5_POS	G
H	XO_FREQ0/LOS0	VDDA	VSSA	VSS	VSS	VSS	VSS	VSS	DPLL1_LOCK	IN8	VSSD	VDDD_1_8	H
J	XO_FREQ1/LOS1	XO_FREQ2/LOS2	VSS	VSS	VSS	VSS	VSS	VSS	INT_REQ	IN7	IN4_NEG	IN4_POS	J
K	VDDA	VDDA	TRSTB	VSSAO	OUT2	RSTB	VSSDO	IC	IC	IC	IN3_NEG	IN3_POS	K
L	VSSA	VSSA	TDI	VDDAO	TDO	IC	VDDDO	OUT1	VSSD	VDDD_1_8	IN2_NEG	IN2_POS	L
M	OUT4_POS	OUT4_NEG	VSSAO	VDDAO	OUT3_POS	OUT3_NEG	VSSDO	VDDDO	IC	IC	IN1_NEG	IN1_POS	M
	1	2	3	4	5	6	7	8	9	10	11	12	

Figure 2. Pin Assignment (Top View)

2 PIN DESCRIPTION

Table 1: Pin Description

Pin No.	Name	I/O	Type	Description
Global Control Signal				
E1	OSCI	I	CMOS	OSCI: Crystal Oscillator System Clock A clock provided by a crystal oscillator is input on this pin. It is the system clock for the device. The oscillator frequency is selected via pins XO_FREQ0 ~ XO_FREQ3.
A11	SONET/SDH/ LOS3	I pull-down	CMOS	SONET/SDH: SONET / SDH Frequency Selection During reset, this pin determines the default value of the IN_SONET_SDH bit (b2, 09H): High: The default value of the IN_SONET_SDH bit is '1' (SONET); Low: The default value of the IN_SONET_SDH bit is '0' (SDH). After reset, the value on this pin takes no effect. LOS3- This pin is used to disqualify input clocks. See input clocks section for more details.
K6	RSTB	I pull-up	CMOS	RSTB: Reset Refer to section 2.2 reset operation for detail.
H1 J1 J2	XO_FREQ0/ LOS0 XO_FREQ1/ LOS1 XO_FREQ2/ LOS2	I pull-down	CMOS	XO_FREQ0 ~ XO_FREQ2: These pins set the oscillator frequency. XO_FREQ[2:0] Oscillator Frequency (MHz) 000 10.000 001 12.800 010 13.000 011 19.440 100 20.000 101 24.576 110 25.000 111 30.720 LOS0 ~ LOS2 - These pins are used to disqualify input clocks. See input clocks section for more details.
Input Clock and Frame Synchronization Input Signal				
M12 M11	IN1_POS IN1_NEG	I	PECL/LVDS	IN1_POS / IN1_NEG: Positive / Negative Input Clock 1 This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
L12 L11	IN2_POS IN2_NEG	I	PECL/LVDS	IN2_POS / IN2_NEG: Positive / Negative Input Clock 2 This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
K12 K11	IN3_POS IN3_NEG	I	PECL/LVDS	IN3_POS / IN3_NEG: Positive / Negative Input Clock 3 This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
J12 J11	IN4_POS IN4_NEG	I	PECL/LVDS	IN4_POS / IN4_NEG: Positive / Negative Input Clock 4 This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
G12 G11	IN5_POS IN5_NEG	I	PECL/LVDS	IN5_POS / IN5_NEG: Positive / Negative Input Clock 5 This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
F12 F11	IN6_POS IN6_NEG	I	PECL/LVDS	IN6_POS / IN6_NEG: Positive / Negative Input Clock 6 This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
J10	IN7	I pull-down	CMOS	IN7: Input Clock 7 This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
H10	IN8	I pull-down	CMOS	IN8: Input Clock 8 This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
G10	IN9	I pull-down	CMOS	IN9: Input Clock 9 This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.

Table 1: Pin Description (Continued)

Pin No.	Name	I/O	Type	Description
F10	IN10	I pull-down	CMOS	IN10: Input Clock 10 This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
E11	IN11	I pull-down	CMOS	IN11: Input Clock 11 This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
E10	IN12	I pull-down	CMOS	IN12: Input Clock 12 This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
Output Frame Synchronization Signal				
E12	FRSYNC _8K_1PPS	O	CMOS	FRSYNC_8K_1PPS: 8 kHz Frame Sync Output An 8 kHz signal or a 1PPS sync signal is output on this pin.
C12	MFRSYNC _2K_1PPS	O	CMOS	MFRSYNC_2K_1PPS: 2 kHz Multiframe Sync Output A 2 kHz signal or a 1PPS sync signal is output on this pin.
Output Clock				
L8 K5	OUT1 OUT2	O	CMOS	OUT1 ~ OUT2: Output Clock 1 ~ 2
M5 M6	OUT3_POS OUT3_NEG	O	PECL/LVDS	OUT3_POS / OUT3_NEG: Positive / Negative Output Clock 3 The LVDS output has internal 100 ohm termination.
M1 M2	OUT4_POS OUT4_NEG	O	PECL/LVDS	OUT4_POS / OUT4_NEG: Positive / Negative Output Clock 4 The LVDS output has internal 100 ohm termination.
A1 A2	OUT5_POS OUT5_NEG	O	PECL/LVDS	OUT5_POS / OUT5_NEG: Positive / Negative Output Clock 5 The LVDS output has internal 100 ohm termination.
A3 A4	OUT6_POS OUT6_NEG	O	PECL/LVDS	OUT6_POS / OUT6_NEG: Positive / Negative Output Clock 6 The LVDS output has internal 100 ohm termination.
C4	OUT7	O	CMOS	OUT7: Output Clock 7
D12	OUT8	O	CMOS	OUT8: Output Clock 8
D11	OUT9	O	CMOS	OUT9: Output Clock 9
A8 B8	OUT10_POS OUT10_NEG	O	PECL/LVDS	OUT10_POS / OUT10_NEG: Positive / Negative Output Clock 10
A6 B6	OUT11_POS OUT11_NEG	O	PECL/LVDS	OUT11_POS / OUT11_NEG: Positive / Negative Output Clock 11
Miscellaneous				
C9, A9, D8	CAP1, CAP2, CAP3			CAP1, CAP2 and CAP3: Analog Power Filter Capacitor connection 1 to 3. These capacitors are be part of the power filtering.
A12	XTAL1_IN	I	Analog	Crystal oscillator 1 input. Determines first of two frequency families (Sonet/SDH, Ethernet or Ethernet*66/64) available for APLL3. Connect to ground if XTAL1 is not used.
B12	XTAL1_OUT	O	Analog	Crystal oscillator 1 output. Leave open if XTAL1 is not used.
A10	XTAL2_IN	I	Analog	Crystal oscillator 2 input. Determines first of two frequency families (chosen from Sonet/SDH, Ethernet or Ethernet*66/64) available for APLL3. Connect to ground if XTAL2 is not used
B10	XTAL2_OUT	O	Analog	Crystal oscillator 2 output. Leave open if XTAL2 is not used.
Lock Signal				
E9	DPLL3_LOCK	O	CMOS	DPLL3_LOCK This pin goes high when DPLL3 is locked

Table 1: Pin Description (Continued)

Pin No.	Name	I/O	Type	Description
G9	DPLL2_LOCK	O	CMOS	DPLL2_LOCK This pin goes high when DPLL2 is locked
H9	DPLL1_LOCK	O	CMOS	DPLL1_LOCK This pin goes high when DPLL1 is locked
Microprocessor Interface				
J9	INT_REQ	O Tri-state	CMOS	INT_REQ: Interrupt Request This pin is used as an interrupt request. The output characteristics are determined by the HZ_EN bit (b1, 0CH) and the INT_POL bit (b0, 0CH).
B11 C11	MPU_MODE1/ I2CM_SCL MPU_MODE0/ I2CM_SDA	I/O pull-up	CMOS/ Open Drain	MPU_MODE[1:0]: Microprocessor Interface Mode Selection During reset, these pins determine the default value of the MPU_SEL_CNFG[1:0] bits as follows: 00: I2C mode 01 ~ 10: Reserved 11: EEPROM mode I2CM_SCL: Serial Clock Line In I2C master mode, the serial clock is output on this pin. I2CM_SDA: Serial Data Input for I2C Master Mode In I2C master mode, this pin is used as the for the serial data.
D9	I2C_AD2	I pull-down	CMOS	I2C_AD2: Device Address Bit 2 I2C_AD[2:1] pins are the address bus of the microprocessor interface.
E5	I2C_AD1	I pull-down	CMOS	I2C_AD1: Device Address Bit 1 2C_AD[2:1] pins are the address bus of the microprocessor interface.
D10	I2C_SCL	I pull-down	CMOS	I2C_SCL: Serial Clock Line The serial clock is input on this pin.
C5	I2C_SDA	I/O pull-up	Open Drain	I2C_SDA: Serial Data Input/Output This pin is used as the input/output for the serial data.
JTAG (per IEEE 1149.1)				
F1	TMS	I pull-up	CMOS	TMS: JTAG Test Mode Select The signal on this pin controls the JTAG test performance and is sampled on the rising edge of TCK.
K3	TRSTB	I pull-up	CMOS	TRST: JTAG Test Reset (Active Low) A low signal on this pin resets the JTAG test port. This pin should be connected to ground when JTAG is not used.
G1	TCK	I pull-down	CMOS	TCK: JTAG Test Clock The clock for the JTAG test is input on this pin. TDI and TMS are sampled on the rising edge of TCK and TDO is updated on the falling edge of TCK. If TCK is idle at a low level, all stored-state devices contained in the test logic will indefinitely retain their state.
L3	TDI	I pull-up	CMOS	TDI: JTAG Test Data Input The test data are input on this pin. They are clocked into the device on the rising edge of TCK.
L5	TDO	O tri-state	CMOS	TDO: JTAG Test Data Output The test data are output on this pin. They are clocked out of the device on the falling edge of TCK. TDO pin outputs a high impedance signal except during the process of data scanning.
Power & Ground				
C1, C6, C7, D2, F2, F9, G2, H2, K1, K2	VDDA	Power	-	VDDA: Analog Core Power - +3.3V DC nominal
A5, A7, B2, B3, L4, M4	VDDAO	Power		VDDAO: Analog Output Power - +3.3V DC nominal
E4, E6, L7, M8	VDDDO	Power		VDDDO: Digital Output Power - +3.3V DC nominal
D5, F7	VDDD	Power		VDDD: Digital Core Power - +3.3V DC nominal

Table 1: Pin Description (Continued)

Pin No.	Name	I/O	Type	Description
L10, H12	VDDD_1_8	Power		VDDD_1_8: Digital Core Power - +1.8V DC nominal
B9, C2, D1, D6, D7, E2, E8, F3, F8, H3, L1, L2	VSSA	Ground	-	VSSA: Ground
B1, B4, B5, B7, K4, M3	VSSAO	Ground		VSSAO: Ground
E7, F4, K7, M7	VSSDO	Ground		VSSDO: Ground
D4, F6, H11, L9	VSSD	Ground		VSSD: Ground
D3	VSSCOM	Ground	-	VSSCOM: Ground
C3, F5, G4, G5, G6, G8, H4, H5, H6, H7, H8, J3, J4, J5, J6, J7, J8	VSS	Ground	-	VSS: Ground
Other				
C8, C10, E3, G3, G7, K8 K9, K10, L6, M9, M10	IC	-	-	IC: Internal Connection Internal Use. This pin must be left open for normal operation.

2.1 RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

2.1.1 INPUTS

Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Single-Ended Clock Inputs

For protection, unused single-ended clock inputs should be tied to ground.

Differential Clock Inputs

For applications not requiring the use of a differential input, both *_POS and *_NEG can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from _POS to ground.

XTAL Inputs

For applications not requiring the use of a crystal oscillator input, both _IN and _OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from _IN to ground.

2.1.2 OUTPUTS

Status Pins

For applications not requiring the use of a status pin, we recommend bringing out to a test point for debugging purposes.

Single-Ended Clock Outputs

All unused single-ended clock outputs can be left floating, or can be brought out to a test point for debugging purposes.

Differential Clock Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

2.2 RESET OPERATION

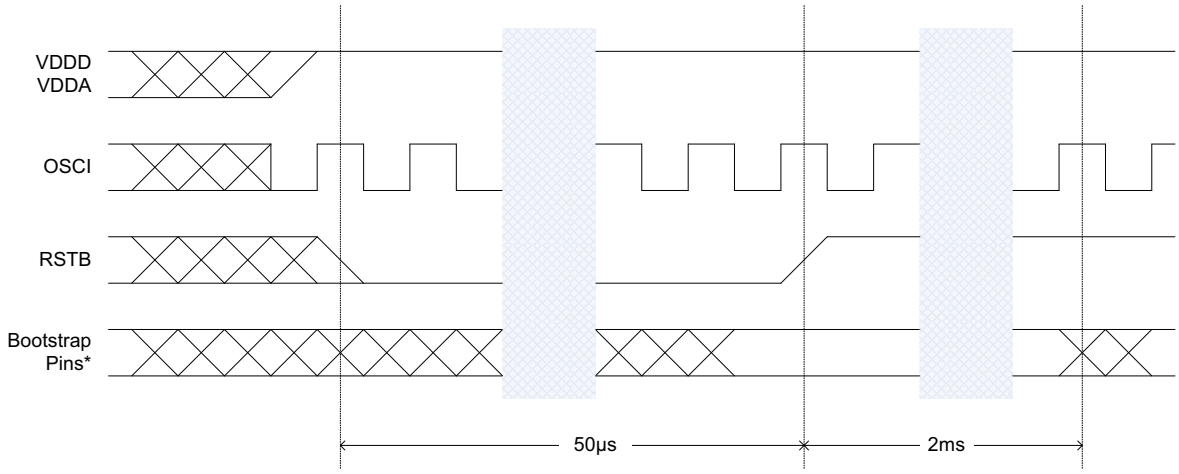
The device must be reset properly in order to ensure operations conform with specification.

To properly reset the device, the RSTB pin must be held at a low value for at least 50 usec. The device should be brought out of reset only at the time when power supplies are stabilized and the system clock is available on OSCi pin. The RSTB can be held low until this time, or pulsed low for at least 50us after this time.

The bootstrap pins (XO_FREQ[2:0], MPU_MODE[1:0], I2C_AD[2:1], SONET/SDH) need to be held at desired states for at least 2ms after de-assertion of RSTB pin to allow correct sampling. See Figure 3 for detail.

If loading from an EEPROM, the maximum time from RSTB de-assert to have stable clocks is 100ms. Note that if there is a bad EEPROM read sequence and the EEPROM loading is repeated once or twice (three times halts the device), then this time can be 2 or 3 times longer respectively. If not loading from EEPROM the maximum time from RSTB de-assert to have stable clocks is 10ms.

An on-board reset circuit or a commercially available voltage supervisory can be used to generate the reset signal. It is also feasible to use a standalone power-up RC reset circuit. When using a power-up RC reset circuit, careful consideration must be taken into account to fine tune the circuit properly based on each power supply's specification to ensure the power supply rise time is fast enough with respect to the RC time constant of the RC circuit.



* Bootstrap pins are: XO_FREQ[2:0], MPU_MODE[1:0], I2C_AD[2:1], SONET/SDH

Figure 3. Reset timing diagram

3 FUNCTIONAL DESCRIPTION

3.1 HARDWARE FUNCTIONAL DESCRIPTION

3.1.1 SYSTEM CLOCK

A crystal oscillator should be used as an input on the OSCI pin. This clock is provided for the device as a system clock. The system clock is used as a reference clock for all the internal circuits. The active edge of the system clock can be selected by the OSC_EDGE bit in xo_freq_cnfg register.

Eight common oscillator frequencies can be used for the stable System Clock. The oscillator frequency can be set by pins or by xo_freq_cnfg register as shown in Table 2.

Table 2: Oscillator Frequencies

xo_freq[2:0] pins xo_freq_cnfg[2:0] bits	Oscillator Frequency (MHz)
000	10.000
001	12.800
010	13.000
011	19.440
100	20.000
101	24.576
110	25.000
111	30.720

An offset from the nominal frequency may be compensated by setting the NOMINAL_FREQ_VALUE[23:0] bits. The calibration range is within ±741 ppm.

The crystal oscillator should be chosen accordingly to meet different applications and standard requirements. (See AN-807 Recommended Crystal Oscillators for NetSynchro WAN PLL).

3.1.2 MODES OF OPERATION

3.1.2.1 DPLL1 and DPLL2 Operating Mode

The DPLL1 and DPLL2 can operate in several different modes as shown in Table 3.

The DPLL1 and DPLL2 operating mode is controlled by the DPLL1_OPERATING_MODE[3:0] bits and DPLL2_OPERATING_MODE[3:0] bits respectively.

Table 3: DPLL1/2 Operating Mode Control

DPLL1/2_OPERATING_MODE[3:0]	DPLL1/2 Operating Mode
0000	Automatic
0001	Forced - Free-Run
0010	Forced - Holdover
0011	Reserved
0100	Forced - Locked
0101	Forced - Pre-Locked2
0110	Forced - Pre-Locked
0111	Forced - Lost-Phase
1000-1111	Reserved

When the operating mode is switched automatically, the operation of the internal state machine is shown in Figure 4.

Whether the operating mode is under external control or is switched automatically, the current operating mode is always indicated by the DPLL1/2_DPLL_OPERATING_STS[3:0] bits. When the operating mode switches, the DPLL1/2_OPERATING_STS bit will be set. If the DPLL1/2_OPERATING_STS bit is ‘1’, an interrupt will be generated if the corresponding mask bit is set to “1”, the mask bit is set to “0” by default.

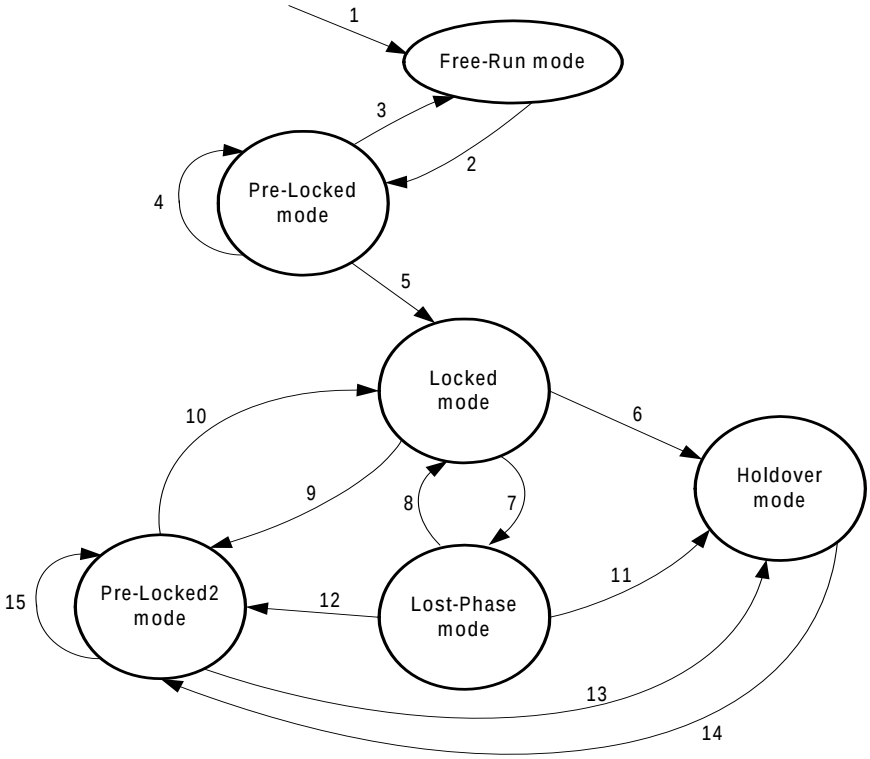


Figure 4. DPLL Automatic Operating Mode

Notes to Figure 4:

1. Reset.

2. An input clock is selected.

3. The DPLL selected input clock is disqualified AND No qualified input clock is available.

4. The DPLL selected input clock is switched to another one.

5. The DPLL selected input clock is locked (the DPLL_LOCK bit is '1').

6. The DPLL selected input clock is disqualified AND No qualified input clock is available.

7. The DPLL selected input clock is unlocked (the DPLL_LOCK bit is '0').

8. The DPLL selected input clock is locked again (the DPLL_LOCK bit is '1').

9. The DPLL selected input clock is switched to another one.

10. The DPLL selected input clock is locked (the DPLL_LOCK bit is '1').

11. The DPLL selected input clock is disqualified AND No qualified input clock is available.

12. The DPLL selected input clock is switched to another one.

13. The DPLL selected input clock is disqualified AND No qualified input clock is available.

14. An input clock is selected.

15. The DPLL selected input clock is switched to another one.

The causes of Item 4, 9, 12, 15 - 'the *DPLL* selected input clock is switched to another one' - are: (The *DPLL* selected input clock is disqualified AND Another input clock is switched to) OR (In Revertive switching, a qualified input clock with a higher priority is switched to) OR (The DPLL selected input clock is switched to another one Forced selection).

3.1.2.1.1 Free-Run Mode

In Free-Run mode, the DPLL1/2 output refers to the system clock and is not affected by any input clock. The accuracy of the DPLL1/2 output is equal to that of the system clock.

3.1.2.1.2 Pre-Locked Mode

In Pre-Locked mode, the DPLL1/2 output attempts to track the selected input clock.

The Pre-Locked mode is a secondary, temporary mode.

3.1.2.1.3 Locked Mode

In Locked mode, the DPLL1/2 is locked to the input clock. The phase and frequency offset of the DPLL1/2 output track those of the DPLL1/2 selected input clock.

For a closed loop, different bandwidths and damping factors can be used. They are set by the DPLL1/2_LOCKED_BW[4:0] bits and the DPLL1/2_LOCKED_DAMPING[2:0] bits respectively. DPLL1/2_LOCKED_BW[4] must be set to 1.

The locked bandwidth is selectable can be set as shown in Table 4.

Table 4: DPLL1/2 Locked Bandwidth

DPLL1/2_LOCKED_BW[3:0]	BW
0000	18 Hz
0001	35 Hz
0010	71 Hz
0011	142 Hz
0100	283 Hz
0101	567 Hz
0110-1111	Reserved

3.1.2.1.4 Pre-Locked2 Mode

In Pre-Locked2 mode, the DPLL1/2 output attempts to track the selected input clock.

The Pre-Locked2 mode is a secondary, temporary mode.

3.1.2.1.5 Lost-Phase Mode

In Lost-Phase mode, the DPLL1/2 output attempts to track the selected input clock.

The Lost-Phase mode is a secondary, temporary mode.

3.1.2.1.6 Holdover Mode

In Holdover mode, the DPLL1/2 resorts to the stored frequency data acquired in Locked mode to control its output. The DPLL1/2 output is not phase locked to any input clock.

The holdover mode is set to current averaged value with holdover filter BW of ~1.5mHz. In this mode the initial frequency offset is better than 1.1e-5ppm assuming that there is no in-band jitter/wander at the input just before entering holdover state.

The offset value can be read from the holdover_freq_cnfg[39:0] bits by setting the read_avg bit to “1”.

The holdover frequency resolution is calculated as follows:

*Holdover Frequency resolution: HO_freq_res = (77760/1638400) * 2^-48*

The Holdover value read from register bits holdover_freq_cnfg[[39:0] must be converted to decimal:

HO_value_dec = holdover_freq_cnfg[39:0] value in decimal

The frequency offset in ppm is calculated as follows:

*Holdover Frequency Offset (ppm) = (HO_freq_res * HO_value_dec)/(1-((HO_freq_res * HO_value_dec)/1e6))*

3.1.2.1.7 Hitless Reference Switching

Bit hitless_switch_en in DPLL1/2_mon_sw_pbo_cnfg register can be used to set hitless reference switching. When a Hitless Switching (HS) event is triggered, the phase offset of the selected input clock with respect to the DPLL1/2 output is measured. The device then automatically accounts for the measured phase offset and compensates for the appropriate phase offset into the DPLL output so that the phase transients on the DPLL1/2 output are minimized. The input frequencies should be set to frequencies equal to 8kHz or higher.

If hitless_switch_en is set to “1”, a HS event is triggered if any one of the following conditions occurs:

- DPLL1/2 selected input clock switches to a different reference
- DPLL1/2 exits from Holdover mode or Free-Run mode

For the two conditions, the phase transients on the DPLL1/2 output are minimized to be no more than 0.61 ns with HS. The HS can also be frozen at the current phase offset by setting the hitless_switch_freeze bit in DPLL1/2_mon_sw_pbo_cnfg register. When the HS is frozen, the device will ignore any further HS events triggered by the above two conditions, and maintain the current phase offset.

When the HS is disabled, there may be a phase shift on the DPLL1/2 output, as the DPLL1/2 output tracks back to 0 degree phase offset with respect to the DPLL1/2 selected input clock. This phase shift can be limited; see section 3.1.2.1.8 Phase Slope Limit on page 15.

3.1.2.1.8 Phase Slope Limit

Both DPLL1 and DPLL2 provide a phase slope limiting feature to limit the rate of output phase movement. The limit level is selectable via DPLL1/2_ph_limit[1:0] bits in DPLL1/2_bw_overshoot_cnfg register. The options are shown in Table 5.

Table 5: DPLL1/2 Phase Slope Limit

DPLL1/2_ph_limit[1:0]	Phase Slope Limit
00	61µs/s (GR-1244 ST3)
01	885ns/s (GR-1244-CORE ST2 and 3E, GR-253-CORE ST3 and G.8262 EEC option 2)
10	7.5 µs/s (G.813 opt1, G.8262 EEC-option 1)
11	unlimited / 1.4 ms/s (default)
*Note: The default phase slope limiting is set to 0 ns/s, therefore, the phase slope limiting must be set to the proper value to meet different standards according to this table. For PSL = 885 ns/s, it is recommended that a TCXO be used.	

3.1.2.1.9 Frequency Offset Limit

The DPLL1/2 output is limited to be within the programmed DPLL hard limit (refer to Chapter 3.1.4.3).

3.1.2.2 DPLL3 Operating Mode

The DPLL3 operating mode is controlled by the DPLL3_OPERATING_MODE[2:0] bits, as shown in Table 6. DPLL3 is disabled by default, write “0” to bit DPLL3_dpll_pdn in pdn_conf register to enable it.

Table 6: DPLL3 Operating Mode Control

DPLL3_OPERATING_MODE[2:0]	DPLL3 Operating Mode
000	Automatic
001	Forced - Free-Run
010	Forced - Holdover
100	Forced - Locked

When the operating mode is switched automatically, the operation of the internal state machine is shown in Figure 5:

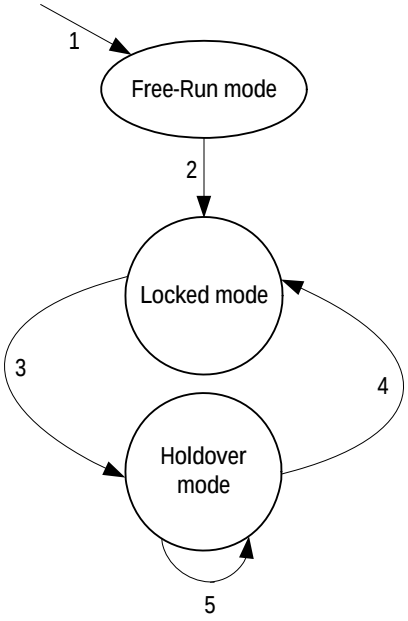


Figure 5. DPLL3 Automatic Operating Mode

Notes to Figure 5:

1. *Reset.*
2. *An input clock is selected.*
3. *(The DPLL3 selected input clock is disqualified) OR (A qualified input clock with a higher priority is switched to) OR (The DPLL3 selected input clock is switched to another one by Forced selection).*
4. *An input clock is selected.*
5. *No input clock is selected.*

3.1.2.2.1 Free-Run Mode

In Free-Run mode, the DPLL3 output refers to the system clock and is not affected by any input clock. The accuracy of the DPLL3 output is equal to that of the system clock.

3.1.2.2.2 Locked Mode

In Locked mode, the DPLL3 is locked to the input clock. The phase and frequency offset of the DPLL3 output track those of the DPLL3 selected input clock.

DPLL3 is a wide BW DPLL, with loop bandwidth higher than 25Hz.

3.1.2.2.3 Holdover Mode

In Holdover mode, the DPLL3 has 2 modes of operation for the holdover set by DPLL3_auto_avg bit in DPLL3_holdover_mode_cnfg register.

DPLL3_auto_avg = 0: holdover frequency is the instantaneous value of integral path just before entering holdover. If the DPLL3 was locked to an input clock reference that has no in-band jitter/wander and was then manually set to go into holdover, the initial frequency accuracy is 4.4X10-8 ppm.

DPLL3_auto_avg = 1: averaged frequency value is used as holdover frequency. The holdover average bandwidth is about 1.5mHz. In this mode the initial frequency offset is 1.1e-5ppm assuming that there is no in-band jitter/wander at the input just before entering holdover state.

3.1.2.2.4 Frequency Offset Limit

The DPLL3 output is limited to be within the DPLL hard limit (refer to Chapter 3.1.4.3).

3.1.3 INPUT CLOCKS AND FRAME SYNC

The 82P33741 has 12 input clocks that can also be used for frame sync pulses.

The 82P33741 supports Telecom and Ethernet frequencies from 1PPS up to 650 MHz.

Any of the input clocks can be used as a frame pulse or sync signal. The SYNC_sel[3:0] bits in IN*n*_los_sync_cnfg ($12 \leq n \leq 1$) registers sets which pin is used as frame pulse or sync signal.

IN1 to IN12 can be used for 2 kHz, 4 kHz or 8 kHz frame pulses or 1PPS sync signal.The input frequency should match the setting in the sync_freq[1:0] bits in DPLL1/2_input_mode_cnfg register.

3.1.3.1 Input Clock Pre-divider

Each input clock is assigned an internal Pre-divider. The Pre-divider can be used to divide the clock frequency down to a convenient frequency, such as 8 kHz for the internal DPLL1 and DPLL2. Note that T1 and E1 references can exhibit substantial jitter with frequencies above 4 kHz. These references should be applied to DPLL1 or DPLL2 without being divided down to 8 kHz.

For IN1 ~ IN12, the DPLL required frequency is set by the corresponding IN_FREQ[3:0] bits.

Table 7: IN_FREQ[3:0] DPLL Frequency

IN_FREQ[3:0] Bits	DPLL Frequency
0000	8 kHz
0001	1.544 MHz / 2.048 MHz (depends on SONET/ SDH bit)
0010	6.48 MHz
0011–1000	Reserved
1001	2 kHz
1010	4 kHz
1011	1 PPS
1100	6.25 MHz
1101–1111	Reserved

Each Pre-divider consists of an FEC divider and a DivN divider,. IN3~IN8 also include an HF (High Frequency) divider. Figure 6 shows a block diagram of the pre-dividers for an input clock.

For 2 kHz, 4 kHz or 8 kHz input clock frequency only, the Pre-divider should be bypassed by setting INn_DIV[1:0] bits = “0” ($1 \leq n \leq 6$), DIRECT_DIV bit = “0”, and LOCK_8K bit = “0”. The corresponding IN_FREQ[3:0] bits should be set to match the input frequency.

The HF divider, which is available for IN1 ~ IN6, should be used when the input clock is higher than (>) 162.5 MHz. The input clock can be divided by 4, 5 or can bypass the HF divider, as determined by the INn_DIV[1:0] bits ($1 \leq n \leq 6$).

The DivN divider can be bypassed, as determined by the DIRECT_DIV bit and the LOCK_8K bit. When DivN divider is bypassed, the corresponding IN_FREQ[3:0] bits should be set to match the input frequency. DIVN must be bypassed on a reference clock input that is also associated with another reference input used as SYNC.

When the DivN divider is used for INn ($1 \le n \le 12$), the division factor setting should observe the following order:

1. *Write the lower eight bits of the division factor to the PRE_DIVN_VALUE[7:0] bits;*
2. *Write the higher eight bits of the division factor to the PRE_DIVN_VALUE[14:8] bits.*

The division factor is calculated as follows:

Division Factor = (the frequency of the clock input to the DivN divider ÷ the frequency of the DPLL required clock set by the IN_FREQ[3:0] bits) - 1

The Pre-divider configuration and the division factor setting depend on the input clock on one of the IN3 ~ IN14pins and the DPLL required clock.

For the fractional input divider, the FEC divider, each input clock has a 16-bit (fec_divp_cnfg[15:0]) that represents the value of the numerator and a 16-bit (fec_divq_cnfg[15:0]) that represents the value of the denominator of FEC divider. The FEC division factor is calculated as follows:

FEC Division Factor = (fec_divp_cnfg[15:0]) ÷ (fec_divq_cnfg[15:0])

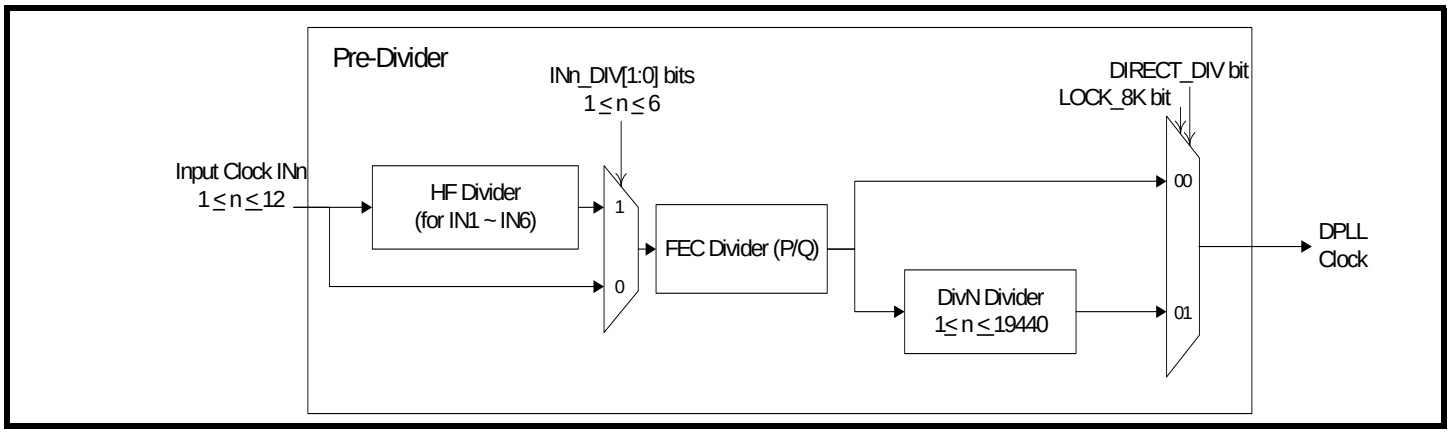


Figure 6. Pre-divider for an input clock

3.1.3.2 Input Clock Quality Monitoring

The qualities of all the input clocks are always monitored in the following aspects:

- Activity
- Frequency

LOS monitoring is only conducted on IN1 and IN2. Activity and frequency monitoring are conducted on all the input clocks.

The qualified clocks are available for selection for all 3 DPLLs.

3.1.3.2.1 Activity Monitoring

Activity is monitored by using an internal leaky bucket accumulator, as shown in Figure 7.

Each input clock is assigned an internal leaky bucket accumulator. The input clock is monitored for each period of 128 ms, the internal leaky bucket accumulator is increased by 1 when an event is detected; and it is decreased by 1 when no event is detected within the period set by the decay rate. The event is that an input clock drifts outside (>) ±500 ppm with respect to the system clock within a 128 ms period.

There are four configurations (0 - 3) for a leaky bucket accumulator. The leaky bucket configuration for an input clock is selected by the corresponding BUCKET_SEL[1:0] bits. Each leaky bucket configuration consists of four elements: upper threshold, lower threshold, bucket size and decay rate.

The bucket size is the capability of the accumulator. If the number of the accumulated events reach the bucket size, the accumulator will stop increasing even if further events are detected. The upper threshold is a point above which a no-activity alarm is raised. The lower threshold is a point below which the no-activity alarm is cleared. The decay rate is a certain period during which the accumulator decreases by 1 if no event is detected.

The leaky bucket configuration is programmed by one of four groups of register bits: the BUCKET_SIZE_n_DATA[7:0] bits, the UPPER_THRESHOLD_n_DATA[7:0] bits, the LOWER_THRESHOLD_n_DATA[7:0] bits and the DECAY_RATE_n_DATA[1:0] bits respectively; 'n' is 0 ~ 3.

The no-activity alarm status of the input clock is indicated by the INn_NO_ACTIVITY_ALARM bit ($12 \ge n \ge 1$).

The input clock with a no-activity alarm is disqualified for clock selection for the DPLLs.

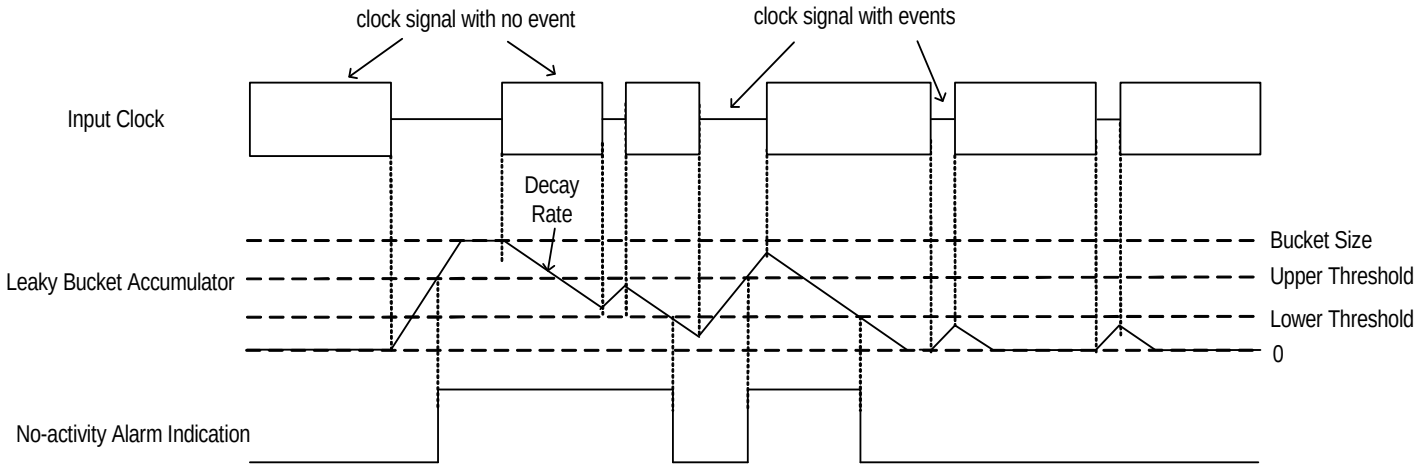


Figure 7. Input Clock Activity Monitoring

3.1.3.2.2 Frequency Monitoring

Frequency is monitored by comparing the input clock with a reference clock. The reference clock can be derived from the system clock or the output of DPLL1, as determined by the FREQ_MON_CLK bit.

Each reference clock has a hard frequency monitor and a soft frequency monitor. Both monitors have two thresholds, rejecting threshold and accepting threshold, which are set in HARD_FREQ_MON_-THRESHOLD[7:0] and SOFT_FREQ_MON_THRESHOLD[7:0]. So four frequency alarm thresholds are set for frequency monitoring: Hard Alarm Accepting Threshold, Hard Alarm Rejecting Threshold, Soft Alarm Accepting Threshold and Soft Alarm Rejecting Threshold.

The frequency hard alarm accepting threshold can be calculated as follows:

Frequency Hard Alarm Accepting Threshold (ppm) = (HARD_FREQ_MON_THRESHOLD[7:4] + 1) X FREQ_MON_FACTOR[3:0] (b3~0, FREQ_MON_FACTOR_CNFG)

The frequency hard alarm rejecting threshold can be calculated as follows:

Frequency Hard Alarm Rejecting Threshold (ppm) = (HARD_FREQ_MON_THRESHOLD[3:0] + 1) X FREQ_MON_FACTOR[3:0] (b3~0, FREQ_MON_FACTOR_CNFG)

When the input clock frequency rises to above the hard alarm rejecting threshold, the INn_FREQ_HARD_ALARM bit ($12 \geq n \geq 1$) will alarm and indicate ‘1’. The alarm will remain until the frequency is down to below the hard alarm accepting threshold, then the INn_FREQ_HARD_ALARM bit will return to ‘0’. There is a hysteresis between frequency monitoring, refer to Figure 8. Hysteresis Frequency Monitoring page 19.

The soft alarm is indicated by the INn_FREQ_SOFT_ALARM bit ($12 \geq n \geq 1$) in the same way as hard alarm.

The input clock with a frequency hard alarm is disqualified for clock selection for the DPLLs, but the soft alarm doesn’t affect the clock selection for the DPLLs.

The frequency of each input clock with respect to the reference clock can be read by doing the following step:

1. *Read the value in the IN_FREQ_VALUE[7:0] bits and calculate as follows:*

   *Input Clock Frequency (ppm) = IN_FREQ_VALUE[7:0] * FREQ_MON_FACTOR[3:0]*

Note that the value set by the FREQ_MON_FACTOR[3:0] bits depends on the application.

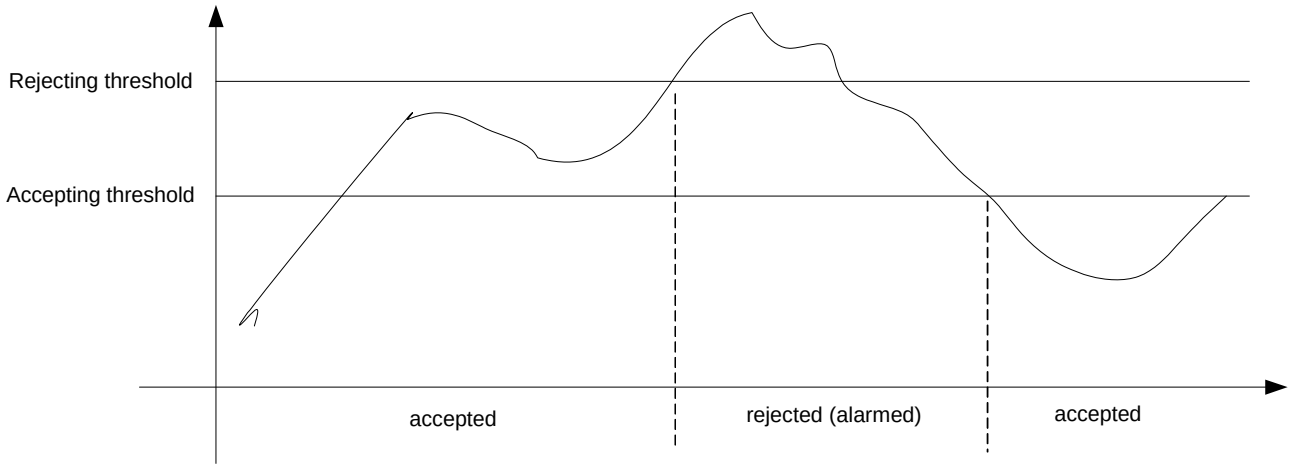


Figure 8. Hysteresis Frequency Monitoring

3.1.3.3 Input Clock Selection

For DPLL1, DPLL2 and DPLL3, the DPLL1/2/3_INPUT_SEL[3:0] bits (register DPLL1/2/3_input_sel_cnfg) determine the input clock selection, as shown in Table 8:

Table 8: Input Clock Selection for DPLL1, DPLL2 and DPLL3

DPLL1/2/3 _INPUT_SEL[3:0]	Input Clock Selection
0000	Automatic selection
0001 ~ 1110	Forced selection (IN1 ~ IN14)
1111	Reserved

3.1.3.3.1 Forced Selection

In Forced selection, the selected input clock is set by the DPLL1_INPUT_SEL[3:0], DPLL2_INPUT_SEL[3:0], and DPLL3_INPUT_SEL[4:0] bits. The results of input clocks quality monitoring do not affect the input clock selection if Forced selection is used.

3.1.3.3.2 Automatic Selection

In Automatic selection, the input clock selection is determined by input clock being valid, priority and input clock configuration. The input clock is declared valid depending on the results of input clock quality monitoring (refer to Chapter 3.1.3.2). The input clock can be configured to be valid and therefore be allowed to participate in the locking process by setting to “0” the corresponding INn_VALID bit (12 ≥ n ≥ 1) in DPLL_remote_input_valid_cnfg register, by default all the inputs are not valid, and therefore the user must set the corresponding bit to “0” in order to allow the DPLL to lock to a particular input clock. Within all the qualified input clocks, the one with the highest priority is selected. The priority is set by the corresponding INn_SEL_PRIORITY[3:0] bits in DPLL_INn_sel_priority_cnfg (12 ≥ n ≥ 1). If more than one qualified input clock INn is available, then it is important to set appropriate priorities to the input clocks, two input clocks must not have the same priority. This process is shown in Figure 9.

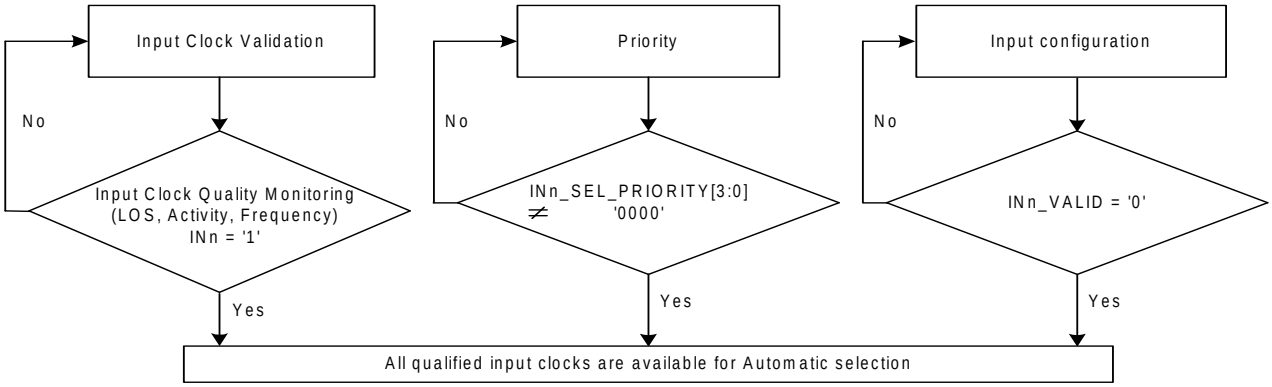


Figure 9. Qualified Input Clocks for Automatic Selection

3.1.3.3.2.1 Input Clock Validation

For all the input clocks, the input is declared valid depending on the results of input clock quality monitoring (refer to Chapter 3.1.3.2). The IN_NOISE_WINDOW bit should be set to ‘1’ if any of INn_FREQ[3:0] is set for frequencies ≤ 8 kHz, by default it is set to ‘0’.

For DPLL1 and DPLL2, the following conditions must be satisfied for the input clock to be valid; otherwise, it is invalid.

- No no-activity alarm (the INn_NO_ACTIVITY_ALARM bit is ‘0’);
- No frequency hard alarm (the INn_FREQ_HARD_ALARM bit is ‘0’);
- No phase lock alarm, i.e., the INn_PH_LOCK_ALARM bit is ‘0’;
- If the ULTR_FAST_SW bit is ‘1’, the DPLL selected input clock misses less than (<) 2 consecutive clock cycles; if the ULTR_FAST_SW bit is ‘0’, this condition is ignored;
- LOS[3:0] are not set to disqualify the input clock

For DPLL3, the following conditions must be satisfied for the input clock to be valid; otherwise, it is invalid.

- No no-activity alarm (the INn_NO_ACTIVITY_ALARM bit is ‘0’);
- No frequency hard alarm (the INn_FREQ_HARD_ALARM bit is ‘0’);
- LOS[3:0] are not set to disqualify the input clock

The INn bit (12 ≥ n ≥ 1) indicates whether or not the clock is valid. When the input clock changes from ‘valid’ to ‘invalid’, or from ‘invalid’ to ‘valid), the INn bit will be set. If the INn bit is ‘1’, an interrupt will be generated.

When the DPLL selected input clock has failed, i.e., the selected input clock changes from ‘valid’ to ‘invalid’, the DPLL_MAIN_REF_FAILED bit will be set. If the DPLL_MAIN_REF_FAILED bit is ‘1’, an interrupt will be generated.

3.1.3.3.2.2 Revertive and Non-Revertive Switching

For DPLL1 and DPLL2, Revertive and Non-Revertive switchings are supported, as selected by the REVERTIVE_MODE bit.

For DPLL3, only Revertive switching is supported.

GR-1244 defines Revertive and Non-Revertive Reference switching. In Non-Revertive switching, a switch to an alternate reference is maintained even after the original reference has recovered from the failure that caused the switch. In Revertive switching, the clock switches back to the original reference after that reference recovers from the failure, independent of the condition of the alternate reference. In Non-Revertive switching, input clock switch is minimized.

In Revertive switching, the selected input clock is switched when another qualified input clock with a higher priority than the current selected input clock is available. Therefore, if REVERTIVE_MODE bit is set to “1”, then the selected input clock is switched if any of the following is satisfied:

- the selected input clock is disqualified;
- another qualified input clock with a higher priority than the selected input clock is available.

A qualified input clock with the highest priority is selected by revertive switching. If more than one qualified input clock INn is available, then it is important to set appropriate priorities to the input clocks, two input clocks must not have the same priority.

In Non-Revertive switching, the DPLL1/2 selected input clock is not switched when another qualified input clock with a higher priority than the current selected input clock becomes available. In this case, the selected input clock is switched and a qualified input clock with the highest priority is selected only when the DPLL1/2 selected input clock is disqualified. If more than one qualified input clock INn is available, then it is important to set appropriate priorities to the input clocks, two input clocks must not have the same priority.

3.1.3.3.3 Selected / Qualified Input Clocks Indication

The selected input clock is indicated by the CURRENTLY_SELECTED_INPUT[3:0] bits.

When the device is configured in Automatic selection and Revertive switching is enabled, the input clock indicated by the CURRENTLY_SELECTED_INPUT[3:0] bits is the same as the one indicated by the HIGHEST_PRIORITY_VALIDATED[3:0] bits.

3.1.3.3.4 Input Clock Loss of Signal

There are 4 LOS input pins (LOS[3:0]) that can be used to disqualify the input clock. If they are set high, then the associated input clock is disqualified to be used as an input clock, and therefore the DPLLs will not lock to that particular input clock.

The 4 LOS pins can be associated with any input clock by setting bits LOS_EN in INn_LOS_SYNC_CNFG (1<n<14) register. By default, the LOS pins are not associated with any input.

3.1.4 DPLL LOCKING PROCESS

The following events are always monitored for the DPLLs locking process:

- Fast Loss;
- Fine Phase Loss;
- Hard Limit Exceeding.

For proper operation, COARSE_PH_LOS_LIMT_EN must be set to 0.

3.1.4.1 Fast Loss

A fast loss is triggered when the selected input clock misses 3 consecutive clock cycles. It is cleared once an active clock edge is detected.

For all DPLL1 and DPLL2 the occurrence of the fast loss will result in the DPLL to unlock if the FAST_LOS_SW bit is ‘1’. For DPLL3, the occurrence of the fast loss will result in the DPLL to unlock regardless of the FAST_LOS_SW bit.

3.1.4.2 Fine Phase Loss

The DPLL compares the selected input clock with the feedback signal. If the phase-compared result exceeds the fine phase limit programmed by the PH_LOS_FINE_LIMT[2:0] bits, a fine phase loss is triggered. It is cleared once the phase-compared result is within the fine phase limit.

For greatest jitter and wander tolerance, set the PH_LOS_FINE_LIMT[2:0] to the largest value.

The occurrence of the fine phase loss will result in DPLL to unlock if the FINE_PH_LOS_LIMT_EN bit is ‘1’.

3.1.4.3 Hard Limit Exceeding

Two limits are available for this monitoring. They are DPLL soft limit and DPLL hard limit. When the frequency of the DPLL output with respect to the system clock exceeds the DPLL soft / hard limit, a DPLL soft / hard alarm will be raised; the alarm is cleared once the frequency is within the corresponding limit. The occurrence of the DPLL soft alarm does not affect the DPLL locking status. The DPLL soft alarm is indicated by the corresponding DPLL_SOFT_FREQ_ALARM bit. The occurrence of the DPLL hard alarm will result in the DPLL to unlock if the FREQ_LIMT_PH_LOS bit is ‘1’.

The DPLL soft limit is set by the DPLL_FREQ_SOFT_LIMT[6:0] bits and can be calculated as follows:

DPLL Soft Limit (ppm) = DPLL_FREQ_SOFT_LIMT[6:0] X 0.724

The DPLL hard limit is set by the DPLL_FREQ_HARD_LIMT[15:0] bits and can be calculated as follows:

DPLL Hard Limit (ppm) = DPLL_FREQ_HARD_LIMT[15:0] X 0.0014

3.1.4.4 Locking Status

The DPLL locking status depends on the locking monitoring results. The DPLL is in locked state if none of the following events is triggered during 2 seconds; otherwise, the DPLL is unlocked.

- Fast Loss (the FAST_LOS_SW bit is '1');
- Fine Phase Loss (the FINE_PH_LOS_LIMT_EN bit is '1');
- DPLL Hard Alarm (the FREQ_LIMT_PH_LOS bit is '1').

If the FAST_LOS_SW bit, the COARSE_PH_LOS_LIMT_EN bit, the FINE_PH_LOS_LIMT_EN bit or the FREQ_LIMT_PH_LOS bit is '0', the DPLL locking status will not be affected even if the corresponding event is triggered. If all these bits are '0', the DPLL will be in locked state in 2 seconds.

The DPLL locking status is indicated by the corresponding DPLL_LOCK bits and by the DPLL_LOCK pins.

3.1.4.5 Phase Lock Alarm

DPLL1 and DPLL2 have a phase lock alarm that will be raised when the selected input clock can not be locked in DPLL1/2 within a certain period. This period can be calculated as follows:

Period (sec.) = TIME_OUT_VALUE[5:0] X MULTI_FACTOR[1:0]

The phase lock alarm is indicated by the corresponding INn_PH_LOCK_ALARM bit ($12 \geq n \geq 1$).

The phase lock alarm can be cleared, as selected by the PH_ALARM_TIMEOUT bit:

- It is cleared when a '1' is written to the corresponding INn_PH_LOCK_ALARM bit;
- It is cleared after the period (= *TIME_OUT_VALUE[5:0] X MULTI_FACTOR[1:0] in second*) starting from the time the alarm is raised.

The selected input clock with a phase lock alarm is disqualified for the DPLL1 and DPLL2 to lock.

Note that phase lock alarm is not available for DPLL3.

3.1.5 APLL1 AND APLL2

APLL1 and APLL2 are provided for a better jitter and wander performance of the device output clocks. The bandwidth for APLL1 and APLL2 is internally set to 22kHz (typical).

The input of both APLLs can be derived from one of the DPLL1 or DPLL2 outputs, as selected by the apll1_path_freq_cnfg[2:0] and apll2_path_freq_cnfg[2:0] bits respectively as shown in Table 9.

Table 9: APLL1/2 input selection

apll1/apll2_path_freq_cnfg[2:0]	APLL1/2 Input Selection
000	622.08 MHz from DPLL1
001	625 MHz from DPLL1
010	644.53125 MHz from DPLL1
011	Reserved
100	622.08 MHz from DPLL2
101	625 MHz from DPLL2
110	644.53125 MHz from DPLL2
1111	Reserved

To following steps should be followed to set APLL1/APLL2 output to Ethernet LAN PHY frequencies.

To initialize the device, write into the following registers:

1. *Write 0x04F4F0 to bits apll1/apll2_divn_frac_cnfg[20:0] of APLL1/APLL2 fractional feedback divider configuration register to set the fractional part of feedback divider for APLL1/APLL2*
2. *Write 0x0051 to bits apll1/apll2_divn_den_cnfg[15:0] of APLL1/APLL2 divisor denominator configuration register to set the denominator part of feedback divider for APLL1/APLL2*
3. *Write 0x0010 to bits apll1/apll2_divisor_num_cnfg[15:0] of APLL1/APLL2 divisor numerator configuration register to set the numerator part of feedback divider for APLL1/APLL2*
4. *Write 0x21 to bits apll1/apll2_divisor_int_cnfg[5:0] of APLL1/APLL2 divisor integer configuration register to set the integer part of feedback divider for APLL1/APLL2*
5. *Write 0x13356218 to bits apll1/apll2_fr_ratio_cnfg[28:0] of APLL1/APLL2 feedback divider configuration register to set the feedback divider for APLL1/APLL2*

After the device has been initialized according to the steps above, follow the following steps when setting APLL1/APLL2 path to 644.53125 MHz:

- Write 1'b1 to dsm_cnfg_en bit to enable the preset programmable feedback divider of APLL1/APLL2 configuration register
- Write the corresponding value in the apll1/apll2_path_freq_cnfg[2:0] bits according to Table 9.

After the device has been initialized according to the steps 1 to 5 above, follow the following steps when setting APLL1/APLL2 path to 625MHz: or 622.08MHz

- Write 1'b0 to dsm_cnfg_en bit to disable the preset programmable feedback divider of APLL1/APLL2 configuration register
- Write the corresponding value in the apll1/apll2_path_freq_cnfg[2:0] bits according to Table 9.

3.1.6 APLL3

The APLL3 is provided for a better jitter and wander performance of the device differential output clocks OUT10 and OUT11.

APLL3 supports 3 clock modes: SONET, Ethernet, and Ethernet LAN. The base frequency for the 3 clock modes are 622.08 MHz, 625 MHz, and 644.53125 MHz respectively. The clock mode selected is determined by the crystal used for the APLL.

The APLL uses a crystal to generate the respective mode's base frequency. The supported crystal frequencies are 24.8832 MHz (SONET), 25 MHz (Ethernet) and 25.78125 MHz (Ethernet LAN). The APLL supports up to two crystal connections, allowing the APLL to support up to two mode's base frequencies.

The input of both APLL3 can be derived from one of the DPLL1 or DPLL2 outputs by configuring internal registers as described in Table 10. The bandwidth for APLL3 is set to greater 30 Hz (typical), therefore the bandwidth of DPLL1 or the DPLL2 that is connected to APLL3 should be set to 18 Hz.

Table 10: APLL3 input selection

Crystal	APLL3 Input	APLL3_mux_cnfg[3:0]	APLL3_div1_cnfg[7:0]	APLL3_div2_cnfg[26:0]	APLL3_pd_sel[14:0]	APLL3_pd_sel[14:0]
24.88320	8100 Hz from DPLL1	0x04	0x01	0x000012BF	0x0001	0x0C00
24.88320	8100 Hz from DPLL2	0x0C	0x01	0x000012BF	0x0001	0x0C00
25.00000	8000 Hz from DPLL1	0x04	0x01	0x000012FB	0x0001	0x0C35
25.00000	8000 Hz from DPLL2	0x0C	0x01	0x000012FB	0x0001	0x0C35
25.78125	7812.5 Hz from DPLL1	0x03	0x01	0x0000063F	0x0001	0x0CE4
25.78125	7812.5 Hz from DPLL2	0x0B	0x01	0x0000063F	0x0001	0x0CE4

3.1.6.1 External Crystals

Suggestions for crystal options and best matching to APR requirements, crystal tolerance considerations and budgets, component placement and crystal wiring to achieve minimum capacity are fully detailed in IDT AN-861, "Recommended Crystals and Layout Guidelines for IDT's VCXO-based Synchronization PLLs.

3.1.7 OUTPUT CLOCKS & FRAME SYNC SIGNALS

The device supports 11 output clocks and 2 frame sync output signals.

3.1.7.1 Output Clocks

OUT1 can be derived either from DPLL1, DPLL2, or APLL1 selected by out1_mux_cnfg[3:0]

OUT2 ~ OUT4 can be derived from APLL1.

OUT5 ~ OUT7 can be derived from APLL2.

OUT1 to OUT7 have an output divider associated with each output. The divider is composed by 2 cascaded dividers, the first divider can be programmed by writing into OUTn_DIV1_CNFG[4:0], the second divider can be programmed by writing into OUTn_DIV2_CNFG[26:0].

Figure 10 shows the diagram for OUT1 output dividers and relevant register bits.

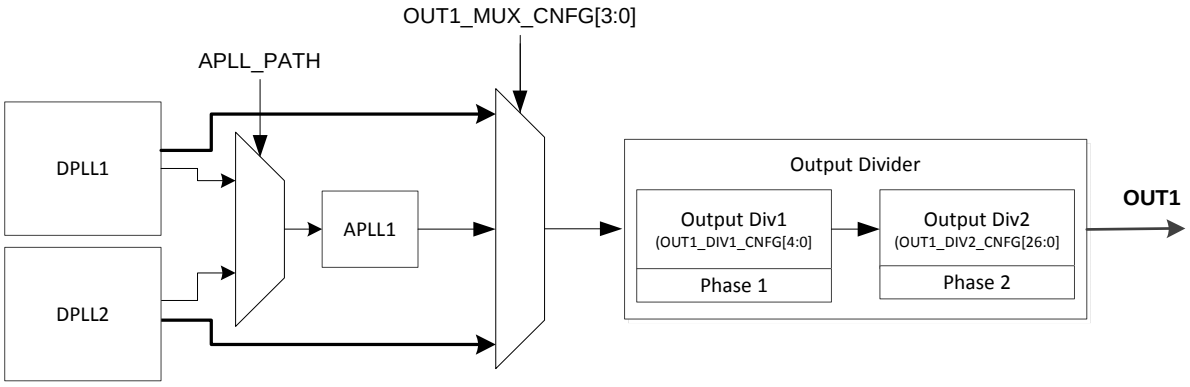


Figure 10. OUT1 output dividers

Figure 11 shows the diagram for OUT2 to OUT7 output dividers and relevant register bits.

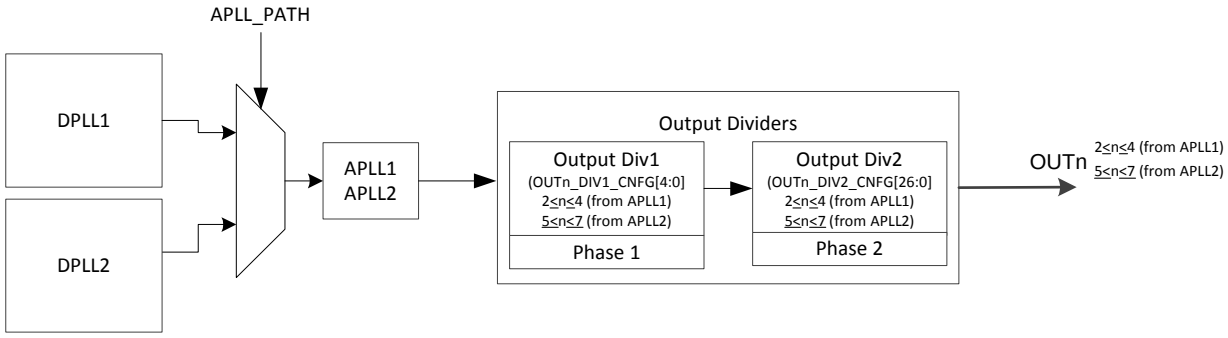


Figure 11. OUT2 to OUT7 output dividers

OUT8 and OUT9 are derived from DPLL3, there is an output divider associated with it. A GUI (Time Commander) can be used to set the following bis in the respective register that are associated with the DPLL3 dividers.

- To set the feedback divider, program dpll3_fb_div_cnfg[13:0] bits of DPLL3 feedback divider register
- To set the fractional divider, program dpll3_divn_frac_cnfg[23:0] of DPLL3 fractional divider register
- To set the denominator of the fractional divider, program dpll3_divn_den_cnfg[15:0] bits of DPLL3 fractional divider denominator register
- To set the numerator of the fractional divider, program dpll3_divn_num_cnfg[15:0] bits of DPLL3 fractional divider numerator register
- To set the integer divider, program dpll3_int_cnfg[7:0]bits of DPLL3 integer divider register

OUT10 and OUT11 are derived from APLL3, refer to Table 11 for the output frequency.

Table 11: Outputs on OUT10~11

OUTn_ODSEL0/1[2:0] (Output Divider)	Outputs on OUT10~11[1]		
	SONET (XTALn = 24.8832 MHz)	ETHERNET (XTALn = 25 MHz)	ETHERNET * 66/64 (XTALn = 25.78125 MHz)
1	622.08 MHz	625 MHz	644.53125 MHz
2	311.04 MHz	312.5 MHz	322.265625 MHz
4	155.52 MHz	156.25 MHz	161.1328125 MHz
5		125 MHz	
8[2]	77.76 MHz		
25[3]		25 MHz	
(OUTn_ENABLE = 0)	Output 'n' is disabled		
(OUTn_ENABLE = 1)	Output 'n' is enabled		

Note:
1. The blank cell means the configuration is reserved. The proper XTAL must be populated for XTAL1~2 based on the selected mode.
2. OUT11 only
3. OUT10 only

OUT1 to OUT9 output clocks can be inverted by setting OUTn_INVERT bit (0: output not inverted, 1: output inverted) in OUTn_MUX_CNFG register for ($1 \leq n \leq 7$), and in OUT8_CNFG and OUT8_CNFG registers for OUT8 and OUT9 respectively.

The output clocks can be squelched by setting OUTn_SQUELCH[1:0] bits (0x: no squelch, 10: squelch to '0', 11: squelch to '1') in OUTn_MUX_CNFG register for ($1 \leq n \leq 7$), and in OUT8_CNFG and OUT9_CNFG registers for OUT1 to OUT9 respectively.

OUT1 to OUT7 output clocks can be individually powered down by setting OUTn_PDN bit to '1' in OUTn_MUX_CNFG register for ($1 < n < 7$).

OUT10 and OUT11 can be enabled or disabled by programming OUT10_ENABLE and OUT11_ENABLE in the OUT10 and OUT11 configuration registers respectively.

82P33741 provides a variety of output frequencies from 1Hz to 650MHz.

APLL1 is always enabled and the default frequency for OUT1, OUT2, and OUT3 is respectively 25 MHz, 125 MHz, and 156.25MHz. OUT4 is squelched by default.

By default, OUT5 to OUT7 are squelched. Set the proper registers to set desired frequency values for OUT5 to OUT7.

DPLL3 is disabled by default, and if it is enabled, then the default frequency for OUT8 and OUT9 is respectively 16.384 MHz and 2.048 MHz.

APLL1, APLL2, and the DPLLs can be configured from an external EEPROM after reset. It can be used to set specific start up frequency values as needed by the application.

OUT10 and OUT11 are powered down by default. APLL3 must be configured via the I2C slave interface to set OUT10 and OUT11 frequency values.

3.1.7.2 Frame Sync Signals

Either an 8 kHz or a 2 kHz frame sync, or a 1PPS sync signal are output on the FRSYNC_8K_1PPS and MFRSYNC_2K_1PPS pins if enabled by the 8K_1PPS_EN and 2K_1PPS EN bits respectively. They are CMOS outputs.

The output sync frequencies are independent of the input sync frequency. The output FRSYNC_8K_1PPS and MFRSYNC_2K_1PPS frequencies are selected through the dpll1/2_fr_mfr_sync_cnfg registers.

Any supported clock frequency at the clock input can be associated with the sync signals.

The frame sync output signals are derived from the DPLL1 and DPLL2 output and are aligned with the output clock. They are synchronized to the frame sync input signal.

The frame/sync output signals align to the first edge of the associated reference clock that occurs after the edge of the frame/sync input signal. The frequency of the associated reference clock must be lower or equal to the frequencies of the output clocks that requires to be aligned with the frame/sync pulse signal.

If the frame sync input signal with respect to the DPLL1/2 selected input clock is above a limit set by the SYNC_MON_LIMT[2:0] bits, an external sync alarm will be raised and the frame/sync input signal is disabled to synchronize the frame/sync output signals. The external sync alarm is cleared once the frame/sync input signal with respect to the DPLL selected input clock is within the limit. If it is within the limit, whether frame/sync input signal is enabled to synchronize the frame sync output signal is determined by the AUTO_EXT_SYNC_EN bit and the EXT_SYNC_EN bit.

When the frame/sync input signal is enabled to synchronize the frame/sync output signal, it is adjusted to align itself with the DPLL selected input clock.

By default, the falling edge of the frame/sync input signal is aligned with the rising edge of the DPLL1/2 selected input clock. The rising edge of frame/sync input signal can be set to be aligned with the rising edge of the DPLL1/2 selected input clock by setting sync_edge bit to “1” in DPLL1/2_sync_edge_cnfg register.

The EX_SYNC_ALARM_MON bit indicates whether frame/sync input signal is in external sync alarm status. The external sync alarm is indicated by the EX_SYNC_ALARM bit. If the EX_SYNC_ALARM bit is ‘1’, the occurrence of the external sync alarm will trigger an interrupt.

The 8 kHz frame pulse, the 2 kHz frame pulse, and the 1PPS sync signal can be inverted by setting the 8K_1PPS_INV and 2K_1PPS_INV bits of Frame Sync and Multiframe Sync Output Configuration Register.

The 8 kHz and the 2 kHz frame sync outputs can be 50:50 duty cycle or pulsed, as determined by the 8K_PUL and 2K_PUL bits respectively. When they are pulsed, the pulse width derived from DPLL1 is defined by the period of OUT1, and the pulse width derived from DPLL2 is defined by the period of an internal clock. They are pulsed on the position of the falling or rising edge of the standard 50:50 duty cycle, as selected by the 2K_8K_PUL_POSITION bit of Frame Sync and Multiframe Sync Output Configuration Register.

3.1.8 INPUT AND OUTPUT PHASE CONTROL

The device has several features to allow a tight control of the phase on the input and output clocks.

3.1.8.1 DPLL1 and DPLL2 Phase offset control

The phase offset of the DPLL1/2 selected input clock with respect to the DPLL1/2 output can be adjusted. If the device is configured as the active PLL in a redundancy system, then the PH_OFFSET_EN bit determines whether the input-to-output phase offset is enabled. If the device is configured as the inactive PLL in a redundancy system, then the input-to-output phase offset is always enabled. If enabled, the input-to-output phase offset can be adjusted by setting the PH_OFFSET_CNFG[28:0] bits in DPLL1/2 phase offset configuration register. The register value is a 2's complement phase offset with a resolution of 0.0745ps and a total range of [20us, - 20us].

The input-to-output phase offset can be calculated as follows:

Phase Offset (ps) = PH_OFFSET[28:0] X 0.0745

3.1.8.2 Input Phase control

All the inputs phase can be controlled individually. They can be programmed with a resolution of 0.61 ns and a range of [77.5 ns,-78.1ns] by setting INn_PHASE_OFFSET_CNFG[7:0] bits ($1 \leq n \leq 12$) in the input phase offset configuration register. The register value is a 2's complement phase offset, the default is zero. The programmed offset is automatically applied to the DPLL1 and DPLL2 when a particular input is selected. If the manual DPLL1 and DPLL2 phase offset control is used then the per-input phase offset is not applied.

3.1.8.3 Output Phase control

The output phase can be controlled individually for outputs OUT1 to OUT7. There is the coarse phase control that allows the output phase to be adjusted as low as 1.6ns. There is a fine phase adjustment that allows the output phase to be adjusted as low as 187.27 ps. The total range is $+/-180^{0}$.

There are two registers associated with the coarse phase adjustment, the OUTn_PH1_CNFG ($1 \leq n \leq 7$) and the OUTn_PH2_CNFG ($1 \leq n \leq 7$) registers. The OUTn_PH1_CNFG register is associated with output divider 1 as shown in Figure 10 and Figure 11, the phase can be adjusted by a step size that is equal to the period of the input of clock of the output Div1, the number set in the OUTn_PH1_CNFG register should not be larger than the number set in OUTn_DIV1_CNFG register. The OUTn_PH2_CNFG register is associated with output divider 2 as shown in Figure 10 and Figure 11, the phase can be adjusted by a step size that is equal to the period of the input of clock of the output Div2, the number set in the OUTn_PH2_CNFG register should not be larger than the number set in OUTn_DIV2_CNFG register.

There is a register that is associated with the fine phase adjustment, the OUTn_FINE_CNFG ($1 \leq n \leq 7$). For the fine phase adjustment, the output clocks must be output from the APLLs, The phase can be adjusted by a step size that is equal to the 1/2 of the period of the VCO. For Ethernet clocks the VCO frequency is 2.5GHz, for Ethernet LAN PHY the VCO frequency is 2.578125 GHz, and for SONET/SDH clocks the VCO frequency is 2.48832 GHz. OUT1 can be output from the DPLLs, and in that case the fine phase adjustment is not available, it is only available if the clocks are output from the APLLs.

The output phase adjustments are not available for OUT8, OUT9, OUT10, and OUT11.

4 POWER SUPPLY FILTERING TECHNIQUES

To achieve optimum jitter performance, power supply filtering is required to minimize supply noise modulation of the output clocks. The common sources of power supply noise are switch power supplies and the high switching noise from the outputs to the internal PLL. The 82P33741 provides separate VDDA and VDDAO power pins for the internal analog PLL, it also provides VDDD and VDDDO pins for the core logic as well as I/O driver circuits.

The suggested power decoupling scheme is shown in Figure 12.

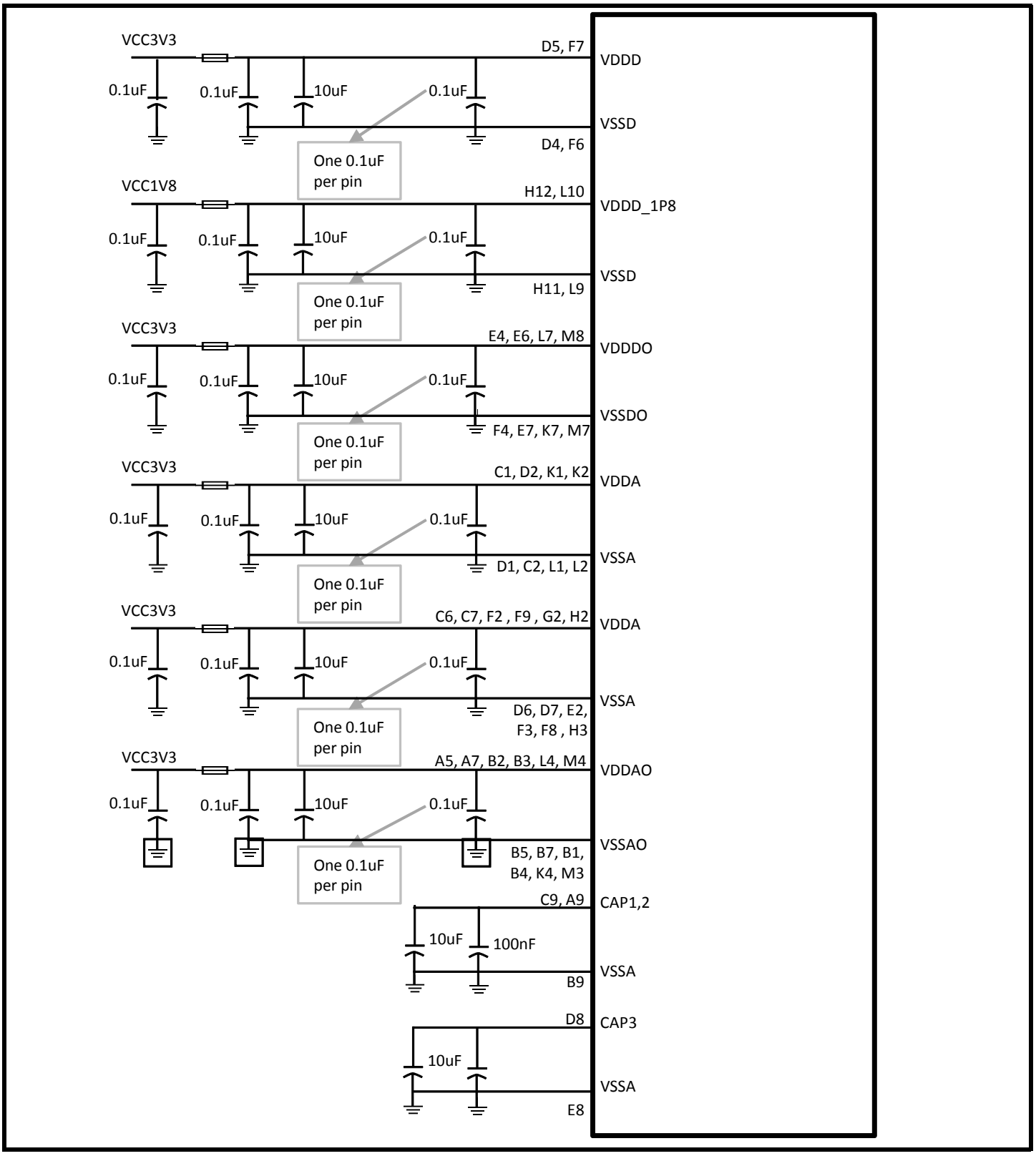


Figure 12. 82P33741 Power Decoupling Scheme

5 MICROPROCESSOR INTERFACE

The microprocessor interface provides access to read and write the registers in the device. The microprocessor interface supports I2C.

5.1 I2C SLAVE MODE

5.1.1 I2C DEVICE ADDRESS

The default value for the higher 4-bit address is 4'b1010, the 2-bit address is set by pins I2C_AD2, I2C_AD1, and the lower bit address I2C_AD0 is used to address the configuration of DPLLs/APLL1/2 and APLL3.

5.1.2 I2C BUS TIMING

Figure 13 shows the definition of I2C bus timing.

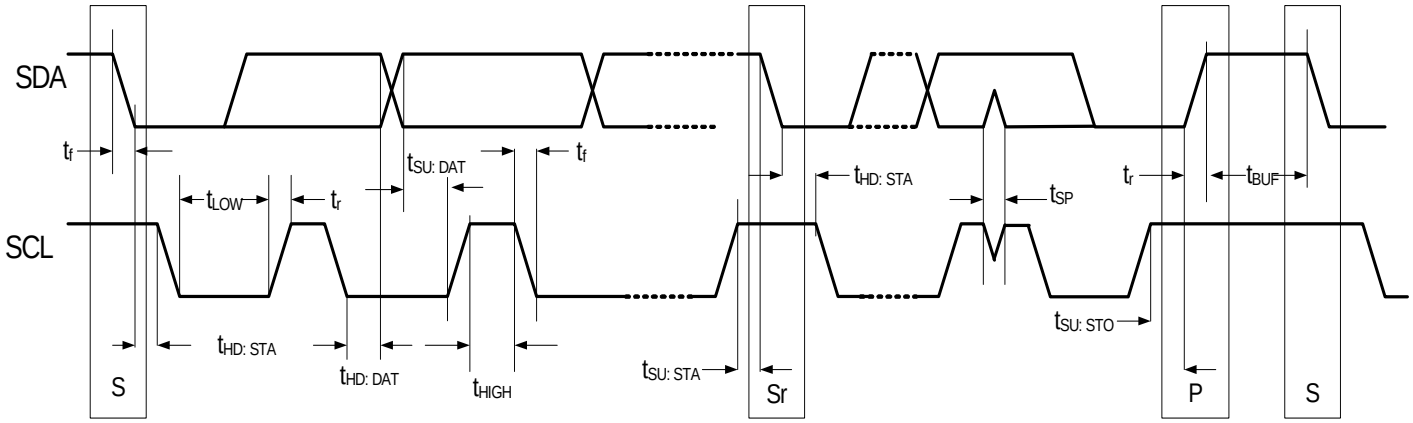


Figure 13. Definition of I2C Bus Timing

Table 12: Timing Definition for Standard Mode and Fast Mode(1)

Symbol	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
SCL	Serial clock frequency	0	100	0	400	kHz
$t_{HD;\ STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	-	0.5	-	µs
t_{LOW}	LOW period of the SCL clock	4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock	4.0	-	0.6	-	µs
$t_{SU;\ STA}$	Set-up time for a repeated START condition	4.7	-	0.6	-	µs
$t_{HD;\ DAT}$	Data hold time: for CBUS compatible masters for I^2C-bus devices	5.0 0(2)	- 3.45(3)	- 0(2)	- 0.9(3)	µs
$t_{SU;\ DAT}$	Data set-up time	250	-	100(4)	-	ns
t_r	Rise time of both SDA and SCL signals	-	1000	20 + 0.1Cb(5)	300	ns
t_f	Fall time of both SDA and SCL signals	-	300	20 + 0.1Cb(5)	300	ns
$t_{SU;\ STO}$	Set-up time for STOP condition	4.0	-	0.6	-	µs
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF
V_{nL}	Noise margin at the LOW level for each connected device (Including hysteresis)	0.1VDD	-	0.1VDD	-	V
V_{nH}	Noise margin at the HIGH level for each connected device (Including hysteresis)	0.2VDD	-	0.2VDD	-	V
t_{sp}	Pulse width of spikes which must be suppressed by the input filter	0	50	0	50	ns

Note:

1. All values referred to V_{IHmin} and V_{ILmax} levels (see Table 20)
2. A device must Internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum $t_{HD;\ DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system, but the requirement $t_{SU;\ DAT} \geqslant 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT} = 1000 + 250 = 1250$ ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released.
5. C_b = total capacitance of one bus line in pF. If mixed with Hs-mode device, faster fall-times according to Table 21 allowed.

n/a = not applicable

5.1.3 SUPPORTED TRANSACTIONS

The supported types of transactions are shown below.

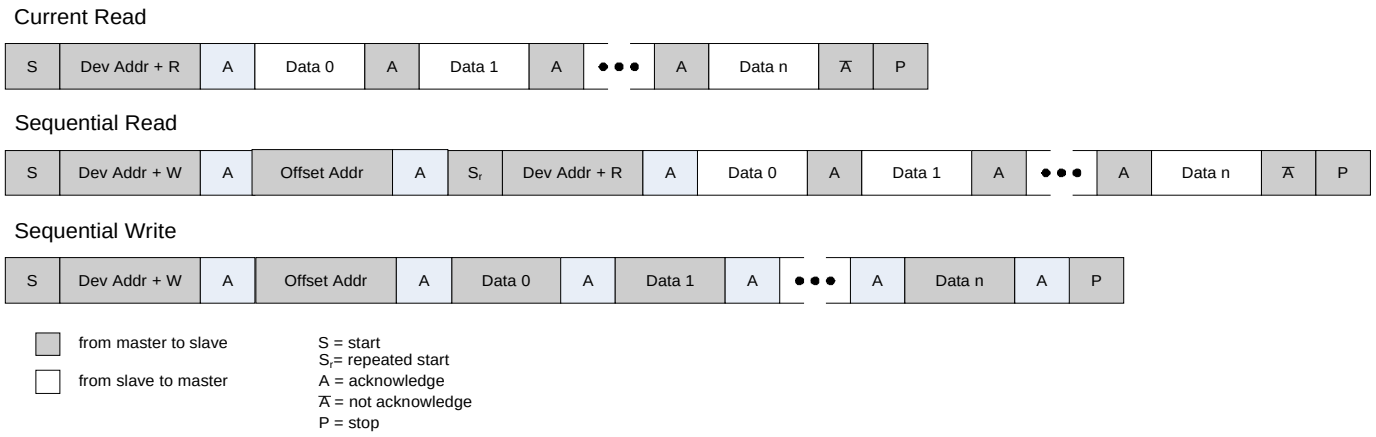


Figure 14. I2C Slave Interface Supported Transactions

Table 13: Description of I2C Slave Interface Supported Transactions

Operation	Description
Current Read	Reads a burst of data from an internal determined starting address, this starting address is equal to the last address accessed during the last read or write operation, incremented by one. If the address exceeds the address space, it will start from 0 again.
Sequential Read	Reads a burst of data from a specified address space. The starting address of the space is specified as offset address.
Sequential Write	Writes a burst of data to a specified address space, the starting address of the space is specified as offset address.

The registers are divided up into pages of 128 bytes with each byte having a separate address. Multi-byte registers need to be accessed in multiple read/write cycles. Address 0x7F is reserved for the page index pointer.

All register accesses are done as 8 bit I2C cycles. The 8-bit address refers to the register offset within the active page. If access to a different page is needed then a separate I2C write must be performed to the page register (0x7F). This makes the new page active and then 8 bit reads and writes can be performed anywhere within that page.

Note that accesses to multi-byte registers should not be interrupted by accesses to other addresses, because that may cause the data to be corrupted. The access of the multi-byte registers is different from the single-byte registers. Take the DPLL1 priority table registers (00H and 01H in page 2) as an example, the write operation for the multi-byte registers follows a fixed sequence. The register (00H) is configured first and the register (01H) is configured last. The two registers are configured continuously and should not be interrupted by any operation. The DPLL1 priority table configuration will take effect after all the two registers are configured. During read operation, the register (00H) is read first and the register (01H) is read last. The priority table configuration register reading should be continuous and not be interrupted by any operation.

5.2 I2C MASTER MODE

The 82P33741 has the capability to read from an external I2C EEPROM upon exit from reset. This reduces the start-up load on the microprocessor by programming the registers in the device-address space 101_0xx1 (registers in device-address space 101_0xx0 must still be written by the microprocessor). This mode uses the MPU_MODE1/I2CM_SCL and the MPU_MODE0/I2CM_SDA pins as the serial clock and the serial data respectively, it requires that both these pins be pulled high through resistors (these resistor values are dependent on the bus capacitance and I2C speed of the application). Access to the 82P33741 registers through the microprocessor interface I2C serial port is not available until the EEPROM reading process is completed.

As an I^2C bus master, the 82P33741 will support the following:

- 8 kbit (1023 x 8) I2C EEPROM with device address 1010000 (for the base block)
- Sequential read (block read) of the entire memory-map for device-excluding APLL3, from byte-address 0x000 to 0x39E
- 7-bit device address mode
- Validation of the EEPROM read data via CCITT-8 CRC check against value stored in memory-map address 0x39E
- Support for 100kHz and 400kHz operation with speed programmability. If bit 7 is set at memory-map address 0x001, the 82P33741 will shift from 100kHz operation to 400kHz operation.
- 2-byte word-addressing (1-byte word addressing is supported by offsetting the memory-map upwards 1 address in the EEPROM)
- Read will abort with an alarm (RD_EEPROM_ERR interrupt status set) if any of the following conditions occur: Slave NACK, CRC failure, Slave Response time-out

As the 82P33741 I2C master bus is meant only to read from a single EEPROM, it has the following restrictions:

- No support for Multi-master
- No support for Slave clock stretching
- No support for I2C Start Byte protocol
- No support for EEPROM Chaining
- No support for Writing to external I2C devices including the EEPROM used for booting

5.2.1 I2C BOOT-UP INITIALIZATION MODE

EEPROM mode is enabled via setting the MPU_MODE[1:0] pins high (through two separate pull-up resistors). Once the RSTB input has been asserted (low) and then de-asserted (high) and the device internal calibration has been completed, the 82P33741 will perform a short block read at 100 kHz to program the EEPROM read speed (100 kHz or 400 kHz). The 82P33741 will then perform a block read to program all the device configuration registers, and check the CRC of the EEPROM data. During the boot-up EEPROM-reading process, the 82P33741 will not respond to microprocessor serial control port accesses. Once the initialization process is completed, the contents of any of the device configuration registers can be further altered by the microprocessor, if desired.

The 82P33741 can work with EEPROMs supporting 2-byte word-addresses or 1-byte word-addresses by using 2-byte word addressing for both. This works in the usual manner for EEPROMs supporting 2-byte word addresses, and gives an address-to-address match between EEPROM and memory-map. For EEPROMs supporting only 1-byte word addresses, the second address byte will cause an addition increment of the address counter, and the memory-map will be read at the next highest EEPROM address,.i.e memory-map (CSR) address 0x00 will be read from EEPROM address 0x01, and memory map address 0x39E will be read from EEPROM address 0x39F.

If a NACK is received to any of the read cycles performed by the 82P33741 during the initialization process, or if the CRC does not match the one stored in memory-map address 0x39E, the boot process will be restarted. This restart can happen up to three times before an abort is declared and the RD_EEPROM_ERR interrupt status bit is set. Also on RD_EEPROM_ERR the MPU_MODE1/ I2CM_SCL and MPU_MODE0/ I2CM_SDA pins are both held low until the interrupt status bit is cleared or the device is reset. The suggested method for dealing with RD_EEPROM_ERR is to externally set the MPU_MODE[1:0] pins to 00 and then reset the 82P33741 so that it will boot into I2C serial port mode.

After a successful EEPROM boot, the 82P33741 will stop toggling the MPU_MODE1/ I2CM_SCL and MPU_MODE0/I2CM_SDA pins, returning them to static high values, and the RD_EEPROM_DONE interrupt status bit will be set. The I2C serial port will now respond to microprocessor reads and writes to the appropriate I2C device address.

5.2.2 EEPROM MEMORY MAP NOTES

The EEPROM memory-map is the same as the control and status register (CSR) map with the following additions and constraints:

1. For EEPROMs supporting 2-byte word-address, the memory-map addresses are the same as the EPPROM addresses; for EEPROMs supporting 1-byte word-address, the memory-map addresses will by mapped to the next address in the EEPROM, i.e. memory-map address 0x00 will be read from EEPROM address 0x01, and memory-map address 0x39E will be read from EEPROM address 0x39F.

2. Memory-map address 0x001, bit 7 is the EEPROM read speed (0 for 100 kps, 1 for 400 kbps)

3. Memory-map address 0x39E is the CRC-8 of the memory-map from 0x000 to 0x39D (the standard CCITT CRC-8 with the data width and result width being 8; the polynomial is (0, 1, 2, 8) or “0x07”). NB: all memory-map addresses from 0x000 to 0x39d are included in the sequential calculation of CRC, including those not used in the CSR - it is recommend that data at unused addresses be set to 0x00.

4. Memory-map addresses 0x392 to 0x39D must be set to the default values shown in the CSR documentation.

5. The device address at memory-map address 0x00f must match the address set by the board.

6. Each memory-map address that is a multiple of 0x7F must contain the pointer to the next page of the CSR i.e

0x07f 0x01

0x0ff 0x02

0x17f 0x03

0x1ff 0x04

0x27f 0x05

0x2ff 0x06

0x37f 0x07

6 JTAG

This device is compliant with the IEEE 1149.1 Boundary Scan standard except the following:

- The output boundary scan cells do not capture data from the core and the device does not support EXTEST instruction;

The JTAG interface timing diagram is shown in Figure - 15.

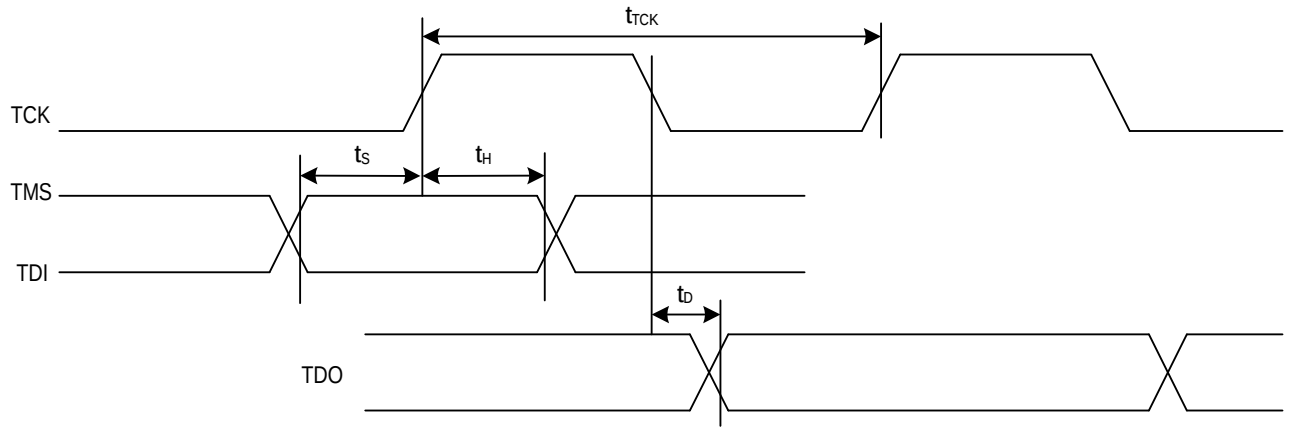


Figure 15. JTAG Interface Timing Diagram

Table 14: JTAG Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{TCK}	TCK period	100			ns
t_S	TMS / TDI to TCK setup time	25			ns
t_H	TCK to TMS / TDI Hold Time	25			ns
t_D	TCK to TDO delay time			50	ns

7 THERMAL MANAGEMENT

The device operates over the industry temperature range -40°C ~ +85°C. To ensure the functionality and reliability of the device, the maximum junction temperature T_{jmax} should not exceed 125°C. In some applications, the device will consume more power and a thermal solution should be provided to ensure the junction temperature T_j does not exceed the T_{jmax}.

7.1 JUNCTION TEMPERATURE

Junction temperature T_j is the temperature of package typically at the geographical center of the chip where the device's electrical circuits are. It can be calculated as follows:

Equation 1: $T_j = T_A + P \times \theta_{JA}$

Where:

θ_{JA} = Junction-to-Ambient Thermal Resistance of the Package

T_j = Junction Temperature

T_A = Ambient Temperature

P = Device Power Consumption

In order to calculate junction temperature, an appropriate θ_{JA} must be used. The θ_{JA} is shown in Table 15:

Table 15 has the thermal results based on JEDEC standard conditions. It is industry practice and IDT practice to publish these results.

If the PCB design differs from the JEDEC standard conditions, then the thermal results will be different.

7.2 THERMAL RELEASE PATH

In order to maximize both the removal of heat from the package, electrical grounding from the package to the board can be done through thermal vias to effectively conduct from the surface of the PCB to the ground plane(s). The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. These recommendations are to be used as a guideline only.

Table 15: Thermal Data

Parameter	Symbol	CONDITIONS	PKG	Typ Values (°C/W)	Notes
Thermal Resistance	θ_{JC}	Junction to Case	BAG144	6.8	JEDEC PCB (8x8 matrix)
	θ_{JB}	Junction to Base		16.2	
	θ_{JA1}	Junction to Air, still air		34.8	
	θ_{JA2}	Junction to Air, 1 m/s air flow		28.8	
	θ_{JA3}	Junction to Air, 2 m/s air flow		26.7	
	θ_{JA4}	Junction to Air, 3 m/s air flow		25.7	

8 ELECTRICAL SPECIFICATIONS

8.1 ABSOLUTE MAXIMUM RATING

Table 16: Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit
V_{DDA}, V_{DDAO}, V_{DDDO},V_{DDD}	Supply Voltage V_{DDA}, V_{DDAO}, V_{DDDO},V_{DDD}	-0.5	3.6	V
$V_{DDD\_1\_8}$	Supply Voltage $V_{DDD\_1\_8}$	-0.5	1.98	V
V_{INCMOS}	Input Voltage (CMOS and Open drain pins)	-0.5	5.5	V
V_{INDIFF}	Input Voltage (Differential pins)	-0.5	V_{DDD}+ 0.5	V
V_{INAN}	Input Voltage (Analog pins)	-0.5	2.2	V
$I_{OUTCONT}$	Output Current (Continuous current)		50	mA
$I_{OUTSURGE}$	Output Current (Surge current)		100	mA
T_A	Ambient Operating Temperature Range	-40	85	°C
T_{STOR}	Storage Temperature	-50	150	°C
Note: CDM Classification - Class III (JESD22 - C101) HBM Classification - Class 2 (JS-001-2010)				

8.2 RECOMMENDED OPERATION CONDITIONS

Table 17: Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DDA}, V_{DDAO}, V_{DDDO},V_{DDD}	Power Supply (DC voltage)	3.135	3.3	3.465	V	
$V_{DDD\_1\_8}$	Power Supply (DC voltage) $V_{DDD\_1\_8}$	1.71	1.8	1.89	V	
T_A	Ambient Temperature Range	-40		85	°C	
I_{DDA}	Analog Supply Current		480.8	548.48	mA	
I_{DDD}	Digital Supply Current (V_{DDD})		41.90	62.05	mA	
$I_{DDD\_1\_8}$	Digital Supply Current ($V_{DDD\_1\_8}$)		81.09	89.49	mA	
I_{DDDO}	Digital Output Supply Current		45.18	64.77	mA	All outputs enabled
I_{DDAO}	Analog Output Supply Current		168.46	220.96	mA	All outputs enabled, unloaded
	Analog Output Supply Current (loaded)		248.26	308.74	mA	All outputs enabled, 6 LVPECL outputs loaded with 150 ohms to GND
P_{TOT}	Total Power Dissipation		2.58	3.29	W	All outputs enabled, excluding the loading

8.3 I/O SPECIFICATIONS

8.3.1 CMOS INPUT / OUTPUT PORT

Table 18: CMOS Input Port Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Condition
V_{IH}	Input Voltage High	2			V	
V_{IL}	Input Voltage Low			0.8	V	
I_{IN}	Input Current			±10	µA	

Table 19: CMOS Input Port with Internal Pull-Up Resistor Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Condition
V_{IH}	Input Voltage High	2			V	
V_{IL}	Input Voltage Low			0.8	V	
P_U	Pull-Up Resistor		50		KΩ	Except RSTB pin
P_U	Pull-Up Resistor (RSTB pin)		25		KΩ	
I_{IN}	Input Current			±150	µA	

Table 20: CMOS Input Port with Internal Pull-Down Resistor Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Condition
V_{IH}	Input Voltage High	2			V	
V_{IL}	Input Voltage Low			0.8	V	
P_D	Pull-Down Resistor		50		KΩ	
I_{IN}	Input Current			±150	µA	

Table 21: CMOS Output Port Electrical Characteristics

Application Pin	Parameter	Description	Min	Typ	Max	Unit	Test Condition
Output Clock	V_{OH}	Output Voltage High	2.4		VDD	V	I_{OH} = -4 mA
	V_{OL}	Output Voltage Low			0.4	V	I_{OL} = 4 mA
	t_R	Rise time		2.2		ns	C_{LOAD} = 15 pF
	t_F	Fall time		2.2		ns	C_{LOAD} = 15 pF
Other Output	V_{OH}	Output Voltage High	2.4			V	I_{OH} = -2 mA
	V_{OL}	Output Voltage Low			0.4	V	I_{OL}= 2 mA
	t_R	Rise Time		7	20	ns	C_{LOAD} = 50 pF
	t_F	Fall Time		7	20	ns	C_{LOAD} = 50 pF

8.3.2 LVPECL / LVDS INPUT / OUTPUT PORT

8.3.2.1 PECL Input Port

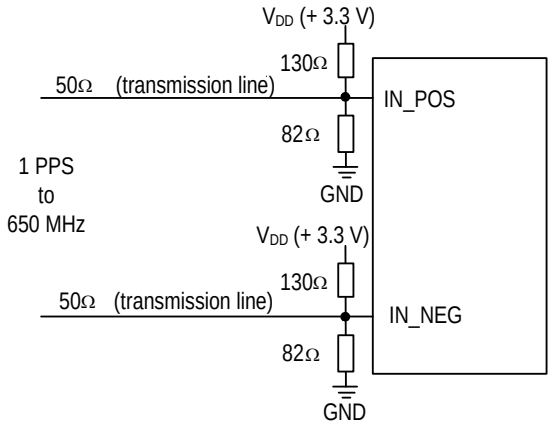


Figure 16. Recommended PECL Input Port Line Termination

Table 22: LVPECL Input Port Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Condition
V_{IL}	Input Low Voltage, Differential Inputs	VDD - 2.5	VDD - 1.5	VDD - 0.5	V	
V_{IH}	Input High Voltage, Differential Inputs	VDD - 2.4	VDD - 1.4	VDD - 0.4	V	
V_{ID}	Input Differential Voltage	0.1	0.7	1.4	V	
V_{IL_S}	Input Low Voltage, Single-ended Input	VSS	VDD - 1.95	VDD - 1.5	V	
V_{IH_S}	Input High Voltage, Single-ended Input	VDD - 1.3	VDD - 0.9	VDD	V	
I_{IH}	Input High Current, Input Differential Voltage V_{ID} = 1.4 V			10	µA	
I_{IL}	Input Low Current, Input Differential Voltage V_{ID} = 1.4 V	-10			µA	

Note:
1. Assuming a differential input voltage of at least 100 mV.
2. Unused differential input terminated to VDD-1.4 V.

8.3.2.2 LVPECL Output Port

8.3.2.2.1 LVPECL Termination for 3.3 V

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. Figure 17 and Figure 18 show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

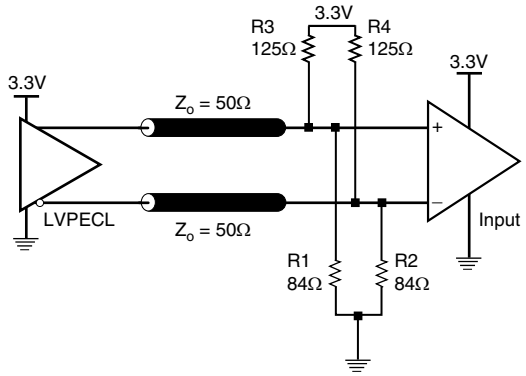


Figure 17. 3.3V LVPECL Output Termination

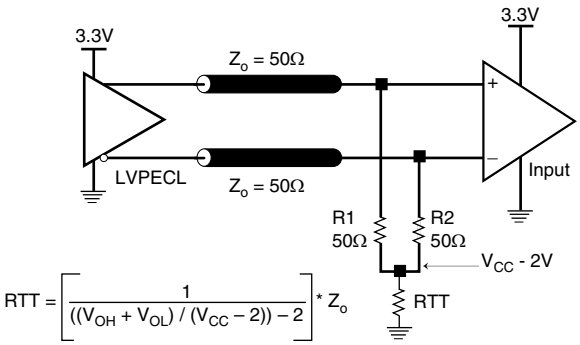


Figure 18. 3.3V LVPECL Output Termination

8.3.2.2.2 LVPECL Termination for 2.5 V

Figure 19 and Figure 20 show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to VCCO – 2V. For VCCO = 2.5V, the VCCO – 2V is very close to ground level. The R3 in Figure 20 can be eliminated and the termination is shown in Figure 21.

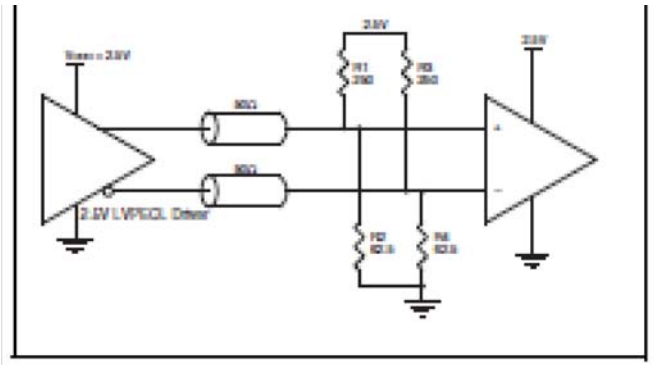


Figure 19. 2.5V LVPECL Output Termination

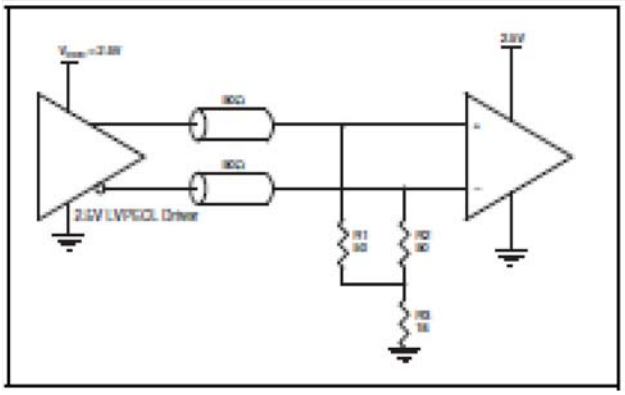


Figure 20. 2.5V LVPECL Output Termination

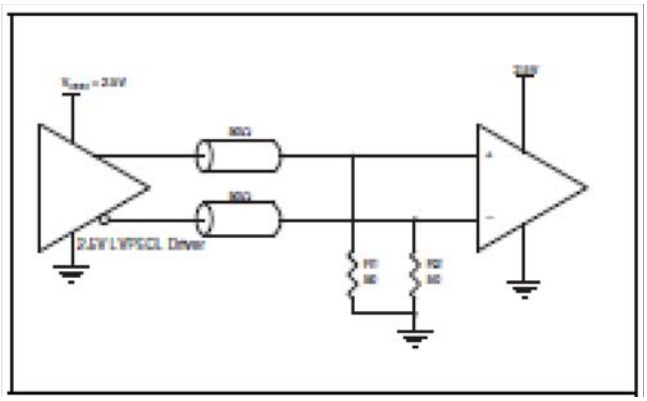


Figure 21. 2.5V LVPECL Output Termination

Table 23: LVPECL Output Port Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Condition
V_{OH}	Output High Voltage; NOTE 1	V_{CCO} – 1.3		V_{CCO} – 0.7	V	
V_{OL}	Output Low Voltage; NOTE 1	V_{CCO} – 2.0		V_{CCO} – 1.5	V	
V_{SWING}	Peak-to-Peak Output Voltage Swing	0.6		1.0	V	
t_{RISE}/t_{FALL}	Output Rise/Fall time	80		400	ps	20% to 80%
NOTE 1: Outputs terminated with 50Ω to V_{CCO} – 2V						

8.3.3 LVDS INPUT / OUTPUT PORT

8.3.3.1 LVDS INPUT PORT

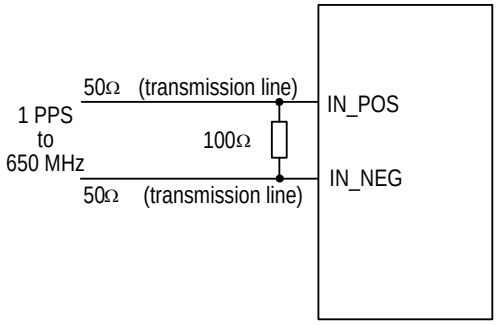


Figure 22. Recommended LVDS Input Port Line Termination

Table 24: LVDS Input Port Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Condition
V_{CM}	Input Common-mode Voltage Range	200	1200	2200	mV	
V_{DIFF}	Input Peak Differential Voltage	100	350	900	mV	
V_{IDTH}	Input Differential Threshold	-100		100	mV	
R_{TERM}	External Differential Termination Impedance		100		Ω	

8.3.3.2 LVDS Output Port

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (ZT) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown at the top part of Figure 23 can be used with either type of output structure. The termination schematic shown at the bottom part of Figure 23, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

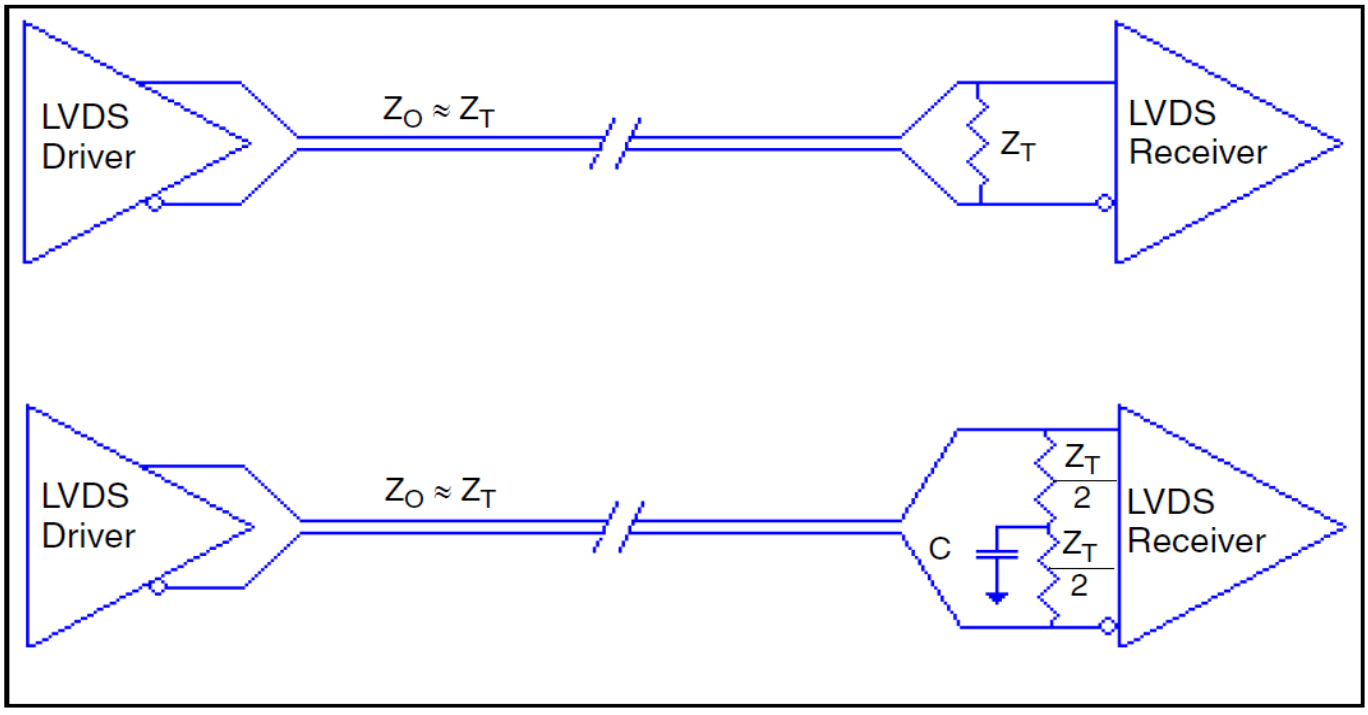


Figure 23. Recommended LVDS Output Port Line Termination

Table 25: LVDS Output Port Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Condition
V_{OD}	Differential Output Voltage	247		454	mV	
ΔV_{OD}	V_{OD} Magnitude Change			50	mV	
V_{OS}	Offset Voltage	1.125		1.375	V	
ΔV_{OS}	V_{OS} Magnitude Change			50	mV	
t_{RISE}/t_{FALL}	Output Rise/Fall time	90		400	ps	20% to 80%

8.3.4 OUTPUT CLOCK DUTY CYCLE

Table 26: Output Clock Duty Cycle (OUT1 - OUT9)

Clock Output Frequency	Min	Typ	Max	Unit	Test Condition
f_{OUT}<570MHz	45		55	%	
f_{OUT}≥570MHz	35		65	%	
NOTE: Output Duty Cycle configured using APLL1 or APLL2.					

Table 27: Output Clock Duty Cycle (OUT10 - OUT11)

Clock Output Frequency	Min	Typ	Max	Unit	Test Condition
f_{OUT}<600MHz	47		53	%	
f_{OUT}≥600MHz	45		55	%	

8.3.5 WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE-ENDED LEVELS

Figure 24 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Suggest edge rate faster than 1V/ns. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

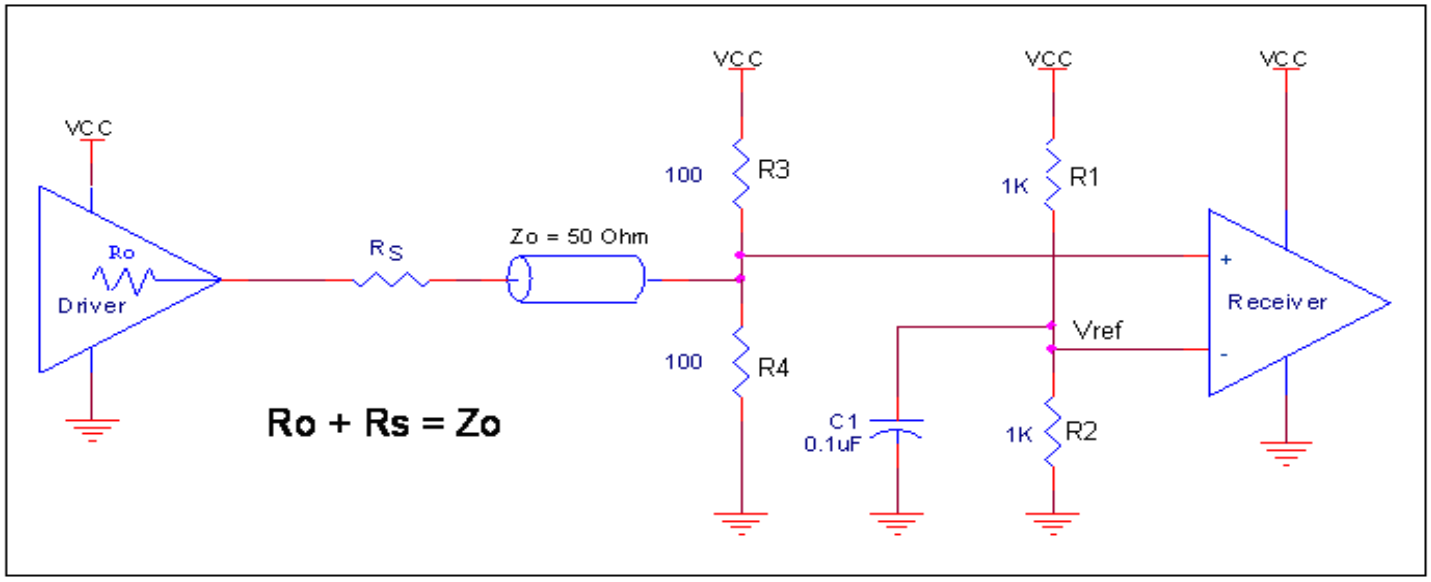


Figure 24. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Vth = VCC*[R2/(R1+R2)]

For the example in Figure 24, R1 = R2, so Vth = VCC/2 =1.65 V

The suggested single-ended signal input:

V_{IHmax} = VCC

V_{ILmin} = 0 V

V_{swing} = 0.6 V ~ VCC

DC offset (Swing Center) = Vth/2 +/- V_{swing}*10%

8.4 JITTER PERFORMANCE

Table 28: Gigabit Ethernet Output Clock Jitter Generation
(jitter measured on one differential output of APLL3 with all other outputs disabled)

Output Frequency	RMS Jitter Typ (ps)	RMS Jitter Max (ps)	Test Filter	Notes
25 MHz	0.26	0.32	2.5 kHz - 5 MHz	ITU-T G.8262 limit 0.5 UI p-p (1 UI = 0.8 ns)
	0.26	0.31	10 kHz - 5 MHz	IDT Target Test Filter for 10GbE
	0.19	0.24	637 kHz - 5 MHz	IEEE 802.3-2008 limit 0.24 UI p-p / 0.0174 UI RMS (1 UI = 0.8 ns)
	0.20	0.23	10 kHz - 1 MHz	
125MHz	0.24	0.30	2.5 kHz to 10 MHz	ITU-T G.8262 limit 0.5 UI p-p (1 UI = 0.8 ns)
	0.25	0.31	10 kHz - 20 MHz	IDT Target Test Filter for 10GbE
	0.15	0.19	637 kHz - 10 MHz	IEEE 802.3-2008 limit 0.24 UI p-p / 0.0174 UI RMS (1 UI = 0.8 ns)
	0.22	0.39	1 kHz - 1 MHz	
	0.20	0.23	10 kHz - 1 MHz	
156.25MHz	0.24	0.29	10 kHz - 20 MHz	IDT Target Test Filter for 10GbE
	0.25	0.30	20 kHz - 40 MHz	ITU-T G.8262 limit 0.5 UI p-p (1 UI = 100.47 ps)
	0.14	0.19	1 MHz - 30 MHz	
	0.10	0.12	1.875 MHz - 20 MHz	IEEE 802.3-2008 limit 0.28 UI p-p / 0.0203 UI RMS (1 UI = 100.47 ps)
	0.22	0.39	1 kHz - 1 MHz	
	0.20	0.23	10 kHz - 1 MHz	

Table 28: Gigabit Ethernet Output Clock Jitter Generation
(jitter measured on one differential output of APLL3 with all other outputs disabled)

Output Frequency	RMS Jitter Typ (ps)	RMS Jitter Max (ps)	Test Filter	Notes
625MHz	0.23	0.28	10 kHz - 20 MHz	IDT Target Test Filter for 10GbE
	0.25	0.31	20 kHz - 80 MHz	ITU-T G.8262 limit 0.5 UI p-p (1 UI = 100.47 ps) ITU-T G.8262 limit 1.2 UI p-p (1 UI = 38.79 ps)
	0.12	0.16	1 MHz - 30 MHz	
	0.07	0.09	1.875 MHz - 20 MHz	IEEE 802.3-2008 limit 0.28 UI p-p / 0.0203 UI RMS (1 UI = 100.47 ps)
	0.22	0.38	1 kHz - 1 MHz	
	0.21	0.24	10 kHz - 1 MHz	
NOTE 1: DPLL locked to input clock NOTE 2: For BER = 10–12, RMS jitter = p-p jitter/13.8 per IEEE 802.3-2008 and IEEE 802.3ae-2002 section 48B.3.1.3.1				

Table 29: Gigabit Ethernet Output Clock Jitter Generation
(jitter measured on one differential output of APLL1/2 with one differential output enabled)

Output Frequency	RMS Jitter Typ (ps)	RMS Jitter Max (ps)	Test Filter	Notes
25 MHz	0.71	1.31	2.5 kHz - 5 MHz	ITU-T G.8262 limit 0.5 UI p-p (1 UI = 0.8 ns)
	0.57	0.84	12 kHz - 5 MHz	
	0.28	0.42	637 kHz - 5 MHz	IEEE 802.3-2008 limit 0.24 UI p-p / 0.0174 UI RMS (1 UI = 0.8 ns)
125MHz	0.72	1.40	2.5 kHz to 10 MHz	ITU-T G.8262 limit 0.5 UI p-p (1 UI = 0.8 ns)
	0.58	0.86	12 kHz - 20 MHz	
	0.20	0.29	637 kHz - 10 MHz	IEEE 802.3-2008 limit 0.24 UI p-p / 0.0174 UI RMS (1 UI = 0.8 ns)

Table 29: Gigabit Ethernet Output Clock Jitter Generation
(jitter measured on one differential output of APLL1/2 with one differential output enabled)

Output Frequency	RMS Jitter Typ (ps)	RMS Jitter Max (ps)	Test Filter	Notes
156.25MHz	0.56	0.85	12 kHz - 20 MHz	
	0.52	0.99	20 kHz - 40 MHz	ITU-T G.8262 limit 0.5 UI p-p (1 UI = 100.47 ps)
	0.23	0.30	1 MHz - 30 MHz	
	0.16	0.22	1.875 MHz - 20 MHz	IEEE 802.3-2008 limit 0.28 UI p-p / 0.0203 UI RMS (1 UI = 100.47 ps)
NOTE 1: DPLL locked to input clock NOTE 2: For BER = 10–12, RMS jitter = p-p jitter/13.8 per IEEE 802.3-2008 and IEEE 802.3ae-2002 section 48B.3.1.3.1				

Table 30: Gigabit Ethernet Output Clock Jitter Generation
(Jitter measured on one CMOS output of APLL1/2 with one CMOS output enabled)

Output Frequency	RMS Jitter Typ (ps)	RMS Jitter Max (ps)	Test Filter	Notes
25 MHz	0.71	1.26	2.5 kHz - 5 MHz	ITU-T G.8262 limit 0.5 UI p-p (1 UI = 0.8 ns)
	0.55	0.83	12 kHz - 5 MHz	
	0.23	0.30	637 kHz - 5 MHz	IEEE 802.3-2008 limit 0.24 UI p-p / 0.0174 UI RMS (1 UI = 0.8 ns)
125MHz	0.78	2.32	2.5 kHz to 10 MHz	ITU-T G.8262 limit 0.5 UI p-p (1 UI = 0.8 ns)
	0.62	0.94	12 kHz - 20 MHz	
	0.21	0.31	637 kHz - 10 MHz	IEEE 802.3-2008 limit 0.24 UI p-p / 0.0174 UI RMS (1 UI = 0.8 ns)
NOTE 1: DPLL locked to input clock NOTE 2: For BER = 10–12, RMS jitter = p-p jitter/13.8 per IEEE 802.3-2008 and IEEE 802.3ae-2002 section 48B.3.1.3.1				

Table 31: Gigabit Ethernet LAN Output Clock Jitter Generation
(jitter measured on one differential output of APLL3 with all other outputs disabled)

Output Frequency	RMS Jitter Typ (ps)	RMS Jitter Max (ps)	Test Filter	Notes
161.1328125 MHz	0.23	0.27	10 kHz - 20 MHz	IDT Target Test Filter for 10GbE
	0.25	0.29	20 kHz - 40 MHz	ITU-T G.8262 limit 0.5 UI p-p (1 UI = 96.97 ps)
	0.14	0.19	1 MHz - 30 MHz	
	0.09	0.12	1.875 MHz - 20 MHz	IEEE 802.3-2008 limit 0.28 UI p-p / 0.0203 UI RMS (1 UI = 96.97 ps)
	0.20	0.22	10 kHz - 1 MHz	
322.265625 MHz	0.23	0.26	10 kHz - 20 MHz	IDT Target Test Filter for 10GbE
	0.25	0.30	20 kHz - 80 MHz	ITU-T G.8262 limit 0.5 UI p-p (1 UI = 96.97 ps)
	0.13	0.16	1 MHz - 30 MHz	
	0.07	0.10	1.875 MHz - 20 MHz	IEEE 802.3-2008 limit 0.28 UI p-p / 0.0203 UI RMS (1 UI = 96.97 ps)
	0.20	0.22	10 kHz - 1 MHz	
644.53125 MHz	0.23	0.27	10 kHz - 20 MHz	IDT Target Test Filter for 10GbE
	0.24	0.28	20 kHz - 80 MHz	ITU-T G.8262 limit 0.5 UI p-p (1 UI = 96.97 ps)
	0.12	0.15	1 MHz - 30 MHz	
	0.07	0.09	1.875 MHz - 20 MHz	IEEE 802.3-2008 limit 0.28 UI p-p / 0.0203 UI RMS (1 UI = 96.97 ps)
	0.20	0.23	10 kHz - 1 MHz	

NOTE 1: DPLL locked to input clock
NOTE 2: For BER = 10–12, RMS jitter = p-p jitter/13.8 per IEEE 802.3-2008 and IEEE 802.3ae-2002 section 48B.3.1.3.1

Table 32: SONET/SDH Output Clock Jitter Generation
(jitter measured on one differential output of APLL3 with all other outputs disabled)

Output Frequency	RMS Jitter Typ (ps)	RMS Jitter Max (ps)	Test Filter	Notes
77.76 MHz	0.25	0.28	12 kHz to 20 MHz	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p / 0.01 UI RMS (STM-16: 1UI = 0.40 ns)
	0.29	1.61	500 Hz to 1.3 MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-1: 1 UI = 6.43 ns)
	0.27	0.46	1 kHz to 5 MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-4: 1 UI = 1.61 ns)
	0.19	0.21	65 kHz to 1.3 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-1: 1 UI = 6.43 ns)
	0.18	0.21	250 kHz to 5 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-4: 1 UI = 1.61 ns)
155.52MHz	0.23	0.26	12 kHz to 20 MHz	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p / 0.01 UI RMS (STM-16: 1UI = 0.40 ns)
	0.29	1.90	500 Hz to 1.3 MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-1: 1 UI = 6.43 ns)
	0.27	0.38	1 kHz to 5 MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-4: 1 UI = 1.61 ns)
	0.24	0.28	5 kHz to 20 MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-16: 1UI = 0.40 ns)
	0.19	0.22	65 kHz to 1.3 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-1: 1 UI = 6.43 ns)
	0.18	0.21	250 kHz to 5 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-4: 1 UI = 1.61 ns)
	0.13	0.15	1 MHz to 20 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-16: 1UI = 0.40 ns)

Table 32: SONET/SDH Output Clock Jitter Generation
(jitter measured on one differential output of APLL3 with all other outputs disabled)

Output Frequency	RMS Jitter Typ (ps)	RMS Jitter Max (ps)	Test Filter	Notes
311.04 MHz	0.23	0.26	12 kHz to 20 MHz	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p / 0.01 UI RMS (STM-16: 1UI = 0.40 ns)
	0.26	0.30	20kHz to 80 MHz	GR-253-CORE and ITU-T G.813 Option 2 limit 0.3 UI p-p (STM-64: 1 UI = 0.10 ns) ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-64: 1 UI = 0.10 ns)
	0.14	0.19	4 MHz to 80 MHz	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p (STM-64: 1 UI = 0.10 ns) ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-64: 1 UI = 0.10 ns)
	0.30	1.77	500 Hz to 1.3 MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-1: 1 UI = 6.43 ns)
	0.27	0.41	1 kHz to 5 MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-4: 1 UI = 1.61 ns)
	0.23	0.27	5 kHz to 20 MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-16: 1UI = 0.40 ns)
	0.19	0.22	65 kHz to 1.3 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-1: 1 UI = 6.43 ns)
	0.18	0.21	250 kHz to 5 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-4: 1 UI = 1.61 ns)
	0.11	0.14	1 MHz to 20 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-16: 1UI = 0.40 ns)

Table 32: SONET/SDH Output Clock Jitter Generation
(jitter measured on one differential output of APLL3 with all other outputs disabled)

Output Frequency	RMS Jitter Typ (ps)	RMS Jitter Max (ps)	Test Filter	Notes
622.08 MHz	0.23	0.26	12 kHz to 20 MHz	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p / 0.01 UI RMS (STM-16: 1UI = 0.40 ns)
	0.25	0.29	20kHz to 80 MHz	GR-253-CORE and ITU-T G.813 Option 2 limit 0.3 UI p-p (STM-64: 1 UI = 0.10 ns) ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-64: 1 UI = 0.10 ns)
	0.10	0.14	4 MHz to 80 MHz	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p (STM-64: 1 UI = 0.10 ns) ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-64: 1 UI = 0.10 ns)
	0.30	1.41	500 Hz to 1.3 MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-1: 1 UI = 6.43 ns)
	0.28	0.51	1 kHz to 5 MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-4: 1 UI = 1.61 ns)
	0.23	0.28	5 kHz to 20 MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-16: 1UI = 0.40 ns)
	0.20	0.23	65 kHz to 1.3 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-1: 1 UI = 6.43 ns)
	0.19	0.22	250 kHz to 5 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-4: 1 UI = 1.61 ns)
	0.11	0.13	1 MHz to 20 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-16: 1UI = 0.40 ns)
NOTE 1: DPLL locked to input clock				

Table 33: SONET/SDH Output Clock Jitter Generation
(jitter measured on one differential output of APLL1/2 with one differential output enabled)

Output Frequency	RMS Jitter Typ (ps)	RMS Jitter Max (ps)	Test Filter	Notes
19.44 MHz	0.53	0.79	12 kHz to 1.3MHz	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p / 0.01 UI RMS (STM-16: 1UI = 0.40 ns)
	0.62	0.90	12kHz to 5MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-1: 1 UI = 6.43 ns)
	0.85	1.41	500 Hz to 1.3 MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-4: 1 UI = 1.61 ns)
	0.86	1.39	1 kHz to 5 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-1: 1 UI = 6.43 ns)
	0.33	0.46	65 kHz to 1.3 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-4: 1 UI = 1.61 ns)
	0.40	0.60	250 kHz to 5 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-4: 1 UI = 1.61 ns)
77.76 MHz	0.58	1.35	12 kHz to 20 MHz	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p / 0.01 UI RMS (STM-16: 1UI = 0.40 ns)
	0.87	1.45	500 Hz to 1.3 MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-1: 1 UI = 6.43 ns)
	0.82	1.38	1 kHz to 5 MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-4: 1 UI = 1.61 ns)
	0.29	0.40	65 kHz to 1.3 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-1: 1 UI = 6.43 ns)
	0.22	0.31	250 kHz to 5 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-4: 1 UI = 1.61 ns)

Table 33: SONET/SDH Output Clock Jitter Generation
(jitter measured on one differential output of APLL1/2 with one differential output enabled)

Output Frequency	RMS Jitter Typ (ps)	RMS Jitter Max (ps)	Test Filter	Notes
155.52 MHz	0.55	0.82	12 kHz to 20 MHz	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p / 0.01 UI RMS (STM-16: 1UI = 0.40 ns)
	0.87	1.52	500 Hz to 1.3 MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-1: 1 UI = 6.43 ns)
	0.81	1.43	1 kHz to 5 MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-4: 1 UI = 1.61 ns)
	0.65	1.03	5 kHz to 20 MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-16: 1UI = 0.40 ns)
	0.29	0.41	65 kHz to 1.3 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-1: 1 UI = 6.43 ns)
	0.21	0.30	250 kHz to 5 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-4: 1 UI = 1.61 ns)
	0.20	0.26	1 MHz to 20 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-16: 1UI = 0.40 ns)
NOTE 1: DPLL locked to input clock				

Table 34: SONET/SDH Output Clock Jitter Generation
(jitter measured on one CMOS output of APLL1/2 with one CMOS output enabled)

Output Frequency	RMS Jitter Typ (ps)	RMS Jitter Max (ps)	Test Filter	Notes
19.44 MHz	0.50	0.75	12 kHz to 1.3MHz	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p / 0.01 UI RMS (STM-16: 1UI = 0.40 ns)
	0.55	0.78	12kHz to 5MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-1: 1 UI = 6.43 ns)
	0.83	2.31	500 Hz to 1.3 MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-4: 1 UI = 1.61 ns)
	0.80	2.27	1 kHz to 5 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-1: 1 UI = 6.43 ns)
	0.29	0.54	65 kHz to 1.3 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-4: 1 UI = 1.61 ns)
	0.28	0.40	250 kHz to 5 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-4: 1 UI = 1.61 ns)
77.76 MHz	0.58	0.91	12 kHz to 20 MHz	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p (STM-4: 1 UI = 1.61 ns)
	0.87	2.39	500 Hz to 1.3 MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-1: 1 UI = 6.43 ns)
	0.82	2.10	1 kHz to 5 MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-4: 1 UI = 1.61 ns)
	0.29	0.42	65 kHz to 1.3 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-1: 1 UI = 6.43 ns)
	0.22	0.37	250 kHz to 5 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-4: 1 UI = 1.61 ns)
NOTE 1: DPLL locked to input clock				

Table 35: DPLL1/DPLL2 Output Clock Jitter Generation
(Jitter measured on one CMOS output of DPLL1/DPLL2 with all other outputs disabled)

Output Frequency	RMS Jitter Typ (ps)	RMS Jitter Max (ps)	Test Filter	Notes
10 MHz	100.11	619.64	100 Hz - 100 kHz	
N x 1.544 MHz (Note 2)	100.63	543.45	100 Hz - 40 kHz	
	16.06	39.94	8 kHz - 40 kHz	ANSI T1.403 limit 0.07 UI p-p (DS1: 1 UI = 647 ns)
N x 2.048 MHz (Note 3)	99.42	449.83	100 Hz - 100 kHz	
	10.66	26.44	18 kHz - 100 kHz	ITU-T G.823 limit 0.2 UI p-p (E1: 1 UI = 488 ns)
34.368 MHz	101.67	202.75	100 Hz - 800 kHz	
	25.62	39.06	10 kHz - 800 kHz	ITU-T G.751 limit 0.05 UI p-p (E3: 1 UI = 29.10 ns)
44.736 MHz	105.16	198.15	100 Hz - 400 kHz	
	20.77	27.44	30 kHz - 400 kHz	

NOTE 1:DPLL1/2 locked to input clock
NOTE 2: Measured on 12.352 MHz output clock
NOTE 3: Measured on 16.384 MHz output clock

Table 36: DPLL3 Output Clock Jitter Generation
(Jitter measured on one CMOS output of DPLL3 with all other outputs disabled)

Output Frequency	RMS Jitter Typ (ps)	RMS Jitter Max (ps)	Test Filter	Notes
N x 2.048 MHz Note 2	147.325	347.530	100 Hz - 100 kHz	
	8.02	17.24	18 kHz - 100 kHz	ITU-T G.823 limit 0.2 UI p-p (E1: 1 UI = 488 ns)
N x 1.544 MHz Note 3	133.88	303.43	100 Hz - 40 kHz	
	0.80	1.47	8 kHz - 40 kHz	ANSI T1.403 limit 0.07 UI p-p (DS1: 1 UI = 647 ns)

NOTE 1:DPLL3 locked to input clock
NOTE 2: Measured on 12.288 MHz output clock
NOTE 3: Measured on 12.352 MHz output clock

8.5 INPUT / OUTPUT CLOCK TIMING

The inputs and outputs are aligned ideally. But due to the circuit delays, there is delay between the inputs and outputs.

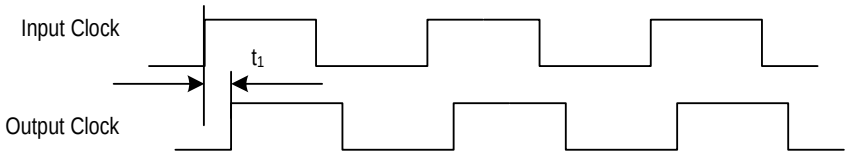


Figure 25. Input / output clock timing

Table 37: Input-to-Output Delay via APLL1/2

Output	t_1 Min (ns)	t_1 Max (ns)	t_1 Range (ns_{pp})
Any LVCMOS Input to any of OUT01, OUT02 or OUT07	13	19	6 (±3 around mean)
Any LVPECL/LVDS Input to any of OUT03, OUT04, OUT5 or OUT06	11.5	16.5	5 (±2.5 around mean)
Any Input to any APLL1/2 Output	10	19	9 (±4.5 around mean)
Any Input to [M]FRSYNC Output	0	8	8 (typical value is 2.5ns)
NOTE 1. The measurements in the above table takes into account any delays in the clock path from any input to any output; through either DPLL1 or DPLL2 and the either APLL1 or APLL2. NOTE 2. The measurements in the above table are over operational temperature, varying power supply and repeated power on/off cycle. NOTE 3. Measurements are taken using an ideal REF input and an ideal System clock to account for only internal delays in the device.			

8.6 OUTPUT / OUTPUT CLOCK TIMING

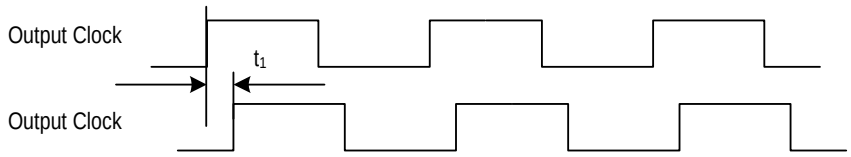


Figure 26. Output / output clock timing

Table 38: APLL1/2 Output-to-Output Delay

Output	t_1 Min (ps)	t_1 Max (ps)
Output-to-Output, LVCMOS (OUT01 to OUT02)	-110	110
Output-to-Output, LVPECL/LVDS (OUT03 to OUT04 or OUT05 to OUT06)	-85	85

PACKAGE OUTLINE DRAWINGS

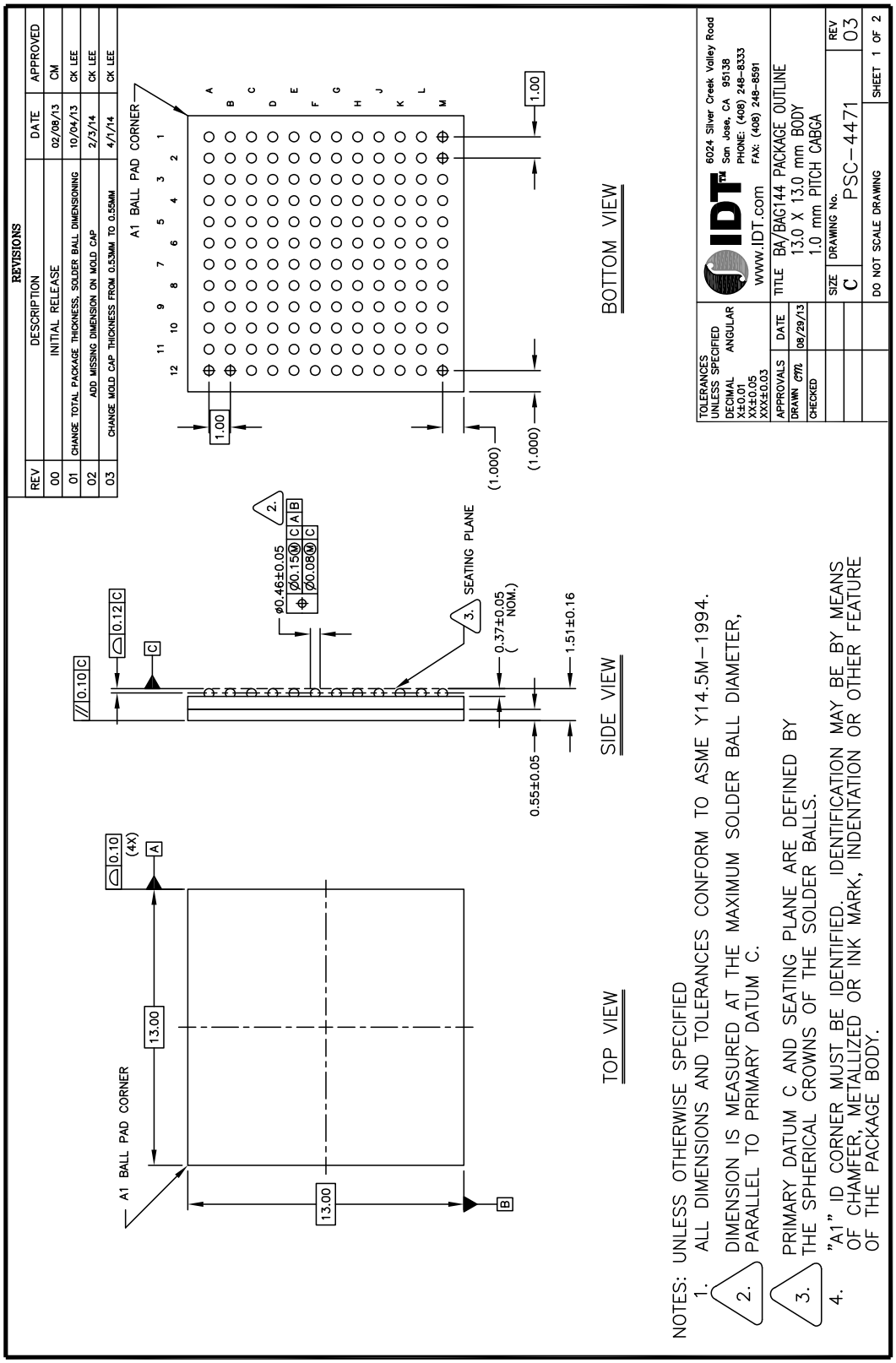


Figure 27. Package Outline Drawings – Page 1

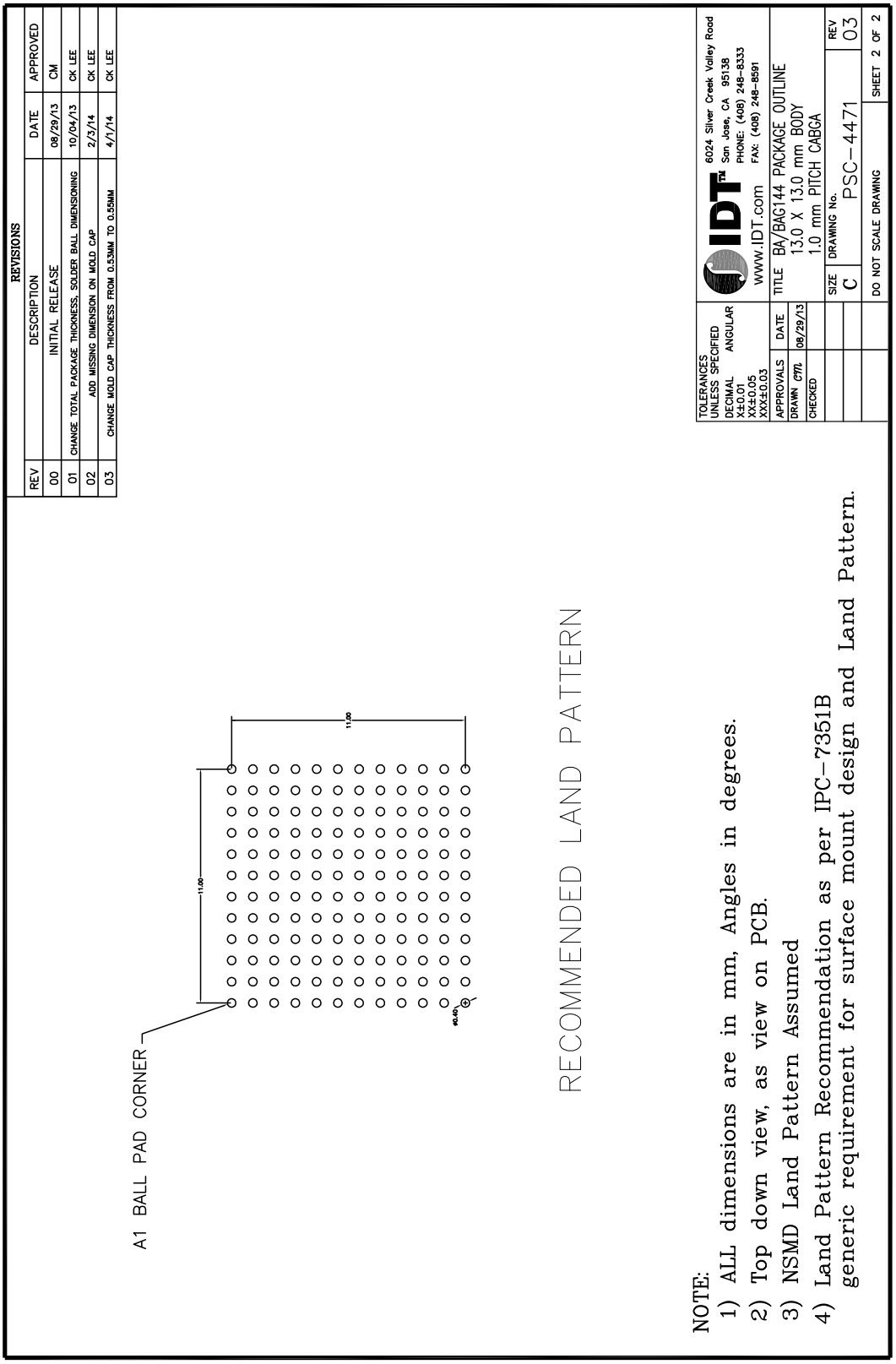


Figure 28. Package Outline Drawings – Page 2

ORDERING INFORMATION

Table 39: Ordering Information

Part/Order Number	Package	Temperature
82P33741BAG	144-pin CABGA green package	-40^0 to $+85^0$C

NOTE: “G” after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

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REVISION HISTORY

Revision Date	Description of Change
September 15, 2017	Updated Table 7 Updated the package outline drawings; however, no mechanical changes
December 8, 2016	Pages 1, 10, 17-18, 23-24, 56-57
October 26, 2016	Page 25
July 14, 2016	Pages 1, 5-6, 43-45, 56
March 21, 2016	Page 44
June 16, 2015	Pages 9, 11, 13, 34
May 13, 2015	Page 42
April 15, 2015	Pages 54, 56-58
February 6, 2015	Pages 32, 54 (Table 40), 57 (Table 42)
January 26, 2014	Page 29
December 19, 2014	Page 42
October 9, 2014	Page 9

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