



**5V/3.3V DUAL DIFFERENTIAL
DATA AND CLOCK
D FLIP-FLOP w/SET AND RESET**

**Precision Edge®
SY100EL29V**

FEATURES

- 3.3V and 5V power supply option
- Differential D, CLK and Q
- Extended V_{EE} range of $-3.0V$ to $-5.5V$
- V_{BB} output for single-ended use
- 1100MHz min. toggle frequency
- Asynchronous Reset and Set
- Fully compatible with Motorola MC100LVEL29 and MC100EL29
- Available in 20-pin SOIC package



Precision Edge®

DESCRIPTION

The SY100EL29V is a dual differential register with differential data (inputs and outputs) and clock. The registers are triggered by a positive transition of the positive clock (CLK) input. A HIGH on the Reset (Rx) asynchronously resets the appropriate register so that the Q outputs go LOW. A HIGH on the Set (Sx) asynchronously resets the appropriate register so that the Q outputs go HIGH. The Set and Reset inputs cannot both be HIGH simultaneously.

The differential input structures are clamped so that the inputs of unused registers can be left open without upsetting the bias network of the devices. The clamping action will assert the /D and the /CLK sides of the inputs. The noninverting input will pull down to V_{EE} and the inverting input will be biased around $V_{CC}/2$. Because of the edge-triggered flip-flop nature of the devices, simultaneously opening both the clock and data inputs will result in an output which reaches an unidentified but valid state.

The fully differential design of the devices makes them ideal for very high frequency applications where a registered data path is necessary.

PIN NAMES

Pin	Function
CLK, /CLK	Differential Clock Inputs
D[0:1], /D[0:1]	Differential Data Inputs
Q[0:1], /Q[0:1]	Differential Data Outputs
R_0, R_1	Reset Inputs
S_0, S_1	Set Inputs
V_{BB}	V_{BB} Reference Output
V_{CC}	V_{CC}
V_{EE}	V_{EE}

TRUTH TABLE

R	S	D	CLK	Q	/Q
L	L	L	Z	L	H
L	L	H	Z	H	L
H	L	X	X	L	H
L	H	X	X	H	L
H	H	X	X	Undef	Undef

NOTE:
Z = LOW-to-HIGH Transition

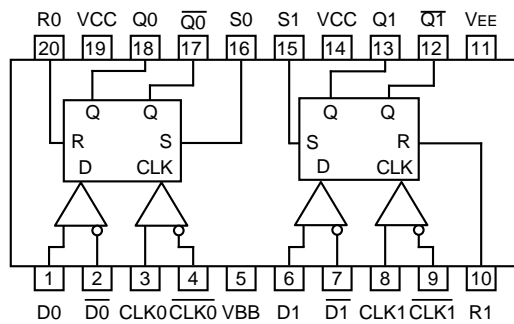
PACKAGE/ORDERING INFORMATION

Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100EL29VZC	Z20-1	Commercial	SY100EL29VZC	Sn-Pb
SY100EL29VZCTR ⁽²⁾	Z20-1	Commercial	SY100EL29VZC	Sn-Pb
SY100EL29VZI	Z20-1	Industrial	SY100EL29VZI	Sn-Pb
SY100EL29VZITR ⁽²⁾	Z20-1	Industrial	SY100EL29VZI	Sn-Pb
SY100EL29VZG ⁽³⁾	Z20-1	Industrial	SY100EL29VZG with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY100EL29VZGTR ^(2, 3)	Z20-1	Industrial	SY100EL29VZG with Pb-Free bar-line indicator	Pb-Free NiPdAu

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.



20-Pin Wide SOIC (Z20-1)

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Value	Unit
V_{EE}	Power Supply ($V_{CC} = 0V$)	-8.0 to 0	VDC
$V_{IN}^{(3)}$	Input Voltage ($V_{CC} = 0V$)	0 to -6.0	VDC
I_{OUT}	Output Current -Continuous -Surge	50 100	mA
T_{LEAD}	Lead Temperature (soldering, 20sec.)	+260	°C
T_A	Operating Temperature Range	-40 to +85	°C
V_{EE}	Operating Range ^{(1),(2)}	-5.7 to -3.0	V

Notes:

1. Absolute maximum rating, beyond which, device life may be impaired, unless otherwise specified on an individual data sheet.
2. Parametric values specified at: 100EL29V Series: -3.0V to -5.5V.
3. In PECL mode operation, $V_I(\text{Max}) = V_{CC}$.

DC ELECTRICAL CHARACTERISTICS
 $V_{EE} = -3.0V$ to $+5.5V$; $V_{CC} = \text{GND}$

Symbol	Parameter	$T_A = -40^\circ\text{C}$		$T_A = 0^\circ\text{C}$		$T_A = +25^\circ\text{C}$			$T_A = +85^\circ\text{C}$		Unit
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{EE}	Power Supply Current	—	50	—	50	—	30	50	—	50	mA
I_{IH}	Input HIGH Current	—	150	—	150	—	—	150	—	150	μA
I_{IL}	Input LOW Current /CLK, /Dn	0.5 -300	— —	0.5 -300	— —	0.5 -300	— —	— —	0.5 -300	— —	μA
V_{BB}	Output Reference Voltage	-1.38	-1.26	-1.38	-1.26	-1.38	—	-1.26	-1.38	-1.26	V

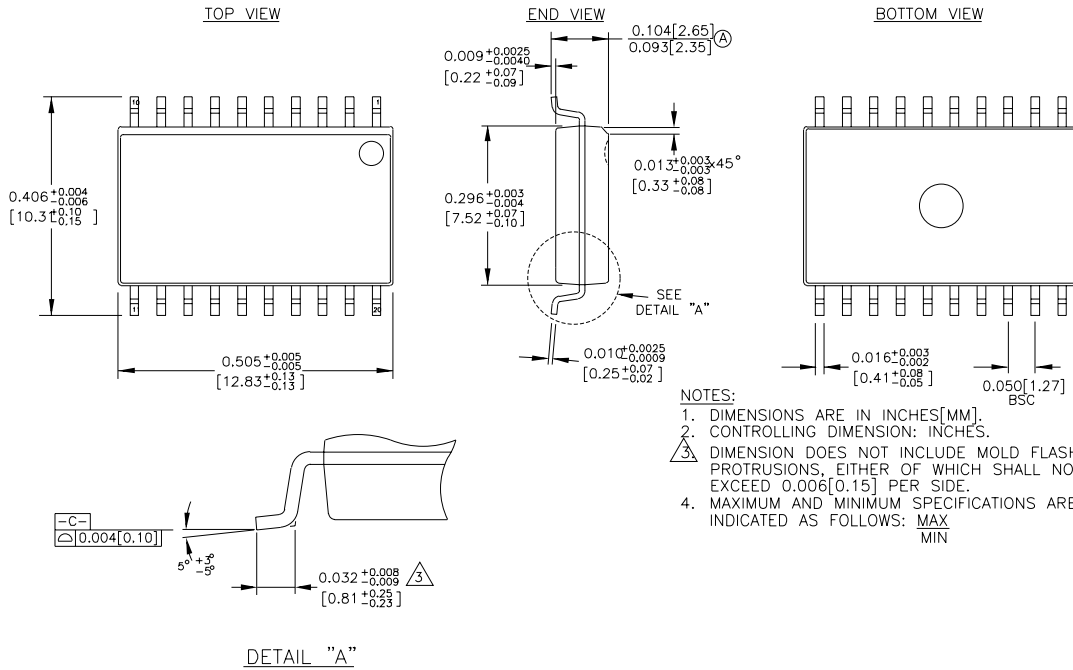
AC ELECTRICAL CHARACTERISTICS $V_{EE} = -3.0V$ to $+5.5V$; $V_{CC} = GND$

Symbol	Parameter	TA = -40°C		TA = 0°C		TA = +25°C			TA = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
f _{MAX}	Max. Toggle Frequency	1.1	—	1.1	—	1.1	—	—	1.1	—	GHz
t _{PD}	Propagation Delay to Output CLK S, R	480 450	680 670	490 450	690 670	500 450	— —	700 670	520 450	720 670	ps
t _S	Set-Up Time, D	200	—	200	—	200	—	—	200	—	ps
t _H	Hold Time, D	150	—	150	—	150	—	—	150	—	ps
t _{RR}	Reset Recovery Time	300	—	300	—	300	—	—	300	—	ps
t _{PW}	Minimum Pulse Width CLK, Set, Reset	400	—	400	—	400	—	—	400	—	ps
V _{CMR}	Common Mode Range ⁽¹⁾										V
	<500mV	-2.0	-0.4	-2.1	-0.4	-2.1	—	-0.4	-2.1	-0.4	
	≥500mV	-1.8	-0.4	-1.9	-0.4	-1.9	—	-0.4	-1.9	-0.4	
V _{PP(AC)}	Minimum Input Swing ⁽²⁾	150	—	150	—	150	—	—	150	—	mV
t _r t _f	Output Rise/Fall Time Q (20–80%)	280	550	280	550	280	330	550	280	550	ps

Notes:

- V_{CMR} is referenced to the most positive side of the differential input signal. Normal operation is obtained when the input signals are within the V_{CMR} range and the input swing is greater than V_{PP(Min.)} and <1V. The lower end of the V_{CMR} range varies 1:1 with V_{EE}. The numbers in the spec table assume a nominal V_{EE} = -3.3V. Note for PECL operation, the V_{CMR(Min)} will be fixed at 3.3V - |V_{CMR(Min)}|.
- Minimum input swing for which AC parameters are guaranteed.

20-PIN SOIC .300" WIDE (Z20-1)



Rev. 03

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