

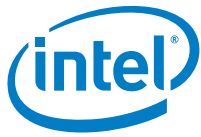
Intel® X557-AT/AT2/AT4 10 GbE PHY Datasheet

Networking Division (ND)

Features:

- 10GBASE-T Performance — Ability to support worst case channels while reducing power and latency when channel characteristics permit:
 - 100 m on augmented CAT 6 (CAT 6A and CAT 7)
 - 55 m on CAT 6 and best-effort using CAT 5e
 - Built-in thermal management capabilities — Enables deployment in thermally constrained environments
 - On-die thermal sensor with alarm and warning thresholds
- Note:** Details describing built-in thermal management capabilities will be made available in a future datasheet release.
- 19 x 19 mm (single/dual port) or 25 x 25 mm (quad port) flip-chip BGA or package — Low cost, flexible heat-sinking, and compatible with volume PCB manufacturing:
 - 1 mm ball pitch
 - Low thermal resistance (θ_{jc})
 - IEEE 802.3an-2008 compliant auto-negotiation — Interoperability with existing Ethernet infrastructure
 - External SPI Flash interface
 - High-Performance full KR (with auto-negotiation) / XFI / SGMII I/F with AC-JTAG- Ensures trouble-free operation over a range of interconnect scenarios
 - Loopback Capability — Enables extensive system test and debug with remote loopback control
 - Supports numerous loopbacks with pass-through capability
 - Integrated MDI Filter and Advanced RFI Cancellation — Patented RFI technology provided improved performance in the presence of RF interference
 - Eliminates external filter components

Order Number: 334279-002
Revision 2.2
June 2017



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Revision History

| Revision | Date | Comments |
|----------|------------|---|
| 2.2 | June 2017 | <ul style="list-style-type: none">• Update Bill Of Material (BOM) - added new Flash components. |
| 2.1 | April 2016 | <ul style="list-style-type: none">• Corrected minor pin table information.• Updated power and peak current information.• Updated BOM. |
| 2.0 | April 2015 | First release (Intel Public). |



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1.0 Overview

1.1 Introduction

The Intel® X557-AT/AT2/AT4 10 GbE PHY (X557) is a single (AT), dual (AT2), quad (AT4) port, 28 nm CMOS 10GBASE-T / 1000BASE-T / 100BASE-TX triple-speed PHY that is designed to be a low-power solution for all Network Interface Cards (NICs), switch, and LAN on Motherboard (LOM) applications that require 10GBASE-T capability.

This section is intended to provide an overview of the X557 and its operating modes.

A block diagram of the X557 is shown in [Figure 1-1](#). Each port uses a common analog front-end for all three modes of operation as well as a common system interface (configurable as dual KR/XFI in 10 GbE, 1000BASE-X for GbE and dual SGMII in 1 GbE / 100 Mb/s). In the 10 GbE mode transmit direction, data from the system interface is equalized and received. This data is then mapped into a virtual internal SGMII interface where blocks of two SGMII frames (32 bits of data + 4 bits of control) are encoded into a single 65-byte block, using the 64-byte/65-byte encoding scheme specified in Clause 55. In 10 GbE mode, 50 of these 65-byte blocks are aggregated together, along with a prepended auxiliary bit, and an appended CRC-8 to form the 3259-bit 10GBASE-T transmission frame payload. This payload is encoded using a combination of LDPC encoding and coset partitioning, with the LDPC encoding adding an additional 325 systematic check bits to produce a 3584-bit 10GBASE-T transmission frame. The coset partitioning effectively divides the frame up into 512 7-bit symbols, where the upper 3 bits are uncoded and describe the coset, while the lower 4 bits are coded and identify an element within the coset. These 8 cosets are then mapped onto a 128-DSQ constellation (a 16 x 16 checkerboard pattern) that is physically encoded as two back-to-back PAM-16 symbols. These symbols are then THP precoded, filtered, and sent out over the four twisted pairs in the cable.

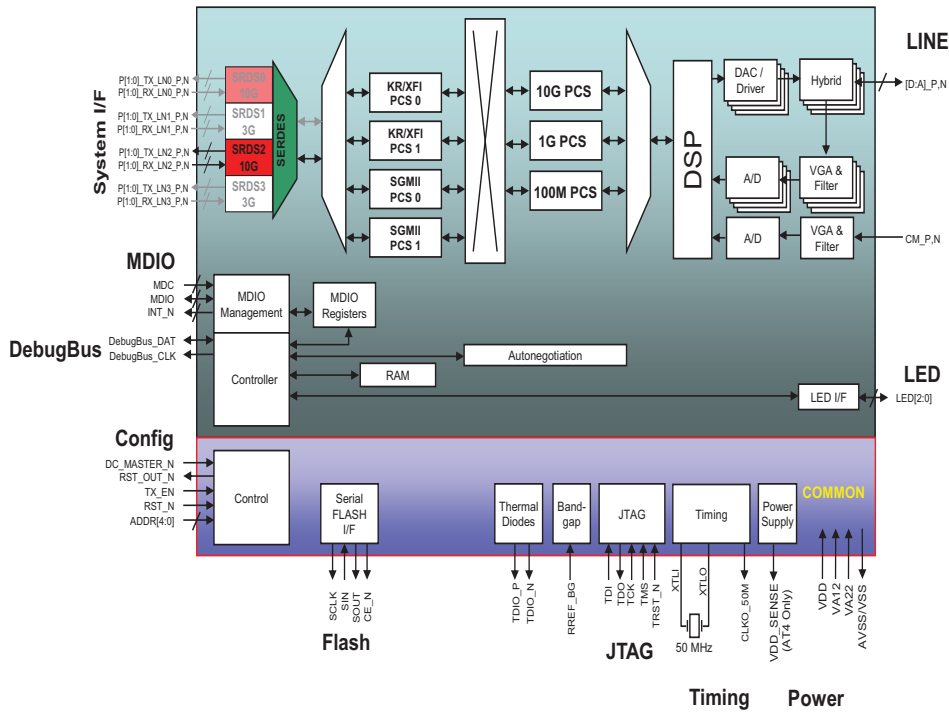


Figure 1-1 Intel® X557 10 GbE PHY Block Diagram

In the receive direction in 10 GbE mode, PAM-16 coded symbols enter the X557 from the line interface and pass through the hybrid, which provides transmit / receive isolation. These symbols are then filtered and amplified prior to being sampled by four high-speed, high-precision A/D converters. The outputs of these A/D converters are then passed through an extensive set of adaptive equalizers that provide both cross-talk and echo cancellation. After timing is recovered, the data from the four channels is aligned and merged together to form the original, but noisy transmission frames. In 10 GbE mode, the data is decoded using an LDPC decoder. However, in 10 GbE mode the data is further sliced using knowledge of the coset partitioning and 128-DSQ mapping to produce the original 10GBASE-T transmission frame payload. The CRC-8 over this payload is then checked to ensure integrity of the unencoded bits. Finally, in all schemes, the auxiliary bit is stripped, the 65-byte blocks remapped into XGMII blocks, and the received Ethernet data transmitted out the MAC interface.

When operating in 1 GbE or 100 Mb/s modes, receive data from the analog front-end is routed to either the 1 GbE or 100 Mb/s PCS where timing is recovered and equalization performed. In 1 GbE mode, Viterbi decoding is also done. From here, the data passes across a virtual GMII interface to the system interface which is SGMII mode on logical Lane 0. In the transmit direction, 1 GbE or 100 Mb/s data is received on the SGMII interface, passed through the 1 GbE or 100 Mb/s PCS and then transmitted by the common analog front-end.

Figure 1-2 shows a typical system-level block diagram of a 10GBASE-T channel with an optional dual-media interface built using the X557. On the line side of the X557, a robust interface providing good common-mode rejection and electrical protection against cable discharge is implemented. On the MAC side, the X557 provides a robust SerDes interface with configurable pre-emphasis and receive equalization. For test coverage, this interface also incorporates AC JTAG.

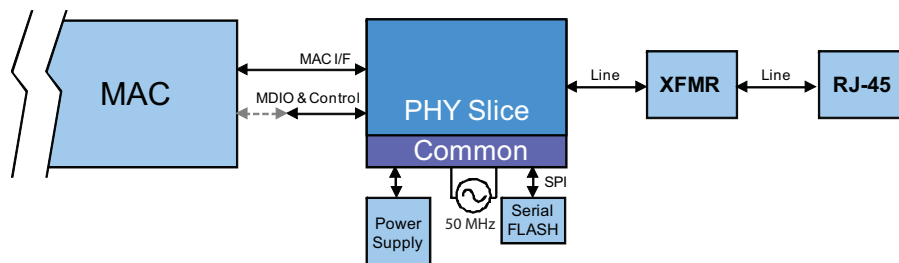


Figure 1-2 X557 10 GbE PHY Block Interconnect

On-chip, the X557 contains a 32-bit micro-controller that manages the state machines and operation of the various elements within the chip. Consequently, there is a great deal of flexibility afforded to the end user because of the presence of this micro-controller, and as such the X557 offers a high degree of control and flexibility. The image for the micro-controller is stored in an optional external SPI Flash. This interface also provides the user the capability of directly programming the Flash during manufacturing.

In addition to the Ethernet interfaces, the X557 provides three 20 mA LED outputs per port that are configurable via software to respond to a variety of conditions such as link activity and connection status. Clocking for the X557 is provided from a 50 MHz differential clock.

Power for the X557 is provided from three supply voltages, with configurable I/O voltage levels. In order to assist the system designer in deploying the X557, a reference design (part numbers, schematics, and layout) is provided that is optimized for performance, efficiency and cost.

1.2 Mechanical

The X557 is packaged in a 19 mm x 19 mm flip-chip, 324-pin BGA (single and dual port) or a 25 mm x 25 mm flip-chip 576 pin BGA (quad port) along with a thermal heat spreader. Consequently, the θ_{jc} is a low 0.42 °C/W. Meanwhile, the die is rated to operate up to 105 °C junction temperature, so engineering an appropriate thermal solution for the target system is a straight-forward task.

1.2.1 Power Supplies

The X557 uses these power supplies: a 0.83V digital supply (VDD), 1.2V and 2.1V analog supplies (VA12 and VA21, respectively) and 2.5V digital I/O. From an operating perspective, no power supply sequencing is required, but it is recommended that all supplies come up following the directions provided in section within 20 ms from the first rail rising to the last rail reaching its 70% voltage level.



For I/O, the X557 offers a separate VDD_IO supply, which sets the logic thresholds for the I/O at 70% / 30% of its voltage. In addition to the VDD_IO supply voltage of 2.5V, a separate control pin (MDIO_1P2_SELECT_N when pulled low) enables pins MDC, MDIO, TX_EN (single/dual port only) and RST_N to operate at 1.2V logic levels, regardless of the voltage on VDD_IO.

AVSS, VSS, and VSS_SRDS must be tied to the same ground plane.

1.2.2 Clocks

The X557-AT uses a 50 MHz differential clock to synthesize all required clocks.

Note: Either a 50 MHz crystal or a 50 MHz oscillator can be implemented with the X557-AT (single port) device (crystal mode or oscillator mode, XTAL_SELECT_N = 0b or XTAL_SELECT_N = 1b). However, a 50 MHz oscillator must be implemented for use with the X557-AT2 (dual port) and X557-AT4 (quad port) devices (LVDS oscillator mode).

1.2.3 Flash

The X557 is capable of operating with a 512 KB (4 Mb) or larger SPI serial Flash.

For Flash I/O, the X557 offers a separate VDD_FLASH supply that is used to run the Flash interface. VDD_FLASH requires 2.5V.

1.2.4 Power-on Default Values

The X557 has a fixed set of hardware default values that exist in the chip for all configurable registers. However, the firmware is capable of storing in its boot image any change to these defaults for up to 48 PHYs within a single image, effectively enabling the user to configure the chip to come out of reset in the desired operating state. This can be done by altering the boot image. Contact your Intel representative for more details about updating boot images.



1.2.5 SerDes Configuration

The X557 is capable of routing any logical SerDes lane to any physical SerDes lane as well as performing polarity inversions. On the line side, in addition to supporting MDI / MDI-X and automatic polarity correction, the X557 supports lane swapping of the A, B, C, and D pairs to enable easy board routing with different magnetics pinouts.

1.3 SerDes

The X557 is designed to be used in conjunction with a triple-speed MAC chip:

- KR/XFI for 10 GbE
- 1000BASE-X for 1 GbE (SerDes logical lane 0)
- SGMII for 100 Mb/s (SerDes logical lane 0)

Note: The X557-AT2 10 GbE PHY internally has four SerDes per PHY, but only physical lane 2 is connected. Consequently, the register map contains information for lanes 0, 1 and 3, but these cannot be used in the X557-AT2. The X557 is capable of being configured so that the MAC interface can start in one of the following modes:

1. Start with the 10 GbE interface on KR/XFI.
2. Start with the 1000BASE-X interface on (SGMII without auto-negotiation).
3. Start with extended SGMII auto-negotiation enabled.
4. Start with all interfaces off.

Once a connection to a link partner has been established, the interface switches to the correct MAC interface speed.

1.4 Power On

The X557 is designed to perform the following operations at boot:

1. Power-up calibration of the internal VCOs and variable power supplies (if variable supply operation is enabled).
2. Provision stored default values. X557 is capable of storing in its firmware image a list of registers whose default values should be overwritten with a user-specified value on power up. Contact your Intel representative for more details about enabling the PHY to be personalized for certain modes of operation.
3. Calibration of the analog front-end.
4. Auto-negotiation.
5. Perform training (as required).
6. Verify error-free operation.

7. Enter steady state.

1.5 Cable Diagnostics

The X557 implements a powerful cable diagnostic algorithm to accurately measure all of the TDR and TDT (cross-channel impulse responses) sequences within the group of four channels. The algorithm used transmits a pseudo-noise sequence with an amplitude of less than 300 mV for a brief period of time, and from this converges the 10GBASE-T equalizers on all of the other channels. From the results of this measurement, the length of each pair, the top impairment along the pair, and the impedance of the cable are flagged. These measurements are reported to an accuracy to $\pm 1\text{m}$ using a cable propagation characteristics of 4.83 ns/m and are presented in the global MMD register map.

1.6 Debug Tools

The X557 supports a full suite of network and system loopbacks at all 10 Gb/s rates. As well the X557 supports a network loopback with pass through and destructive merge, which means that the looped-back traffic is also passed through to the SerDes interface, as well looped back. In the transmit direction, any traffic on the SerDes interface is destructively merged with the loopback traffic. For example, the SerDes traffic takes priority over the looped-back traffic). This enables diagnosis of remote equipment while maintaining a remote session connection during a loopback test. Loopback is shown in [Figure 1-3](#).

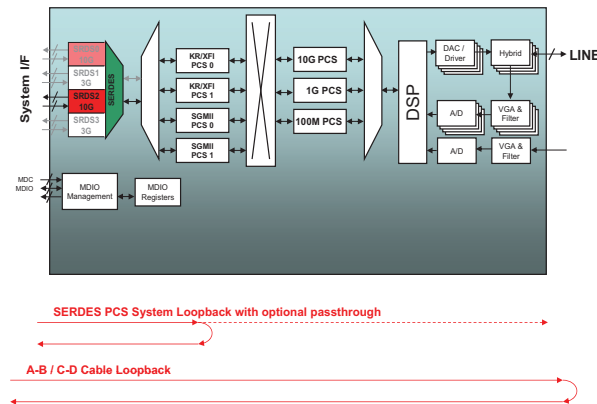


Figure 1-3 X557 Loopback

In addition to the loopbacks, the X557 supports CRC-32 packet checking on both the receive and transmit traffic at all rates, and maintains one second interval packet counters for both bad and good packets.

Finally, the X557 is able to generate all of the IEEE test mode patterns, as well as CRPAT generation and checking in both line and system directions.

On the KR interface, the X557 supports x^9 , x^{31} , square wave, and pseudo-noise generation and checking, as well as CRPAT generation and checking.



1.7 Energy Efficient Ethernet (EEE)

The X557 provides support for EEE on 10GBASE-T and 1000BASE-T interfaces. It is also capable of running in both normal operating mode, where the system controls entering and exiting from the EEE state and autonomous operation on the line where the PHY controls entering and exiting EEE operation via a provisioned no-traffic timer. If no traffic is seen within a certain period of time, the PHY goes to sleep on the line if connected at either 10 GbE or 1 GbE rates. This mode of operation requires the MACs to be in operation because rate pacing during startup is done via pause frames.



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2.0 Hardware Interfaces (X557-AT and X557-AT2)

Note: Any signal name that ends with an asterisk (*) or pin name that ends with _N are active low.

2.1 Management Interface

The management interface on the X557 is a two wire interface with a unidirectional MDC clock and a bidirectional MDIO data. The MDIO interface on the X557 is a robust implementation of this standard. It is designed to operate up to 18 MHz¹ and is capable of withstanding voltages up to double the operating voltage (the theoretical worst-case maximum reflection on an unterminated bus). It uses a Schmitt-trigger in conjunction with a de-bounce state machine to de-bounce the signals, and is capable of hot-insertion. The MDIO data line is capable of pulling low a 280 Ω load tied to 1.2V, and can be configured to support either open-drain, or push-pull operation in the Global General Provisioning 2: Address 1E.C441 register. Push-pull is the default operating mode.

In order to provide flexibility to the implementation, the X557 uses a programmable I/O voltage. The logic thresholds for the I/O are set at 70% and 30% for V_{IH}/V_{OH} and V_{IL}/V_{OL} , respectively for any V_{DD_IO} greater than 1.8V. For 1.2V MDIO operation (affects TX_EN, MDC, MDIO, RST_N) a separate signal called MDIO_1P2_SELECT_N is provided that will force 1.2V operation on these signals, regardless of the V_{DD_IO} voltage.

The management interface enables communication between the Station Management (STA) and a PHY. The STA is the external host controller which is the master of the management interface bus. Consequently, it always sources the MDC clock. When the MDIO is sourced by the STA, the PHY samples the MDIO at the rising edge of MDC. When the MDIO is sourced by the PHY during read operations, the STA samples the MDIO at the rising edge.

1. This is a function of whether the output is set to push-pull or open-drain mode, and on the capacitance of the bus.



Table 2-1 X557-AT

| Signal Name | Pin Name(s) | Pin Number(s) | Type | |
|--------------|---|---------------------------------|------|---|
| Interrupt* | P0_INT_N | K18 | OD | The 2.5V tolerant open-drain interrupt signal from PHY 0 of the X557. On reset this is set high. This input can be driven to operate at 1.2V via the MDIO_1P2_SELECT_N pin, regardless of the voltage on VDD_IO. This open-drain 20 mA outputs are on the VDD_IO domain. |
| MDIO Address | ADDR0 ADDR1 ADDR2 ADDR3 ADDR4 | K15 J15 J16 H16 G17 | I | The logic inputs to set the MDIO PHY address of the X557. These inputs are on the VDD_IO domain and have pull-up resistors associated with them. |
| MDIO Clock | MDC | J18 | I/O | The MDIO clock input for the X557. This tri-state 20 mA I/O is on the VDD_IO domain. |
| MDIO Data | MDIO | L18 | I/O | The MDIO data line (with Schmitt triggered logic levels) for PHY 0 of the X557. On reset, this is set to high-impedance. This tri-state 20 mA I/O is on the VDD_IO domain. |
| Reset Out* | RST_OUT_N | H3 | OD | The open-drain reset output from the X557. This might be used to drive the power-up reset signal for a board, as it outputs the on-chip power-up reset signal from the X557. This open-drain 20 mA output is on the VDD_IO domain. |
| Reset* | RST_N | J4 | I | The hard reset input (with Schmitt triggered logic levels) for the X557. This input can be driven to operate at 1.2V via the MDIO_1P2_SELECT_N pin, regardless of the voltage on VDD_IO. This input is on the VDD_IO domain and has a pull-up resistor associated with it. |
| Tx Enable | TX_EN | F5 | I | When pulled low, this input disables the output line drivers on the X557, and guarantees less than -53 dBm output power. This input can be driven to operate at 1.2V via the MDIO_1P2_SELECT_N pin, regardless of the voltage on VDD_IO. This input is on the VDD_IO domain and has a pull-up resistor associated with it. |



Table 2-2 X557-AT2

| Signal Name | Pin Name(s) | Pin Number(s) | Type | |
|---------------------|----------------------------------|--------------------------|------|---|
| Reserved | TX_DC_RST_N | H2 | O | Reserved. |
| Interrupt [1:0]* | P0_INT_N P1_INT_N | K18 K17 | OD | The 2.5V tolerant open-drain interrupt signal from PHY 0 of the X557. On reset this is set high. This input can be driven to operate at 1.2V via the MDIO_1P2_SELECT_N pin, regardless of the voltage on VDD_IO. These open-drain 20 mA outputs are on the VDD_IO domain. |
| Invert MDIO Address | INV_ADDR0 | K15 | I | When set, these logic inputs invert the corresponding LSBs of the MDIO PHY address of the X557 (XOR function). This is used to change the counting order of the PHYs within the X557. This input is on the VDD_IO domain and has a pull-up resistor associated with it. |
| MDIO Address | ADDR1 ADDR2 ADDR3 ADDR4 | J15 J16 H16 G17 | I | The logic inputs to set the MDIO PHY address of the X557. These inputs are on the VDD_IO domain and have pull-up resistors associated with them. |
| MDIO Clock [1:0] | P0_MDC P1_MDC | J18 J17 | I/O | The MDIO clock input for PHY 0 of the X557. This input can be driven to operate at 1.2V via the MDIO_1P2_SELECT_N pin, regardless of the voltage on VDD_IO. These tri-state 20 mA I/Os are on the VDD_IO domain. |
| MDIO Data [1:0] | P0_MDIO P1_MDIO | L18 L17 | I/O | The MDIO data line (with Schmitt triggered logic levels) for PHY 0 of the X557. On reset, this is set to high-impedance. This I/O can be driven to operate at 1.2V via the MDIO_1P2_SELECT_N pin, regardless of the voltage on VDD_IO. These tri-state 20 mA I/Os are on the VDD_IO domain. |
| Reset Out* | RST_OUT_N | H3 | OD | The open-drain reset output from the X557. This might be used to drive the power-up reset signal for a board, as it outputs the on-chip power-up reset signal from the X557. This open-drain 20 mA output is on the VDD_IO domain. |
| Reset* | RST_N | J4 | I | The hard reset input (with Schmitt triggered logic levels) for the X557. This input can be driven to operate at 1.2V via the MDIO_1P2_SELECT_N pin, regardless of the voltage on VDD_IO. This input is on the VDD_IO domain and has a pull-up resistor associated with it. |
| Tx Enable | TX_EN | F5 | I | When pulled low, this input disables the output line drivers on the X557, and guarantees less than -53 dBm output power. This input can be driven to operate at 1.2V via the MDIO_1P2_SELECT_N pin, regardless of the voltage on VDD_IO. This input is on the VDD_IO domain and has a pull-up resistor associated with it. |



Table 2-3 shows the management interface frame format (802.3-2005 45.3). The fields are described in the sections that follow.

Table 2-3 MDIO Frame Format

| Frame | PRE | ST | OP | PHYAD | MMDAD | TA | Data | Idle |
|-----------------------------|-------|----|----|-------|--------|----|------------------|------|
| Address | 1...1 | 00 | 00 | PPPPP | EEEEEE | 10 | AAAAAAAAAAAAAAAA | Z |
| Write | 1...1 | 00 | 01 | PPPPP | EEEEEE | 10 | DDDDDDDDDDDDDDDD | Z |
| Read | 1...1 | 00 | 11 | PPPPP | EEEEEE | Z0 | DDDDDDDDDDDDDDDD | Z |
| Post-read increment address | 1...1 | 00 | 10 | PPPPP | EEEEEE | Z0 | DDDDDDDDDDDDDDDD | Z |

Idle (idle condition):

The idle condition on the management interface is a high-impedance state. All tri-state drivers are disabled and the pull-up resistor(s) on the MDIO bus will pull the MDIO line to a one.

PRE (preamble):

Normal operation — At the beginning of each transaction, the station management entity will send a sequence of 32 contiguous ones on the MDIO data line, along with 32 corresponding cycles on the MDC to provide the MMD with a pattern that it can use to establish synchronization. Each MMD will observe a sequence of 32 contiguous one bits on MDIO with 32 corresponding cycles on MDC before it responds to any transaction.

Preamble suppression — The MDIO interface can optionally disable preamble detection by setting the *MDIO Preamble Detection Disable* bit in the Global General Provisioning 2: Address 1E.C441 register. In this mode of operation, one or more preamble bit are required followed by the 0x0 start of frame ST bits.

ST (start of frame):

The start of frame for indirect access cycles is indicated by the <00> pattern. This pattern assures a transition from the default one and identifies the frame as an indirect access. Frames that contain the ST=<01> pattern defined in Clause 22 will be ignored by the MMDs within the X557.

OP (operation code):

The operation code field indicates the type of transaction being performed by the frame. A <00> pattern indicates that the frame payload contains the address of the register to access. A <01> pattern indicates that the frame payload contains data to be written to the register whose address was provided in the previous address frame. A <11> pattern indicates that the frame is read operation. A <10> pattern indicates that the frame is a post-read increment address operation.

PHYAD (PHY address):

The PHY address is five bits, allowing for 32 unique PHY addresses, and hence up to 32 PHYs on an MDIO bus. The address of the PHY is determined from ADDR[4:0] for the X557-AT and ADDR[4:1] for the X557-AT2 pins. The first PHY address bit to be transmitted and received is the MSB of the address. The station management entity must have a priori knowledge of the appropriate PHY address for each PHY to which it is attached, whether connected to a single PHY or to multiple PHYs.



MMDAD (MMD address):

The MMD address is five bits, allowing for 32 unique MMDs per PHY. The first MMD address bit transmitted and received is the MSB of the address.

In addition the X557 supports a broadcast mode when the PHYAD is 0x00. Only the write and load address opcodes are supported in broadcast mode. Read and post-read increment opcodes are ignored in broadcast mode. This mode of operation can be enabled via the *MDIO Broadcast Mode Enable* bits in the Global General Provisioning 2: Address 1E.C441 register.

TA (turnaround):

The turnaround time is a 2-bit time spacing between the MMD address field and the data field of a management frame to avoid contention during a read transaction. For a read or post-read increment address transaction, both the STA and the MMD remain in a high-impedance state for the first bit time of the turnaround. The MMD then drives a zero bit during the second bit time of the turnaround of a read or post-read increment address transaction. During a write or address transaction, the STA transmits a one for the first bit time of the turnaround and a zero for the second bit time of the turnaround. This behavior is shown in

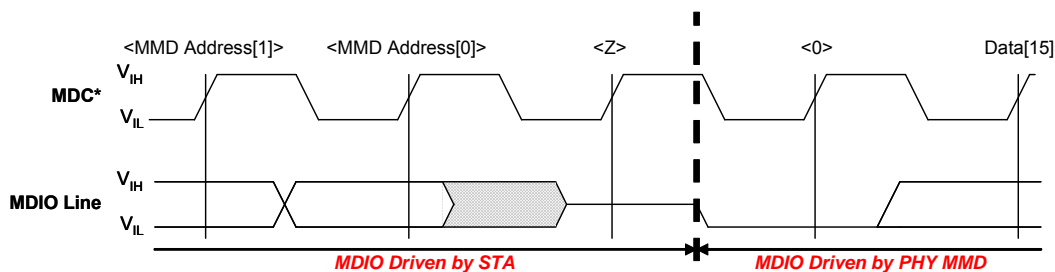


Figure 2-1 MDIO Bus Turn-around During Read Operations

Address / Data:

The address/data field is 16 bits. For an address cycle, it contains the address of the register to be accessed on the next cycle. For the data cycle of a write frame, the field contains the data to be written to the register. For a read or post-read increment address frame, the field contains the contents of the register. The first bit transmitted and received shall be bit 15.

For counters that are greater than 16-bits, the LSW must be read first, then the MSW must be read immediately afterwards. When the LSW is read, the counter is cleared and the MSW is stored in a shadow register. Reading the MSW actually reads the shadow register.

Optionally the host may read the MSW first, then the LSW immediately afterwards by setting the *MDIO Read MSW First Enable* bit in the Global General Provisioning 2: Address 1E.C441 register.



2.1.1 Interrupt

The X557 supports an open-drain interrupt pin per PHY.

2.1.2 Reset

The X557 is capable of generating a RST_OUT_N signal from its internal power-on reset generation circuitry that can be used by the external board circuitry.

Operation of the reset machinery is as follows:

1. Release from the Reset state begins when the RST_N input is high¹, and all of the core power supplies are above their required thresholds. These thresholds are listed in

Table 2-4 Power-on Reset Thresholds for Core Supply Voltages

| Supply | Parameter | Min | Max | Units |
|--------|--|------|------|-------|
| VCC2P1 | Power-on reset threshold for VCC2P1 DC supply. | 1.70 | 1.80 | V |
| VCC1P2 | Power-on reset threshold for VCC1P2 DC supply. | 0.93 | 0.99 | V |
| VDD | Power-on reset threshold for VDD DC supply. | 0.56 | 0.60 | V |

2. Once all of the conditions for release from reset are true, a 20 ms timer engages, the purpose of which is to enable the supplies to settle prior to allowing the PHY to boot.
3. After the 20 ms timer has completed, hardware state machines designed to guarantee PLL and band-gap stability engage.
4. After the PLLs and band-gap are locked and functioning properly, the processor and digital circuitry are released from reset.
5. The PHY image is then loaded and the processor boots.
6. After the processor boots, any provisioned register values are set, and the PHY enters the provisioned operating state.
7. Once this completes, the processor raises the MMD reset bits and sets the reset completed alarm, indicating it has completed reset and is ready for operation.

2.1.3 Configuration

The X557 contains a number of static configuration pins which are used to set the power-up operation of the X557. These signals are:

1. MDIO address ADDR[4:0] for the X557-AT and ADDR[4:1] for the X557-AT2.
2. Transmit Enable

1. Note that there are no timing requirements on issuance of reset relative to the clock.



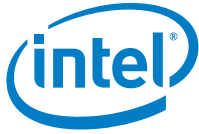
In the X557-AT2 package, the MDIO addressing is tied off internally so that the LSB increments according to the PHY number in the package. This MDIO address can either be overridden via a register in the Global MMD via provisioning, or the incrementation order can be altered via the INV_ADDR0 pin which is exclusive OR'd with address pin ADDR0.

2.2 Serial Flash

2.2.1 SPI Flash Interface

| Signal Name | Pin Name(s) | Pin Number(s) | Type | |
|------------------------|-------------|---------------|------|--|
| Reserved | RX_DC_CLK | J1 | I | Reserved |
| Reserved | TX_DC_CLK | N18 | O | Reserved |
| Reserved | RX_DC_DATA | H1 | I | Reserved |
| Reserved | TX_DC_DATA | M17 | O | Reserved |
| Reserved | DC_MASTER_N | E1 | I | Reserved |
| Reserved | RX_DC_RST_N | N17 | I | Reserved |
| Reserved | TX_DC_RST_N | H2 | O | Reserved |
| Reserved | RX_DC_SOF | J2 | I | Reserved |
| Reserved | TX_DC_SOF | M18 | O | Reserved |
| SPI Chip Enable | CE_N | G2 | O | The SPI CE* signal from the X557 to the serial Flash. On reset this is set high. This 20 mA output is on the VDD_FLASH domain. |
| SPI Serial Clock | SCLK | G1 | O | The SPI clock from the X557 to the serial Flash. On reset this is set low. This 20 mA output is on the VDD_FLASH domain. |
| SPI Serial Input Data | SIN | F1 | I | The SPI input data from the serial FLASH to the X557. This input is on the VDD_FLASH domain and has a pull-up resistor associated with it. |
| SPI Serial Output Data | SOUT | F2 | I | The SPI output data from the X557 to the serial Flash. On reset this is set low. This 20 mA output is on the VDD_FLASH domain. |

The SPI interface is responsible for connecting the X557 to the external Flash memory device. The micro-controller on the X557 accesses the boot code and the X557 default register values from the Flash memory after power-on reset. This Flash memory is also accessible via the MDIO interface for firmware updates and manufacturing burn via the registers in the Global MMD.



The SPI interface is a four wire, unidirectional, serial bus as shown in Figure 2-2. It is composed of a serial clock output SCLK, a serial data output SOUT, a serial data input SIN, and a chip-select CE*. All the signals are unidirectional.

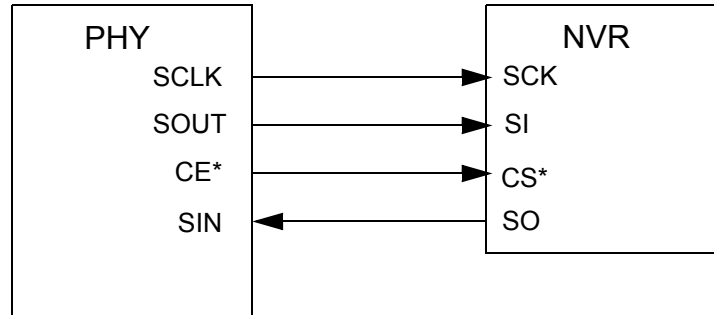


Figure 2-2 SPI Interface Block Diagram

The X557 is set up to function as a Mode 0 (0,0) SPI device, which means that the clock defaults to zero when not bursting. Data on this interface, for both SIN and SOUT, is always sourced on the falling edge of SCLK, and sampled on the rising edge of SCLK.

The following figures show typical read, burst read, and write operations for the X557. In all of these scenarios, the Non-volatile RAM (NVR) interface in the Global MMD is used to access the Flash.

Note: NVR used throughout this document is synonymous with Non-volatile Memory (NVM).

The NVR interface in the X557 is designed to be able to output any arbitrary opcode, followed by a programmable zero to three address bytes, followed by a programmable zero to four data bytes. This allows any variation of opcodes to be output to the attached Flash device. This interface also supports a burst read and write mode, which keeps the CS* line pulled low to enable back-to-back reads and writes. To support this, the NVR interface supports two 16-bit address registers and two 16-bit data registers, which allows up to 4 data bytes in a burst over the SPI interface. In order to extend this to longer bursts, the X557 halts the clock after the last bit in the data burst allowing the host processor to load another block of data to / from the NVR interface. This is shown in Figure 2-3 through Figure 2-5 and enables the data burst to be extended by as many bytes as necessary, without outstripping the MDIO's I/O capabilities.

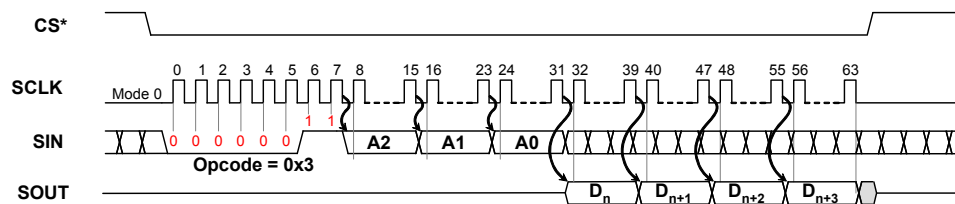


Figure 2-3 SPI Read

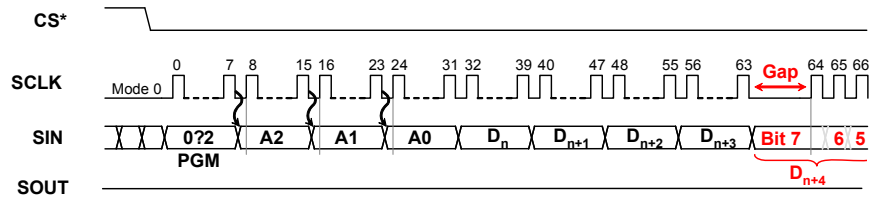


Figure 2-4 SPI Burst Read

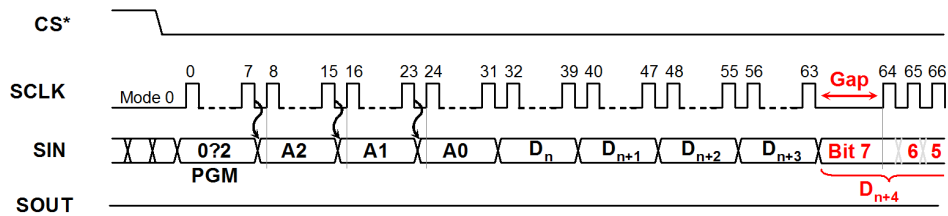


Figure 2-5 SPI Burst Write



Note that typical NVRs require that writing be performed on a block basis, and thus the addresses usually wrap within the block being programmed. As such, it is desirable from a speed and efficiency perspective to attempt to write entire blocks, versus pieces of blocks.

In order to assure that no polling is required on NVR interface, it is recommended that the NVR clock speed be set to at least¹:

$$f_{\text{SCLK}} > \frac{64}{63} \cdot f_{\text{MDIO}}$$

The desired Flash memory should be chosen to be at least 512K bytes in size, and must be capable of interfacing to a 2.5V CMOS SPI.

2.3 Firmware

The X557 contains a 32-bit micro-controller. This micro-controller is designed to have its IRAM and DRAM either loaded on power-up / reset from the attached FLASH or to have its boot image loaded by the host processor via the MDIO interface.

1. This is derived from the fact that the longest burst instruction on the SPI is 64 bits, at one bit per clock, whereas to write a register on the MDIO takes 64 clocks, and the data is not written until the last bit - hence the 63.



2.4 SerDes

Table 2-5 X557-AT

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|-------------|----------------------------|---------------|------|--|
| Lane 0 Rx | P0_RX_LN0_P P0_RX_LN0_N | P2 P1 | I | Physical Lane 0 differential Rx of the X557 SerDes interface. This lane can operate in KR, XFI and SGMII mode |
| Lane 0 Tx | P0_TX_LN0_P P0_TX_LN0_N | T2 T1 | O | Physical Lane 0 differential Tx of the X557 SerDes interface. This lane can operate in KR, XFI and SGMII mode. |
| Lane 1 Rx | P0_RX_LN1_P P0_RX_LN1_N | U2 V2 | I | Physical Lane 1 differential Rx of the X557 SerDes interface. This lane can operate in SGMII mode |
| Lane 1 Tx | P0_TX_LN1_P P0_TX_LN1_N | U3 V3 | O | Physical Lane 1 differential Tx of the X557 SerDes interface. This lane can operate in SGMII mode. |
| Lane 2 Rx | P0_RX_LN2_P P0_RX_LN2_N | U4 V4 | I | Physical Lane 2 differential Rx of the X557 SerDes interface. This lane can operate in KR, XFI and SGMII mode |
| Lane 2 Tx | P0_TX_LN2_P P0_TX_LN2_N | U6 V6 | O | Physical Lane 2 differential Tx of the X557 SerDes interface. This lane can operate in KR, XFI and SGMII mode. |
| Lane 3 Rx | P0_RX_LN3_P P0_RX_LN3_N | U7 V7 | I | Physical Lane 3 differential Rx of the X557 SerDes interface. This lane can operate in SGMII mode. |
| Lane 3 Tx | P0_TX_LN3_P P0_TX_LN3_N | U8 V8, | O | Physical Lane 3 differential Tx of the X557 SerDes interface. This lane can operate in SGMII mode. |

Table 2-6 X557-AT2

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|-------------|--|------------------------|------|--|
| Lane 0 Rx | P0_RX_LN0_P P0_RX_LN0_N P1_RX_LN0_P P1_RX_LN0_N | P2 P1 U10 V10 | I | Physical Lane 0 differential Rx of the X557 SerDes interface. This lane can operate in KR, XFI and SGMII mode. |
| Lane 0 Tx | P0_TX_LN0_P P0_TX_LN0_N P1_TX_LN0_P P1_TX_LN0_N | T2 T1 U12 V12 | O | Physical Lane 0 differential Tx of the X557 SerDes interface. This lane can operate in KR, XFI and SGMII mode. |



| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|-------------|--|------------------------|------|--|
| Lane 1 Rx | P0_RX_LN1_P P0_RX_LN1_N P1_RX_LN1_P P1_RX_LN1_N | U2 V2 U13 V13 | I | Physical Lane 1 differential Rx of the X557 SerDes interface. This lane can operate in SGMII mode. |
| Lane 1 Tx | P0_TX_LN1_P P0_TX_LN1_N P1_TX_LN1_P P1_TX_LN1_N | U3 V3 U14 V14 | O | Physical Lane 1 differential Tx of the X557 SerDes interface. This lane can operate in SGMII mode. |
| Lane 2 Rx | P0_RX_LN2_P P0_RX_LN2_N P1_RX_LN2_P P1_RX_LN2_N | U4 V4 U15 V15 | I | Physical Lane 2 differential Rx of the X557 SerDes interface. This lane can operate in KR, XFI and SGMII mode |
| Lane 2 Tx | P0_TX_LN2_P P0_TX_LN2_N P1_TX_LN2_P P1_TX_LN2_N | U6 V6 U17 V17 | O | Physical Lane 2 differential Tx of the X557 SerDes interface. This lane can operate in KR, XFI and SGMII mode. |
| Lane 3 Rx | P0_RX_LN3_P P0_RX_LN3_N P1_RX_LN3_P P1_RX_LN3_N | U7, V7, T17, T18 | I | Physical Lane 3 differential Rx of the X557 SerDes interface. This lane can operate in SGMII mode |
| Lane 3 Tx | P0_TX_LN3_P P0_TX_LN3_N P1_TX_LN3_P P1_TX_LN3_N | U8, V8, R17, R18 | O | Physical Lane 3 differential Tx of the X557 SerDes interface. This lane can operate in SGMII mode. |

The X557 SerDes interface is both robust and flexible and provides numerous loopback and diagnostic capabilities that eases system interface-PHY board design and bring up as well as AC JTAG. The interface is capable of providing arbitrary lane swapping and inversion. In the transmit direction, there is a programmable 4-tap equalizer (1 pre-cursor, and 2 post-cursor taps) as well as the ability to program the Tx drive strength and Tx termination. In the receive direction, there is programmable gain and programmable boost.

In SGMII mode, the interface operates at 1.25 Gb/s over SerDes logical Lane 0 and is compliant to the Cisco* SGMII specification[10]. In KR mode, one 10 GbE interface is provided operating over Lane 2.

The SerDes interface on the X557 also contains diagnostic pattern generation and checking functionality listed [Table 2-7](#):

Table 2-7 KR Diagnostic Pattern Capabilities

| Test | Description | Generate | Check | Invert |
|---------------|-----------------------|----------|-------|--------|
| x^9 PRBS | $x^9 + x^5 + 1$ | 3 | 3 | 3 |
| x^{31} PRBS | $x^{31} + x^{28} + 1$ | 3 | 3 | 3 |



| Test | Description | Generate | Check | Invert |
|--------------|-----------------------|----------|-------|--------|
| Square Wave | Clause 49.2.12 | 3 | 3 | 3 |
| Pseudo-Noise | | 3 | 3 | 3 |
| CRPAT | IEEE 802.3 Annex48A.4 | 3 | 3 | 3 |

Table 2-8 SGMII Diagnostic Pattern Capabilities

| Test | Description | Generate | Check | Invert |
|-------|-----------------------|----------|-------|--------|
| CRPAT | IEEE 802.3 Annex48A.4 | 3 | 3 | 3 |

All of the parameters associated with the SerDes interface have provisionable default values, which means that the X557 SerDes interface can be tailored to power-up with the optimal settings for any given application.

2.5 SerDes Operating Modes

For the purposes of this discussion, the X557 can be viewed as a set of blocks as shown below:

On the left side of the diagram is the system interface, which consists of the four SerDes lanes. Lanes 0 and 2 have the ability to run at rates from 1.25 Gb/s to 10.3125 Gb/s. These lanes support SGMII and KR. The other two lanes only support 1.25 Gb/s and 3.125 Gb/s rates (SGMII). At the PCS layer, there are two SGMII cores and two KR cores.

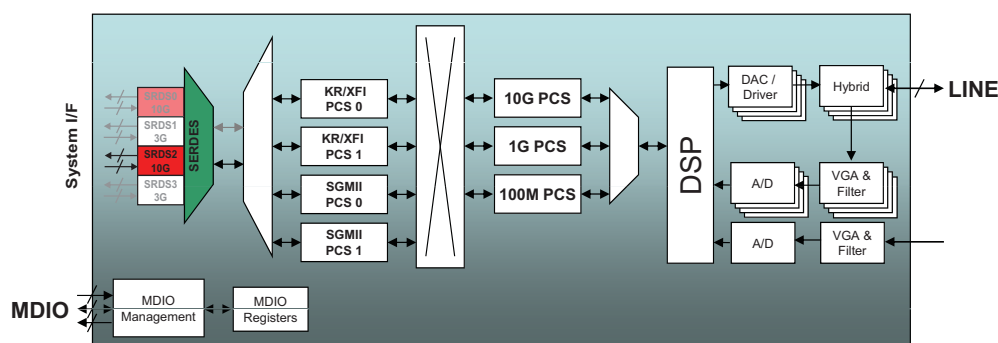


Figure 2-6 X557-AT/AT2 Operational Blocks

These different SerDes operating modes are summarized in [Table 2-9](#).



Table 2-9 SerDes Lane Assignments for Different Operating Modes

| Interface | Operating Mode / Core Used | Lane 0 | Lane 1 | Lane 2 | Lane 3 |
|-----------|----------------------------|--------|--------|--------|--------|
| System | SGMII1 | X | X | X | X |
| | KR1 | | | X | |

2.6 SerDes System I/F Startup

In startup on the system interface side, there are three different operating scenarios for the SerDes I/F:

- 10 GbE mode (KR or XFI)
- 1000BASE-X mode
- SGMII
- All-off mode

These different modes affect only the system interface and function independently of whether the MDI interface is selected or not.

2.6.1 10 GbE Mode

1. In this mode, which is the hardware default, the X557 comes up in the pre-configured 10 GbE mode (KR/XFI) and transmits Local Faults / Idles, and remains in this state until a connection to a link partner is established.
2. After connection to a link partner has been established, the X557 will either stay in the pre-configured 10 GbE mode, or switch to 1000BASE-X mode on logical Lane 0, or 100 Mb/s SGMII mode depending on that the auto-negotiated line rate was.
3. Once the SerDes I/F has synchronized, traffic flows.
 - a. If the link fails and the system interface was in 10 GbE mode, the X557 generates a Local Fault message towards the system I/F, effectively restarting. If the link had transitioned to 1 GbE operation, the SerDes is restarted in 10 GbE mode generating Local Faults / Idles.
4. Auto-negotiation restarts after the link break timer expires.

2.6.2 1000BASE-X Mode

1. In this mode the X557 comes up in 1000BASE-X mode on logical Lane 0 and transmits idles, and remains in this state until a connection to a link partner is established.
2. After a connection to a link partner has been established, the X557 will either stay in 1000BASE-X mode, or switch to the pre-configured 10 GbE mode, or 100 Mb/s SGMII mode depending on that the auto-negotiated line rate was.



3. Once the SerDes I/F has synchronized, traffic flows.
4. If the link fails and the system interface was in the pre-configured 10 GbE mode (KR/XFI), the X557 generates a Local Fault message towards the system I/F, and effectively restarts in 1000BASE-X mode, generating Idles. Otherwise the link just stays in 1000BASE-X mode generating Idles.
5. Auto-negotiation restarts after the link break timer expires.

2.6.3 SGMII Mode

1. In this mode, the X557 comes up in SGMII mode. After sending and receiving an ACK on an SGMII link-down, auto-negotiation message (see [Table 2-11](#)), the SerDes transmits idles and remains in this state until a link partner connection is established.
2. After a connection to a link partner has been established, the X557 sends an SGMII link-up, auto-negotiation message with the appropriate rate (see [Table 2-11](#)) and receives an ACK.
3. Upon receiving the acknowledge from the system interface, the X557 either switches to 100 Mb/s SGMII mode, stays in 1 GbE SGMII mode (essentially 1000BASE-X) or switches to the pre-configured 10 GbE mode (KR or XFI), depending on whether the auto-negotiated line rate was 1 GbE / 100 Mb/s or 10 GbE.
4. Once the SerDes interface has synchronized, traffic flows.
5. If the link fails and the X557 was in the pre-configured 10 GbE mode, the X557 generates a local fault message towards the system interface and then transitions back to SGMII mode, where it sends and receives an ACK on an SGMII link-down, auto-negotiation message and then resumes transmitting idles. If the link fails and the X557 was in 1 GbE SGMII mode, the X557 first sends and receives an ACK on an SGMII link-down, auto-negotiation message and then resumes transmitting idles with no interruption in SerDes operation. If the system interface was in 100 Mb/s SGMII mode, the SerDes transitions back to SGMII mode, where it sends and receives an ACK on an SGMII link-down, auto-negotiation message and then resumes transmitting idles.
6. Auto-negotiation restarts after the link break timer expires.



2.6.4 All-Off Mode

1. In this mode the Intel® X557-AT/AT2/AT4 10 GbE PHY comes up with the system interface off, and remains in this state until connection to a link partner is established.
2. After connection to a link partner has been established, the Intel® X557-AT/AT2/AT4 10 GbE PHY will either turn on 1000BASE-X on logical Lane 0, or turn on the pre-configured 10 GbE mode (KR), or 100 Mb/s SGMII mode depending on that the auto-negotiated line rate was.
3. Once the SerDes I/F has synchronized, traffic flows.
4. If the link fails and was in the pre-configured 10 GbE mode, the Intel® X557-AT/AT2/AT4 10 GbE PHY generates a Local Fault message towards the system I/F and shuts off. Otherwise the system interface just shuts off.
5. Auto-negotiation restarts after the link break timer expires.

2.6.5 Interrupts

In all of these modes, the processor has the ability to generate an interrupt upon completing auto-negotiation.

2.7 MDI

Table 2-10 X557-AT2

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|--------------|--------------------|---------------|------|--|
| PHY 0 CMS | P0_CM_P P0_CM_N | E8 D8 | I/O | PHY 0 Common Mode Sense Input. |
| PHY 0 Pair A | P0_A_P P0_A_N | B2 A2 | I/O | PHY 0 Pair A of the X557 line interface. These should connect to the Pair A inputs of the transformer, with capacitive bypassing via the center-tap. On reset this is set to high-impedance. |
| PHY 0 Pair B | P0_B_P P0_B_N | B4 A4 | I/O | PHY 0 Pair B of the X557 line interface. These should connect to the Pair B inputs of the transformer, with capacitive bypassing via the center-tap. On reset this is set to high-impedance. |
| PHY 0 Pair C | P0_C_P P0_C_N | B6 A6 | I/O | PHY 0 Pair C of the X557 line interface. These should connect to the Pair C inputs of the transformer, with capacitive bypassing via the center-tap. On reset this is set to high-impedance. |
| PHY 0 Pair D | P0_D_P P0_D_N | B8 A8 | I/O | PHY 0 Pair D of the X557 line interface. These should connect to the Pair D inputs of the transformer, with capacitive bypassing via the center-tap. On reset this is set to high-impedance. |



| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|--------------|--------------------|---------------|------|--|
| PHY 1 CMS | P1_CM_P P1_CM_N | C18 B18 | I/O | PHY 1 Common Mode Sense Input. |
| PHY 1 Pair A | P1_A_P P1_A_N | B11 A11 | I/O | PHY 1 Pair A of the X557 line interface. These should connect to the Pair A inputs of the transformer, with capacitive bypassing via the center-tap. On reset this is set to high-impedance. |
| PHY 1 Pair B | P1_B_P P1_B_N | B13 A13 | I/O | PHY 1 Pair B of the X557 line interface. These should connect to the Pair B inputs of the transformer, with capacitive bypassing via the center-tap. On reset this is set to high-impedance. |
| PHY 1 Pair C | P1_C_P P1_C_N | B15 A15 | I/O | PHY 1 Pair C of the X557 line interface. These should connect to the Pair C inputs of the transformer, with capacitive bypassing via the center-tap. On reset this is set to high-impedance. |
| PHY 1 Pair D | P1_D_P P1_D_N | B17 A17 | I/O | PHY 1 Pair D of the X557 line interface. These should connect to the Pair D inputs of the transformer, with capacitive bypassing via the center-tap. On reset this is set to high-impedance. |

Table 2-11 X557-AT

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|-------------|--------------|---------------|------|--|
| CMS | CM_P CM_N | E8 D8 | I/O | Common Mode Sense Input. |
| Pair A | A_P A_N | B2 A2 | I/O | Pair A of the X557 line interface. These should connect to the Pair A inputs of the transformer, with capacitive bypassing via the center-tap. On reset this is set to high-impedance. |
| Pair B | B_P B_N | B4 A4 | I/O | Pair B of the X557 line interface. These should connect to the Pair B inputs of the transformer, with capacitive bypassing via the center-tap. On reset this is set to high-impedance. |
| Pair C | C_P C_N | B6 A6 | I/O | Pair C of the X557 line interface. These should connect to the Pair C inputs of the transformer, with capacitive bypassing via the center-tap. On reset this is set to high-impedance. |
| Pair D | D_P D_N | B8 A8 | I/O | Pair D of the X557 line interface. These should connect to the Pair D inputs of the transformer, with capacitive bypassing via the center-tap. On reset this is set to high-impedance. |

In 10 GbE mode, the line interface on the Intel® X557-AT/AT2/AT4 10 GbE PHY is capable of driving up to 100 m of CAT-6a unshielded twisted pair or 100 m of CAT-7 shielded cable (100 Ω differential impedance). It can also drive 55 m of CAT-6 cable, and a lesser distance of CAT-5e cable¹. In 1 GbE and 100 Mb/s modes, it can drive 130m of CAT-5e (or better) cable. It is designed to drive this via a quad, 50 Ω, center-tapped 1:1 transformer connected to an RJ-45 PCB-mount jack.

1. This distance is indeterminate because CAT-5e cable performance is not specified past 100 MHz.



The line interface on the Intel® X557-AT/AT2/AT4 10 GbE PHY supports automatic A/B and C/D pair swaps, inversions (auto-X), and semi-cross (A/B or C/D only). It also supports a provisioned ABCD to DCBA pair reversal for ease of routing with stack-jacks via bit 1.E400.0 and the MDI_CFG pin, which sets the configuration on power-up. Note that this reversal does not swap polarities, thus A+ maps to D+, etc.

2.8 Timing

The Intel® X557-AT/AT2/AT4 10 GbE PHY contains a high-performance synthesizer, which is capable of producing all of the clocks required internally, as well as sourcing the recovered 50 MHz CMOS clock for use by other components in the system. This synthesizer operates from either an external 100 μ W 50.000 MHz crystal (future X557-AT) or from a differential 50 MHz clock.

Note: Either a 50 MHz crystal or a 50 MHz oscillator can be implemented with the X557-AT (single port) device (crystal mode or oscillator mode, XTAL_SELECT_N = 0b or XTAL_SELECT_N = 1b). However, a 50 MHz oscillator must be implemented for use with the X557-AT2 (dual port) and X557-AT4 (quad port) devices (LVDS oscillator mode, XTAL_SELECT_N = 1b).

Table 2-12 X557-AT2

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|-------------|------------------|---------------|------|--|
| Clock Input | CLK_P CLK_N | F18 G18 | I | The 50 MHz differential LVDS reference clock input for the X557. This DC-coupled input has an internal 100 Ω termination resistor associated with it. |
| Reserved | RNC_N15 | N15 | I | Reserved |
| Reserved | RNC_D1 RNC_C1 | D1 C1 | I | Reserved |
| Reserved | RNC_D2 | D2 | O | Reserved |
| Reserved | RNC_E2 | E2 | O | Reserved |



Table 2-13 X557-AT

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|--------------------------|------------------|---------------|------|--|
| Crystal Input (future) | XTAL_I | F18 | I | The 50 MHz reference clock input for the X557. When XTAL_SELECT_N is pulled low, these pins operate in crystal mode, otherwise they are the differential LVDS inputs for an external oscillator, with XTAL_I being the positive input and XTAL_O being the negative input. In oscillator mode, this DC-coupled input has an internal 100 Ω termination resistor associated with it. |
| Crystal Output (future) | XTAL_O | G18 | I | The 50 MHz crystal oscillator output of the X557. This connects to the output of an inverting amplifier. In XO mode, this is high-impedance. |
| Reserved | RNC_N15 | N15 | I | Reserved |
| Reserved | RNC_D1 RNC_C1 | D1 C1 | I | Reserved |
| Reserved | RNC_D2 | D2 | O | Reserved |
| 50 MHz Clock Termination | 50M_CLK_TERM | G13 | I | Selects whether PHY provides 100 Ω differential termination for a 50 MHz clock input: 1b = Terminated. 0b = Open. This input is on the VDD_IO domain and has a pull-up resistor associated with it. |
| Clock Source Select* | XTAL_SELECT_N | F17 | I | The 50 MHz reference clock source selector for the X557-AT. When XTAL_SELECT_N is pulled low, these XTAL_I and XTAL_O pins operate in crystal mode; otherwise, they operate in LVDS oscillator input mode. This input is on the VDD_IO domain and has a pull-up resistor associated with it. |



2.9 LED

The X557 supports three 20 mA open-drain CMOS LED outputs.

Table 2-14 X557-AT2

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|-----------------|-------------------------------|----------------|------|---|
| PHY 0 LED [2:0] | P0_LED0 P0_LED1 P0_LED2 | K1 L1 M1 | OD | The 2.5V tolerant, open-drain LED outputs for PHY 0. These open-drain 20 mA outputs are on the VDD_IO domain. |
| PHY 1 LED [2:0] | P1_LED0 P1_LED1 P1_LED2 | K2 L2 M2 | OD | The 2.5V tolerant, open-drain LED outputs for PHY 1. These open-drain 20 mA outputs are on the VDD_IO domain. |

Table 2-15 X557-AT

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|-------------|----------------------|----------------|------|---|
| LED [2:0] | LED0 LED1 LED2 | K1 L1 M1 | OD | The 2.5V tolerant, open-drain LED outputs for the PHY. These open-drain 20 mA outputs are on the VDD_IO domain. |



2.10 Reference Resistors

The X557 relies on 1% precision resistors to calibrate its internal voltage levels.

Table 2-16 X557-AT2

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|----------------------------|----------------------|---------------|--------|---|
| Bandgap Reference Resistor | RREF_BG0 RREF_BG1 | A10 B10 | Analog | The connection point for the bandgap reference resistor. This should be a precision 1%, 2.00 kΩ resistor tied to ground |

Table 2-17 X557-AT

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|----------------------------|-------------|---------------|--------|---|
| Bandgap Reference Resistor | RREF_BG | A10 | Analog | The connection point for the bandgap reference resistor. This should be a precision 1%, 2.00 kΩ resistor tied to ground |

2.11 Test

The X557 supports a IEEE 1149.1 compliant JTAG interface, with 1149.6 AC JTAG support on the SerDes interface. Note that for normal operation, TRST_N should be held low.

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|------------------|-------------|---------------|------|--|
| JTAG Clock | TCK | K14 | I | The JTAG clock input. This input is on the VDD_IO domain and has a pull-down associated with it. |
| JTAG Data Input | TDI | L14 | I | The JTAG data input signal. This input is on the VDD_IO domain and has a pull-down associated with it. |
| JTAG Data Output | TDO | L15 | O | The JTAG data output signal. This 20 mA output is on the VDD_IO domain. |



| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|----------------------|-------------|---------------|------|--|
| JTAG Reset* | TRST_N | M15 | I | The JTAG reset signal. If JTAG is not used, this pin must be pulled low. This input is on the VDD_IO domain and has a pull-up associated with it. |
| JTAG Test Mode State | TMS | M16 | I | The JTAG test mode state signal. This input is on the VDD_IO domain and has a pull-down associated with it. |

2.12 Metrology

The X557 contains two thermal diodes (note that the X557-AT only has one thermal diode) that can be used to monitor the die temperature without going through the MDIO registers. The “P” indicates the anode terminal (such as current input) of the thermal diode.

Table 2-18 X557-AT2

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|---------------------|----------------------|---------------|--------|--------------------------------|
| PHY 0 Thermal Diode | TDIO_P_0 TDIO_N_0 | G3 F3 | Analog | PHY 0 thermal diode terminals. |
| PHY 1 Thermal Diode | TDIO_P_1 TDIO_N_1 | F14 G15 | Analog | PHY 1 thermal diode terminals. |

Table 2-19 X557-AT

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|---------------|----------------------|---------------|--------|--------------------------|
| Thermal Diode | TDIO_P_0 TDIO_N_0 | G3 F3 | Analog | Thermal diode terminals. |



2.13 Debug

The X557 supports a side-access port to the MDIO register space via a slave SMBus. Addressing for this SMBus is provisioned on a per PHY basis. It is recommended that every design connect these SMBus pins to a header to allow in-system debug. This obviates the need to disconnect the MDIO lines, and allows for normal system operation during debug.

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|----------------|--------------|---------------|------|--|
| DebugBus Clock | DebugBus_CLK | H17 | I | Clock signal for slave SMBus used for debug port into PHY MDIO register space. This signal requires a pull-up to VDD_IO. This input is on the VDD_IO domain and has a pull-down associated with it. |
| DebugBus Data | DebugBus_DAT | H18 | I/O | Data signal for slave SMBus used for debug port into the PHYs MDIO register space. This signal requires a pull-up to VDD_IO. This 20 mA I/O is on the VDD_IO domain and has a pull-down associated with it. |

2.14 Power

The X557 uses four separate power supplies to minimize power consumption:

- 0.83V
- 1.2V
- 2.1V
- 2.5V

As mentioned earlier, in order to provide maximum flexibility to the implementation, the X557 utilizes a programmable I/O voltage. The logic thresholds for the I/O are set at 70% and 30% for VIH/VOH and VIL/VOL respectively for any VDD_IO greater than 1.8V. For 1.2V MDIO operation (affects TX_EN, MDC, MDIO, RST_N), a separate signal called MDIO_1P2_SELECT_N is provided that will force 1.2V operation on these signals, regardless of the VDD_IO voltage.

Table 2-20 X557-AT2

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|-------------|-------------|---|--------|---------------------|
| AVDD | VCC1P2 | D4, D6, E5, E7, E9, D11, D13, D15, E12, E14 | Supply | 1.2V analog supply. |
| AVDD22 | VCC2P1 | A3, A5, A7, A9, C3, C5, C7, C9, A12, A14, A16, C12, C14, C16, D17 | Supply | 2.1V analog supply. |



| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|----------------------|------------------------------|--|--------|---|
| AVSS | AVSS | B3, B5, B7, B9, B12, B14, B16, C2, C4, C6, C8, C11, C13, C15, C17, D3, D5, D7, D9, D12, D14, D16, D18, E4, E11, E13, E15, E17, F6, F8, F10, F12, G5, G7, G9, G11, H6, H8, H10, H12 | Supply | Analog ground. |
| AVSSPLL | VSS | E6, E15 | Supply | Analog ground for PHY PLL. |
| Analog VDD | VDD | E10, E16 | Supply | 0.83V supply for digital circuitry in the AFE. |
| VCC Crystal | VCC2P1 | E18 | Supply | 2.1V supply for the crystal oscillator. |
| VDD | VDD | J6, J8, J10, J12, K5, K7, K9, K11, K13, L6, L8, L10, L12, M7, M9, M11, M13, N6, N8, N10, N12, P5, P7, P9, P11, P13, R8, R10, R12 | Supply | 0.83V digital supply. |
| VDD FLASH | VDD_FLASH | E3 | Supply | Flash I/O power supply (2.5V). |
| VDD I/O Power Supply | VDD_IO | J3, K4, K16, L16 | Supply | The power supply(2.5V) for the general I/O on the X557. |
| VDD I/O Select | MDIO_1P2_SELECT_N | H4 | I | When pulled low, this signal sets the I/O voltages for MDC, MDIO, and RST_N to 1.2V levels, regardless of the VDD_IO voltage. This input is on the VDD_IO domain and has a pull-up associated with it. |
| VDD SerDes | VDD | R5, R15, T8, T10, T12 | Supply | SerDes 0.83V digital supply. |
| VDD22 SerDes | VCC2P1 | P4, P15, R3, R16 | Supply | SerDes 2.1V supply. |
| VREG SerDes | P0_VREG_SRDS P1_VREG_SRDS | T4, T6, T14, T16 | Supply | SerDes regulator output used for decoupling and monitoring. |
| VSS | VSS | J5, J7, J9, J11, J13, K6, K8, K10, K12, L7, L9, L11, L13, M6, M8, M10, M12, N5, N7, N9, N11, N13, P6, P8, P10, P12, R7, R9, R11, R13 | Supply | Digital ground. |
| VSS SerDes | VSS | N1, N2, P3, P17, P18, R1, R2, R4, R6, R14, T3, T5, T7, T9, T11, T13, T15, U1, U5, U9, U11, U16, U18, V5, V9, V11, V16 | Supply | SerDes ground. |



Table 2-21 X557-AT

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|----------------------|-------------------|---|--------|---|
| AVDD | VCC1P2 | D4, D6, E5, E7, E9 | Supply | 1.2V analog supply. |
| AVDD22 | VCC2P1 | A3, A5, A7, A9, C3, C5, C7, C9 | Supply | 2.1V analog supply. |
| AVSS | AVSS | B3, B5, B7, B9, B12, B14, B16, C2, C4, C6, C8, C11, C13, C15, C17, D3, D5, D7, D9, D12, D14, D16, D18, E4, E11, E13, E17, F6, F8, F10, F12, G5, G7, G9, G11, H6, H8, H10, H12 | Supply | Analog ground. |
| AVSSPLL | VSS | E6 | Supply | Analog ground for PHY PLL. |
| Analog VDD | VDD | E10 | Supply | 0.83V supply for digital circuitry in the AFE. |
| VCC Crystal | VCC2P1 | E18 | Supply | 2.1V supply for the crystal oscillator. |
| VDD | VDD | J6, J8, J10, J12, K5, K7, K9, K11, K13, L6, L8, L10, L12, M7, M9, M11, M13, N6, N8, N10, N12, P5, P7, P9, P11, P13, R8, R10, R12 | Supply | 0.83V digital supply. |
| VDD FLASH | VDD_FLASH | E3 | Supply | Flash I/O power supply (2.5V). |
| VDD I/O Power Supply | VDD_IO | J3, K4, K16, L16 | Supply | The power supply (2.5) for the general I/O on the X557. |
| VDD I/O Select* | MDIO_1P2_SELECT_N | H4 | I | When pulled low, this signal sets the I/O voltages for MDC, MDIO, and RST_N to 1.2V levels, regardless of the VDD_IO voltage. This input is on the VDD_IO domain and has a pull-up associated with it. |
| VDD SerDes | VDD | R5, T8, T10, T12 | Supply | SerDes 0.83V digital supply. |
| VDD22 SerDes | VCC2P1 | P4, R3 | Supply | SerDes 2.1V supply. |



| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|-------------|-------------|--|----------|---|
| VREG SerDes | VREG_SRDS | T4, T6 | Supply | SerDes regulator output used for decoupling and monitoring. |
| VSS | VSS | J5, J7, J9, J11, J13, K6, K8, K10, K12, L7, L9, L11, L13, M6, M8, M10, M12, N5, N7, N9, N11, N13, P6, P8, P10, P12, R7, R9, R11, R13 | Supply | Digital ground. |
| VSS SerDes | VSS | P18, P17, T15, U16, V16, U18, N1, N2, P3, R1, R2, R4, R6, R14, T3, T5, T7, T9, T11, T13, U1, U5, U9, U11, V5, V9, V11 | VSS_SRDS | SerDes ground. |

2.15 Reserved

Table 2-22 X557-AT2

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|---------------------|---|---|------|--|
| Floating | NC | A1, A18, B1, C10, D10, F7, F9, F11, F15, F17, G6, G8, G10, G12, G13, G16, H5, H7, H9, H11, H13, H15, L4 | | These pins are floating in the package and can be connected as convenience dictates. |
| Reserved No Connect | RNC_M3, RNC_K3, RNC_F13, RNC_G14, RNC_N4, RNC_M4, RNC_F4, RNC_G4, RNC_H14, RNC_J14, RNC_P14, RNC_M14, RNC_N14, RNC_F16, RNC_V1, RNC_M5, RNC_L5, RNC_N16, RNC_P16, RNC_V18 | M3, K3, F13, G14, N4, M4, F4, G4, H14, J14, P14, M14, N14, F16, V1, M5, L5, N16, P16, V18 | | Reserved no-connect signal. These pins must be left unconnected in the PCB design. |
| Reserved VDD_IO | RVDD_L3 RVDD_N3 | L3 N3 | I | Reserved VDD_IO signal. These pins must be connected to VDD_IO (2.5V). This input is on the VDD_IO domain and has a pull-up resistor associated with it. |



Table 2-23 X557-AT

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description | |
|---------------------|---|--|------|--|--|
| Floating | NC | A11, A12, A13, A14, A15, A16, A17, B10, B11, B13, B15, B17, B18, C12, C14, C16, C18, D11, D13, D15, D17, E12, E14, E16, F7, F9, F11, F14, G6, G8, G10, G12, G15, H5, H7, H9, H11, H13, J17, K2, K17, L2, L17, M2, M3, N3, P15, R15, R16, R17, R18, T16, T17, T18, U10, U12, U13, U14, U15, U17, V10, V12, V13, V14, V15, V17 | | | These pins are floating in the package and can be connected as convenience dictates. |
| Reserved Ground | RG_L4, RG_A1, RG_A18 | L4, A1, A18 | I | Reserved ground signal. These pins must be connected to digital ground in the PCB design. These inputs are on the VDD_IO domain and have pull-downs associated with them. | |
| Reserved No Connect | RNC_K3, RNC_E2, RNC_T14, RNC_B1, RNC_F13, RNC_G14, RNC_N4, RNC_M4, RNC_F4, RNC_G4, RNC_C10, RNC_D10, RNC_F15, RNC_G16, RNC_H15, RNC_H14, RNC_J14, RNC_P14, RNC_M14, RNC_N14, RNC_N16, RNC_P16, RNC_V18, RNC_F16, RNC_V1, RNC_M5, RNC_L5 | K3, E2, T14, B1, F13, G14, N4, M4, F4, G4, C10, D10, F15, G16, H15, H14, J14, P14, M14, N14, N16, P16, V18, F16, V1, M5, L5 | | Reserved no-connect signal. These pins must be left unconnected in the PCB design. | |
| Reserved VDD_IO | RVDD_L3 | L3 | I | Reserved VDD_IO signal. This pin must be connected to VDD_IO (2.5V). This input is on the VDD_IO domain and has a pull-up resistor associated with it. | |



2.16 Pinouts

The pinouts for the X557-AT and X557-AT2 are shown in the following two figures. The signals are color coded to group similar functionalities together. The view is looking from the top of the chip.

| | A_N | VA22 | B_N | VA22 | C_N | VA22 | D_N | VA22 | | | | | | | | | | |
|---|-------------|-------------|-----------|----------------------|--------|---------------|----------|----------|--------|---------|-----|-----|--------------|---------|---------|---------|---------------|--------------|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |
| > | RG_A1 | A_N | VCC2P1 | B_N | VCC2P1 | C_N | VCC2P1 | D_N | VCC2P1 | RG_A18 | NC | NC | NC | NC | NC | NC | NC | RG_A18 |
| ⊖ | RNC_B1 | A_P | VSS | B_P | VSS | C_P | VSS | D_P | VSS | NC | NC | VSS | NC | VSS | NC | VSS | NC | NC |
| ⊕ | RNC_C1 | VSS | VCC2P1 | VSS | VCC2P1 | VSS | VCC2P1 | VSS | VCC2P1 | RNC_C10 | VSS | NC | VSS | NC | VSS | NC | VSS | NC |
| ⊖ | RNC_D1 | RNC_D2 | VSS | VCC1P2 | VSS | VCC1P2 | VSS | DM_N | VSS | RNC_D10 | NC | VSS | NC | VSS | NC | VSS | NC | VSS |
| ⊕ | DC_MASTER_N | RNC_E2 | VDD_CLAMP | VSS | VCC1P2 | VSS | VCC1P2 | DM_P | VCC1P2 | VDD | VSS | NC | VSS | NC | VSS | NC | VSS | VCC2P1 |
| ⊖ | SIN | SOUT | TDIO_N_0 | RNC_F4 | TX_EN | VSS | NC | VSS | NC | VSS | NC | VSS | RNC_F13 | NC | RNC_F15 | RNC_F16 | XTAL_SELECT_N | XTAL_I |
| ⊕ | SCLK | CE_N | TDIO_P_0 | RNC_G4 | VSS | NC | VSS | NC | VSS | NC | VSS | NC | SIM_CLK_TERM | RNC_G14 | NC | RNC_G16 | ADDR4 | XTAL_O |
| ⊖ | RX_DC_DATA | TX_DC_RST_N | RST_OUT_N | MDIO_INT_EN_SELECT_N | NC | VSS | NC | VSS | NC | VSS | NC | VSS | NC | RNC_H14 | RNC_H15 | ADDR3 | DebugBus_CLK | DebugBus_DAT |
| ⊕ | RX_DC_CLK | RX_DC_SOF | VSS_G3 | RST_N | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | RNC_J14 | ADDR1 | ADDR2 | NC | MDC |
| ⊖ | LED0 | NC | RNC_K3 | VDD_G3 | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | TCK | ADDR0 | VSS_G3 | NC | P0_INT_N |
| ⊕ | LED1 | NC | RVDD | RG_L4 | RNC_L6 | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | TDI | TDO | VSS_G3 | NC | MDIO |
| ⊖ | LED2 | NC | NC | RNC_M4 | RNC_M5 | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | RNC_M14 | TRST_N | TMS | TX_DC_DATA | TX_DC_SOF |
| ⊕ | VSS | VSS | NC | RNC_N4 | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | RNC_N14 | RNC_N15 | RNC_N16 | RX_DC_RST_N | TX_DC_CLH |
| ⊖ | RX_LN0_N | RX_LN0_P | VSS | VCC2P1 | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | RNC_P14 | NC | RNC_P16 | VSS | VSS |
| ⊕ | VSS | VSS | VCC2P1 | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | NC | NC | NC | NC |
| ⊖ | TX_LN0_N | TX_LN0_P | VSS | P0_VREGL_SRDS | VSS | P0_VREGL_SRDS | VSS | VDD | VSS | VDD | VSS | VDD | VSS | RNC_T14 | VSS | NC | NC | NC |
| ⊕ | VSS | RX_LN1_P | TX_LN1_P | RX_LN2_P | VSS | TX_LN2_P | RX_LN3_P | TX_LN3_P | VSS | NC | VSS | NC | NC | NC | NC | VSS | NC | VSS |
| ⊖ | RNC_V1 | RX_LN1_N | TX_LN1_N | RX_LN2_N | VSS | TX_LN2_N | RX_LN3_N | TX_LN3_N | VSS | NC | VSS | NC | NC | NC | NC | VSS | NC | RNC_V18 |

Figure 2-7 X557-AT



| | | | | | | | | | | | | | | | | | | | |
|---|-------------|-------------|-------------|--------------------|--------|----------------|-------------|-------------|-------|-------------|--------|-------------|-------------|----------------|-------------|--------------|--------------|--------------|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | |
| > | NC | P0_A_N | VCCP1 | P0_B_N | VCCP1 | P0_C_N | VCCP1 | P0_D_N | VCCP1 | VDD | P1_A_N | VCCP1 | P1_B_N | VCCP1 | P1_C_N | VCCP1 | P1_D_N | NC | > |
| ⊖ | NC | P0_A_P | VSS | P0_B_P | VSS | P0_C_P | VSS | P0_D_P | VSS | VDD | P1_A_P | VSS | P1_B_P | VSS | P1_C_P | VSS | P1_D_P | P1_CM_N | ⊖ |
| ⊖ | RNC_C1 | VSS | VCCP1 | VSS | VCCP1 | VSS | VCCP1 | VSS | VCCP1 | NC | VSS | VCCP1 | VSS | VCCP1 | VSS | VCCP1 | VSS | P1_CM_P | ⊖ |
| ⊖ | RNC_D1 | RNC_D2 | VSS | VCCP2 | VSS | VCCP2 | VSS | P0_CM_N | VSS | NC | VCCP2 | VSS | VCCP2 | VSS | VCCP2 | VSS | VCCP1 | VSS | ⊖ |
| ⊖ | DC_MASTER_N | RNC_E2 | VDD_P0_N | VSS | VCCP2 | VSS | VCCP2 | P0_CM_P | VCCP2 | VDD | VSS | VCCP2 | VSS | VCCP2 | VSS | VDD | VSS | VCCP1 | ⊖ |
| ⊖ | SIN | SOUT | TDIO_N_0 | RNC_F4 | TX_EN | VSS | NC | VSS | NC | VSS | NC | VSS | RNC_F13 | TDIO_P_1 | NC | RNC_F16 | NC | CLK_P | ⊖ |
| ⊖ | SCLK | CE_N | TDIO_P_0 | RNC_G4 | VSS | NC | VSS | NC | VSS | NC | VSS | NC | RNC_G14 | TDIO_M_1 | NC | ADDR1 | CLK_N | ⊖ | ⊖ |
| ⊖ | RX_DC_DATA | TX_DC_RST_N | RST_OUT_N | RNC_H1, R2, R3, R4 | NC | VSS | NC | VSS | NC | VSS | NC | VSS | NC | RNC_H14 | NC | ADDR1 | DebugBus_CLK | DebugBus_DAT | ⊖ |
| ⊖ | RX_DC_CLK | RX_DC_SOF | VDD_L3 | RST_N | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | RNC_J14 | ADDR1 | ADDR2 | P1_MD0 | P1_MD0 | ⊖ |
| ⊖ | P0_LED0 | P1_LED0 | RNC_K3 | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | TX | HW_ADDR2 | VSS | P1_INT_N | P1_INT_N | ⊖ |
| ⊖ | P0_LED1 | P1_LED1 | RVDD_L3 | NC | RNC_L5 | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | TDI | TDO | VSS | P1_MD0 | P1_MD0 | ⊖ |
| ⊖ | P0_LED2 | P1_LED2 | RNC_M3 | RNC_M4 | RNC_M5 | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | RNC_M14 | TRST_N | TMS | TX_DC_DATA | TX_DC_SOF | ⊖ |
| ⊖ | VSS | VSS | RVDD_N0 | RNC_M4 | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | RNC_N14 | RNC_N15 | RNC_N16 | RX_DC_RST_N | TX_DC_CLK | ⊖ |
| ⊖ | P0_RX_LN0_N | P0_RX_LN0_P | VSS | VCCP1 | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | RNC_P14 | VCCP1 | RNC_P16 | VSS | VSS | ⊖ |
| ⊖ | VSS | VSS | VCCP1 | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VSS | VDD | VCCP1 | P1_TX_LN0_P | P1_TX_LN0_N | ⊖ | ⊖ |
| ⊖ | P0_TX_LN0_N | P0_TX_LN0_P | VSS | P0_VREG_SRDS | VSS | P0_VREG_L_SRDS | VSS | VDD | VSS | VDD | VSS | VDD | VSS | P1_VREG_L_SRDS | VSS | P1_VREG_SRDS | P1_RX_LN0_P | P1_RX_LN0_N | ⊖ |
| ⊖ | VSS | P0_RX_LN1_P | P0_TX_LN1_P | P0_RX_LN2_P | VSS | P0_TX_LN2_P | P0_RX_LN3_P | P0_TX_LN3_P | VSS | P1_RX_LN0_P | VSS | P1_TX_LN0_P | P1_RX_LN1_P | P1_TX_LN1_P | P1_RX_LN2_P | VSS | P1_TX_LN2_P | VSS | ⊖ |
| ⊖ | RNC_V1 | P0_RX_LN1_N | P0_TX_LN1_N | P0_RX_LN2_N | VSS | P0_TX_LN2_N | P0_RX_LN3_N | P0_TX_LN3_N | VSS | P1_RX_LN0_N | VSS | P1_TX_LN0_N | P1_RX_LN1_N | P1_TX_LN1_N | P1_RX_LN2_N | VSS | P1_TX_LN2_N | RNC_V18 | ⊖ |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | |

Figure 2-8 X557-AT2



NOTE: *This page intentionally left blank.*



3.0 Hardware Interfaces (X557-AT4)

Note: Any signal name that ends with an asterisk (*) or pin name that ends with _N are active low.

3.1 Management Interface

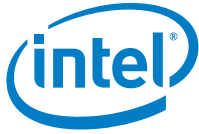
The management interface on the X557 is a two wire interface with a unidirectional MDC clock and a bidirectional MDIO data. The MDIO interface on the X557 is a robust implementation of this standard. It is designed to operate up to 18 MHz¹ and is capable of withstanding voltages up to double the operating voltage (the theoretical worst-case maximum reflection on an unterminated bus). It uses a Schmitt-trigger in conjunction with a de-bounce state machine to de-bounce the signals, and is capable of hot-insertion. The MDIO data line is capable of pulling low a 280 Ω load tied to 1.2V, and can be configured to support either open-drain, or push-pull operation in the Global General Provisioning 2: Address 1E.C441 register. Push-pull is the default operating mode.

In order to provide flexibility to the implementation, the X557 uses a programmable I/O voltage. The logic thresholds for the I/O are set at 70% and 30% for V_{IH}/V_{OH} and V_{IL}/V_{OL} , respectively for any VDD_{IO} greater than 1.8V. For 1.2V MDIO operation (affects TX_EN, MDC, MDIO, RST_N) a separate signal called MDIO_1P2_SELECT_N is provided that will force 1.2V operation on these signals, regardless of the VDD_{IO} voltage.

The management interface enables communication between the Station Management (STA) and a PHY. The STA is the external host controller which is the master of the management interface bus. Consequently, it always sources the MDC clock. When the MDIO is sourced by the STA, the PHY samples the MDIO at the rising edge of MDC. When the MDIO is sourced by the PHY during read operations, the STA samples the MDIO at the rising edge.

| Signal Name | Pin Name(s) | Pin Number(s) | Type | |
|------------------|--|--------------------------|------|---|
| Reserved | TX_DC_RST_N | M2 | O | Reserved. |
| Interrupt* [3:0] | P0_INT_N P1_INT_N P2_INT_N P3_INT_N | L22 L21 L23 L24 | OD | The 2.5V tolerant open-drain interrupt signal from PHY 0 of the X557. On reset this is set high. This input can be driven to operate at 1.2V via the MDIO_1P2_SELECT_N pin, regardless of the voltage on VDD_{IO} . These open-drain 20 mA outputs are on the VDD_{IO} domain. |

1. This is a function of whether the output is set to push-pull or open-drain mode, and on the capacitance of the bus.



| Signal Name | Pin Name(s) | Pin Number(s) | Type | |
|---------------------|--|--------------------------|------|---|
| Invert MDIO Address | INV_ADDR0 INV_ADDR1 | T2 R4 | I | When set, these logic inputs invert the corresponding LSBs of the MDIO PHY address of the X557 (XOR function). This is used to change the counting order of the PHYs within the X557. These inputs are on the VDD_IO domain and have pull-ups associated with them. |
| MDIO Address | ADDR1 ADDR2 ADDR3 | J24 J23 J22 | I | The logic inputs to set the MDIO PHY address of the X557. These inputs are on the VDD_IO domain and have pull-up resistors associated with them. |
| MDIO Clock [3:0] | P0_MDC P1_MDC P2_MDC P3_MDC | K22 K21 K23 K24 | I/O | The MDIO clock input for PHY 0 of the X557. This input can be driven to operate at 1.2V via the MDIO_1P2_SELECT_N pin, regardless of the voltage on VDD_IO. These tri-state 20 mA I/Os are on the VDD_IO domain. |
| MDIO Data [3:0] | P0_MDIO P1_MDIO P2_MDIO P3_MDIO | M22 M21 M23 M24 | I/O | The MDIO data line (with Schmitt triggered logic levels) for PHY 0 of the X557. On reset, this is set to high-impedance. This I/O can be driven to operate at 1.2V via the MDIO_1P2_SELECT_N pin, regardless of the voltage on VDD_IO. These tri-state 20 mA I/Os are on the VDD_IO domain. |
| Reset Out* | RST_OUT_N | L2 | OD | The open-drain reset output from the X557. This might be used to drive the power-up reset signal for a board, as it outputs the on-chip power-up reset signal from the X557. This open-drain 20 mA output is on the VDD_IO domain. |
| Reset* | RST_N | T1 | I | The hard reset input (with Schmitt triggered logic levels) for the X557. This input can be driven to operate at 1.2V via the MDIO_1P2_SELECT_N pin, regardless of the voltage on VDD_IO. This input is on the VDD_IO domain and has a pull-up resistor associated with it. |



Table 3-1 shows the management interface frame format (802.3-2005 45.3). The fields are described in the sections that follow.

Table 3-1 MDIO Frame Format

| Frame | PRE | ST | OP | PHYAD | MMDAD | TA | Data | Idle |
|-----------------------------|-------|----|----|-------|--------|----|------------------|------|
| Address | 1...1 | 00 | 00 | PPPPP | EEEEEE | 10 | AAAAAAAAAAAAAAAA | Z |
| Write | 1...1 | 00 | 01 | PPPPP | EEEEEE | 10 | DDDDDDDDDDDDDDDD | Z |
| Read | 1...1 | 00 | 11 | PPPPP | EEEEEE | Z0 | DDDDDDDDDDDDDDDD | Z |
| Post-read increment address | 1...1 | 00 | 10 | PPPPP | EEEEEE | Z0 | DDDDDDDDDDDDDDDD | Z |

Idle (idle condition):

The idle condition on the management interface is a high-impedance state. All tri-state drivers are disabled and the pull-up resistor(s) on the MDIO bus will pull the MDIO line to a one.

PRE (preamble):

Normal operation — At the beginning of each transaction, the station management entity will send a sequence of 32 contiguous ones on the MDIO data line, along with 32 corresponding cycles on the MDC to provide the MMD with a pattern that it can use to establish synchronization. Each MMD will observe a sequence of 32 contiguous one bits on MDIO with 32 corresponding cycles on MDC before it responds to any transaction.

Preamble suppression — The MDIO interface can optionally disable preamble detection by setting the *MDIO Preamble Detection Disable* bit in the Global General Provisioning 2: Address 1E.C441 register. In this mode of operation, one or more preamble bit are required followed by the 0x0 start of frame ST bits.

ST (start of frame):

The start of frame for indirect access cycles is indicated by the <00> pattern. This pattern assures a transition from the default one and identifies the frame as an indirect access. Frames that contain the ST=<01> pattern defined in Clause 22 will be ignored by the MMDs within the X557.

OP (operation code):

The operation code field indicates the type of transaction being performed by the frame. A <00> pattern indicates that the frame payload contains the address of the register to access. A <01> pattern indicates that the frame payload contains data to be written to the register whose address was provided in the previous address frame. A <11> pattern indicates that the frame is read operation. A <10> pattern indicates that the frame is a post-read increment address operation.

PHYAD (PHY address):

The PHY address is five bits, allowing for 32 unique PHY addresses, and hence up to 32 PHYs on an MDIO bus. The address of the PHY is determined from ADDR[4:2] for the pins. The first PHY address bit to be transmitted and received is the MSB of the address. The station management entity must have a priori knowledge of the appropriate PHY address for each PHY to which it is attached, whether connected to a single PHY or to multiple PHYs.



MMDAD (MMD address):

The MMD address is five bits, allowing for 32 unique MMDs per PHY. The first MMD address bit transmitted and received is the MSB of the address.

In addition the X557 supports a broadcast mode when the PHYAD is 0x00. Only the write and load address opcodes are supported in broadcast mode. Read and post-read increment opcodes are ignored in broadcast mode. This mode of operation can be enabled via the *MDIO Broadcast Mode Enable* bits in the Global General Provisioning 2: Address 1E.C441 register.

TA (turnaround):

The turnaround time is a 2-bit time spacing between the MMD address field and the data field of a management frame to avoid contention during a read transaction. For a read or post-read increment address transaction, both the STA and the MMD remain in a high-impedance state for the first bit time of the turnaround. The MMD then drives a zero bit during the second bit time of the turnaround of a read or post-read increment address transaction. During a write or address transaction, the STA transmits a one for the first bit time of the turnaround and a zero for the second bit time of the turnaround. This behavior is shown in

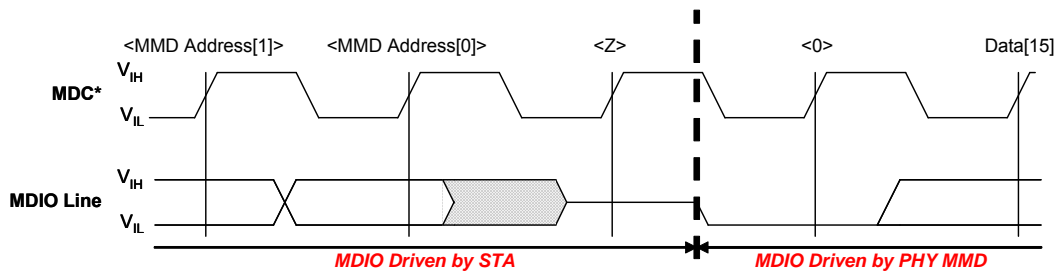


Figure 3-1 MDIO Bus Turn-around During Read Operations

Address / Data:

The address/data field is 16 bits. For an address cycle, it contains the address of the register to be accessed on the next cycle. For the data cycle of a write frame, the field contains the data to be written to the register. For a read or post-read increment address frame, the field contains the contents of the register. The first bit transmitted and received shall be bit 15.

For counters that are greater than 16-bits, the LSW must be read first, then the MSW must be read immediately afterwards. When the LSW is read, the counter is cleared and the MSW is stored in a shadow register. Reading the MSW actually reads the shadow register.

Optionally the host may read the MSW first, then the LSW immediately afterwards by setting the *MDIO Read MSW First Enable* bit in the Global General Provisioning 2: Address 1E.C441 register.



3.1.1 Interrupt

The X557 supports an open-drain interrupt pin per PHY.

3.1.2 Reset

The X557 is capable of generating a RST_OUT_N signal from its internal power-on reset generation circuitry that can be used by the external board circuitry.

Operation of the reset machinery is as follows:

1. Release from the Reset state begins when the RST_N input is high¹, and all of the core power supplies are above their required thresholds. These thresholds are listed in

Table 3-2 Power-on Reset Thresholds for Core Supply Voltages

| Supply | Parameter | Min | Max | Units |
|--------|--|------|------|-------|
| VCC2P1 | Power-on reset threshold for VCC2P1 DC supply. | 1.70 | 1.80 | V |
| VCC1P2 | Power-on reset threshold for VCC1P2 DC supply. | 0.93 | 0.99 | V |
| VDD | Power-on reset threshold for VDD DC supply. | 0.56 | 0.60 | V |

2. Once all of the conditions for release from reset are true, a 20 ms timer engages, the purpose of which is to enable the supplies to settle prior to allowing the PHY to boot.
3. After the 20 ms timer has completed, hardware state machines designed to guarantee PLL and band-gap stability engage.
4. After the PLLs and band-gap are locked and functioning properly, the processor and digital circuitry are released from reset.
5. The PHY image is then loaded and the processor boots.
6. After the processor boots, any provisioned register values are set, and the PHY enters the provisioned operating state.
7. Once this completes, the processor raises the MMD reset bits and sets the reset completed alarm, indicating it has completed reset and is ready for operation.

3.1.3 Configuration

The X557 contains a number of static configuration pins which are used to set the power-up operation of the X557. These signals are:

1. ADDR[4:2].
2. Transmit Enable

1. Note that there are no timing requirements on issuance of reset relative to the clock.



In the X557 package, the MDIO addressing is tied off internally so that the LSB increments according to the PHY number in the package. This MDIO address can either be overridden via a register in the Global MMD via provisioning, or the incrementation order can be altered via the INV_ADDR0 pin which is exclusive OR'd with address pin ADDR0.

3.2 Serial Flash

| Signal Name | Pin Name(s) | Pin Number(s) | Type | |
|------------------------|-------------|---------------|------|--|
| Reserved | RX_DC_CLK | N1 | I | Reserved |
| Reserved | TX_DC_CLK | P24 | O | Reserved |
| Reserved | RX_DC_DATA | M1 | I | Reserved |
| Reserved | TX_DC_DATA | N23 | O | Reserved |
| Reserved | DC_MASTER_N | H1 | I | Reserved |
| Reserved | RX_DC_RST_N | P23 | I | Reserved |
| Reserved | RX_DC_SOF | N2 | I | Reserved |
| Reserved | TX_DC_SOF | N24 | O | Reserved |
| SPI Chip Enable* | CE_N | K2 | O | The SPI CE* signal from the X557 to the serial Flash. On reset this is set high. This 20 mA output is on the VDD_FLASH domain. |
| SPI Serial Clock | SCLK | K1 | O | The SPI clock from the X557 to the serial Flash. On reset this is set low. This 20 mA output is on the VDD_FLASH domain. |
| SPI Serial Input Data | SIN | J1 | I | The SPI input data from the serial FLASH to the X557. This input is on the VDD_FLASH domain and has a pull-up resistor associated with it. |
| SPI Serial Output Data | SOUT | J2 | I | The SPI output data from the X557 to the serial Flash. On reset this is set low. This 20 mA output is on the VDD_FLASH domain. |



3.2.1 SPI Flash Interface

The SPI interface is responsible for connecting the X557 to the external Flash memory device. The micro-controller on the X557 accesses the boot code and the X557 default register values from the Flash memory after power-on reset. This Flash memory is also accessible via the MDIO interface for firmware updates and manufacturing burn via the registers in the Global MMD.

The SPI interface is a four wire, unidirectional, serial bus as shown in Figure 3-2. It is composed of a serial clock output SCLK, a serial data output SOUT, a serial data input SIN, and a chip-select CE*. All the signals are unidirectional.

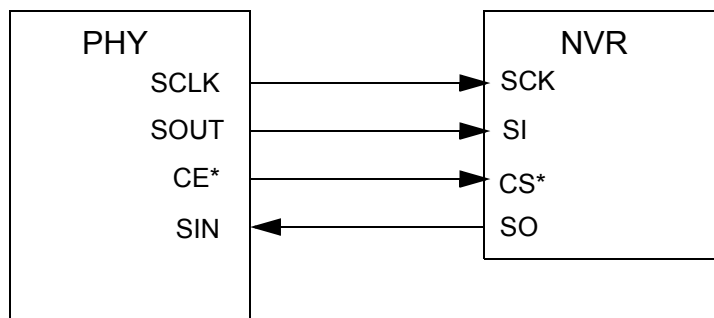


Figure 3-2 SPI Interface Block Diagram

The X557 is set up to function as a Mode 0 (0,0) SPI device, which means that the clock defaults to zero when not bursting. Data on this interface, for both SIN and SOUT, is always sourced on the falling edge of SCLK, and sampled on the rising edge of SCLK.

The following figures show typical read, burst read, and write operations for the X557. In all of these scenarios, the NVR interface in the Global MMD is used to access the Flash.

The NVR interface in the X557 is designed to be able to output any arbitrary opcode, followed by a programmable zero to three address bytes, followed by a programmable zero to four data bytes. This allows any variation of opcodes to be output to the attached Flash device. This interface also supports a burst read and write mode, which keeps the CS* line pulled low to enable back-to-back reads and writes. To support this, the NVR interface supports two 16-bit address registers and two 16-bit data registers, which allows up to 4 data bytes in a burst over the SPI interface. In order to extend this to longer bursts, the X557 halts the clock after the last bit in the data burst allowing the host processor to load another block of data to / from the NVR interface. This is shown in Figure 3-3 through Figure 3-5 and enables the data burst to be extended by as many bytes as necessary, without outstripping the MDIO’s I/O capabilities.

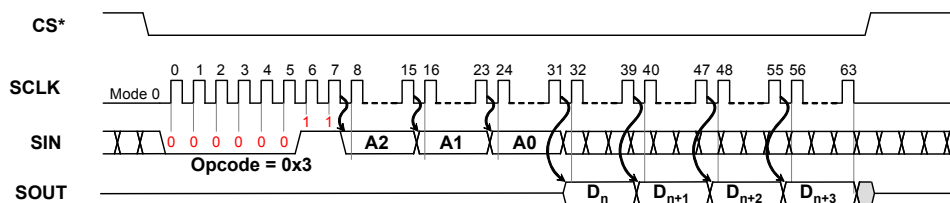


Figure 3-3 SPI Read

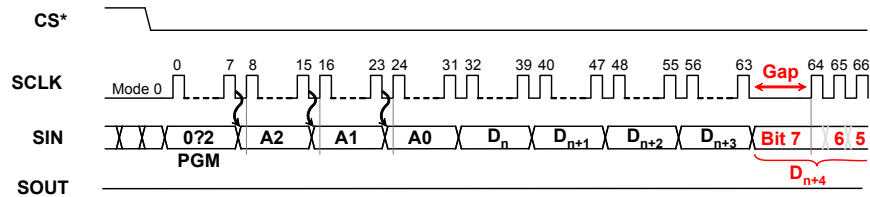


Figure 3-4 SPI Burst Read

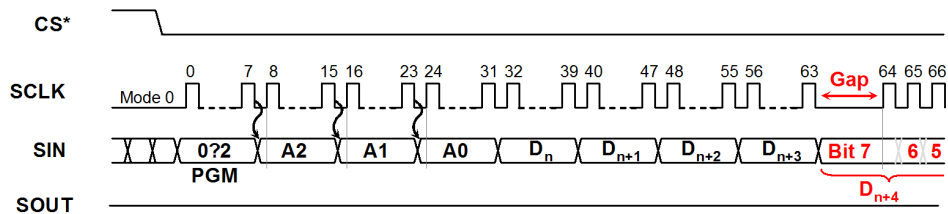


Figure 3-5 SPI Burst Write

Note that typical NVRs require that writing be performed on a block basis, and thus the addresses usually wrap within the block being programmed. As such, it is desirable from a speed and efficiency perspective to attempt to write entire blocks, versus pieces of blocks.

In order to assure that no polling is required on NVR interface, it is recommended that the NVR clock speed be set to at least¹:

$$f_{SCLK} > \frac{64}{63} \cdot f_{MDIO}$$

The desired Flash memory should be chosen to be at least 512K bytes in size, and must be capable of interfacing to a 2.5V CMOS SPI.

3.3 Firmware

The X557 contains a 32-bit micro-controller. This micro-controller is designed to have its IRAM and DRAM loaded on power-up / reset from the attached FLASH, or to have its boot image loaded by the host processor via the MDIO interface.

1. This is derived from the fact that the longest burst instruction on the SPI is 64 bits, at one bit per clock, whereas to write a register on the MDIO takes 64 clocks, and the data is not written until the last bit - hence the 63.



3.4 SerDes

Table 3-3 X557-AT4

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|-----------------|----------------------------|---------------|------|---|
| PHY 0 Lane 0 Rx | P0_RX_LN0_P P0_RX_LN0_N | V2 V1 | I | PHY 0 physical Lane 0 differential Rx of the X557 SerDes interface. This lane can operate in KR,XFI and SGMII mode |
| PHY 0 Lane 0 Tx | P0_TX_LN0_P P0_TX_LN0_N | Y2 Y1 | O | PHY 0 physical Lane 0 differential Tx of the X557 SerDes interface. This lane can operate in KR,XFI and SGMII mode. |
| PHY 0 Lane 2 Rx | P0_RX_LN2_P P0_RX_LN2_N | AB2 AB1 | I | PHY 0 physical Lane 2 differential Rx of the X557 SerDes interface. This lane can operate in KR,XFI and SGMII mode |
| PHY 0 Lane 2 Tx | P0_TX_LN2_P P0_TX_LN2_N | AC3 AD3 | O | PHY 0 physical Lane 2 differential Tx of the X557 SerDes interface. This lane can operate in KR,XFI and SGMII mode. |
| PHY 1 Lane 0 Rx | P1_RX_LN0_P P1_RX_LN0_N | AC5 AD5 | I | PHY 1 physical Lane 0 differential Rx of the X557 SerDes interface. This lane can operate in KR,XFI and SGMII mode |
| PHY 1 Lane 0 Tx | P1_TX_LN0_P P1_TX_LN0_N | AC7 AD7 | O | PHY 1 physical Lane 0 differential Tx of the X557 SerDes interface. This lane can operate in KR,XFI and SGMII mode. |
| PHY 1 Lane 2 Rx | P1_RX_LN2_P P1_RX_LN2_N | AC9 AD9 | I | PHY 1 physical Lane 2 differential Rx of the X557 SerDes interface. This lane can operate in KR,XFI and SGMII mode |
| PHY 1 Lane 2 Tx | P1_TX_LN2_P P1_TX_LN2_N | AC11 AD11 | O | PHY 1 physical Lane 2 differential Tx of the X557 SerDes interface. This lane can operate in KR,XFI and SGMII mode. |
| PHY 2 Lane 0 Rx | P2_RX_LN0_P P2_RX_LN0_N | AC14 AD14 | I | PHY 2 physical Lane 0 differential Rx of the X557 SerDes interface. This lane can operate in KR,XFI and SGMII mode |
| PHY 2 Lane 0 Tx | P2_TX_LN0_P P2_TX_LN0_N | AC16 AD16 | O | PHY 2 physical Lane 0 differential Tx of the X557 SerDes interface. This lane can operate in KR,XFI and SGMII mode. |
| PHY 2 Lane 2 Rx | P2_RX_LN2_P P2_RX_LN2_N | AC18 AD18 | I | PHY 2 physical Lane 2 differential Rx of the X557 SerDes interface. This lane can operate in KR,XFI and SGMII mode |
| PHY 2 Lane 2 Tx | P2_TX_LN2_P P2_TX_LN2_N | AC20 AD20 | O | PHY 2 physical Lane 2 differential Tx of the X557 SerDes interface. This lane can operate in KR,XFI and SGMII mode. |
| PHY 3 Lane 0 Rx | P3_RX_LN0_P P3_RX_LN0_N | AC22 AD22 | I | PHY 3 physical Lane 0 differential Rx of the X557 SerDes interface. This lane can operate in KR,XFI and SGMII mode |
| PHY 3 Lane 0 Tx | P3_TX_LN0_P P3_TX_LN0_N | AB23 AB24 | O | PHY 3 physical Lane 0 differential Tx of the X557 SerDes interface. This lane can operate in KR,XFI and SGMII mode. |



| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|-----------------|----------------------------|---------------|------|---|
| PHY 3 Lane 2 Rx | P3_RX_LN2_P P3_RX_LN2_N | Y23 Y24 | I | PHY 3 physical Lane 2 differential Rx of the X557 SerDes interface. This lane can operate in KR,XFI and SGMII mode |
| PHY 3 Lane 2 Tx | P3_TX_LN2_P P3_TX_LN2_N | V23 V24 | O | PHY 3 physical Lane 2 differential Tx of the X557 SerDes interface. This lane can operate in KR,XFI and SGMII mode. |

The SerDes interface on the X557 also contains diagnostic pattern generation and checking functionality that is listed [Table 3-4](#):

Table 3-4 KR Diagnostic Pattern Capabilities

| Test | Description | Generate | Check | Invert |
|---------------|-----------------------|----------|-------|--------|
| x^9 PRBS | $x^9 + x^5 + 1$ | 3 | 3 | 3 |
| x^{31} PRBS | $x^{31} + x^{28} + 1$ | 3 | 3 | 3 |
| Square Wave | Clause 49.2.12 | 3 | 3 | 3 |
| Pseudo-Noise | | 3 | 3 | 3 |
| CRPAT | IEEE 802.3 Annex48A.4 | 3 | 3 | 3 |

Table 3-5 SGMII Diagnostic Pattern Capabilities

| Test | Description | Generate | Check | Invert |
|-------|-----------------------|----------|-------|--------|
| CRPAT | IEEE 802.3 Annex48A.4 | 3 | 3 | 3 |

All of the parameters associated with the SerDes interface have provisionable default values, which means that the X557 SerDes interface can be tailored to power-up with the optimal settings for any given application.

3.5 SerDes Operating Modes

For the purposes of this discussion, the X557 can be viewed as a set of blocks as shown in [Figure 2-6](#):

On the left side of the diagram is the system interface, which consists of the two SerDes lanes. Lanes 0 and 2 have the ability to run at rates from 1.25 Gb/s to 10.3125 Gb/s. These lanes support SGMII and KR. In the X557, only two of the four SerDes lanes on the chip are actually run out, but these lanes are still referred to as Lane 0 and Lane 2. At the PCS layer, there are two SGMII cores and two KR cores even though only the two SGMII and KR cores are used.



These different SerDes operating modes are summarized in Table 3-6.

Table 3-6 SerDes Lane Assignments for Different Operating Modes

| Interface | Operating Mode / Core Used | Lane 0 | Lane 1 | Lane 2 | Lane 3 |
|-----------|----------------------------|--------|--------|--------|--------|
| System | SGMII1 | | | X | |
| | KR1 | | | X | |

3.6 SerDes System I/F Startup

In startup on the system interface side, there are three different operating scenarios for the SerDes I/F:

- 10 GbE mode (KR or XFI)
- 1000BASE-X mode
- SGMII
- All-off mode

These different modes affect only the system interface and function independently of whether the MDI interface is selected or not.

3.6.1 10 GbE Mode

1. In this mode, which is the hardware default, the X557 comes up in the pre-configured 10 GbE mode (KR) and transmits Local Faults / Idles, and remains in this state until a connection to a link partner is established.
2. After connection to a link partner has been established, the X557 will either stay in the pre-configured 10 GbE mode, or switch to 1000BASE-X mode on logical Lane 0, or 100 Mb/s SGMII mode depending on that the auto-negotiated line rate was.
3. Once the SerDes I/F has synchronized, traffic flows.
 - a. If the link fails and the system interface was in 10 GbE mode, the X557 generates a Local Fault message towards the system I/F, effectively restarting. If the link had transitioned to 1 GbE operation, the SerDes is restarted in 10 GbE mode generating Local Faults / Idles.
4. Auto-negotiation restarts after the link break timer expires.

3.6.2 1000BASE-X Mode

1. In this mode the X557 comes up in 1000BASE-X mode on logical Lane 0 and transmits idles, and remains in this state until a connection to a link partner is established.



2. After a connection to a link partner has been established, the X557 will either stay in 1000BASE-X mode, or switch to the pre-configured 10 GbE mode, or 100 Mb/s SGMII mode depending on that the auto-negotiated line rate was.
3. Once the SerDes I/F has synchronized, traffic flows.
4. If the link fails and the system interface was in the pre-configured 10 GbE mode (KR), the X557 generates a Local Fault message towards the system I/F, and effectively restarts in 1000BASE-X mode, generating Idles. Otherwise the link just stays in 1000BASE-X mode generating Idles.
5. Auto-negotiation restarts after the link break timer expires.

3.6.3 SGMII Mode

1. In this mode, the X557 comes up in SGMII mode. After sending and receiving an ACK on an SGMII link-down, auto-negotiation message (see [Table 2-11](#)), the SerDes transmits idles and remains in this state until a link partner connection is established.
2. After a connection to a link partner has been established, the X557 sends an SGMII link-up, auto-negotiation message with the appropriate rate (see [Table 2-11](#)) and receives an ACK.
3. Upon receiving the acknowledge from the system interface, the X557 either switches to 100 Mb/s SGMII mode, stays in 1 GbE SGMII mode (essentially 1000BASE-X) or switches to the pre-configured 10 GbE mode (KR or XFI), depending on whether the auto-negotiated line rate was 1 GbE / 100 Mb/s or 10 GbE.
4. Once the SerDes interface has synchronized, traffic flows.
5. If the link fails and the X557 was in the pre-configured 10 GbE mode, the X557 generates a local fault message towards the system interface and then transitions back to SGMII mode, where it sends and receives an ACK on an SGMII link-down, auto-negotiation message and then resumes transmitting idles. If the link fails and the X557 was in 1 GbE SGMII mode, the X557 first sends and receives an ACK on an SGMII link-down, auto-negotiation message and then resumes transmitting idles with no interruption in SerDes operation. If the system interface was in 100 Mb/s SGMII mode, the SerDes transitions back to SGMII mode, where it sends and receives an ACK on an SGMII link-down, auto-negotiation message and then resumes transmitting idles.
6. Auto-negotiation restarts after the link break timer expires.

3.6.4 All-Off Mode

1. In this mode the Intel® X557-AT/AT2/AT4 10 GbE PHY comes up with the system interface off, and remains in this state until connection to a link partner is established.
2. After connection to a link partner has been established, the Intel® X557-AT/AT2/AT4 10 GbE PHY will either turn on 1000BASE-X on logical Lane 0, or turn on the pre-configured 10 GbE mode (KR), or 100 Mb/s SGMII mode depending on that the auto-negotiated line rate was.
3. Once the SerDes I/F has synchronized, traffic flows.
4. If the link fails and was in the pre-configured 10 GbE mode, the Intel® X557-AT/AT2/AT4 10 GbE PHY generates a Local Fault message towards the system I/F and shuts off. Otherwise the system interface just shuts off.
5. Auto-negotiation restarts after the link break timer expires.



3.6.5 Interrupts

In all of these modes, the processor has the ability to generate an interrupt upon completing auto-negotiation.

3.7 MDI

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|--------------|--------------------|---------------|------|--|
| PHY 0 CMS | P0_CM_P P0_CM_N | B7 A7 | I/O | PHY 0 Common Mode Sense Input. |
| PHY 0 Pair A | P0_A_P P0_A_N | B3 A3 | I/O | PHY 0 Pair A of the X557 line interface. These should connect to the Pair A inputs of the transformer, with capacitive bypassing via the center-tap. On reset this is set to high-impedance. |
| PHY 0 Pair B | P0_B_P P0_B_N | E3 D3 | I/O | PHY 0 Pair B of the X557 line interface. These should connect to the Pair B inputs of the transformer, with capacitive bypassing via the center-tap. On reset this is set to high-impedance. |
| PHY 0 Pair C | P0_C_P P0_C_N | B5 A5 | I/O | PHY 0 Pair C of the X557 line interface. These should connect to the Pair C inputs of the transformer, with capacitive bypassing via the center-tap. On reset this is set to high-impedance. |
| PHY 0 Pair D | P0_D_P P0_D_N | E5 D5 | I/O | PHY 0 Pair D of the X557 line interface. These should connect to the Pair D inputs of the transformer, with capacitive bypassing via the center-tap. On reset this is set to high-impedance. |
| PHY 1 CMS | P1_CM_P P1_CM_N | E7 D7 | I/O | PHY 1 Common Mode Sense Input. |
| PHY 1 Pair A | P1_A_P P1_A_N | E9 D9 | I/O | PHY 1 Pair A of the X557 line interface. These should connect to the Pair A inputs of the transformer, with capacitive bypassing via the center-tap. On reset this is set to high-impedance. |
| PHY 1 Pair B | P1_B_P P1_B_N | B9 A9 | I/O | PHY 1 Pair B of the X557 line interface. These should connect to the Pair B inputs of the transformer, with capacitive bypassing via the center-tap. On reset this is set to high-impedance. |
| PHY 1 Pair C | P1_C_P P1_C_N | E11 D11 | I/O | PHY 1 Pair C of the X557 line interface. These should connect to the Pair C inputs of the transformer, with capacitive bypassing via the center-tap. On reset this is set to high-impedance. |
| PHY 1 Pair D | P1_D_P P1_D_N | B11 A11 | I/O | PHY 1 Pair D of the X557 line interface. These should connect to the Pair D inputs of the transformer, with capacitive bypassing via the center-tap. On reset this is set to high-impedance. |
| PHY 2 CMS | P2_CM_P P2_CM_N | E18 D18 | I/O | PHY 2 Common Mode Sense Input. |



| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|--------------|--------------------|---------------|------|--|
| PHY 2 Pair A | P2_A_P P2_A_N | B14 A14 | I/O | PHY 2 Pair A of the X557 line interface. These should connect to the Pair A inputs of the transformer, with capacitive bypassing via the center-tap. On reset this is set to high-impedance. |
| PHY 2 Pair B | P2_B_P P2_B_N | E14 D14 | I/O | PHY 2 Pair B of the X557 line interface. These should connect to the Pair B inputs of the transformer, with capacitive bypassing via the center-tap. On reset this is set to high-impedance. |
| PHY 2 Pair C | P2_C_P P2_C_N | B16 A16 | I/O | PHY 2 Pair C of the X557 line interface. These should connect to the Pair C inputs of the transformer, with capacitive bypassing via the center-tap. On reset this is set to high-impedance. |
| PHY 2 Pair D | P2_D_P P2_D_N | E16 D16 | I/O | PHY 2 Pair D of the X557 line interface. These should connect to the Pair D inputs of the transformer, with capacitive bypassing via the center-tap. On reset this is set to high-impedance. |
| PHY 3 CMS | P3_CM_P P3_CM_N | B18 A18 | I/O | PHY 3 Common Mode Sense Input. |
| PHY 3 Pair A | P3_A_P P3_A_N | E20 D20 | I/O | PHY 3 Pair A of the X557 line interface. These should connect to the Pair A inputs of the transformer, with capacitive bypassing via the center-tap. On reset this is set to high-impedance. |
| PHY 3 Pair B | P3_B_P P3_B_N | B20 A20 | I/O | PHY 3 Pair B of the X557 line interface. These should connect to the Pair B inputs of the transformer, with capacitive bypassing via the center-tap. On reset this is set to high-impedance. |
| PHY 3 Pair C | P3_C_P P3_C_N | E22 D22 | I/O | PHY 3 Pair C of the X557 line interface. These should connect to the Pair C inputs of the transformer, with capacitive bypassing via the center-tap. On reset this is set to high-impedance. |
| PHY 3 Pair D | P3_D_P P3_D_N | B22 A22 | I/O | PHY 3 Pair D of the X557 line interface. These should connect to the Pair D inputs of the transformer, with capacitive bypassing via the center-tap. On reset this is set to high-impedance. |

In 10 GbE mode, the line interface on the Intel® X557-AT/AT2/AT4 10 GbE PHY is capable of driving up to 100 m of CAT-6a unshielded twisted pair or 100 m of CAT-7 shielded cable (100 Ω differential impedance). It can also drive 55 m of CAT-6 cable, and a lesser distance of CAT-5e cable¹. In 1 GbE and 100 Mb/s modes, it can drive 130m of CAT-5e (or better) cable. It is designed to drive this via a quad, 50 Ω, center-tapped 1:1 transformer connected to an RJ-45 PCB-mount jack.

The line interface on the Intel® X557-AT/AT2/AT4 10 GbE PHY supports automatic A/B and C/D pair swaps, inversions (auto-X), and semi-cross (A/B or C/D only). It also supports a provisioned ABCD to DCBA pair reversal for ease of routing with stack-jacks via bit 1.E400.0 and the MDI_CFG pin, which sets the configuration on power-up. Note that this reversal does not swap polarities, thus A+ maps to D+, etc.

1. This distance is indeterminate because CAT-5e cable performance is not specified past 100 MHz.



3.8 Timing

The Intel® X557-AT/AT2/AT4 10 GbE PHY contains a high-performance synthesizer, which is capable of producing all of the clocks required internally, as well as sourcing the recovered 50 MHz CMOS clock for use by other components in the system. This synthesizer operates from a differential 50 MHz clock.

Note: An oscillator can only be used with the X557-AT4.

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|-------------|------------------|---------------|------|--|
| Clock Input | CLK_P CLK_N | F1 G1 | I | The 50 MHz differential LVDS reference clock input for the X557. This DC-coupled input has an internal 100 Ω termination resistor associated with it. |
| Reserved | RNC_T20 | T20 | I | Reserved |
| Reserved | RNC_H2 RNC_H3 | H2 H3 | I | Reserved |
| Reserved | RNC_L1 | L1 | O | Reserved |
| Reserved | RNC_H4 | H4 | | Reserved |

3.9 LED

The X557 supports three 20 mA open-drain CMOS LED outputs.

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|--------------------|-------------------------------|-------------------|------|---|
| PHY 0 LED [2:0] | P0_LED0 P0_LED1 P0_LED2 | R1 R2 R3 | OD | The 2.5V tolerant, open-drain LED outputs for PHY 0. These open-drain 20 mA outputs are on the VDD_IO domain. |
| PHY 1 LED [2:0] | P1_LED0 P1_LED1 P1_LED2 | P1 P2 P3 | OD | The 2.5V tolerant, open-drain LED outputs for PHY 1. These open-drain 20 mA outputs are on the VDD_IO domain. |
| PHY 2 LED [2:0] | P2_LED0 P2_LED1 P2_LED2 | R20 P20 N20 | OD | The 2.5V tolerant, open-drain LED outputs for PHY 2. These open-drain 20 mA outputs are on the VDD_IO domain. |
| PHY 3 LED [2:0] | P3_LED0 P3_LED1 P3_LED2 | H20 K20 L20 | OD | The 2.5V tolerant, open-drain LED outputs for PHY 3. These open-drain 20 mA outputs are on the VDD_IO domain. |



3.10 Reference Resistors

The X557 relies on 1% precision resistors to calibrate its internal voltage levels.

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|----------------------------|--|--------------------------|--------|---|
| Bandgap Reference Resistor | RREF_BG0 RREF_BG1 RREF_BG2 RREF_BG3 | A12 B12 B13 A13 | Analog | The connection point for the bandgap reference resistor. This should be a precision 1%, 2.00 kΩ resistor tied to ground |

3.11 Test

The X557 supports a IEEE 1149.1 compliant JTAG interface, with 1149.6 AC JTAG support on the SerDes interface. Note that for normal operation, TRST_N should be held low.

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|----------------------|-------------|---------------|------|--|
| JTAG Clock | TCK | R22 | I | The JTAG clock input. This input is on the VDD_IO domain and has a pull-down associated with it. |
| JTAG Data Input | TDI | T21 | I | The JTAG data input signal. This input is on the VDD_IO domain and has a pull-down associated with it. |
| JTAG Data Output | TDO | T22 | O | The JTAG data output signal. This 20 mA output is on the VDD_IO domain. |
| JTAG Reset | TRST_N | T23 | I | The JTAG reset signal. If JTAG is not used, this pin must be pulled low. This input is on the VDD_IO domain and has a pull-up associated with it. |
| JTAG Test Mode State | TMS | T24 | I | The JTAG test mode state signal. This input is on the VDD_IO domain and has a pull-down associated with it. |



3.12 Metrology

The X557 contains two thermal diodes that can be used to monitor the die temperature without going through the MDIO registers. The “P” indicates the anode terminal (i.e. current input) of the thermal diode.

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|---------------------|----------------------|---------------|--------|--------------------------------|
| PHY 0 Thermal Diode | TDIO_P_0 TDIO_N_0 | N4 M4 | Analog | PHY 0 thermal diode terminals. |
| PHY 3 Thermal Diode | TDIO_P_3 TDIO_N_3 | H22 H21 | Analog | PHY 3 thermal diode terminals. |

3.13 Debug

The X557 supports a side-access port to the MDIO register space via a slave SMBus. Addressing for this SMBus is provisioned on a per PHY basis. It is recommended that every design connect these SMBus pins to a header to allow in-system debug. This obviates the need to disconnect the MDIO lines, and allows for normal system operation during debug.

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|----------------|--------------|---------------|------|--|
| DebugBus Clock | DebugBus_CLK | D24 | I | Clock signal for slave SMBus used for debug port into PHY MDIO register space. This signal requires a pull-up to VDD_IO. This input is on the VDD_IO domain and has a pull-down associated with it. |
| DebugBus Data | DebugBus_DAT | C24 | I/O | Data signal for slave SMBus used for debug port into the PHYs MDIO register space. This signal requires a pull-up to VDD_IO. This 20 mA I/O is on the VDD_IO domain and has a pull-down associated with it. |

3.14 Power

The X557 uses four separate power supplies to minimize power consumption:

- 0.83V
- 1.2V
- 2.1V



- 2.5V

As mentioned earlier, in order to provide maximum flexibility to the implementation, the X557 utilizes a programmable I/O voltage. The logic thresholds for the I/O are set at 70% and 30% for VIH/VOH and VIL/VOL respectively for any VDD_IO greater than 1.8V. For 1.2V MDIO operation (affects TX_EN, MDC, MDIO, RST_N), a separate signal called MDIO_1P2_SELECT_N is provided that will force 1.2V operation on these signals, regardless of the VDD_IO voltage.

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|----------------------|--|--|--------|---|
| AVDD | VCC1P2A VCC1P2B | F2, F4, F6, F8, F10, G3, G5, G7, G9, G11, F15, F17, F19, F21, F23, F24, G14, G16, G18, G20, G22 | Supply | 1.2V analog supply. |
| AVDD22 | P0_VCC2P1 P1_VCC2P1 P2_VCC2P1 P3_VCC2P1 | A2, A4, A6, C2, C4, A8, A10, C6, C8, C10, A15, A17, C15, C17, C19, A19, A21, A23, C21, C23 | Supply | 2.1V analog supply. |
| AVSS | VSS | B2, B4, B6, B8, B10, B15, B17, B19, B21, B23, C1, C3, C5, C7, C9, C11, C14, C16, C18, C20, C22, D2, D4, D6, D8, D10, D15, D17, D19, D21, D23, E1, E2, E4, E6, E8, E10, E12, E13, E15, E17, E19, E21, E23, E24, F3, F5, F7, F9, F11, F13, F14, F16, F18, F20, F22, G2, G6, G10, G12, G17, G21, G23, G24, H5, H7, H9, H11, H13, H15, H19, J6, J8, J10, J12, J14, J16, J18, J20, K7, K9, K11, K13, K15, K17, K19, L6, L8, L10, L12, L14, L16, L18 | Supply | Analog ground. |
| AVSSPLL | VSS | G4, G8, G15, vG19 | Supply | Analog ground for PHY PLL. |
| Analog VDD | VDD | F12, G13 | Supply | 0.83V supply for digital circuitry in the AFE. |
| VCC Crystal | VCC2P1 | D1 | Supply | 2.1V supply for the crystal oscillator. |
| VDD | VDD | M6, M8, M10, M12, M14, M16, M18, N5, N7, N9, N11, N13, N15, N17, N19, P6, P8, P10, P12, P14, P16, P18, R5, R7, R9, R11, R13, R15, R17, T6, T8, T10, T12, T14, T16, T18, U5, U7, U9, U11, U13, U15, U17, U19, V6, V8, V10, V12, V14, V16, V18, V20 | Supply | 0.83V digital supply. |
| VDD FLASH | VDD_FLASH | M3 | Supply | Flash I/O power supply (2.5V). |
| VDD I/O Power Supply | VDD_IO | H23, L4, R24, U3 | Supply | The power supply(2.5V) for the general I/O on the X557. |



| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|----------------|--|---|--------|---|
| VDD I/O Select | MDIO_1P2_SELECT_N | L5 | I | When pulled low, this signal sets the I/O voltages for MDC, MDIO, and RST_N to 1.2V levels, regardless of the VDD_IO voltage. This input is on the VDD_IO domain and has a pull-up associated with it. |
| VDD SerDes | VDD_SRDS | V4, V21, Y4, Y21, AA5, AA7, AA9, AA11, AA13, AA16, AA18, AA20 | Supply | SerDes 0.83V digital supply. |
| VDD22 SerDes | VCC2P1_SRDS | W3, W22, AA3, AA22, AB12, AB14 | Supply | SerDes 2.1V supply. |
| VDD_SENSE | VDD_SENSE | U20 | Supply | Package supply sense point for 0.83V digital supply. |
| VREG SerDes | P0_VREG_SRDS P1_VREG_SRDS P2_VREG_SRDS P3_VREG_SRDS | AB4, AB6, AB8, AB10, AB15, AB17, AB19, AB21 | Supply | SerDes regulator output used for decoupling and monitoring. |
| VSS | VSS | M5, M7, M9, M11, M13, M15, M17, M19, N6, N8, N10, N12, N14, N16, N18, P5, P7, P9, P11, P13, P15, P17, R6, R8, R10, R12, R14, R16, R18, T5, T7, T9, T11, T13, T15, T17, T19, U6, U8, U10, U12, U14, U16, U18, V5, V7, V9, V11, V13, V15, V17, V19 | Supply | Digital ground. |
| VSS SerDes | VSS | U1, U2, U23, U24, V3, V22, W1, W2, W4, W6, W8, W10, W12, W14, W16, W18, W20, W21, W23, W24, Y3, Y5, Y7, Y9, Y11, Y13, Y15, Y17, Y19, AA1, AA2, AA4, AA6, AA8, AA10, AA12, AA14, AA15, AA17, AA19, AA21, AA23, AA24, AB5, AB9, AB11, AB13, AB16, AB20, AB22, AC1, AC2, AC4, AC6, AC8, AC10, AC12, AC13, AC15, AC17, AC19, AC21, AC23, AC24, AD2, AD4, AD6, AD8, AD10, AD12, AD13, AD15, AD17, AD19, AD21, AD23 | Supply | SerDes ground. |



3.15 Reserved

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description | |
|---------------------|--|--|------|--|--|
| Floating | NC | H6, H8, H10, H12, H14, H16, H18, J7, J9, J11, J13, J15, J17, J19, K6, K8, K10, K12, K14, K16, K18, L7, L9, L11, L13, L15, L17, L19, R23, W5, W7, W9, W11, W13, W15, W17, W19, Y6, Y8, Y10, Y12, Y14, Y16, Y18, Y20 | NC | NC | These pins are floating in the package and can be connected as convenience dictates. |
| Reserved Ground | RG_J3, RG_A1, RG_K3, RG_AD1, RG_A24, RG_AD24 | J3, A1, K3, AD1, A24, AD24 | I | Reserved ground signal. These pins must be connected to digital ground in the PCB design. These inputs are on the VDD_IO domain and have pull-downs associated with them. | |
| Reserved No Connect | RNC_L3, RNC_P4, RNC_N21, RNC_J21, RNC_B1, RNC_J4, RNC_J5, RNC_U4, RNC_T4, RNC_K4, RNC_K5, RNC_P22, RNC_P21, RNC_R21, RNC_H24, RNC_AB3, RNC_R19, RNC_P19, RNC_C12, RNC_D12, RNC_AB7, RNC_B24, RNC_D13, RNC_C13, RNC_AB18, RNC_U22, RNC_U21, RNC_Y22 | L3, P4, N21, J21, B1, J4, J5, U4, T4, K4, K5, P22, P21, R21, H24, AB3, R19, P19, C12, D12, AB7, B24, D13, C13, AB18, U22, U21, Y22 | | Reserved no connect signal. These pins must be left unconnected in the PCB design. | |
| Reserved VDD_IO | RVDD_N3, RVDD_T3, RVDD_N22, RVDD_M20 | N3, T3, N22, M20 | I | Reserved VDD_IO signal. These pins must be connected to VDD_IO (2.5V) This input is on the VDD_IO domain and has a pull-up resistor associated with it. | |



3.16 Pinouts

The pinouts for the X557 is shown in the following figure. The signals are color coded to group similar functionalities together. The view is looking from the top of the chip.

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|-------------|-----------|------------|--------------|-----------|--------------|-----------|--------------|-----------|--------------|-----------|------------|-----------|------------|--------------|-----------|--------------|-----------|--------------|-----------|--------------|-----------|-----------|-----------|------------|-----------|---------|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | | | | |
| > | R0_A0 | P0_VCCP1 | P0_A0N | P0_VCCP1 | P0_C0N | P0_VCCP1 | P0_G0N | P0_VCCP1 | P0_B0N | P0_VCCP1 | P0_D0N | R0C_D12 | R0C_D13 | P2_A0N | P2_VCCP1 | P2_C0N | P2_VCCP1 | P0_G0N | P0_VCCP1 | P0_B0N | P0_VCCP1 | P0_D0N | P0_VCCP1 | R0C_A04 | > | | | |
| ⊖ | R0C_B1 | VSS | P0_A0P | VSS | P0_C0P | VSS | P0_G0P | VSS | P0_B0P | VSS | P0_D0P | R0C_D12 | R0C_D13 | P2_A0P | VSS | P2_C0P | VSS | P0_G0P | P0_VCCP1 | VSS | P0_B0P | VSS | P0_D0P | VSS | R0C_B24 | ⊖ | | |
| ⊖ | VSS | P0_VCCP1 | VSS | P0_VCCP1 | VSS | P1_VCCP1 | VSS | P1_VCCP1 | VSS | P1_VCCP1 | VSS | R0C_D12 | R0C_D13 | VSS | P2_VCCP1 | VSS | P2_VCCP1 | VSS | P2_VCCP1 | VSS | P2_VCCP1 | VSS | P2_VCCP1 | VSS | P2_VCCP1 | Debug_CLK | | |
| ⊖ | VCCP1 | VSS | P0_B0N | VSS | P0_D0N | VSS | P1_G0N | VSS | P1_A0N | VSS | P1_C0N | R0C_D12 | R0C_D13 | P2_B0N | VSS | P2_D0N | VSS | P2_G0N | VSS | P0_A0N | VSS | P1_C0N | VSS | P1_VCCP1 | VSS | Debug_CLK | | |
| m | VSS | VSS | P0_B0P | VSS | P0_D0P | VSS | P1_G0P | VSS | P1_A0P | VSS | P1_C0P | VSS | VSS | P2_B0P | VSS | P2_D0P | VSS | P2_G0P | VSS | P0_A0P | VSS | P1_C0P | VSS | VSS | VSS | m | | |
| ⊖ | CLK_P | VCCIP2A | VSS | VCCIP2A | VSS | VCCIP2A | VSS | VCCIP2A | VSS | VCCIP2A | VSS | VDD | VSS | VSS | VCCIP2B | VSS | VCCIP2B | VSS | VCCIP2B | VSS | VCCIP2B | VSS | VCCIP2B | VSS | VCCIP2B | ⊖ | | |
| ⊖ | CLK_N | VSS | VCCIP2A | VSS | VCCIP2A | VSS | VCCIP2A | VSS | VCCIP2A | VSS | VCCIP2A | VSS | VDD | VCCIP2B | VSS | VCCIP2B | VSS | VCCIP2B | VSS | VCCIP2B | VSS | VCCIP2B | VSS | VCCIP2B | VSS | ⊖ | | |
| ⊖ | DC_MASTER_N | R0C_H0 | R0C_H0 | R0C_H4 | VSS | NC | VSS | NC | VSS | NC | VSS | NC | VSS | NC | VSS | NC | VSS | NC | VSS | NC | VSS | P1_LED0 | TDD_N_3 | TDD_P_3 | VSS_D1 | R0C_H24 | | |
| ← | SN | SOUT | R0C_J0 | R0C_J4 | R0C_J5 | VSS | NC | VSS | NC | VSS | NC | VSS | NC | VSS | NC | VSS | NC | VSS | NC | VSS | NC | VSS | R0C_B1 | ADDR0 | ADDR2 | ADDR3 | ← | |
| ⊖ | SQL | CE_N | R0C_K0 | R0C_K4 | R0C_K5 | NC | VSS | NC | VSS | NC | VSS | NC | VSS | NC | VSS | NC | VSS | NC | VSS | NC | VSS | P1_LED1 | P1_M0C | P1_M0C | P2_M0C | P1_M0C | ⊖ | |
| ⊖ | R0C_L1 | RST_OUT_N | R0C_L3 | VSS_D1 | R0C_L4 | VSS | NC | VSS | NC | VSS | NC | VSS | NC | VSS | NC | VSS | NC | VSS | NC | VSS | NC | P1_LED2 | P1_INT_N | P1_INT_N | P2_INT_N | P1_INT_N | ⊖ | |
| ⊖ | R0C_DATA | R0C_RST_N | R0C_RST_N | TDD_N_6 | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | R0C_M03 | P1_M03 | P1_M03 | P2_M03 | P1_M03 | ⊖ | |
| ⊖ | R0C_CLK | R0C_SF | R0C_SF | TDD_P_3 | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | P1_LED2 | R0C_N01 | R0C_N02 | R0C_DATA | R0C_SF | ⊖ | |
| ⊖ | P1_LED0 | P1_LED1 | P1_LED2 | R0C_P4 | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | R0C_P19 | P1_LED1 | R0C_P21 | R0C_P22 | R0C_RST_N | R0C_CLK | ⊖ |
| ⊖ | P0_LED0 | P0_LED1 | P0_LED2 | R0C_A00R1 | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | R0C_R19 | P1_LED0 | R0C_R21 | TK | NC | VSS_D1 | ⊖ |
| ← | RST_N | R0C_A00R0 | R0C_T3 | R0C_T4 | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | R0C_T0 | TDI | TDO | TRST_N | TMS | ← | |
| ⊖ | VSS | VSS | VSS_D1 | R0C_U4 | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | ⊖ | |
| ← | P0_RX_L0N | P0_RX_L0P | VSS | VDD_SRD0 | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | ← | |
| ⊖ | VSS | VSS | VCCP1_SRD0 | VSS | NC | VSS | NC | VSS | NC | VSS | NC | VSS | NC | VSS | NC | VSS | NC | VSS | NC | VSS | NC | VSS | VSS | VSS | VCCP1_SRD0 | VSS | VSS | ⊖ |
| ← | P0_TX_L0N | P0_TX_L0P | VSS | VDD_SRD0 | VSS | NC | VSS | NC | VSS | NC | VSS | NC | VSS | NC | VSS | NC | VSS | NC | VSS | NC | VSS | NC | VDD_SRD0 | R0C_Y22 | P0_RX_L0N | P0_RX_L0N | ← | |
| ⊖ | VSS | VSS | VCCP1_SRD0 | VSS | VDD_SRD0 | VSS | VDD_SRD0 | VSS | VDD_SRD0 | VSS | VDD_SRD0 | VSS | VDD_SRD0 | VSS | VDD_SRD0 | VSS | VDD_SRD0 | VSS | VDD_SRD0 | VSS | VDD_SRD0 | VSS | VDD_SRD0 | VSS | VDD_SRD0 | VSS | VSS | ⊖ |
| ⊖ | P0_RX_L0N | P0_RX_L0P | R0C_A03 | P0_VREG_SRD0 | VSS | P0_VREG_SRD0 | R0C_A07 | P1_VREG_SRD0 | VSS | P1_VREG_SRD0 | VSS | VCCP1_SRD0 | VSS | VCCP1_SRD0 | P2_VREG_SRD0 | VSS | P2_VREG_SRD0 | R0C_A08 | P3_VREG_SRD0 | VSS | P3_VREG_SRD0 | VSS | P0_TX_L0N | P0_TX_L0N | P0_TX_L0N | P0_TX_L0N | ⊖ | |
| ⊖ | VSS | VSS | P0_TX_L0P | VSS | P0_RX_L0N | VSS | P0_TX_L0P | VSS | P0_RX_L0N | VSS | P0_TX_L0P | VSS | P0_RX_L0N | VSS | P0_TX_L0P | VSS | P0_RX_L0N | VSS | P0_TX_L0P | VSS | P0_RX_L0N | VSS | P0_TX_L0P | VSS | P0_RX_L0N | VSS | VSS | ⊖ |
| ⊖ | R0C_A01 | VSS | P0_TX_L0N | VSS | P0_RX_L0N | VSS | P0_TX_L0N | VSS | P0_RX_L0N | VSS | P0_TX_L0N | VSS | VSS | P0_RX_L0N | VSS | P0_TX_L0N | VSS | P0_RX_L0N | VSS | P0_TX_L0N | VSS | P0_RX_L0N | VSS | P0_TX_L0N | VSS | P0_RX_L0N | VSS | ⊖ |

Figure 3-6 X557-AT4



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4.0 Register Definitions

4.1 Introduction

The X557 is internally divided into a series of MDIO Manageable Devices (MMDs), each of which performs a logical function as per the 10GBASE-T standard.

Here the MMD #1 contains the PMA, which is basically the analog front-end of the chip. This is connected to MMD #3, which contains the PCS that handles the 10GBASE-T transmission frame coding and decoding, including the 128-DSQ and LDPC work.

In addition to these MMDs, there are three others:

- MMD #7 — Contains the auto-negotiation function.
- MMD #29 — Contains the controls for the GbE and 100M PCS machinery.
- MMD# 30 — Contains the global control functionality for the X557.

Not shown, but present within the X557, is MMD #31, which is used for proprietary purposes as an adjunct to the PMA.

Note: NVR used throughout this document is synonymous with Non-volatile Memory (NVM).

4.2 Register Structure

A map of the regions is shown in [Figure 4-1](#). Any attempt to read from the reserved MMD addresses returns a value of 0x00, and any writes to these addresses have no effect.

Table 4-1 MMD Device Addresses

| 5-bit Device Address (Hex) | MMD Name |
|----------------------------|----------------------------|
| 0 | Reserved |
| 1 | PMA/PMD (128 DSQ) |
| 2 | Reserved |
| 3 | PCS (64/65B coder/decoder) |
| 4 | Reserved |
| 5 - 6 | Reserved |
| 7 | Auto-negotiation |
| 8 - 1C | Reserved |



Table 4-1 MMD Device Addresses

| 5-bit Device Address (Hex) | MMD Name |
|----------------------------|----------|
| 1D | GbE |
| 1E | Global |

4.3 Format and Nomenclature

Registers within the device are referenced in the format:

Region . Register . Bit

where **Region** corresponds to the MMD region being addressed, **Register** corresponds to the register address within the MMD region, and **Bit** is the bit within the register. All registers within the MDIO register space are 16 bits. The address of the register is the 16-bit MDIO address.

All read and write operations are word-based, which means that the entire 16-bit register is read or written (versus individual bits). There are several different bit types within the MDIO register space. A list of these bit types are found in Table 6.2.

Table 4-2 Field Types within the MDIO Register Space

| Abbreviation | Type | Description |
|--------------|-------------------------|---|
| LL | Latching Low | If the condition the bit is monitoring goes low, this bit latches low, generates a maskable interrupt, and stays low until read. Reading this bit resets it to one. This bit is read-only. |
| LH | Latching High | If the condition the bit is monitoring goes high, this bit latches high, generates a maskable interrupt, and stays high until read. Reading this bit resets it to zero. This bit is read-only. |
| LRF | Latch Rising or Falling | Set high on either a rising or falling edge. If a transition occurs, this bit latches high, generates a maskable interrupt, and stays high until read. Reading this bit resets it to zero. This bit is read-only. |
| PD | Provisionable Defaults | Indicates that the default value associated with this field is provisionable. |
| R/W | Read/Write | Field can be both read from and written to. |
| RO | Read Only | Read-only field. Writes are ignored. |
| ROS | Read Only Static | Read-only static field. The same value is always returned. Writes are ignored. |
| RSV | Reserved | Reserved. Do not modify. |
| SC | Self-Clearing | A read/write register which resets itself upon completion of an action. |
| SCT | Saturating Counter | A read-only counter that saturates at the limit, and is cleared on read. |
| SCTL | Saturating Counter LSW | The Least Significant Word of a Saturating Counter. This register clears the pair to zero on read and snapshots the mate MSW to shadow memory, awaiting read. |
| SCTM | Saturating Counter MSW | The Most Significant Word of a Saturating Counter. Reading this completes the read process of the register pair. |



4.4 Structure

The following structure is used for registers:

1. All Clause 45 registers (registers defined in Clause 45) are placed in their respective areas within the MMDs as specified.
2. Intel-specific registers associated with each of the Clause 45 MMDs are placed in the Intel-specific area beginning at 0xC000, according to the register map shown in [Figure 4-3](#).

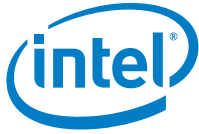
Table 4-3 Register Layout

| Base Offset (Hex) | Description |
|-------------------|---------------------------------|
| C000 | Tx & Overall MMD Control |
| C400 | Tx & Overall MMD Provisioning |
| C800 | Tx & Overall MMD State |
| CC00 | Tx & Overall MMD Alarms |
| D000 | Standard Interrupt Mask |
| D400 | Tx & Overall MMD Interrupt Mask |
| D800 | Tx & Overall MMD Debug |
| DC00 | Reserved |
| E000 | Rx Control |
| E400 | Rx Provisioning |
| E800 | Rx State |
| EC00 | Rx Alarms |
| F000 | Standard Interrupt Mask |
| F400 | Rx Interrupt Mask |
| F800 | Rx Debug |
| FC00 | Global Interrupt Flags |

The table is split into a transmit portion and a receive portion, with the transmit portion also containing any overall Intel-specific registers for the MMD. In this table, the following definitions apply:

Table 4-4 Terms Used within the Register Layout

| Term | Definition |
|-------------------------------|---|
| Control | Action bits that affect the operation of the MMD, such as reset. |
| Provisioning | Static provisioning bits that control the behavior of the MMD. |
| State | Bits that reflect the state of the MMD. |
| Alarm | Bits that can generate maskable interrupts. |
| Standard Interrupt Mask | Interrupt masks for alarm bits defined in the Clause 45 register set. |
| Intel-Specific Interrupt Mask | Interrupt masks for Intel-Specific alarms. |



- 3. Interrupts are handled in a hierarchical fashion, with the top-level interrupt indication being the INT* interrupt pin on the X557. Below this are two maskable interrupt trees: one composed of standard interrupts, and one composed of Intel-defined interrupts. The top level summary register for these trees resides at the end of the register space in MMD #30 - the Global MMD (1E.FC00). Feeding this are interrupt registers from each of the individual MMDs.
 - a. The standard interrupt tree is designed so that the source of any interrupt can be determined in a maximum of two reads.
 - b. The Intel-defined interrupt tree requires at most three reads to determine the source of an interrupt.
 - c. All interrupts are maskable, whether they are from the Standard interrupt tree, or from the Intel-specific interrupt tree.

4.5 Registers and Documentation

The registers for the X557 are provided in the following tables, listed in numerical order of their MMD address. Associated with these registers is a set of C-language header files and associated Doxygen[8] documentation for them. These header files contain all of the appropriate C-structures to access the registers and fields within the registers.

4.6 Device Registers

4.6.1 Registers Summary

Table 4-5 Registers Summary

| Address | Name | Page |
|----------------------|--|------|
| PMA Registers | | |
| 1.0 | PMA Standard Control 1 | 82 |
| 1.1 | PMA Standard Status 1 | 83 |
| 1.2 | PMA Standard Device Identifier 1 | 83 |
| 1.3 | PMA Standard Device Identifier 2 | 83 |
| 1.4 | PMA Standard Speed Ability | 83 |
| 1.5 | PMA Standard Devices in Package 1 | 84 |
| 1.6 | PMA Standard Devices in Package 2 | 85 |
| 1.7 | PMA Standard Control 2 | 85 |
| 1.8 | PMA Standard Status 2 | 85 |
| 1.9 | PMD Standard Transmit Disable Control | 87 |
| 1.A | PMD Standard Signal Detect | 87 |
| 1.B | PMD Standard 10G Extended Ability Register | 88 |
| 1.E | PMA Standard Package Identifier 1 | 88 |
| 1.F | PMA Standard Package Identifier 2 | 89 |



Table 4-5 Registers Summary (Continued)

| Address | Name | Page |
|----------------------|---|------|
| 1.81 | PMA 10GBASE-T Status | 89 |
| 1.82 | PMA 10GBASE-T Pair Swap and Polarity Status | 89 |
| 1.83 | PMA 10GBASE-T Tx Power Back-off and Short Reach Setting | 89 |
| 1.84 | PMA 10GBASE-T Test Modes | 90 |
| 1.85 | PMA 10GBASE-T SNR Operating Margin Channel A | 91 |
| 1.86 | PMA 10GBASE-T SNR Operating Margin Channel B | 91 |
| 1.87 | PMA 10GBASE-T SNR Operating Margin Channel C | 91 |
| 1.88 | PMA 10GBASE-T SNR Operating Margin Channel D | 91 |
| 1.89 | PMA 10GBASE-T SNR Minimum Operating Margin Channel A | 92 |
| 1.8A | PMA 10GBASE-T SNR Minimum Operating Margin Channel B | 92 |
| 1.8B | PMA 10GBASE-T SNR Minimum Operating Margin Channel C | 92 |
| 1.8C | PMA 10GBASE-T SNR Minimum Operating Margin Channel D | 92 |
| 1.8D | PMA 10GBASE-T Receive Signal Power Channel A | 93 |
| 1.8E | PMA 10GBASE-T Receive Signal Power Channel B | 93 |
| 1.8F | PMA 10GBASE-T Receive Signal Power Channel C | 93 |
| 1.90 | PMA 10GBASE-T Receive Signal Power Channel D | 93 |
| 1.91 | PMA 10GBASE-T Skew Delay 1 | 94 |
| 1.92 | PMA 10GBASE-T Skew Delay 2 | 94 |
| 1.93 | PMA 10GBASE-T Fast Retrain Status and Control | 94 |
| 1.C412 | PMA Transmit Reserved Vendor Provisioning 0 | 95 |
| 1.C413 | PMA Transmit Reserved Vendor Provisioning 1 | 95 |
| 1.CC00 | PMA Transmit Vendor Alarms 1 | 95 |
| 1.CC01 | PMA Transmit Vendor Alarms 2 | 95 |
| 1.CC02 | PMA Transmit Vendor Alarms 3 | 96 |
| 1.D000 | PMA Transmit Standard Interrupt Mask 1 | 96 |
| 1.D001 | PMA Transmit Standard Interrupt Mask 2 | 96 |
| 1.D400 | PMA Transmit Vendor LASI Interrupt Mask 1 | 96 |
| 1.D401 | PMA Transmit Vendor LASI Interrupt Mask 2 | 97 |
| 1.D402 | PMA Transmit Vendor LASI Interrupt Mask 3 | 97 |
| 1.D800 | PMA Transmit Vendor Debug 1 | 97 |
| 1.E400 | PMA Receive Reserved Vendor Provisioning 1 | 97 |
| 1.E800 | PMA Receive Vendor State 1 | 98 |
| 1.E810 | PMA Receive Reserved Vendor State 1 | 98 |
| 1.E811 | PMA Receive Reserved Vendor State 2 | 98 |
| 1.FC00 | PMA Vendor Global Interrupt Flags 1 | 98 |
| PCS Registers | | |
| 3.0 | PCS Standard Control 1 | 100 |
| 3.1 | PCS Standard Status 1 | 101 |
| 3.2 | PCS Standard Device Identifier 1 | 101 |
| 3.3 | PCS Standard Device Identifier 2 | 101 |



Table 4-5 Registers Summary (Continued)

| Address | Name | Page |
|---------|--|------|
| 3.4 | PCS Standard Speed Ability | 101 |
| 3.5 | PCS Standard Devices in Package 1 | 102 |
| 3.6 | PCS Standard Devices in Package 2 | 102 |
| 3.7 | PCS Standard Control 2 | 103 |
| 3.8 | PCS Standard Status 2 | 103 |
| 3.E | PCS Standard Package Identifier 1 | 104 |
| 3.F | PCS Standard Package Identifier 2 | 104 |
| 3.14 | PCS EEE Capability Register | 104 |
| 3.16 | PCS EEE Wake Error Counter | 104 |
| 3.20 | PCS 10G Status 1 | 105 |
| 3.21 | PCS 10G Status 2 | 105 |
| 3.22 | PCS 10GBASE-R Test Pattern Seed A 1 | 105 |
| 3.23 | PCS 10GBASE-R Test Pattern Seed A 2 | 106 |
| 3.24 | PCS 10GBASE-R Test Pattern Seed A 3 | 106 |
| 3.25 | PCS 10GBASE-R Test Pattern Seed A 4 | 106 |
| 3.26 | PCS 10GBASE-R Test Pattern Seed B 1 | 106 |
| 3.27 | PCS 10GBASE-R Test Pattern Seed B 2 | 106 |
| 3.28 | PCS 10GBASE-R Test Pattern Seed B 3 | 106 |
| 3.29 | PCS 10GBASE-R Test Pattern Seed B 4 | 107 |
| 3.2A | PCS 10GBASE-R PCS Test-Pattern Control | 107 |
| 3.2B | PCS 10GBASE-R PCS Test-Pattern Error Counter | 107 |
| 3.C400 | PCS Transmit Vendor Provisioning 1 | 107 |
| 3.C401 | PCS Transmit Vendor Provisioning 2 | 108 |
| 3.C410 | PCS Transmit Reserved Vendor Provisioning 1 | 108 |
| 3.C455 | PCS Transmit XFI Vendor Provisioning 1 | 108 |
| 3.C456 | PCS Transmit XFI Vendor Provisioning 2 | 108 |
| 3.C457 | PCS Transmit XFI Vendor Provisioning 3 | 108 |
| 3.C458 | PCS Transmit XFI Vendor Provisioning 4 | 109 |
| 3.C459 | PCS Transmit XFI Vendor Provisioning 5 | 109 |
| 3.C45A | PCS Transmit XFI Vendor Provisioning 6 | 109 |
| 3.C45B | PCS Transmit XFI Vendor Provisioning 7 | 109 |
| 3.C45C | PCS Transmit XFI Vendor Provisioning 8 | 109 |
| 3.C460 | PCS Transmit XFI0 Vendor Provisioning 1 | 110 |
| 3.C461 | PCS Transmit XFI0 Vendor Provisioning 2 | 110 |
| 3.C470 | PCS Transmit XFI1 Vendor Provisioning 1 | 111 |
| 3.C471 | PCS Transmit XFI1 Vendor Provisioning 2 | 111 |
| 3.C820 | PCS Transmit Vendor FCS No Error Frame Counter 1 | 112 |
| 3.C821 | PCS Transmit Vendor FCS No Error Frame Counter 2 | 112 |
| 3.C822 | PCS Transmit Vendor FCS Error Frame Counter 1 | 112 |
| 3.C823 | PCS Transmit Vendor FCS Error Frame Counter 2 | 112 |



Table 4-5 Registers Summary (Continued)

| Address | Name | Page |
|---------|--|------|
| 3.C860 | PCS Transmit XFI0 Vendor State 1 | 112 |
| 3.C861 | PCS Transmit XFI0 Vendor State 2 | 113 |
| 3.C862 | PCS Transmit XFI0 Vendor State 3 | 113 |
| 3.C863 | PCS Transmit XFI0 Vendor State 4 | 113 |
| 3.C870 | PCS Transmit XFI1 Vendor State 1 | 113 |
| 3.C871 | PCS Transmit XFI1 Vendor State 2 | 113 |
| 3.C872 | PCS Transmit XFI1 Vendor State 3 | 113 |
| 3.C873 | PCS Transmit XFI1 Vendor State 4 | 114 |
| 3.C880 | PCS Transmit XGS Vendor State 1 | 114 |
| 3.C881 | PCS Transmit XGS Vendor State 2 | 114 |
| 3.C882 | PCS Transmit XGS Vendor State 3 | 114 |
| 3.C883 | PCS Transmit XGS Vendor State 4 | 114 |
| 3.C884 | PCS Transmit XGS Vendor State 5 | 114 |
| 3.CC00 | PCS Transmit Vendor Alarms 1 | 115 |
| 3.CC01 | PCS Transmit Vendor Alarms 2 | 115 |
| 3.CC02 | PCS Transmit Vendor Alarms 3 | 115 |
| 3.CC03 | PCS Transmit Vendor Alarms 4 | 115 |
| 3.D000 | PCS Standard Interrupt Mask 1 | 116 |
| 3.D001 | PCS Standard Interrupt Mask 2 | 116 |
| 3.D002 | PCS Standard Interrupt Mask 3 | 116 |
| 3.D400 | PCS Transmit Vendor Interrupt Mask 1 | 117 |
| 3.D401 | PCS Transmit Vendor Interrupt Mask 2 | 117 |
| 3.D402 | PCS Transmit Vendor Interrupt Mask 3 | 117 |
| 3.D403 | PCS Transmit Vendor Interrupt Mask 4 | 117 |
| 3.D800 | PCS Transmit Vendor Debug 1 | 118 |
| 3.E400 | PCS Receive Vendor Provisioning 1 | 118 |
| 3.E460 | PCS Receive XFI0 Provisioning 1 | 118 |
| 3.E461 | PCS Receive XFI0 Provisioning 2 | 118 |
| 3.E470 | PCS Receive XFI1 Provisioning 1 | 119 |
| 3.E471 | PCS Receive XFI1 Provisioning 2 | 119 |
| 3.E800 | PCS Receive Vendor State 1 | 120 |
| 3.E810 | PCS Receive Vendor CRC-8 Error Counter 1 | 120 |
| 3.E811 | PCS Receive Vendor CRC-8 Error Counter 2 | 120 |
| 3.E812 | PCS Receive Vendor FCS No Error Frame Counter 1 | 120 |
| 3.E813 | PCS Receive Vendor FCS No Error Frame Counter 2 | 120 |
| 3.E814 | PCS Receive Vendor FCS Error Frame Counter 1 | 121 |
| 3.E815 | PCS Receive Vendor FCS Error Frame Counter 2 | 121 |
| 3.E820 | PCS Receive Vendor Uncorrected Frame Counter 1 | 121 |
| 3.E821 | PCS Receive Vendor Uncorrected Frame Counter 2 | 121 |
| 3.E840 | PCS Receive Vendor Corrected Frame 1 Iteration Counter 1 | 122 |



Table 4-5 Registers Summary (Continued)

| Address | Name | Page |
|---------|--|------|
| 3.E841 | PCS Receive Vendor Corrected Frame 1 Iteration Counter 2 | 122 |
| 3.E842 | PCS Receive Vendor Corrected Frame 2 Iteration Counter 1 | 122 |
| 3.E843 | PCS Receive Vendor Corrected Frame 2 Iteration Counter 2 | 122 |
| 3.E844 | PCS Receive Vendor Corrected Frame 3 Iteration Counter 1 | 123 |
| 3.E845 | PCS Receive Vendor Corrected Frame 3 Iteration Counter 2 | 123 |
| 3.E846 | PCS Receive Vendor Corrected Frame 4 Iteration Counter 1 | 123 |
| 3.E847 | PCS Receive Vendor Corrected Frame 4 Iteration Counter 2 | 123 |
| 3.E848 | PCS Receive Vendor Corrected Frame 5 Iteration Counter 1 | 124 |
| 3.E849 | PCS Receive Vendor Corrected Frame 5 Iteration Counter 2 | 124 |
| 3.E850 | PCS Receive Vendor Corrected Frame 6 Iteration Counter | 124 |
| 3.E851 | PCS Receive Vendor Corrected Frame 7 Iteration Counter | 124 |
| 3.E852 | PCS Receive Vendor Corrected Frame 8 Iteration Counter | 125 |
| 3.E860 | PCS Receive XFI0 Vendor State 1 | 125 |
| 3.E861 | PCS Receive XFI0 Vendor State 2 | 125 |
| 3.E862 | PCS Receive XFI0 Vendor State 3 | 125 |
| 3.E863 | PCS Receive XFI0 Vendor State 4 | 125 |
| 3.E864 | PCS Receive XFI0 Vendor State 5 | 125 |
| 3.E865 | PCS Receive XFI0 Vendor State 6 | 126 |
| 3.E866 | PCS Receive XFI0 Vendor State 7 | 126 |
| 3.E870 | PCS Receive XFI1 Vendor State 1 | 126 |
| 3.E871 | PCS Receive XFI1 Vendor State 2 | 126 |
| 3.E872 | PCS Receive XFI1 Vendor State 3 | 126 |
| 3.E873 | PCS Receive XFI1 Vendor State 4 | 126 |
| 3.E874 | PCS Receive XFI1 Vendor State 5 | 127 |
| 3.E875 | PCS Receive XFI1 Vendor State 6 | 127 |
| 3.E876 | PCS Receive XFI1 Vendor State 7 | 127 |
| 3.EC00 | PCS Receive Vendor Alarms 1 | 127 |
| 3.EC01 | PCS Receive Vendor Alarms 2 | 128 |
| 3.EC02 | PCS Receive Vendor Alarms 3 | 128 |
| 3.EC03 | PCS Receive Vendor Alarms 4 | 128 |
| 3.EC04 | PCS Receive Vendor Alarms 5 | 128 |
| 3.EC05 | PCS Receive Vendor Alarms 6 | 128 |
| 3.EC06 | PCS Receive Vendor Alarms 7 | 129 |
| 3.F400 | PCS Receive Vendor Interrupt Mask 1 | 129 |
| 3.F401 | PCS Receive Vendor Interrupt Mask 2 | 130 |
| 3.F402 | PCS Receive Vendor Interrupt Mask 3 | 130 |
| 3.F403 | PCS Receive Vendor Interrupt Mask 4 | 130 |
| 3.F404 | PCS Receive Vendor Interrupt Mask 5 | 130 |
| 3.F405 | PCS Receive Vendor Interrupt Mask 6 | 131 |
| 3.F406 | PCS Receive Vendor Interrupt Mask 7 | 131 |



Table 4-5 Registers Summary (Continued)

| Address | Name | Page |
|-----------------------------------|---|------|
| 3.F800 | PCS Receive Vendor Debug 1 | 131 |
| 3.FC00 | PCS Vendor Global Interrupt Flags 1 | 132 |
| 3.FC02 | PCS Vendor Global Interrupt Flags 3 | 133 |
| PHY XS Registers | | |
| 4.0 | PHY XS Standard Control 1 | 134 |
| 4.1 | PHY XS Standard Status 1 | 134 |
| 4.2 | PHY XS Standard Device Identifier 1 | 135 |
| 4.3 | PHY XS Standard Device Identifier 2 | 135 |
| 4.4 | PHY XS Standard Speed Ability | 135 |
| 4.5 | PHY XS Standard Devices in Package 1 | 135 |
| 4.6 | PHY XS Standard Devices in Package 2 | 136 |
| 4.8 | PHY XS Standard Status 2 | 136 |
| 4.E | PHY XS Standard Package Identifier 1 | 137 |
| 4.F | PHY XS Standard Package Identifier 2 | 137 |
| 4.14 | PHY XS EEE Capability Register | 137 |
| 4.16 | PHY XS EEE Wake Error Counter | 137 |
| 4.18 | PHY XS Standard XGXS Lane Status | 137 |
| 4.19 | PHY XS Standard XGXS Test Control | 138 |
| 4.C180 | PHY XS SERDES Configuration 1 | 138 |
| 4.C1C0 | PHY XS SERDES Lane 0 Configuration 1 | 138 |
| 4.C1D0 | PHY XS SERDES Lane 1 Configuration 1 | 138 |
| 4.C1E0 | PHY XS SERDES Lane 2 Configuration 1 | 139 |
| 4.C1F0 | PHY XS SERDES Lane 3 Configuration 1 | 139 |
| 4.C200 | PHY XS SERDES LUT 256 | 139 |
| 4.FC00 | PHY XS Vendor Global Interrupt Flags 1 | 139 |
| Auto-negotiation Registers | | |
| 7.0 | Auto-negotiation Standard Control 1 | 140 |
| 7.1 | Auto-negotiation Standard Status 1 | 140 |
| 7.2 | Auto-negotiation Standard Device Identifier 1 | 141 |
| 7.3 | Auto-negotiation Standard Device Identifier 2 | 141 |
| 7.5 | Auto-negotiation Standard Devices in Package 1 | 141 |
| 7.6 | Auto-negotiation Standard Devices in Package 2 | 142 |
| 7.8 | Auto-negotiation Standard Status 2 | 142 |
| 7.E | Auto-negotiation Standard Package Identifier 1 | 143 |
| 7.F | Auto-negotiation Standard Package Identifier 2 | 143 |
| 7.10 | Auto-negotiation Advertisement Register | 143 |
| 7.13 | Auto-negotiation Link Partner Base Page Ability Register | 144 |
| 7.16 | Auto-negotiation Extended Next Page Transmit Register | 145 |
| 7.17 | Auto-negotiation Extended Next Page Unformatted Code Register 1 | 146 |
| 7.18 | Auto-negotiation Extended Next Page Unformatted Code Register 2 | 146 |



Table 4-5 Registers Summary (Continued)

| Address | Name | Page |
|---------|--|------|
| 7.19 | Auto-negotiation Link Partner Extended Next Page Ability Register | 146 |
| 7.1A | Auto-negotiation Link Partner Extended Next Page Unformatted Code Register 1 | 147 |
| 7.1B | Auto-negotiation Link Partner Extended Next Page Unformatted Code Register 2 | 147 |
| 7.20 | Auto-negotiation 10GBASE-T Control Register | 147 |
| 7.21 | Auto-negotiation 10GBASE-T Status Register | 147 |
| 7.3C | Auto-negotiation EEE Advertisement Register | 148 |
| 7.3D | Auto-negotiation EEE Link Partner Ability Register | 148 |
| 7.C200 | KR0 Auto-negotiation Control | 149 |
| 7.C201 | KR0 Auto-negotiation Status | 149 |
| 7.C210 | KR0 Auto-negotiation Advertisement Word 1 | 150 |
| 7.C211 | KR0 Auto-negotiation Advertisement Word 2 | 151 |
| 7.C212 | KR0 Auto-negotiation Advertisement Word 3 | 151 |
| 7.C213 | KR0 Link Partner Auto-negotiation Advertisement Word 1 | 151 |
| 7.C214 | KR0 Link Partner Auto-negotiation Advertisement Word 2 | 152 |
| 7.C215 | KR0 Link Partner Auto-negotiation Advertisement Word 3 | 152 |
| 7.C216 | KR0 Auto-negotiation Extended Next Page Advertisement Word 1 | 152 |
| 7.C217 | KR0 Auto-negotiation Extended Next Page Advertisement Word 2 | 153 |
| 7.C218 | KR0 Auto-negotiation Extended Next Page Advertisement Word 3 | 153 |
| 7.C219 | KR0 Link Partner Auto-negotiation Extended Next Page Advertisement Word 1 | 153 |
| 7.C21A | KR0 Link Partner Auto-negotiation Extended Next Page Advertisement Word 2 | 153 |
| 7.C21B | KR0 Link Partner Auto-negotiation Extended Next Page Advertisement Word 3 | 153 |
| 7.C300 | KR1 Auto-negotiation Control | 153 |
| 7.C301 | KR1 Auto-negotiation Status | 154 |
| 7.C310 | KR1 Auto-negotiation Advertisement Word 1 | 154 |
| 7.C311 | KR1 Auto-negotiation Advertisement Word 2 | 155 |
| 7.C312 | KR1 Auto-negotiation Advertisement Word 3 | 155 |
| 7.C313 | KR1 Link Partner Auto-negotiation Advertisement Word 1 | 156 |
| 7.C314 | KR1 Link Partner Auto-negotiation Advertisement Word 2 | 156 |
| 7.C315 | KR1 Link Partner Auto-negotiation Advertisement Word 3 | 157 |
| 7.C316 | KR1 Auto-negotiation Extended Next Page Advertisement Word 1 | 157 |
| 7.C317 | KR1 Auto-negotiation Extended Next Page Advertisement Word 2 | 157 |
| 7.C318 | KR1 Auto-negotiation Extended Next Page Advertisement Word 3 | 157 |
| 7.C319 | KR1 Link Partner Auto-negotiation Extended Next Page Advertisement Word 1 | 157 |
| 7.C31A | KR1 Link Partner Auto-negotiation Extended Next Page Advertisement Word 2 | 158 |
| 7.C31B | KR1 Link Partner Auto-negotiation Extended Next Page Advertisement Word 3 | 158 |
| 7.C400 | Auto-negotiation Vendor Provisioning 1 | 158 |
| 7.C410 | Auto-negotiation Reserved Vendor Provisioning 1 | 159 |
| 7.C800 | Auto-negotiation Vendor Status 1 | 159 |
| 7.C810 | Auto-negotiation Reserved Vendor Status 1 | 160 |
| 7.C811 | Auto-negotiation Reserved Vendor Status 2 | 161 |



Table 4-5 Registers Summary (Continued)

| Address | Name | Page |
|----------------------|---|------|
| 7.C812 | Auto-negotiation Reserved Vendor Status 3 | 161 |
| 7.C813 | Auto-negotiation Reserved Vendor Status 4 | 161 |
| 7.C814 | Auto-negotiation Reserved Vendor Status 5 | 161 |
| 7.CC00 | Auto-negotiation Transmit Vendor Alarms 1 | 161 |
| 7.CC01 | Auto-negotiation Transmit Vendor Alarms 2 | 162 |
| 7.D000 | Auto-negotiation Standard Interrupt Mask 1 | 162 |
| 7.D001 | Auto-negotiation Standard Interrupt Mask 2 | 162 |
| 7.D400 | Auto-negotiation Transmit Vendor Interrupt Mask 1 | 163 |
| 7.D401 | Auto-negotiation Transmit Vendor Interrupt Mask 2 | 163 |
| 7.D402 | Auto-negotiation Transmit Vendor Interrupt Mask 3 | 163 |
| 7.E820 | Auto-negotiation Receive Link Partner Status 1 | 163 |
| 7.E821 | Auto-negotiation Receive Link Partner Status 2 | 164 |
| 7.E822 | Auto-negotiation Receive Link Partner Status 3 | 164 |
| 7.E823 | Auto-negotiation Receive Link Partner Status 4 | 164 |
| 7.E830 | Auto-negotiation Receive Reserved Vendor Status 1 | 164 |
| 7.E831 | Auto-negotiation Receive Reserved Vendor Status 2 | 165 |
| 7.E832 | Auto-negotiation Receive Reserved Vendor Status 3 | 165 |
| 7.EC00 | Auto-negotiation Receive Vendor Alarms 1 | 165 |
| 7.EC01 | Auto-negotiation Receive Vendor Alarms 2 | 166 |
| 7.EC02 | Auto-negotiation Receive Vendor Alarms 3 | 166 |
| 7.EC03 | Auto-negotiation Receive Vendor Alarms 4 | 166 |
| 7.F400 | Auto-negotiation Receive Vendor Interrupt Mask 1 | 166 |
| 7.F401 | Auto-negotiation Receive Vendor Interrupt Mask 2 | 167 |
| 7.F402 | Auto-negotiation Receive Vendor Interrupt Mask 3 | 167 |
| 7.F403 | Auto-negotiation Receive Vendor Interrupt Mask 4 | 167 |
| 7.FC00 | Auto-negotiation Vendor Global Interrupt Flags 1 | 167 |
| GbE Registers | | |
| 1D.2 | GbE Standard Device Identifier 1 | 169 |
| 1D.3 | GbE Standard Device Identifier 2 | 169 |
| 1D.5 | GbE Standard Devices in Package 1 | 169 |
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4.6.2 Detailed Register Descriptions

4.6.2.1 PMA Registers

4.6.2.1.1 PMA Standard Control 1: Address 1.0

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------|--------|-----------|---------|---|
| Loopback | 0 | R/W PD | 0b | Enables the PMA Analog System Loopback. 0b = Normal operation. 1b = Enable loopback mode. Note: This is a processor intensive operation. Completion of this operation can be monitored via 1E.C831.F (refer to Section 4.6.2.6.83). Note: PMA loopback is not supported. |
| Reserved | 1 | RSV | | Reserved. Do not modify. |
| 10G Speed Selection [3:0] | 5:2 | ROS | 0x0 | 0000b = 10 GbE xxx1b = 10PASS-TS / 2BASE-TL xx1xb = Reserved x1xxb = Reserved 1xxxb = Reserved |
| Speed Selection MSB | 6 | R/W PD | 1b | Combination of bits {6,D}. 00b = 10 Mb/s 01b = 100 Mb/s 10b = 1000 Mb/s 11b = Speed set by Bits [5:2] |
| Reserved | A:7 | RSV | | Reserved. Do not modify. |
| Low Power | B | R/W PD | 0b | A 1b written to this register causes the PMA to enter low-power mode. If a global chip low-power state is desired, use 1E.0.B (refer to Section 4.6.2.6.1). 0b = Normal operation. 1b = Low-power mode. Note: This is a processor intensive operation. Completion of this operation can be monitored via 1E.C831.F (refer to Section 4.6.2.6.83). |
| Reserved | C | RSV | | Reserved. Do not modify. |
| Speed Selection LSB | D | R/W PD | 1b | Combination of bits {6,D}. 00b = 10 Mb/s 01b = 100 Mb/s 10b = 1000 Mb/s 11b = Speed set by Bits [5:2] |
| Reserved | E | RSV | | Reserved. Do not modify. |
| Reset | F | R/W SC | 1b | The reset bit is automatically cleared upon completion of the reset sequence by the microcontroller. 0b = Normal operation. 1b = PMA reset. This bit is set to 1b during reset. The reset is internally stretched by approximately 1.7 μ s. Therefore the MDIO or uP should allow for 1.7 μ s before writing any PMA registers after this bit is set. |



4.6.2.1.2 PMA Standard Status 1: Address 1.1

| Field Name | Bit(s) | Type | Default | Description |
|-------------------------|--------|------|---------|--|
| Reserved | 0 | RSV | | Reserved. Do not modify. |
| Low Power Ability | 1 | ROS | 1b | Indicates whether the PHY supports a low power mode. 0b = No low-power mode supported. 1b = PMA supports low-power mode. |
| PMA Receive Link Status | 2 | LL | | Status of the PMA receive link. 0b = Link lost since last read. 1b = Link up. Indicates the status of the PMA receive link. This is the latch version of 1.E800.0 (refer to Section 4.6.2.1.46). Note: This is latching low, so it can only be used to detect link drops, and not the current status of the link, without performing back-to-back reads. |
| Reserved | 6:3 | RSV | | Reserved. Do not modify. |
| Fault | 7 | RO | | Top-level fault indicator flag for the PMA. This bit is set if either of the two bits 1.8.B or 1.8.A are set (refer to Section 4.6.2.1.9). 0b = No fault detected. 1b = Fault condition detected. |
| Reserved | F:8 | RSV | | Reserved. Do not modify. |

4.6.2.1.3 PMA Standard Device Identifier 1: Address 1.2

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------|--------|------|---------|----------------------------|
| Device ID MSW [1F:10] | F:0 | RO | | Bits [31:16] of Device ID. |

4.6.2.1.4 PMA Standard Device Identifier 2: Address 1.3

| Field Name | Bit(s) | Type | Default | Description |
|---------------------|--------|------|---------|---------------------------|
| Device ID LSW [F:0] | F:0 | RO | | Bits [15:0] of Device ID. |

4.6.2.1.5 PMA Standard Speed Ability: Address 1.4

| Field Name | Bit(s) | Type | Default | Description |
|-------------------|--------|------|---------|---|
| PMA 10G Capable | 0 | ROS | 1b | Always set to 1b in the X557. 0b = PMA is not 10 GbE capable. 1b = PMA is 10 GbE capable. |
| 2BASE-TL Capable | 1 | ROS | 0b | Always set to 0b in the X557. 0b = PMA is not 2BASE-TL capable. 1b = PMA is 2BASE-TL capable. |
| 10PASS-TS Capable | 2 | ROS | 0b | Always set to 0b in the X557. 0b = PMA is not 10PASS-TS capable. 1b = PMA is 10PASS-TS capable. |



| Field Name | Bit(s) | Type | Default | Description |
|------------------|--------|------|---------|---|
| Reserved | 3 | RSV | | Reserved. Do not modify. |
| PMA 1G Capable | 4 | ROS | 1b | Always set to 1b in the X557. 0b = PMA is not 1 GbE capable. 1b = PMA is 1 GbE capable. |
| PMA 100M Capable | 5 | ROS | 1b | Always set to 1b in the X557. 0b = PMA is not 100 Mb/s capable. 1b = PMA is 100 Mb/s capable. |
| PMA 10M Capable | 6 | ROS | 0b | Always set to 0b in the X557. 0b = PMA is not 10 Mb/s capable. 1b = PMA is 10 Mb/s capable. |
| Reserved | F:7 | RSV | | Reserved. Do not modify. |

4.6.2.1.6 PMA Standard Devices in Package 1: Address 1.5

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------|--------|------|---------|--|
| Clause 22 Registers Present | 0 | ROS | 0b | Always set to 0b, as there are no Clause 22 registers in the X557. 0b = Clause 22 registers are not present in package. 1b = Clause 22 registers are present in package. |
| PMA Present | 1 | ROS | 1b | Always set to 1b, as there is PMA functionality in the X557. 0b = PMA is not present. 1b = PMA is present in package. |
| WIS Present | 2 | ROS | 0b | Always set to 0b, as there is no WIS functionality in the X557. 0b = WIS is not present in package. 1b = WIS is present in package. |
| PCS Present | 3 | ROS | 1b | Always set to 1b, as there is PCS functionality in the X557. 0b = PCS is not present in package. 1b = PCS is present in package. |
| PHY XS Present | 4 | ROS | 1b | Always set to 1b, as there is a PHY XS interface in the X557. 0b = PHY XS is not present in package. 1b = PHY XS is present in package. |
| DTE XS Present | 5 | ROS | 0b | Always set to 0b. 0b = DTE XS is not present in package. 1b = DTE XS is present in package. |
| TC Present | 6 | ROS | 0b | Always set to 0b, as there is no TC functionality in the X557. 0b = TC is not present in package. 1b = TC is present in package. |
| Auto-negotiation Present | 7 | ROS | 1b | Always set to 1b, as there is auto-negotiation in the X557. 0b = Auto-negotiation is not present in package. 1b = Auto-negotiation is present in package. |
| Reserved | F:8 | RSV | | Reserved. Do not modify. |



4.6.2.1.7 PMA Standard Devices in Package 2: Address 1.6

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------------|--------|------|---------|---|
| Reserved | C:0 | RSV | | Reserved. Do not modify. |
| Clause 22 Extension Present | D | ROS | 1b | Always set to 1b, as the X557 utilizes this device for the GbE registers. 0b = Clause 22 Extension is not present in package. 1b = Clause 22 Extension is present in package. |
| Vendor Specific Device #1 Present | E | ROS | 1b | Always set to 1b, as the X557 utilizes this device for the Global registers. 0b = Device #1 is not present in package. 1b = Device #1 is present in package. |
| Vendor Specific Device #2 Present | F | ROS | 1b | Always set to 1b, as the X557 utilizes this device for the DSP PMA registers. 0b = Device #2 is not present in package. 1b = Device #2 is present in package. |

4.6.2.1.8 PMA Standard Control 2: Address 1.7

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------|--------|------|---------|---|
| PMA Device Type [3:0] | 3:0 | ROS | 0x9 | Always set to 0x9, as the X557 is a 10GBASE-T device. 0000b = 10GBASE-CX4 PMA/PMD type 0001b = 10GBASE-EW PMA/PMD type 0010b = 10GBASE-LW PMA/PMD type 0011b = 10GBASE-SW PMA/PMD type 0100b = 10GBASE-LX4 PMA/PMD type 0101b = 10GBASE-ER PMA/PMD type 0110b = 10GBASE-LR PMA/PMD type 0111b = 10GBASE-SR PMA/PMD type 1000b = 10GBASE-LRM PMA/PMD type 1001b = 10GBASE-T PMA type 1010b = 10GBASE-KX4 PMA/PMD type 1011b = 10GBASE-KR PMA/PMD type 1100b = 1000BASE-T PMA/PMD type 1101b = 1000BASE-KX PMA/PMD type 1110b = 100BASE-TX PMA/PMD type 1111b = 10BASE-T PMA/PMD type |
| Reserved | F:4 | RSV | | Reserved. Do not modify. |

4.6.2.1.9 PMA Standard Status 2: Address 1.8

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------|--------|------|---------|---|
| PMA Loopback Ability | 0 | ROS | 1b | Always set to 1b, as the PMA in the X557 supports loopback. 0b = PMA does not support loopback. 1b = PMA supports loopback. |
| PMA 10GBASEEW Capable | 1 | ROS | 0b | Always set to 0b, as the PMA in the X557 only supports 10GBASE-T. 0b = PMA does not support 10GBASE-EW. 1b = PMA supports 10GBASE-EW. |
| PMA 10GBASELW Capable | 2 | ROS | 0b | Always set to 0b, as the PMA in the X557 only supports 10GBASE-T. 0b = PMA does not support 10GBASE-LW. 1b = PMA supports 10GBASE-LW. |



| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------|--------|------|---------|--|
| PMA 10GBASESW Capable | 3 | ROS | 0b | Always set to 0b, as the PMA in the X557 only supports 10GBASE-T. 0b = PMA does not support 10GBASE-SW. 1b = PMA supports 10GBASE-SW. |
| PMA 10GBASELX4 Capable | 4 | ROS | 0b | Always set to 0b, as the PMA in the X557 only supports 10GBASE-T. 0b = PMA does not support 10GBASE-LX4. 1b = PMA supports 10GBASE-LX4. |
| PMA 10GBASEER Capable | 5 | ROS | 0b | Always set to 0b, as the PMA in the X557 only supports 10GBASE-T. 0b = PMA does not support 10GBASE-ER. 1b = PMA supports 10GBASE-ER. |
| PMA 10GBASELR Capable | 6 | ROS | 0b | Always set to 0b, as the PMA in the X557 only supports 10GBASE-T. 0b = PMA does not support 10GBASE-LR. 1b = PMA supports 10GBASE-LR. |
| PMA 10GBASESR Capable | 7 | ROS | 0b | Always set to 0b, as the PMA in the X557 only supports 10GBASE-T. 0b = PMA does not support 10GBASE-SR. 1b = PMA supports 10GBASE-SR. |
| PMD Transmit Disable Ability | 8 | ROS | 1b | Indicates whether the PMD has the capability of disabling its transmitter. 0b = PMD does not have the capability of disabling the transmitter. 1b = PMD has the capability of disabling the transmitter. This field is always set to 1b, as the PMD in the X557 has this ability. |
| Extended Abilities | 9 | ROS | 1b | Always set to 1b, as the PMA in the X557 has extended abilities. 0b = PMA does not have extended abilities. 1b = PMA has extended abilities. |
| Receive Fault | A | LH | | Indicates whether there is a fault somewhere along the receive path. 0b = No fault condition on receive path. 1b = Fault condition on receive path. This is a hardware fault and should never occur during normal operation. |
| Transmit Fault | B | LH | | Indicates whether there is a fault somewhere along the transmit path. 0b = No fault condition on transmit path. 1b = Fault condition on transmit path. This is a hardware fault and should never occur during normal operation. |
| Receive Fault Location Ability | C | ROS | 1b | Indicates whether the PMA has the ability to locate faults along the receive path. 0b = PMA does not have the capability to detect a fault condition on the receive path. 1b = PMA has the capability to detect a fault condition on the receive path. |
| Transmit Fault Location Ability | D | ROS | 1b | Indicates whether the PMA has the ability to locate faults along the transmit path. 0b = PMA does not have the capability to detect a fault condition on the transmit path. 1b = PMA has the capability to detect a fault condition on the transmit path. |
| Device Present [1:0] | F:E | ROS | 10b | Always set to 10b, as the PMA is present in the X557. 00b = No device at this address. 01b = No device at this address. 10b = Device present at this address. 11b = No device at this address. |



4.6.2.1.10 PMD Standard Transmit Disable Control: Address 1.9

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------------|--------|--------|---------|--|
| PMD Global Transmit Disable | 0 | R/W PD | 0b | When set, this bit disables (and overrides) all four channels, and sets the average launch power on all pairs to less than -53 dBm. 0b = Normal operation. 1b = Disable output on all channels. Note: This is a processor intensive operation. Completion of this operation can be monitored via 1E.C831.F (refer to Section 4.6.2.6.83). |
| PMD Channel 0 Transmit Disable | 1 | R/W PD | 0b | When disabled, the average launch power on a pair is set to less than -53 dBm. 0b = Normal operation. 1b = Disable output on transmit channel 0. Note: This is a processor intensive operation. Completion of this operation can be monitored via 1E.C831.F (refer to Section 4.6.2.6.83). |
| PMD Channel 1 Transmit Disable | 2 | R/W PD | 0b | When disabled, the average launch power on a pair is set to less than -53 dBm. 0b = Normal operation. 1b = Disable output on transmit channel 1. Note: This is a processor intensive operation. Completion of this operation can be monitored via 1E.C831.F (refer to Section 4.6.2.6.83). |
| PMD Channel 2 Transmit Disable | 3 | R/W PD | 0b | When disabled, the average launch power on a pair is set to less than -53 dBm. 0b = Normal operation. 1b = Disable output on transmit channel 2. Note: This is a processor intensive operation. Completion of this operation can be monitored via 1E.C831.F (refer to Section 4.6.2.6.83). |
| PMD Channel 3 Transmit Disable | 4 | R/W PD | 0b | When disabled, the average launch power on a pair is set to less than -53 dBm. 0b = Normal operation. 1b = Disable output on transmit channel 3. Note: This is a processor intensive operation. Completion of this operation can be monitored via 1E.C831.F (refer to Section 4.6.2.6.83). |
| Reserved | F:5 | RSV | | Reserved. Do not modify. |

4.6.2.1.11 PMD Standard Signal Detect: Address 1.A

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------|--------|------|---------|---|
| PMD Global Signal Detect | 0 | RO | | This bit is marked when all required, valid Ethernet signals to create a connection are present on the line. 0b = No signal detected. 1b = Signals detected on all required channels. |
| PMD Channel 0 Signal Detect | 1 | RO | | This bit is used to indicate the presence of signals on a given pair. A signal is defined as an auto-negotiation pulse or Ethernet signals. 0b = No signal detected. 1b = Signal detected on receive channel 0. |
| PMD Channel 1 Signal Detect | 2 | RO | | This bit is used to indicate the presence of signals on a given pair. A signal is defined as an auto-negotiation pulse or Ethernet signals. 0b = No signal detected. 1b = Signal detected on receive channel 1. |
| PMD Channel 2 Signal Detect | 3 | RO | | This bit is used to indicate the presence of signals on a given pair. A signal is defined as an auto-negotiation pulse or Ethernet signals. 0b = No signal detected. 1b = Signal detected on receive channel 2. |



| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------|--------|------|---------|---|
| PMD Channel 3 Signal Detect | 4 | RO | | This bit is used to indicate the presence of signals on a given pair. A signal is defined as an auto-negotiation pulse or Ethernet signals. 0b = No signal detected. 1b = Signal detected on receive channel 3. |
| Reserved | F:5 | RSV | | Reserved. Do not modify. |

4.6.2.1.12 PMD Standard 10G Extended Ability Register: Address 1.B

| Field Name | Bit(s) | Type | Default | Description |
|-------------------------|--------|------|---------|--|
| PMA 10GBASECX4 Capable | 0 | ROS | 0b | Always set to 0b, as the PMA in the X557 does not support 10GBASE-CX4. 0b = PMA incapable of 10GBASE-CX4. 1b = PMA capable of 10GBASE-CX4. |
| PMA 10GBASELRM Capable | 1 | ROS | 0b | Always set to 0b, as the PMA in the X557 does not support 10GBASE-LRM. 0b = PMA incapable of 10GBASE-LRM. 1b = PMA capable of 10GBASE-LRM. |
| PMA 10GBASET Capable | 2 | ROS | 1b | Always set to 1b, as the PMA in the X557 supports 10BASE-T. 0b = PMA incapable of 10BASE-T. 1b = PMA capable of 10BASE-T. |
| PMA 10GBASEKX4 Capable | 3 | ROS | 1b | Always set to 1b, as the PMA in the X557 supports 10BASE-KX4. 0b = PMA incapable of 10BASE-KX4. 1b = PMA capable of 10BASE-KX4. |
| PMA 10GBASEKR Capable | 4 | ROS | 1b | Always set to 1b, as the PMA in the X557 supports 10BASE-KR. 0b = PMA incapable of 10BASE-KR. 1b = PMA capable of 10BASE-KR. |
| PMA 1000BASE-T Capable | 5 | ROS | 1b | Always set to 1b, as the PMA in the X557 supports 1000BASE-T. 0b = PMA incapable of 1000BASE-T. 1b = PMA capable of 1000BASE-T. |
| PMA 1000BASE-KX Capable | 6 | ROS | 1b | Always set to 1b, as the PMA in the X557 supports 1000BASE-KX. 0b = PMA incapable of 1000BASE-KX. 1b = PMA capable of 1000BASE-KX. |
| PMA 100BASETX Capable | 7 | ROS | 1b | Always set to 1b, as the PMA in the X557 supports 100BASE-TX. 0b = PMA incapable of 100BASE-TX. 1b = PMA capable of 100BASE-TX. |
| PMA 10BASE-T Capable | 8 | ROS | 0b | Always set to 0b, as the PMA in the X557 does not support 10BASE-TX. 0b = PMA incapable of 10BASE-T. 1b = PMA capable of 10BASE-T. |
| Reserved | F:9 | RSV | | Reserved. Do not modify. |

4.6.2.1.13 PMA Standard Package Identifier 1: Address 1.E

| Field Name | Bit(s) | Type | Default | Description |
|------------------------|--------|------|---------|-----------------------------|
| Package ID MSW [1F:10] | F:0 | RO | | Bits [31:16] of Package ID. |



4.6.2.1.14 PMA Standard Package Identifier 2: Address 1.F

| Field Name | Bit(s) | Type | Default | Description |
|----------------------|--------|------|---------|----------------------------|
| Package ID LSW [F:0] | F:0 | RO | | Bits [15:0] of Package ID. |

4.6.2.1.15 PMA 10GBASE-T Status: Address 1.81

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------------|--------|------|---------|--|
| Link Partner Information Valid | 0 | RO | | When set, this bit indicates that the startup protocol (55.4.2.5) has completed. 0b = 10GBASE-T Link Partner information is not valid. 1b = 10GBASE-T Link Partner information is valid. |
| Reserved | F:1 | RSV | | Reserved. Do not modify. |

4.6.2.1.16 PMA 10GBASE-T Pair Swap and Polarity Status: Address 1.82

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------------|--------|------|---------|--|
| MDI / MD-X Connection State [1:0] | 1:0 | RO | | Indicates the current status of pair swaps at the MDI/MD-X. 00b = Pair A / B and C / D crossover. 01b = Pair C / D crossover. 10b = Pair A / B crossover. 11b = No crossover. |
| Reserved | 7:2 | RSV | | Reserved. Do not modify. |
| Pair Polarity [3:0] | B:8 | RO | | When set, this bit indicates that the wires on the respective pair are reversed. 0b = Polarity of Pair is normal. 1b = Polarity of Pair is reversed. Where: [0] = Pair A Polarity [1] = Pair B Polarity [2] = Pair C Polarity [3] = Pair D Polarity |
| Reserved | F:C | RSV | | Reserved. Do not modify. |

4.6.2.1.17 PMA 10GBASE-T Tx Power Back-off and Short Reach Setting: Address 1.83

| Field Name | Bit(s) | Type | Default | Description |
|------------------|--------|--------|---------|--|
| Short Reach Mode | 0 | R/W PD | 0b | When set, this bit places the PMA into short-reach mode. 0b = PMA is in normal operation. 1b = Set PMA to operate in short-reach mode. |
| Reserved | 9:1 | RSV | | Reserved. Do not modify. |



| Field Name | Bit(s) | Type | Default | Description |
|-------------------------------------|--------|------|---------|--|
| Tx Power Backoff [2:0] | C:A | RO | | The power back-off of the PMA. 000b = 0 dB 001b = 2 dB 010b = 4 dB 011b = 6 dB 100b = 8 dB 101b = 10 dB 110b = 12 dB 111b = 14 dB |
| Link Partner Tx Power Backoff [2:0] | F:D | RO | | The power back-off of the link partner. 000b = 0 dB 001b = 2 dB 010b = 4 dB 011b = 6 dB 100b = 8 dB 101b = 10 dB 110b = 12 dB 111b = 14 dB |

4.6.2.1.18 PMA 10GBASE-T Test Modes: Address 1.84

| Field Name | Bit(s) | Type | Default | Description |
|------------------------------------|--------|--------|---------|---|
| Reserved | 9:0 | RSV | | Reserved. Do not modify. |
| Transmitter Test Frequencies [2:0] | C:A | R/W PD | 000b | The test frequencies associated with Test Mode #4 in [F:D]. 000b = Reserved 001b = Dual Tone #1 010b = Dual Tone #2 011b = Reserved 100b = Dual Tone #3 101b = Dual Tone #4 110b = Dual Tone #5 111b = Reserved |
| Test Mode Control [2:0] | F:D | R/W PD | 000b | Test mode control for the PMA as defined in Section 55.5.2 of 802.3an. 000b = Normal operation. 001b = Master source for slave mode jitter test. 010b = Master mode jitter test. 011b = Slave mode jitter test. 100b = Transmitter distortion test. 101b = PSD and power level test. 110b = Transmitter Droop test. 111b = Pseudo random test mode for BER Monitor. Note: This is a processor intensive operation. Completion of this operation can be monitored via 1E.C831.F (refer to Section 4.6.2.6.83). |



4.6.2.1.19 PMA 10GBASE-T SNR Operating Margin Channel A: Address 1.85

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------------|--------|------|---------|---|
| Channel A Operating Margin [F:0] | F:0 | RO | | Operating margin (dB) of Channel A. The excess SNR that is enjoyed by the channel, over and above the minimum SNR required to operate at a BER of 10^{-12} . It is reported with 0.1 dB of resolution to an accuracy of 0.5 dB within the range of -12.7 dB to 12.7 dB. The number is in offset binary, with 0.0 dB represented by 0x8000. |

4.6.2.1.20 PMA 10GBASE-T SNR Operating Margin Channel B: Address 1.86

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------------|--------|------|---------|---|
| Channel B Operating Margin [F:0] | F:0 | RO | | Operating margin (dB) of Channel B. The excess SNR that is enjoyed by the channel, over and above the minimum SNR required to operate at a BER of 10^{-12} . It is reported with 0.1 dB of resolution to an accuracy of 0.5 dB within the range of -12.7 dB to 12.7 dB. The number is in offset binary, with 0.0 dB represented by 0x8000. |

4.6.2.1.21 PMA 10GBASE-T SNR Operating Margin Channel C: Address 1.87

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------------|--------|------|---------|---|
| Channel C Operating Margin [F:0] | F:0 | RO | | Operating margin (dB) of Channel C. The excess SNR that is enjoyed by the channel, over and above the minimum SNR required to operate at a BER of 10^{-12} . It is reported with 0.1 dB of resolution to an accuracy of 0.5 dB within the range of -12.7 dB to 12.7 dB. The number is in offset binary, with 0.0 dB represented by 0x8000. |

4.6.2.1.22 PMA 10GBASE-T SNR Operating Margin Channel D: Address 1.88

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------------|--------|------|---------|---|
| Channel D Operating Margin [F:0] | F:0 | RO | | Operating margin (dB) of Channel D. The excess SNR that is enjoyed by the channel, over and above the minimum SNR required to operate at a BER of 10^{-12} . It is reported with 0.1 dB of resolution to an accuracy of 0.5 dB within the range of -12.7 dB to 12.7 dB. The number is in offset binary, with 0.0 dB represented by 0x8000. |



4.6.2.1.23 PMA 10GBASE-T SNR Minimum Operating Margin Channel A: Address 1.89

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|--|
| Channel A Minimum Operating Margin [F:0] | F:0 | RO | | Minimum operating margin (dB) of Channel A since last link up. The excess SNR that is enjoyed by the channel, over and above the minimum SNR required to operate at a BER of 10^{-12} . It is reported with 0.1 dB of resolution to an accuracy of 0.5 dB within the range of -12.7 dB to 12.7 dB. The number is in offset binary, with 0.0 dB represented by 0x8000. |

4.6.2.1.24 PMA 10GBASE-T SNR Minimum Operating Margin Channel B: Address 1.8A

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|--|
| Channel B Minimum Operating Margin [F:0] | F:0 | RO | | Minimum operating margin (dB) of Channel B since last link up. The excess SNR that is enjoyed by the channel, over and above the minimum SNR required to operate at a BER of 10^{-12} . It is reported with 0.1 dB of resolution to an accuracy of 0.5 dB within the range of -12.7 dB to 12.7 dB. The number is in offset binary, with 0.0 dB represented by 0x8000. |

4.6.2.1.25 PMA 10GBASE-T SNR Minimum Operating Margin Channel C: Address 1.8B

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|--|
| Channel C Minimum Operating Margin [F:0] | F:0 | RO | | Minimum operating margin (dB) of Channel C since last link up. The excess SNR that is enjoyed by the channel, over and above the minimum SNR required to operate at a BER of 10^{-12} . It is reported with 0.1 dB of resolution to an accuracy of 0.5 dB within the range of -12.7 dB to 12.7 dB. The number is in offset binary, with 0.0 dB represented by 0x8000. |

4.6.2.1.26 PMA 10GBASE-T SNR Minimum Operating Margin Channel D: Address 1.8C

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|--|
| Channel D Minimum Operating Margin [F:0] | F:0 | RO | | Minimum operating margin (dB) of Channel D since last link up. The excess SNR that is enjoyed by the channel, over and above the minimum SNR required to operate at a BER of 10^{-12} . It is reported with 0.1 dB of resolution to an accuracy of 0.5 dB within the range of -12.7 dB to 12.7 dB. The number is in offset binary, with 0.0 dB represented by 0x8000. |



4.6.2.1.27 PMA 10GBASE-T Receive Signal Power Channel A: Address 1.8D

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------------|--------|------|---------|---|
| Channel A Received Signal Power [F:0] | F:0 | RO | | Received signal power (dBm) for Channel A. The received signal power on the channel. It is reported with 0.1 dB of resolution to an accuracy of 0.5 dB within the range of -20.0 dB to +5.5dB. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000. |

4.6.2.1.28 PMA 10GBASE-T Receive Signal Power Channel B: Address 1.8E

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------------|--------|------|---------|---|
| Channel B Received Signal Power [F:0] | F:0 | RO | | Received signal power (dBm) for Channel B. The received signal power on the channel. It is reported with 0.1 dB of resolution to an accuracy of 0.5 dB within the range of -20.0 dB to +5.5dB. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000. |

4.6.2.1.29 PMA 10GBASE-T Receive Signal Power Channel C: Address 1.8F

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------------|--------|------|---------|---|
| Channel C Received Signal Power [F:0] | F:0 | RO | | Received signal power (dBm) for Channel C. The received signal power on the channel. It is reported with 0.1 dB of resolution to an accuracy of 0.5 dB within the range of -20.0 dB to +5.5dB. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000. |

4.6.2.1.30 PMA 10GBASE-T Receive Signal Power Channel D: Address 1.90

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------------|--------|------|---------|---|
| Channel D Received Signal Power [F:0] | F:0 | RO | | Received signal power (dBm) for Channel D. The received signal power on the channel. It is reported with 0.1 dB of resolution to an accuracy of 0.5 dB within the range of -20.0 dB to +5.5dB. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000. |



4.6.2.1.31 PMA 10GBASE-T Skew Delay 1: Address 1.91

| Field Name | Bit(s) | Type | Default | Description |
|--------------------|--------|------|---------|--|
| Reserved | 7:0 | RSV | | Reserved. Do not modify. |
| Skew Delay B [6:0] | E:8 | RO | | Skew delay for pair B. The skew delay reports the current skew delay on each of the pair with respect to physical pair A. It is reported with 1.25 ns resolution to an accuracy of 2.5 ns. The number is in two's complement notation with positive values representing delay and negative values representing advance with respect to physical pair A. If the delay exceed the maximum amount that can be represented by the range (-80 ns to +78.75 ns), the field displays the maximum respective value. |
| Reserved | F | RSV | | Reserved. Do not modify. |

4.6.2.1.32 PMA 10GBASE-T Skew Delay 2: Address 1.92

| Field Name | Bit(s) | Type | Default | Description |
|--------------------|--------|------|---------|--|
| Skew Delay C [6:0] | 6:0 | RO | | Skew delay for pair C. The skew delay reports the current skew delay on each of the pair with respect to physical pair A. It is reported with 1.25 ns resolution to an accuracy of 2.5 ns. The number is in two's complement notation with positive values representing delay and negative values representing advance with respect to physical pair A. If the delay exceed the maximum amount that can be represented by the range (-80 ns to +78.75 ns), the field displays the maximum respective value. |
| Reserved | 7 | RSV | | Reserved. Do not modify. |
| Skew Delay D [6:0] | E:8 | RO | | Skew delay for pair D. The skew delay reports the current skew delay on each of the pair with respect to physical pair A. It is reported with 1.25 ns resolution to an accuracy of 2.5 ns. The number is in two's complement notation with positive values representing delay and negative values representing advance with respect to physical pair A. If the delay exceed the maximum amount that can be represented by the range (-80 ns to +78.75 ns), the field displays the maximum respective value. |
| Reserved | F | RSV | | Reserved. Do not modify. |

4.6.2.1.33 PMA 10GBASE-T Fast Retrain Status and Control: Address 1.93

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------------|--------|------|---------|--|
| Fast Retrain Enable | 0 | R/W | 0b | 0b = Fast retrain capability is disabled. 1b = Fast retrain capability is enabled. |
| Fast Retrain Signal Type [1:0] | 2:1 | R/W | 00b | 00b = PHY signals IDLE during fast retrain. 01b = PHY signals Local Fault during fast retrain. 10b = PHY signals Link Interruption during fast retrain. 11b = Reserved. |
| Fast Retrain Negotiated | 3 | RO | | 0b = Fast retrain capability was not negotiated. 1b = Fast retrain capability was negotiated. |
| Fast Retrain Ability | 4 | RO | | 0b = Fast retrain capability is not supported. 1b = Fast retrain capability is supported. |
| Reserved | 5 | RSV | | Reserved. Do not modify. |



| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------|--------|------|---------|---|
| LD Fast Retrain Count [4:0] | A:6 | SCT | 0x00 | Counts the number of fast retrains requested by the local device. Saturating clear on read counter. |
| LP Fast Retrain Count [4:0] | F:B | SCT | 0x00 | Counts the number of fast retrains requested by the link partner. Saturating clear on read counter. |

4.6.2.1.34 PMA Transmit Reserved Vendor Provisioning 0: Address 1.C412

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|--------|---------|---|
| Tx Polarity Invert Enable [3:0] | 3:0 | R/W | 0x0 | Bit 0 corresponds to Lane A, Bit 1 to Lane B, and so on. 1b = Invert corresponding Tx lane |
| Reserved Spare Transmit Provisioning 0 [9:0] | D:4 | R/W PD | 0x000 | Reserved for future use |
| Test Mode Rate [1:0] | F:E | R/W PD | 00b | This field controls the data rate for the test mode activated with register 1.84 (refer to Section 4.6.2.1.18). 00b = 10 GbE Test Mode All other values are reserved. |

4.6.2.1.35 PMA Transmit Reserved Vendor Provisioning 1: Address 1.C413

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|--------|---------|--|
| Incremental Tx PSD Target [7:0] | 7:0 | R/W PD | 0x00 | Deviation from the current TX PSD target based on registers A.A and A.B in 2's complement form s7. |
| Reserved Spare Transmit Provisioning 1 [3:0] | B:8 | R/W PD | 0x0 | Reserved for future use. |
| Channel Mask [3:0] | F:C | R/W PD | 0x0 | Channel mask specifying which channels are affected by the TX PSD target. |

4.6.2.1.36 PMA Transmit Vendor Alarms 1: Address 1.CC00

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |

4.6.2.1.37 PMA Transmit Vendor Alarms 2: Address 1.CC01

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |



4.6.2.1.38 PMA Transmit Vendor Alarms 3: Address 1.CC02

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------------------|--------|------|---------|---|
| Reset Complete | 0 | LH | | This bit is a mirror of 1E.CC00.6 (refer to Section 4.6.2.6.94), but has associated with it a known zero bit that can be used to ascertain that H/W reset has completed, enabling Reset Complete to be read in one shot without double-polling and dealing with tristate MDIO issues. It avoids the problem of not knowing if/when the H/W complete phase of a reset has occurred when double-polling 1b = Hardware and Firmware reset has completed. |
| Zero | 1 | ROS | 0b | Used to provide a guaranteed zero location in the same register as Reset Complete. Defined as 0. |
| Reserved PMA Transmit Alarms 3 [D:0] | F:2 | LH | | Reserved for internal use. |

4.6.2.1.39 PMA Transmit Standard Interrupt Mask 1: Address 1.D000

| Field Name | Bit(s) | Type | Default | Description |
|------------------------------|--------|--------|---------|--|
| Reserved | 1:0 | RSV | | Reserved. Do not modify. |
| PMA Receive Link Status Mask | 2 | R/W PD | 0b | Mask for Bit 1.1.2 (refer to Section 4.6.2.1.2). 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | F:3 | RSV | | Reserved. Do not modify. |

4.6.2.1.40 PMA Transmit Standard Interrupt Mask 2: Address 1.D001

| Field Name | Bit(s) | Type | Default | Description |
|---------------------|--------|--------|---------|---|
| Reserved | 9:0 | RSV | | Reserved. Do not modify. |
| Receive Fault Mask | A | R/W PD | 0b | Bit 1.8.A (refer to Section 4.6.2.1.9). 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Transmit Fault Mask | B | R/W PD | 0b | Bit 1.8.B (refer to Section 4.6.2.1.9). 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | F:C | RSV | | Reserved. Do not modify. |

4.6.2.1.41 PMA Transmit Vendor LASI Interrupt Mask 1: Address 1.D400

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |



4.6.2.1.42 PMA Transmit Vendor LASI Interrupt Mask 2: Address 1.D401

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |

4.6.2.1.43 PMA Transmit Vendor LASI Interrupt Mask 3: Address 1.D402

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |

4.6.2.1.44 PMA Transmit Vendor Debug 1: Address 1.D800

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------|--------|--------|---------|--|
| Reserved | E:0 | RSV | | Reserved. Do not modify. |
| PMA Digital System Loopback | F | R/W PD | 0b | 1b = Enable PMA digital system loopback. |

4.6.2.1.45 PMA Receive Reserved Vendor Provisioning 1: Address 1.E400

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------|--------|--------|---------|--|
| MDI Configuration | 0 | R/W PD | 0b | <p>The setting of this bit determines whether the MDI is reversed or not.</p> <p>Note: The reversal does not change pair polarity (i.e., A+ maps to D+, etc.).</p> <p>The value of this bit is set during auto-negotiation to the value of the MDI_CFG pin unless the Force MDI Configuration bit (1.E400.1) is asserted. When the Force MDI Configuration bit is asserted the MDI_CFG pin is ignored and this bit is unchanged from its default or provisioned value.</p> <p>If this bit is changed manually after auto-negotiation completes, auto-negotiation must be restarted to achieve the desired MDI configuration.</p> <p>0b = MDI Normal (ABCD -> ABCD) 1b = MDI Reversed (ABCD -> DCBA)</p> |
| Force MDI Configuration | 1 | R/W PD | 0b | <p>Normally the MDI reversal configuration is taken from the MDI_CFG pin. If the Force MDI Configuration bit is asserted, the MDI_CFG pin is ignored and the current provisioned value of the MDI configuration bit is used instead.</p> <p>0b = Set MDI Configuration based on state of MDI_CFG. 1b = Ignore state of MDI_CFG pin.</p> |
| Enable Intel Fast Retrain | 2 | R/W PD | 0b | <p>If the link partner is an Intel PHY and also has Fast Retrain enabled, use a special retrain sequence to bring the link back up without going back through the auto-negotiation sequence.</p> <p>0b = Disable PMA Fast Link Retrain. 1b = Enable PMA Fast Link Retrain.</p> |



| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------------|--------|--------|---------|--|
| Reserved Receive Provisioning 1 [B:0] | E:3 | R/W PD | 0x000 | Reserved for future use. |
| External PHY Loopback | F | R/W PD | 0b | External PHY loopback expects a loopback connector such that Pair A is connected to Pair B, and Pair C is connected to Pair D. 0b = Normal operation. 1b = Enable external PHY loopback. This is a processor intensive operation. Completion of this operation can be monitored via 1E.C831.F (refer to Section 4.6.2.6.83). |

4.6.2.1.46 PMA Receive Vendor State 1: Address 1.E800

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------|--------|------|---------|--|
| PMA Receive Link Current Status | 0 | RO | | This is the current state of 1.1.2 (refer to Section 4.6.2.1.2). 1b = Rx link good |
| Reserved | F:1 | RSV | | Reserved. Do not modify. |

4.6.2.1.47 PMA Receive Reserved Vendor State 1: Address 1.E810

| Field Name | Bit(s) | Type | Default | Description |
|------------------------------------|--------|------|---------|--|
| Accumulated Fast Retrain Time[F:0] | F:0 | RO | | Accumulated time in milliseconds spent in fast retrain since the last auto-negotiation sequence. This is a saturating register. |

4.6.2.1.48 PMA Receive Reserved Vendor State 2: Address 1.E811

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|--|
| Total Number Of RFI Training Link Recovery Events Since Last AutoNeg [7:0] | 7:0 | RO | | The count of the cumulative number of RFI Training Link Recovery Events since last auto-negotiation. This register is automatically reset to 0 during auto-negotiation. The result is reported modulo 256 (wrap around). |
| Total Number Of Link Recovery Events Since Last AutoNeg [7:0] | F:8 | RO | | The count of the cumulative number of Link Recovery Events since last auto-negotiation. This register is automatically reset to 0 during auto-negotiation. It increments once for each series of back-to-back Fast Retrain events. The result is reported modulo 256 (wrap around). |

4.6.2.1.49 PMA Vendor Global Interrupt Flags 1: Address 1.FC00

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------|--------|------|---------|---|
| Reserved | 9:0 | RSV | | Reserved. Do not modify. |
| Standard Alarm 2 Interrupt | A | RO | | An interrupt was generated from either bit 1.8.B or 1.8.A. An interrupt was generated from status register (Section 4.6.2.1.9, "PMA Standard Status 2: Address 1.8") and the corresponding mask register (Section 4.6.2.1.40, "PMA Transmit Standard Interrupt Mask 2: Address 1.D001"). |



| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------------|--------|------|---------|---|
| Standard Alarm 1 Interrupt | B | RO | | An interrupt was generated from bit 1.1.2. An interrupt was generated from status register (Section 4.6.2.1.2, "PMA Standard Status 1: Address 1.1") and the corresponding mask register (Section 4.6.2.1.39, "PMA Transmit Standard Interrupt Mask 1: Address 1.D000"). |
| Reserved | C | RSV | | Reserved. Do not modify. |
| Vendor Specific Tx Alarms 3 Interrupt | D | RO | | An interrupt was generated from status register (Section 4.6.2.1.38, "PMA Transmit Vendor Alarms 3: Address 1.CC02") and the corresponding mask register (Section 4.6.2.1.43, "PMA Transmit Vendor LASI Interrupt Mask 3: Address 1.D402"). 1b = Interrupt |
| Vendor Specific Tx Alarms 2 Interrupt | E | RO | | An interrupt was generated from status register (Section 4.6.2.1.37, "PMA Transmit Vendor Alarms 2: Address 1.CC01") and the corresponding mask register (Section 4.6.2.1.42, "PMA Transmit Vendor LASI Interrupt Mask 2: Address 1.D401"). 1b = Interrupt |
| Vendor Specific Tx Alarms 1 Interrupt | F | RO | | An interrupt was generated from status register (Section 4.6.2.1.36, "PMA Transmit Vendor Alarms 1: Address 1.CC00") and the corresponding mask register (Section 4.6.2.1.41, "PMA Transmit Vendor LASI Interrupt Mask 1: Address 1.D400"). 1b = Interrupt |



4.6.2.2 PCS Registers

4.6.2.2.1 PCS Standard Control 1: Address 3.0

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------|--------|-----------|---------|--|
| Reserved | 1:0 | RSV | | Reserved. Do not modify. |
| 10G Speed Selection [3:0] | 5:2 | R/W PD | 0x0 | 0000b = 10 GbE xxx1b = 10PASS-TS / 2BASE-TL xx1xb = Reserved x1xxb = Reserved 1xxxb = Reserved |
| Speed Selection MSB | 6 | R/W PD | 1b | Combination of bits {6,D}. 00b = 10 Mb/s 01b = 100 Mb/s 10b = 1000 Mb/s 11b = Speed set by Bits [5:2] |
| Reserved | 9:7 | RSV | | Reserved. Do not modify. |
| Clock Stop Enable | A | R/W PD | 0b | 0b = Clock not stoppable. 1b = The PHY may stop the clock during LPI. |
| Low Power | B | R/W PD | 0b | A one written to this register causes the PCS to enter low-power mode. If a global chip low-power state is desired, use 1E.0.B (refer to Section 4.6.2.6.1). 0b = Normal operation. 1b = Low-power mode. Note: This is a processor intensive operation. Completion of this operation can be monitored via 1E.C831.F (refer to Section 4.6.2.6.83). |
| Reserved | C | RSV | | Reserved. Do not modify. |
| Speed Selection LSB | D | R/W PD | 1b | Combination of bits {6,D}. 00b = 10 Mb/s 01b = 100 Mb/s 10b = 1000 Mb/s 11b = Speed set by Bits [5:2] |
| Loopback | E | R/W PD | 0b | Enables the PCS DSQ System Loopback. 0b = Normal operation. 1b = Enable loopback mode. Note: This is a processor intensive operation. Completion of this operation can be monitored via 1E.C831.F (refer to Section 4.6.2.6.83). Note: PCS loopback is not supported. |
| Reset | F | R/W SC | 1b | Resets the entire PHY. 0b = Normal operation 1b = PCS reset The reset bit is automatically cleared upon completion of the reset sequence by the microcontroller. This bit is set to 1b during reset. The reset is internally stretched by approximately 1.7 μ s. Therefore the MDIO or uP should allow for 1.7 μ s before writing any PCS registers after this bit is set. |



4.6.2.2.2 PCS Standard Status 1: Address 3.1

| Field Name | Bit(s) | Type | Default | Description |
|-------------------------|--------|------|---------|---|
| Reserved | 0 | RSV | | Reserved. Do not modify. |
| Reserved | 1 | ROS | 1b | Reserved. Do not modify. |
| PCS Receive Link Status | 2 | LL | | Indicates the status of the PCS receive link. 0b = Link lost since last read. 1b = Link up. This is a latching low version of Bit 3.20.C (refer to Section 4.6.2.2.14). |
| Reserved | 5:3 | RSV | | Reserved. Do not modify. |
| Clock Stop Capable | 6 | ROS | 0b | 0b = Clock not stoppable. 1b = The MAC may stop the clock during LPI. |
| Fault | 7 | RO | | The top-level fault indicator flag for the PCS block, 0b = No fault detected. 1b = Fault condition detected. This bit is set if either of the two bits 3.8.B or 3.8.A are set (refer to Section 4.6.2.2.9). |
| Rx LPI Indication | 8 | RO | | 0b = Rx PCS is not currently receiving LPI. 1b = Rx PCS is currently receiving LPI. |
| Tx LPI Indication | 9 | RO | | 0b = Tx PCS is not currently receiving LPI. 1b = Tx PCS is currently receiving LPI. |
| Rx LPI Received | A | LH | | 0b = LPI not received. 1b = Rx PCS has received LPI. |
| Tx LPI Received | B | LH | | 0b = LPI not received. 1b = Tx PCS has received LPI. |
| Reserved | F:C | RSV | | Reserved. Do not modify. |

4.6.2.2.3 PCS Standard Device Identifier 1: Address 3.2

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------|--------|------|---------|----------------------------|
| Device ID MSW [1F:10] | F:0 | RO | | Bits [31:16] of Device ID. |

4.6.2.2.4 PCS Standard Device Identifier 2: Address 3.3

| Field Name | Bit(s) | Type | Default | Description |
|---------------------|--------|------|---------|---------------------------|
| Device ID LSW [F:0] | F:0 | RO | | Bits [15:0] of Device ID. |

4.6.2.2.5 PCS Standard Speed Ability: Address 3.4

| Field Name | Bit(s) | Type | Default | Description |
|-------------|--------|------|---------|---|
| 10G Capable | 0 | ROS | 1b | This is always set to 1b in the X557. 0b = PCS is not 10 Gb/s capable. 1b = PCS is 10 Gb/s capable. |



| Field Name | Bit(s) | Type | Default | Description |
|------------------------------|--------|------|---------|---|
| 10PASS-TS / 2BASE-TL Capable | 1 | ROS | 0b | This is always set to 0b in the X557. 0b = PCS is not 10PASS-TS / 2BASE-TL capable. 1b = PCS is 10PASS-TS / 2BASE-TL capable. |
| Reserved | F:2 | RSV | | Reserved. Do not modify. |

4.6.2.2.6 PCS Standard Devices in Package 1: Address 3.5

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------|--------|------|---------|--|
| Clause 22 Registers Present | 0 | ROS | 0b | Always set to 0b, as there are no Clause 22 registers in the X557. 0b = Clause 22 registers are not present in package. 1b = Clause 22 registers are present in package. |
| PMA Present | 1 | ROS | 1b | Always set to 1b, as there is PMA functionality in the X557. 0b = PMA is not present. 1b = PMA is present in package. |
| WIS Present | 2 | ROS | 0b | Always set to 0b, as there is no WIS functionality in the X557. 0b = WIS is not present in package. 1b = WIS is present in package. |
| PCS Present | 3 | ROS | 1b | Always set to 1b, as there is PCS functionality in the X557. 0b = PCS is not present in package. 1b = PCS is present in package. |
| PHY XS Present | 4 | ROS | 1b | Always set to 1b, as there is a PHY XS interface in the X557. 0b = PHY XS is not present in package. 1b = PHY XS is present in package. |
| DTE XS Present | 5 | ROS | 0b | Always set to 0b. 0b = DTE XS is not present in package. 1b = DTE XS is present in package. |
| TC Present | 6 | ROS | 0b | Always set to 0b, as there is no TC functionality in the X557. 0b = TC is not present in package. 1b = TC is present in package. |
| Auto-negotiation Present | 7 | ROS | 1b | Always set to 1b, as there is auto-negotiation in the X557. 0b = Auto-negotiation is not present in package. 1b = Auto-negotiation is present in package. |
| Reserved | F:8 | RSV | | Reserved. Do not modify. |

4.6.2.2.7 PCS Standard Devices in Package 2: Address 3.6

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------|--------|------|---------|---|
| Reserved | C:0 | RSV | | Reserved. Do not modify. |
| Clause 22 Extension Present | D | ROS | 1b | Always set to 1b, as the X557 utilizes this device for the GbE registers. 0b = Clause 22 Extension is not present in package. 1b = Clause 22 Extension is present in package. |



| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------------|--------|------|---------|---|
| Vendor Specific Device #1 Present | E | ROS | 1b | Always set to 1b, as the X557 utilizes this device for the Global registers. 0b = Device #1 is not present in package. 1b = Device #1 is present in package. |
| Vendor Specific Device #2 Present | F | ROS | 1b | Always set to 1b, as the X557 utilizes this device for the DSP PMA registers. 0b = Device #2 is not present in package. 1b = Device #2 is present in package. |

4.6.2.2.8 PCS Standard Control 2: Address 3.7

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------|--------|--------|---------|--|
| PCS Device Type [1:0] | 1:0 | R/W PD | 11b | 00b = 10GBASE-R 01b = 10GBASE-X 10b = 10GBASE-W 11b = 10GBASE-T |
| Reserved | F:2 | RSV | | Reserved. Do not modify. |

4.6.2.2.9 PCS Standard Status 2: Address 3.8

| Field Name | Bit(s) | Type | Default | Description |
|-------------------|--------|------|---------|--|
| 10GBASE-R capable | 0 | ROS | 1b | Always set to 1b, as the PCS in the AQR205 only supports 10GBASE-T and 10GBASE-R. 0b = PCS does not support 10GBASE-R. 1b = PCS supports 10GBASE-R PCS type. |
| 10GBASE-X capable | 1 | ROS | 0b | Always set to 0b, as the PCS in the X557 only supports 10GBASE-T and 10GBASE-R. 0b = PCS does not support 10GBASE-X. 1b = PCS supports 10GBASE-X PCS type. |
| 10GBASE-W capable | 2 | ROS | 0b | Always set to 0b, as the PCS in the X557 only supports 10GBASE-T and 10GBASE-R. 0b = PCS does not support 10GBASE-W. 1b = PCS supports 10GBASE-W PCS type. |
| 10GBASE-T capable | 3 | ROS | 1b | Always set to 1b, as the PCS in the X557 only supports 10GBASE-T and 10GBASE-R. 0b = PCS does not support 10GBASE-T. 1b = PCS supports 10GBASE-T PCS type. |
| Reserved | 9:4 | RSV | | Reserved. Do not modify. |
| Receive Fault | A | LH | | Indicates whether there is a fault somewhere along the receive path. This bit is duplicated at 3.EC04.2 (refer to Section 4.6.2.2.115). |
| Transmit Fault | B | LH | | Indicates whether there is a fault somewhere along the transmit path. This bit is duplicated at 3.CC01.0 (refer to Section 4.6.2.2.59). 0b = No fault condition on transmit path. 1b = Fault condition on transmit path. |
| Reserved | D:C | RSV | | Reserved. Do not modify. |



| Field Name | Bit(s) | Type | Default | Description |
|----------------------|--------|------|---------|---|
| Device Present [1:0] | F:E | ROS | 10b | Always set to 10b, as the PCS registers reside here in the X557. 00b = No device at this address. 01b = No device at this address. 10b = Device present at this address. 11v = No device at this address. |

4.6.2.2.10 PCS Standard Package Identifier 1: Address 3.E

| Field Name | Bit(s) | Type | Default | Description |
|------------------------|--------|------|---------|-----------------------------|
| Package ID MSW [1F:10] | F:0 | RO | | Bits [31:16] of Package ID. |

4.6.2.2.11 PCS Standard Package Identifier 2: Address 3.F

| Field Name | Bit(s) | Type | Default | Description |
|----------------------|--------|------|---------|----------------------------|
| Package ID LSW [F:0] | F:0 | RO | | Bits [15:0] of Package ID. |

4.6.2.2.12 PCS EEE Capability Register: Address 3.14

| Field Name | Bit(s) | Type | Default | Description |
|-----------------|--------|------|---------|--|
| Reserved | 0 | RSV | | Reserved. Do not modify. |
| 100BASE-TX EEE | 1 | ROS | 0b | 0b = Do not advertise that the 100BASETX has EEE capability. 1b = Advertise that the 100BASE-TX has EEE capability. |
| 1000BASE-T EEE | 2 | ROS | 1b | 0b = Do not advertise that the 1000BASET has EEE capability. 1b = Advertise that the 1000BASE-T has EEE capability. |
| 10GBASE-T EEE | 3 | ROS | 1b | 0b = Do not advertise that the 10GBASET has EEE capability. 1b = Advertise that the 10GBASE-T has EEE capability. |
| 1000BASE-KX EEE | 4 | ROS | 1b | 0b = Do not advertise that the 1000BASEKX has EEE capability. 1b = Advertise that the 1000BASE-KX has EEE capability. |
| 10GBASE-KX4 EEE | 5 | ROS | 1b | 0b = Do not advertise that the 10GBASEKX4 has EEE capability. 1b = Advertise that the 10GBASE-KX4 has EEE capability. |
| 10GBASE-KR EEE | 6 | ROS | 1b | 0b = Do not advertise that the 10GBASEKR has EEE capability. 1b = Advertise that the 10GBASE-KR has EEE capability. |
| Reserved | F:7 | RSV | | Reserved. Do not modify. |

4.6.2.2.13 PCS EEE Wake Error Counter: Address 3.16

| Field Name | Bit(s) | Type | Default | Description |
|------------------------------|--------|------|---------|---|
| EEE Wake Error Counter [F:0] | F:0 | SCT | 0x0000 | This register is a 16-bit saturating clear on read counter. The wake error source is configured with 1E.C4A1.A:8. The default wake error source is from the RPL. |



4.6.2.2.14 PCS 10G Status 1: Address 3.20

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|---|
| 10G PCS Block Lock | 0 | RO | | When set, this bit indicates that 10 GbE PCS Framer has acquired frame synchronization and is locked. The interrupt for this bit is at 3.21.F (refer to Section 4.6.2.2.15). |
| 10G High BER | 1 | RO | | When set, this bit indicates a high BER is being seen at the PCS. 0b = PCS is reporting a BER $f^{-fn}10^{-4}$ 1b = PCS is reporting a BER $d 10^{-4}$ The interrupt for this bit is at 3.21.E (Section 4.6.2.2.15). The status bit for medium BER is found in 1E.CC01 (refer to Section 4.6.2.6.95). |
| 10GBASE-R PRBS31 Pattern Testing Ability | 2 | ROS | 1b | 0b = PCS is not able to support PRBS31 pattern testing on KR Interface. 1b = PCS is able to support PRBS31 pattern testing on KR Interface. |
| 10GBASE-R PRBS9 Pattern Testing Ability | 3 | ROS | 1b | 0b = PCS is not able to support PRBS9 pattern testing on KR Interface. 1b = PCS is able to support PRBS9 pattern testing on KR Interface. |
| Reserved | B:4 | RSV | | Reserved. Do not modify. |
| 10G Receive Link Status | C | RO | | When set, this bit indicates that the 10 GbE Receive Link is functioning properly. 0b = 10 GbE Receive Link Down 1b = 10 GbE Receive Link Up This is a non-latching version of bit 3.1.2 (refer to Section 4.6.2.2.2). The Receive Link is up when the Block Lock status is asserted and the High BER is deasserted. |
| Reserved | F:D | RSV | | Reserved. Do not modify. |

4.6.2.2.15 PCS 10G Status 2: Address 3.21

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------|--------|------|---------|---|
| Errored Block Counter [7:0] | 7:0 | SCT | 0x00 | A saturating count of the number of times a bad 65B block is received. Clear on read. In 10GBASE-T mode, this is taken from the state machine in Figure 55.16 in the 10GBASE-T specification. |
| Errored Frame Counter [5:0] | D:8 | SCT | 0x00 | A saturating count of the number of times a bad LDPC frame is received. Clear on read. In 10GBASE-T mode, this is taken from the state machine in Figure 55.14 in the 10GBASE-T specification. |
| High BER Latched | E | LH | | When set, this bit indicates a high BER is being seen at the PCS. This is the interrupt for bit 3.20.1 (refer to Section 4.6.2.2.14). |
| PCS Block Lock Latched | F | LL | | When set, this bit indicates that 10 GbE PCS Framer has acquired frame synchronization and is locked. 0b = 10GBASE-T PCS Framer is not locked. 1b = 10GBASE-T PCS Framer is Locked. This is the interrupt for bit 3.20.0 (refer to Section 4.6.2.2.14). |

4.6.2.2.16 PCS 10GBASE-R Test Pattern Seed A 1: Address 3.22

| Field Name | Bit(s) | Type | Default | Description |
|-------------------------------------|--------|--------|---------|-----------------------------------|
| Test Pattern Seed A Bits 15:0 [F:0] | F:0 | R/W PD | 0x0000 | Test pattern seed A, Bits [15:0]. |



4.6.2.2.17 PCS 10GBASE-R Test Pattern Seed A 2: Address 3.23

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|-----------|---------|------------------------------------|
| Test Pattern Seed A Bits 31:16 [1F:10] | F:0 | R/W PD | 0x0000 | Test pattern seed A, Bits [31:16]. |

4.6.2.2.18 PCS 10GBASE-R Test Pattern Seed A 3: Address 3.24

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|-----------|---------|------------------------------------|
| Test Pattern Seed A Bits 47:32 [2F:20] | F:0 | R/W PD | 0x0000 | Test pattern seed A, Bits [47:32]. |

4.6.2.2.19 PCS 10GBASE-R Test Pattern Seed A 4: Address 3.25

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|-----------|---------|------------------------------------|
| Test Pattern Seed A Bits 57:48 [39:30] | 9:0 | R/W PD | 0x0000 | Test pattern seed A, Bits [57:48]. |
| Reserved | F:A | RSV | | Reserved. Do not modify. |

4.6.2.2.20 PCS 10GBASE-R Test Pattern Seed B 1: Address 3.26

| Field Name | Bit(s) | Type | Default | Description |
|-------------------------------------|--------|-----------|---------|-----------------------------------|
| Test Pattern Seed B Bits 15:0 [F:0] | F:0 | R/W PD | 0x0000 | Test pattern seed B, Bits [15:0]. |

4.6.2.2.21 PCS 10GBASE-R Test Pattern Seed B 2: Address 3.27

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|-----------|---------|------------------------------------|
| Test Pattern Seed B Bits 31:16 [1F:10] | F:0 | R/W PD | 0x0000 | Test pattern seed B, Bits [31:16]. |

4.6.2.2.22 PCS 10GBASE-R Test Pattern Seed B 3: Address 3.28

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|-----------|---------|------------------------------------|
| Test Pattern Seed B Bits 47:32 [2F:20] | F:0 | R/W PD | 0x0000 | Test pattern seed B, Bits [47:32]. |



4.6.2.2.23 PCS 10GBASE-R Test Pattern Seed B 4: Address 3.29

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|--------|---------|------------------------------------|
| Test Pattern Seed B Bits 57:48 [39:30] | 9:0 | R/W PD | 0x000 | Test pattern seed B, Bits [57:48]. |
| Reserved | F:A | RSV | | Reserved. Do not modify. |

4.6.2.2.24 PCS 10GBASE-R PCS Test-Pattern Control: Address 3.2A

| Field Name | Bit(s) | Type | Default | Description |
|-------------------------------------|--------|--------|---------|--|
| Data Pattern Select | 0 | R/W PD | 0b | 0b = LF data pattern. 1b = Zeros data pattern. |
| Test-Pattern Select | 1 | R/W PD | 0b | 0b = Pseudo random test pattern. 1b = Square wave test pattern. |
| Receive Test-Pattern Enable | 2 | R/W PD | 0b | 0b = Disable receive test-pattern testing. 1b = Enable receive test-pattern testing. |
| Transmit Test-Pattern Enable | 3 | R/W PD | 0b | 0b = Disable transmit test pattern. 1b = Enable transmit test pattern. |
| PRBS31 Transmit Test-Pattern Enable | 4 | R/W PD | 0b | 0b = Enable PRBS31 test-pattern mode on the transmit path. 1b = Enable PRBS31 test-pattern mode on the transmit path. |
| PRBS31 Receive Test-Pattern Enable | 5 | R/W PD | 0b | 0b = Enable PRBS31 test-pattern mode on the receive path. 1b = Enable PRBS31 test-pattern mode on the receive path. |
| PRBS9 Transmit Test-Pattern Enable | 6 | R/W PD | 0b | 0b = Disable PRBS9 test-pattern mode on the transmit path. 1b = Enable PRBS9 test-pattern mode on the transmit path. |
| Reserved | F:7 | RSV | | Reserved. Do not modify. |

4.6.2.2.25 PCS 10GBASE-R PCS Test-Pattern Error Counter: Address 3.2B

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------------|--------|--------|---------|----------------|
| Test-Pattern Error Counter [F:0] | F:0 | R/W PD | 0x0000 | Error Counter. |

4.6.2.2.26 PCS Transmit Vendor Provisioning 1: Address 3.C400

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------|--------|--------|---------|--|
| PCS Tx Auxiliary Bit Value | 0 | R/W PD | 0b | The value that is set in the auxiliary bit of the PCS transmission frame. This bit is currently undefined in the 802.3an standard. |
| Reserved | F:1 | RSV | | Reserved. Do not modify. |



4.6.2.2.27 PCS Transmit Vendor Provisioning 2: Address 3.C401

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |

4.6.2.2.28 PCS Transmit Reserved Vendor Provisioning 1: Address 3.C410

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|--------|---------|--|
| PCS IEEE Loopback Passthrough Disable | 0 | R/W PD | 0b | When set, this bit disables the output of the PHY when IEEE loopback is set. 1b = Disable data passthrough on IEEE loopback. |
| Reserved Transmit Provisioning 1 [F:1] | F:1 | R/W PD | 0x0000 | Reserved for future use |

4.6.2.2.29 PCS Transmit XFI Vendor Provisioning 1: Address 3.C455

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------------------|--------|------|---------|--|
| XFI Test Pattern Seed A Word 0 [F:0] | F:0 | R/W | 0x0000 | XFI test pattern seed A, Bits [15:0]. 10GBASE-R Test Pattern Seed A. Used for both XFI0 and XFI1. |

4.6.2.2.30 PCS Transmit XFI Vendor Provisioning 2: Address 3.C456

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------------------|--------|------|---------|---|
| XFI Test Pattern Seed A Word 1 [F:0] | F:0 | R/W | 0x0000 | XFI test pattern seed A, Bits [31:16]. 10GBASE-R Test Pattern Seed A. Used for both XFI0 and XFI1. |

4.6.2.2.31 PCS Transmit XFI Vendor Provisioning 3: Address 3.C457

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------------------|--------|------|---------|---|
| XFI Test Pattern Seed A Word 2 [F:0] | F:0 | R/W | 0x0000 | XFI test pattern seed A, Bits [47:32]. 10GBASE-R Test Pattern Seed A. Used for both XFI0 and XFI1. |



4.6.2.2.32 PCS Transmit XFI Vendor Provisioning 4: Address 3.C458

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------------------|--------|------|---------|---|
| XFI Test Pattern Seed A Word 3 [9:0] | 9:0 | R/W | 0x000 | XFI test pattern seed A, Bits [57:48]. 10GBASE-R Test Pattern Seed A. Used for both XF10 and XF11. |
| Reserved | F:A | RSV | | Reserved. Do not modify. |

4.6.2.2.33 PCS Transmit XFI Vendor Provisioning 5: Address 3.C459

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------------------|--------|------|---------|--|
| XFI Test Pattern Seed B Word 0 [F:0] | F:0 | R/W | 0x0000 | XFI test pattern seed B, Bits [15:0]. 10GBASE-R Test Pattern Seed B. Used for both XF10 and XF11. |

4.6.2.2.34 PCS Transmit XFI Vendor Provisioning 6: Address 3.C45A

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------------------|--------|------|---------|---|
| XFI Test Pattern Seed B Word 1 [F:0] | F:0 | R/W | 0x0000 | XFI test pattern seed B, Bits [31:16]. 10GBASE-R Test Pattern Seed B. Used for both XF10 and XF11. |

4.6.2.2.35 PCS Transmit XFI Vendor Provisioning 7: Address 3.C45B

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------------------|--------|------|---------|---|
| XFI Test Pattern Seed B Word 2 [F:0] | F:0 | R/W | 0x0000 | XFI test pattern seed B, Bits [47:32]. 10GBASE-R Test Pattern Seed B. Used for both XF10 and XF11. |

4.6.2.2.36 PCS Transmit XFI Vendor Provisioning 8: Address 3.C45C

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------------------|--------|------|---------|---|
| XFI Test Pattern Seed B Word 3 [9:0] | 9:0 | R/W | 0x000 | XFI test pattern seed B, Bits [57:48]. 10GBASE-R Test Pattern Seed B. Used for both XF10 and XF11. |
| Reserved | F:A | RSV | | Reserved. Do not modify. |



4.6.2.2.37 PCS Transmit XFIO Vendor Provisioning 1: Address 3.C460

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------|--------|--------|---------|---|
| Reserved | 0 | RSV | | Reserved. Do not modify. |
| XFIO PCS Scrambler Disable | 1 | R/W PD | 0b | PCS Scrambler Disable. 1b = Disable PCS scrambler. |
| Reserved | F:2 | RSV | | Reserved. Do not modify. |

4.6.2.2.38 PCS Transmit XFIO Vendor Provisioning 2: Address 3.C461

| Field Name | Bit(s) | Type | Default | Description |
|-------------------------------------|--------|------|---------|--|
| XFIO PCS Loss Of Lock Inject | 0 | R/W | 0b | Inject error to cause loss of block_lock at far end. 1b = Inject loss of lock |
| XFIO PCS High BER Inject | 1 | R/W | 0b | Inject error to cause HI_BER at far-end. 1b = Inject PCS High BER. |
| XFIO Inject Single Error | 2 | R/W | 0b | Inject single error on the 10GBASE-R Test Pattern including pseudo-random, PRB31 or PRBS9. 1b = Inject single error. |
| XFIO Local Fault Inject | 3 | R/W | 0b | Inject Local_Fault. 1b = Inject local fault. |
| XFIO Test Pattern Enable | 4 | R/W | 0b | 10GBASE-R Pseudo-Random Test Pattern Enable. 0b = Disable 1b = Enable |
| XFIO Test PRBS-31 Enable | 5 | R/W | 0b | 10GBASE-R PRBS 31 Test Pattern Enable. 0b = Disable 1b = Enable Note: This is a processor intensive operation. Completion of this operation can be monitored via 1E.C831.F (refer to Section 4.6.2.6.83). |
| XFIO Test PRBS-9 Enable | 6 | R/W | 0b | 10GBASE-R PRBS 9 Test Pattern Enable 0b = Disable 1b = Enable Note: This is a processor intensive operation. Completion of this operation can be monitored via 1E.C831.F (refer to Section 4.6.2.6.83). |
| XFIO Test Mode Select | 7 | R/W | 0b | 10GBASE-R Test Pattern Select. 0b = Pseudo-random 1b = Square wave |
| XFIO Test Data Select | 8 | R/W | 0b | 10GBASE-R Data Pattern Select. 0b = LF 1b = Zero |
| XFIO Test Square Wave Test Duration | 9 | R/W | 0b | 10GBASE-R Square Wave Test Duration. Repeating pattern of n ones, followed by n zeros, where n = 6 or 11. 0b = 6 ones followed by 6 zeros. 1b = 11 ones followed by 11 zeros. |
| Reserved | F:A | RSV | | Reserved. Do not modify. |



4.6.2.2.39 PCS Transmit XFI 1 Vendor Provisioning 1: Address 3.C470

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------|--------|-----------|---------|--|
| Reserved | 0 | RSV | | Reserved. Do not modify. |
| XFI1 PCS Scrambler Disable | 1 | R/W PD | 0b | PCS Scrambler Disable. 1b = Disable PCS scrambler |
| Reserved | F:2 | RSV | | Reserved. Do not modify. |

4.6.2.2.40 PCS Transmit XFI 1 Vendor Provisioning 2: Address 3.C471

| Field Name | Bit(s) | Type | Default | Description |
|-------------------------------------|--------|------|---------|--|
| XFI0 PCS Loss Of Lock Inject | 0 | R/W | 0b | Inject error to cause loss of block_lock at far end. 1b = Inject loss of lock |
| XFI0 PCS High BER Inject | 1 | R/W | 0b | Inject error to cause HI_BER at far-end. 1b = Inject PCS High BER. |
| XFI0 Inject Single Error | 2 | R/W | 0b | Inject single error on the 10GBASE-R Test Pattern including pseudo-random, PRB31 or PRBS9. 1b = Inject single error. |
| XFI0 Local Fault Inject | 3 | R/W | 0b | Inject Local_Fault. 1b = Inject local fault. |
| XFI0 Test Pattern Enable | 4 | R/W | 0b | 10GBASE-R Pseudo-Random Test Pattern Enable. 0b = Disable 1b = Enable |
| XFI0 Test PRBS-31 Enable | 5 | R/W | 0b | 10GBASE-R PRBS 31 Test Pattern Enable. 0b = Disable 1b = Enable Note: This is a processor intensive operation. Completion of this operation can be monitored via 1E.C831.F (refer to Section 4.6.2.6.83). |
| XFI0 Test PRBS-9 Enable | 6 | R/W | 0b | 10GBASE-R PRBS 9 Test Pattern Enable 0b = Disable 1b = Enable Note: This is a processor intensive operation. Completion of this operation can be monitored via 1E.C831.F (refer to Section 4.6.2.6.83). |
| XFI0 Test Mode Select | 7 | R/W | 0b | 10GBASE-R Test Pattern Select. 0b = Pseudo-random 1b = Square wave |
| XFI0 Test Data Select | 8 | R/W | 0b | 10GBASE-R Data Pattern Select. 0b = LF 1b = Zero |
| XFI0 Test Square Wave Test Duration | 9 | R/W | 0b | 10GBASE-R Square Wave Test Duration. Repeating pattern of n ones, followed by n zeros, where n = 6 or 11. 0b = 6 ones followed by 6 zeros. 1b = 11 ones followed by 11 zeros. |
| Reserved | F:A | RSV | | Reserved. Do not modify. |



4.6.2.2.41 PCS Transmit Vendor FCS No Error Frame Counter 1: Address 3.C820

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|--|
| 10GBASE-T Good Frame Counter LSW [F:0] | F:0 | SCTL | 0x0000 | 10GBASE-T Good Frame Counter LSW. Counts Ethernet good frames (i.e., no Ethernet CRC-3/FCS errors). |

4.6.2.2.42 PCS Transmit Vendor FCS No Error Frame Counter 2: Address 3.C821

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|--|
| 10GBASE-T Good Frame Counter MSW [19:10] | 9:0 | SCTM | 0x000 | 10GBASE-T Good Frame Counter MSW. Counts Ethernet good frames (i.e., no Ethernet CRC-3/FCS errors). |
| Reserved | F:A | RSV | | Reserved. Do not modify. |

4.6.2.2.43 PCS Transmit Vendor FCS Error Frame Counter 1: Address 3.C822

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|---|
| 10GBASE-T Error Frame Counter LSW [F:0] | F:0 | SCTL | 0x0000 | 10GBASE-T Bad Frame Counter LSW. Counts Ethernet bad frames (i.e., no Ethernet CRC-32/FCS errors). |

4.6.2.2.44 PCS Transmit Vendor FCS Error Frame Counter 2: Address 3.C823

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|---|
| 10GBASE-T Error Frame Counter MSW [19:10] | 9:0 | SCTM | 0x000 | 10GBASE-T Bad Frame Counter MSW. Counts Ethernet bad frames (i.e., no Ethernet CRC-32/FCS errors). |
| Reserved | F:A | RSV | | Reserved. Do not modify. |

4.6.2.2.45 PCS Transmit XFIO Vendor State 1: Address 3.C860

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------------|--------|------|---------|--|
| XFIO Good Frame Counter LSW [F:0] | F:0 | SCTL | 0x0000 | XFIO Good Frame Counter LSW. Counts Ethernet good frames (i.e., no Ethernet CRC-32/FCS errors). |



4.6.2.2.46 PCS Transmit XFIO Vendor State 2: Address 3.C861

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------------|--------|------|---------|--|
| XFIO Good Frame Counter MSW [9:0] | 9:0 | SCTM | 0x000 | XFIO Good Frame Counter MSW. Counts Ethernet good frames (i.e., no Ethernet CRC-32/FCS errors). |
| Reserved | F:A | RSV | | Reserved. Do not modify. |

4.6.2.2.47 PCS Transmit XFIO Vendor State 3: Address 3.C862

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------------|--------|------|---------|---|
| XFIO Bad Frame Counter LSW [F:0] | F:0 | SCTL | 0x0000 | XFIO Bad Frame Counter LSW. Counts Ethernet bad frames (i.e., Ethernet CRC-32/FCS errors). |

4.6.2.2.48 PCS Transmit XFIO Vendor State 4: Address 3.C863

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------------|--------|------|---------|---|
| XFIO Bad Frame Counter MSW [9:0] | 9:0 | SCTM | 0x000 | XFIO Bad Frame Counter MSW. Counts Ethernet bad frames (i.e., Ethernet CRC-32/FCS errors). |
| Reserved | F:A | RSV | | Reserved. Do not modify. |

4.6.2.2.49 PCS Transmit XFI 1 Vendor State 1: Address 3.C870

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------------|--------|------|---------|--|
| XFI1 Good Frame Counter LSW [F:0] | F:0 | STCL | 0x0000 | XFI1 Good Frame Counter LSW. Counts Ethernet good frames (i.e., no Ethernet CRC-32/FCS errors). |

4.6.2.2.50 PCS Transmit XFI 1 Vendor State 2: Address 3.C871

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------------|--------|------|---------|--|
| XFI1 Good Frame Counter MSW [9:0] | 9:0 | STCM | 0x000 | XFI1 Good Frame Counter MSW. Counts Ethernet good frames (i.e., no Ethernet CRC-32/FCS errors). |
| Reserved | F:A | RSV | | Reserved. Do not modify. |

4.6.2.2.51 PCS Transmit XFI 1 Vendor State 3: Address 3.C872

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------------|--------|------|---------|--|
| XFI1 Bad Frame Counter LSW [F:0] | F:0 | SCTL | 0x0000 | XFI1 Bad Frame Counter LSW. Counts Ethernet bad frames (i.e. Ethernet CRC-32/FCS errors). |



4.6.2.2.52 PCS Transmit XFI 1 Vendor State 4: Address 3.C873

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------------|--------|------|---------|---|
| XFI1 Bad Frame Counter MSW [9:0] | 9:0 | SCTM | 0x000 | XFI1 Bad Frame Counter MSW. Counts Ethernet bad frames (i.e. Ethernet CRC-32/FCS errors). |
| Reserved | F:A | RSV | | Reserved. Do not modify. |

4.6.2.2.53 PCS Transmit XGS Vendor State 1: Address 3.C880

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------------------|--------|------|---------|--|
| XGS Collision Events Counter 0 [7:0] | 7:0 | SCT | 0x00 | 1 GbE/100 Mb/s PHY collision events: Byte location from 1 to 64 counter. |
| Reserved | F:8 | RSV | | Reserved. Do not modify. |

4.6.2.2.54 PCS Transmit XGS Vendor State 2: Address 3.C881

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------------------|--------|------|---------|---|
| XGS Collision Events Counter 1 [7:0] | 7:0 | SCT | 0x00 | 1 GbE/100 Mb/s PHY collision events: Byte location from 65 to 96 counter. |
| Reserved | F:8 | RSV | | Reserved. Do not modify. |

4.6.2.2.55 PCS Transmit XGS Vendor State 3: Address 3.C882

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------------------|--------|------|---------|--|
| XGS Collision Events Counter 2 [7:0] | 7:0 | SCT | 0x00 | 1 GbE/100 Mb/s PHY collision events: Byte location from 97 to 128 counter. |
| Reserved | F:8 | RSV | | Reserved. Do not modify. |

4.6.2.2.56 PCS Transmit XGS Vendor State 4: Address 3.C883

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------------------|--------|------|---------|---|
| XGS Collision Events Counter 3 [7:0] | 7:0 | SCT | 0x00 | 1 GbE/100 Mb/s PHY collision events: Byte location from 129 to 192 counter. |
| Reserved | F:8 | RSV | | Reserved. Do not modify. |

4.6.2.2.57 PCS Transmit XGS Vendor State 5: Address 3.C884

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------------------|--------|------|---------|---|
| XGS Collision Events Counter 4 [7:0] | 7:0 | SCT | 0x00 | 1 GbE/100 Mb/s PHY collision events: Byte location from 193 to 320 counter. |
| Reserved | F:8 | RSV | | Reserved. Do not modify. |



4.6.2.2.58 PCS Transmit Vendor Alarms 1: Address 3.CC00

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|--------------------------|
| Reserved | 0 | LH | | Reserved for future use. |
| Reserved PCS Transmit Vendor Alarms 1 [F:1] | F:1 | LH | | Reserved for future use. |

4.6.2.2.59 PCS Transmit Vendor Alarms 2: Address 3.CC01

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|--------------------------|
| Reserved PCS Transmit Vendor Alarms 2 [F:0] | F:0 | LH | | Reserved for future use. |

4.6.2.2.60 PCS Transmit Vendor Alarms 3: Address 3.CC02

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|--------------------------|
| Reserved PCS Transmit Vendor Alarms 3 [F:0] | F:0 | LH | | Reserved for future use. |

4.6.2.2.61 PCS Transmit Vendor Alarms 4: Address 3.CC03

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|---|
| XFI0 Transmit LOF Detected | 0 | LH | | 1b = Loss of Frame detected. |
| Reserved | 2:1 | RSV | | Reserved. Do not modify. |
| XFI0 Transmit 64B Encode Error | 3 | LH | | 1b = 64B Encode Error. |
| XFI0 Transmit Reserved XGMII Character Received | 4 | LH | | 1b = Reserved XGMII Character Received. |
| XFI0 Transmit Invalid XGMII Character Received | 5 | LH | | 1b = Invalid XGMII Character Received. |
| Reserved | 7:6 | RSV | | Reserved. Do not modify. |
| XFI1 Transmit LOF Detected | 8 | LH | | 1b = Loss of Frame detected. |
| Reserved | A:9 | RSV | | Reserved. Do not modify. |
| XFI1 Transmit 64B Encode Error | B | LH | | 1b = 64B Encode Error. |
| XFI1 Transmit Reserved XGMII Character Received | C | LH | | 1b = Reserved XGMII Character Received. |
| XFI1 Transmit Invalid XGMII Character Received | D | LH | | 1b = Invalid XGMII Character Received. |
| Reserved | F:E | RSV | | Reserved. Do not modify. |



4.6.2.2.62 PCS Standard Interrupt Mask 1: Address 3.D000

| Field Name | Bit(s) | Type | Default | Description |
|------------------------------|--------|--------|---------|---|
| Reserved | 1:0 | RSV | | Reserved. Do not modify. |
| PCS Receive Link Status Mask | 2 | R/W PD | 0b | Mask for Bit 3.1.2 (refer to Section 4.6.2.2.2). 0b = Disable interrupt generation. 1b = Enable interrupt generation. Note: This bit also shows up as Bit 3.20.C, but only as a status bit (refer to Section 4.6.2.2.14). |
| Reserved | 9:3 | RSV | | Reserved. Do not modify. |
| Rx LPI Received Mask | A | R/W PD | 0b | Mask for Bit 3.1.A (refer to Section 4.6.2.2.2). 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Tx LPI Received Mask | B | R/W PD | 0b | Mask for Bit 3.1.B (refer to Section 4.6.2.2.2). 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | F:C | RSV | | Reserved. Do not modify. |

4.6.2.2.63 PCS Standard Interrupt Mask 2: Address 3.D001

| Field Name | Bit(s) | Type | Default | Description |
|---------------------|--------|--------|---------|--|
| Reserved | 9:0 | RSV | | Reserved. Do not modify. |
| Receive Fault Mask | A | R/W PD | 0b | Mask for Bit 3.8.A (refer to Section 4.6.2.2.9). 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Transmit Fault Mask | B | R/W PD | 0b | Mask for Bit 3.8.B (refer to Section 4.6.2.2.9). 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | F:C | RSV | | Reserved. Do not modify. |

4.6.2.2.64 PCS Standard Interrupt Mask 3: Address 3.D002

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------------|--------|--------|---------|---|
| Reserved | D:0 | RSV | | Reserved. Do not modify. |
| 10GBASE-T High BER Latched Mask | E | R/W PD | 0b | When set, this bit indicates that 10GBASE-T PCS Framer has acquired frame synchronization and is locked. This is the interrupt for bit 3.21.F (refer to Section 4.6.2.2.15). 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| 10GBASE-T PCS Block Lock Latched Mask | F | R/W PD | 0b | When set, this bit indicates a high BER is being seen at the PCS. This is the interrupt for bit 3.21.E (refer to Section 4.6.2.2.15). 0b = Disable interrupt generation. 1b = Enable interrupt generation. |



4.6.2.2.65 PCS Transmit Vendor Interrupt Mask 1: Address 3.D400

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|--------|---------|---|
| Reserved | 0 | R/W PD | 0b | Reserved for future use. |
| Reserved PCS Transmit Vendor Alarms 1 Mask [F:1] | F:1 | R/W PD | 0x0000 | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |

4.6.2.2.66 PCS Transmit Vendor Interrupt Mask 2: Address 3.D401

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|--------|---------|---|
| Reserved PCS Transmit Vendor Alarms 2 Mask [F:0] | F:0 | R/W PD | 0x0000 | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |

4.6.2.2.67 PCS Transmit Vendor Interrupt Mask 3: Address 3.D402

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|--------|---------|---|
| Reserved PCS Transmit Vendor Alarms 3 Mask [F:0] | F:0 | R/W PD | 0x0000 | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |

4.6.2.2.68 PCS Transmit Vendor Interrupt Mask 4: Address 3.D403

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|--------|---------|---|
| Reserved | 2:0 | RSV | | Reserved. Do not modify. |
| XFI0 Transmit Encode 64B Error Mask | 3 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| XFI0 Transmit Reserved XGMII Character Error Mask | 4 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| XFI0 Transmit Invalid XGMII Character Error Mask | 5 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | A:6 | RSV | | Reserved. Do not modify. |
| XFI1 Transmit Encode 64B Error Mask | B | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| XFI1 Transmit Reserved XGMII Character Error Mask | C | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| XFI1 Transmit Invalid XGMII Character Error Mask | D | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | F:E | RSV | | Reserved. Do not modify. |



4.6.2.2.69 PCS Transmit Vendor Debug 1: Address 3.D800

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------|--------|-----------|---------|---|
| Reserved | C:0 | RSV | | Reserved. Do not modify. |
| PCS Tx Inject Frame Error | D | R/W | 0b | Setting this bit injects an error at the location contained in Bits [C:0] in the next PCS transmission frame. 1b = Inject frame error |
| PCS Tx Inject CRC Error | E | R/W | 0b | Setting this bit injects a CRC error in a single frame. 1b = Inject CRC error. |
| PCS Tx Scrambler Disable | F | R/W PD | 0b | Setting this bit disables the Tx scrambler during regular data transmission (i.e., scrambler functionality during training and startup is unmodified). 0b = Normal Operation. 1b = Tx Scrambler Disabled. |

4.6.2.2.70 PCS Receive Vendor Provisioning 1: Address 3.E400

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------------|--------|-----------|---------|---|
| PCS Rx Error LDPC Frame Enable | 0 | R/W PD | 1b | Error the entire LDPC frame payload upon uncorrectable LDPC parity or CRC error. 0b = Disable erroring the LDPC frame payload. 1b = Enable erroring the LDPC frame payload. |
| Reserved | F:1 | RSV | | Reserved. Do not modify. |

4.6.2.2.71 PCS Receive XFIO Provisioning 1: Address 3.E460

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------|--------|------|---------|---|
| Reserved | 0 | RSV | | Reserved. Do not modify. |
| XFIO Rx Descrambler Disable | 1 | R/W | 0b | PCS Descrambler Disable 1b = XFIO Disable PCS scrambler. |
| Reserved | F:2 | RSV | | Reserved. Do not modify. |

4.6.2.2.72 PCS Receive XFIO Provisioning 2: Address 3.E461

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------|--------|------|---------|---|
| Reserved | 2:0 | RSV | | Reserved. Do not modify. |
| XFIO Local Fault Inject | 3 | R/W | 0b | Inject Local_Fault. 1b = XFIO Inject local fault |
| XFIO Test Pattern Enable | 4 | R/W | 0b | 10GBASE-R Pseudo-Random Test Pattern Enable. 1b = XFIO Enable test pattern |



| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------|--------|------|---------|---|
| XFI0 Test Mode Select [2:0] | 7:5 | R/W | 000b | Test Pattern Select: 000b = Pseudo-random 100b = Square-wave x10b = PRBS-9 xx1b = PRBS-31 The source for the pseudo-random test is determined by Bit [8]. |
| XFI0 Test Data Source | 8 | R/W | 0b | XFI0 Data pattern select 0b = Local-fault (LF) input for pseudo-random test. 1b = All-zero input for pseudo-random test. This bit determines the source of the data for the pseudo-random test (selected by Bits [7:5]). |
| Reserved | F:9 | RSV | | Reserved. Do not modify. |

4.6.2.2.73 PCS Receive XFI 1 Provisioning 1: Address 3.E470

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------|--------|------|---------|--|
| Reserved | 0 | RSV | | Reserved. Do not modify. |
| XFI1 Rx Descrambler Disable | 1 | R/W | 0b | PCS Descrambler Disable. 1b = XFI1 Disable PCS scrambler. |
| Reserved | F:2 | RSV | | Reserved. Do not modify. |

4.6.2.2.74 PCS Receive XFI 1 Provisioning 2: Address 3.E471

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------|--------|------|---------|---|
| Reserved | 2:0 | RSV | | Reserved. Do not modify. |
| XFI1 Local Fault Inject | 3 | R/W | 0b | Inject Local_Fault. 1b = XFI0 Inject local fault |
| XFI1 Test Pattern Enable | 4 | R/W | 0b | 10GBASE-R Pseudo-Random Test Pattern Enable. 1b = XFI0 Enable test pattern |
| XFI1 Test Mode Select [2:0] | 7:5 | R/W | 000b | Test Pattern Select: 000b = Pseudo-random 100b = Square-wave x10b = PRBS-9 xx1b = PRBS-31 The source for the pseudo-random test is determined by Bit [8]. |
| XFI1 Test Data Source | 8 | R/W | 0b | XFI1 Data pattern select 0b = Local-fault (LF) input for pseudo-random test. 1b = All-zero input for pseudo-random test. This bit determines the source of the data for the pseudo-random test (selected by Bits [7:5]). |
| Reserved | F:9 | RSV | | Reserved. Do not modify. |



4.6.2.2.75 PCS Receive Vendor State 1: Address 3.E800

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------------|--------|------|---------|---|
| PCS Rx Current Value of Auxiliary Bit | 0 | RO | | The current value of the PCS Rx auxiliary bit. This value has a maskable interrupt associated with it in 3.EC00.0 (refer to Section 4.6.2.2.111). |
| Reserved | F:1 | RSV | | Reserved. Do not modify. |

4.6.2.2.76 PCS Receive Vendor CRC-8 Error Counter 1: Address 3.E810

| Field Name | Bit(s) | Type | Default | Description |
|-------------------------------|--------|------|---------|--|
| CRC-8 Error Counter LSW [F:0] | F:0 | SCTL | 0x0000 | Lower 16 bits of CRC-8 error counter. When the LSW is read, the MSW is copied to a shadow register, then both the LSW and MSW are cleared. The LSW of the counter must be read first. The MSW of the counter must be read immediately after the LSW is read. A saturating counter that counts the number of CRC-8 errors (but without LDPC frame parity error) has been detected on the received LDPC frame. |

4.6.2.2.77 PCS Receive Vendor CRC-8 Error Counter 2: Address 3.E811

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------|--------|------|---------|--|
| CRC-8 Error Counter MSW [15:10] | 5:0 | SCTM | 0x00 | Upper 6 bits of CRC-8 error counter. The MSW of the counter must be read immediately after the LSW of the counter is read. The MSW is actually a shadow copy of the MSW of the counter and is loaded after the LSW of the counter is read. A saturating counter that counts the number of CRC-8 errors (but without LDPC frame parity error) has been detected on the received LDPC frame. |
| Reserved | F:6 | RSV | | Reserved. Do not modify. |

4.6.2.2.78 PCS Receive Vendor FCS No Error Frame Counter 1: Address 3.E812

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|---|
| 10GBASE-T Good Frame Counter LSW [F:0] | F:0 | SCTL | 0x0000 | 10GBASE-T Good Frame Counter LSW. Counts Ethernet good frames (i.e., no Ethernet CRC-32/FCS errors). |

4.6.2.2.79 PCS Receive Vendor FCS No Error Frame Counter 2: Address 3.E813

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|---|
| 10GBASE-T Good Frame Counter MSW [19:10] | 9:0 | SCTM | 0x000 | 10GBASE-T Good Frame Counter MSW. Counts Ethernet good frames (i.e., no Ethernet CRC-32/FCS errors). |



| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:A | RSV | | Reserved. Do not modify. |

4.6.2.2.80 PCS Receive Vendor FCS Error Frame Counter 1: Address 3.E814

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|---|
| 10GBASE-T Error Frame Counter LSW [F:0] | F:0 | SCTL | 0x0000 | 10GBASE-T Bad Frame Counter LSW. Counts Ethernet bad frames (i.e., no Ethernet CRC-32/FCS errors). |

4.6.2.2.81 PCS Receive Vendor FCS Error Frame Counter 2: Address 3.E815

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|---|
| 10GBASE-T Error Frame Counter MSW [19:10] | 9:0 | SCTM | 0x0000 | 10GBASE-T Bad Frame Counter MSW. Counts Ethernet bad frames (i.e., no Ethernet CRC-32/FCS errors). |
| Reserved | F:A | RSV | | Reserved. Do not modify. |

4.6.2.2.82 PCS Receive Vendor Uncorrected Frame Counter 1: Address 3.E820

| Field Name | Bit(s) | Type | Default | Description |
|-------------------------------------|--------|------|---------|---|
| Uncorrected Frame Counter LSW [F:0] | F:0 | SCTL | 0x0000 | Lower 16 bits of LDPC uncorrected frames which the decoder abandoned. When the LSW is read, the MSW is copied to a shadow register, then both the LSW and MSW are cleared. The LSW of the counter must be read first. The MSW of the counter must be read immediately after the LSW is read. A saturating counter that counts the number of uncorrected frames. |

4.6.2.2.83 PCS Receive Vendor Uncorrected Frame Counter 2: Address 3.E821

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------------|--------|------|---------|--|
| Uncorrected Frame Counter MSW [1F:10] | F:0 | SCTM | 0x0000 | Upper 16 bits of LDPC uncorrected frames which the decoder abandoned. The MSW of the counter must be read immediately after the LSW of the counter is read. The MSW is actually a shadow copy of the MSW of the counter and is loaded after the LSW of the counter is read. A saturating counter that counts the number of uncorrected frames. |



4.6.2.2.84 PCS Receive Vendor Corrected Frame 1 Iteration Counter 1: Address 3.E840

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|--|
| Corrected Frames 1 Iteration Counter LSW [F:0] | F:0 | SCTL | 0x0000 | Lower 16 bits of LDPC corrected frames which converged in 1 iteration. When the LSW is read, the MSW is copied to a shadow register and then both the LSW and MSW are cleared. The LSW of the counter must be read first. The MSW of the counter must be read immediately after the LSW is read. A saturating counter that counts the number of corrected frames which converged in 1 iteration. |

4.6.2.2.85 PCS Receive Vendor Corrected Frame 1 Iteration Counter 2: Address 3.E841

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|--|
| Corrected Frames 1 Iteration Counter MSW [1F:10] | F:0 | SCTM | 0x0000 | Upper 16 bits of LDPC corrected frames which converged in 1 iteration. The MSW of the counter must be read immediately after the LSW of the counter is read. The MSW is actually a shadow copy of the MSW of the counter and is loaded after the LSW of the counter is read. A saturating counter that counts the number of corrected frames which converged in 1 iteration. |

4.6.2.2.86 PCS Receive Vendor Corrected Frame 2 Iteration Counter 1: Address 3.E842

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|--|
| Corrected Frames 2 Iteration Counter LSW [F:0] | F:0 | SCTL | 0x0000 | Lower 16 bits of LDPC corrected frames which converged in 2 iteration. When the LSW is read, the MSW is copied to a shadow register and then both the LSW and MSW are cleared. The LSW of the counter must be read first. The MSW of the counter must be read immediately after the LSW is read. A saturating counter that counts the number of corrected frames which converged in 2 iteration. |

4.6.2.2.87 PCS Receive Vendor Corrected Frame 2 Iteration Counter 2: Address 3.E843

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|--|
| Corrected Frames 2 Iteration Counter MSW [1F:10] | F:0 | SCTM | 0x0000 | Upper 16 bits of LDPC corrected frames which converged in 2 iteration. The MSW of the counter must be read immediately after the LSW of the counter is read. The MSW is actually a shadow copy of the MSW of the counter and is loaded after the LSW of the counter is read. A saturating counter that counts the number of corrected frames which converged in 2 iteration. |



4.6.2.2.88 PCS Receive Vendor Corrected Frame 3 Iteration Counter 1: Address 3.E844

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|--|
| Corrected Frames 3 Iteration Counter LSW [F:0] | F:0 | SCTL | 0x0000 | Lower 16 bits of LDPC corrected frames which converged in 3 iteration. When the LSW is read, the MSW is copied to a shadow register and then both the LSW and MSW are cleared. The LSW of the counter must be read first. The MSW of the counter must be read immediately after the LSW is read. A saturating counter that counts the number of corrected frames which converged in 3 iteration. |

4.6.2.2.89 PCS Receive Vendor Corrected Frame 3 Iteration Counter 2: Address 3.E845

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|--|
| Corrected Frames 3 Iteration Counter MSW [1F:10] | F:0 | SCTM | 0x0000 | Upper 16 bits of LDPC corrected frames which converged in 3 iteration. The MSW of the counter must be read immediately after the LSW of the counter is read. The MSW is actually a shadow copy of the MSW of the counter and is loaded after the LSW of the counter is read. A saturating counter that counts the number of corrected frames which converged in 3 iteration. |

4.6.2.2.90 PCS Receive Vendor Corrected Frame 4 Iteration Counter 1: Address 3.E846

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|--|
| Corrected Frames 4 Iteration Counter LSW [F:0] | F:0 | SCTL | 0x0000 | Lower 16 bits of LDPC corrected frames which converged in 4 iteration. When the LSW is read, the MSW is copied to a shadow register and then both the LSW and MSW are cleared. The LSW of the counter must be read first. The MSW of the counter must be read immediately after the LSW is read. A saturating counter that counts the number of corrected frames which converged in 4 iteration. |

4.6.2.2.91 PCS Receive Vendor Corrected Frame 4 Iteration Counter 2: Address 3.E847

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|--|
| Corrected Frames 4 Iteration Counter MSW [1F:10] | F:0 | SCTM | 0x0000 | Upper 16 bits of LDPC corrected frames which converged in 4 iteration. The MSW of the counter must be read immediately after the LSW of the counter is read. The MSW is actually a shadow copy of the MSW of the counter and is loaded after the LSW of the counter is read. A saturating counter that counts the number of corrected frames which converged in 4 iteration. |



4.6.2.2.92 PCS Receive Vendor Corrected Frame 5 Iteration Counter 1: Address 3.E848

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|--|
| Corrected Frames 5 Iteration Counter LSW [F:0] | F:0 | SCTL | 0x0000 | Lower 16 bits of LDPC corrected frames which converged in 5 iteration. When the LSW is read, the MSW is copied to a shadow register and then both the LSW and MSW are cleared. The LSW of the counter must be read first. The MSW of the counter must be read immediately after the LSW is read. A saturating counter that counts the number of corrected frames which converged in 5 iteration. |

4.6.2.2.93 PCS Receive Vendor Corrected Frame 5 Iteration Counter 2: Address 3.E849

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|--|
| Corrected Frames 5 Iteration Counter MSW [1F:10] | F:0 | SCTM | 0x0000 | Upper 16 bits of LDPC corrected frames which converged in 5 iteration. The MSW of the counter must be read immediately after the LSW of the counter is read. The MSW is actually a shadow copy of the MSW of the counter and is loaded after the LSW of the counter is read. A saturating counter that counts the number of corrected frames which converged in 5 iteration. |

4.6.2.2.94 PCS Receive Vendor Corrected Frame 6 Iteration Counter: Address 3.E850

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|---|
| Corrected Frames 6 Iteration Counter [F:0] | F:0 | SCT | 0x0000 | LDPC corrected frames which converged in 6 iteration. Clear on read. A saturating counter that counts the number of corrected frames which converged in 6 iteration. |

4.6.2.2.95 PCS Receive Vendor Corrected Frame 7 Iteration Counter: Address 3.E851

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|---|
| Corrected Frames 7 Iteration Counter [F:0] | F:0 | SCT | 0x0000 | LDPC corrected frames which converged in 7 iteration. Clear on read. A saturating counter that counts the number of corrected frames which converged in 7 iteration. |



4.6.2.2.96 PCS Receive Vendor Corrected Frame 8 Iteration Counter: Address 3.E852

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|---|
| Corrected Frames 8 Iteration Counter [F:0] | F:0 | SCT | 0x0000 | LDPC corrected frames which converged in 8 iteration. Clear on read. A saturating counter that counts the number of corrected frames which converged in 8 iteration. |

4.6.2.2.97 PCS Receive XFIO Vendor State 1: Address 3.E860

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------------|--------|------|---------|--|
| XFIO Good Frame Counter LSW [F:0] | F:0 | SCTL | 0x0000 | XFIO Good Frame Counter LSW. Counts Ethernet good frames (i.e., no Ethernet CRC-32/FCS errors). |

4.6.2.2.98 PCS Receive XFIO Vendor State 2: Address 3.E861

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------------|--------|------|---------|--|
| XFIO Good Frame Counter MSW [9:0] | 9:0 | SCTM | 0x000 | XFIO Good Frame Counter MSW. Counts Ethernet good frames (i.e., no Ethernet CRC-32/FCS errors). |
| Reserved | F:A | RSV | | Reserved. Do not modify. |

4.6.2.2.99 PCS Receive XFIO Vendor State 3: Address 3.E862

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------------|--------|------|---------|--|
| XFIO Bad Frame Counter LSW [F:0] | F:0 | SCTL | 0x0000 | XFIO Bad Frame Counter LSW. Counts Ethernet bad frames (i.e., no Ethernet CRC-32/FCS errors). |

4.6.2.2.100 PCS Receive XFIO Vendor State 4: Address 3.E863

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------------|--------|------|---------|--|
| XFIO Bad Frame Counter MSW [9:0] | 9:0 | SCTM | 0x000 | XFIO Bad Frame Counter MSW. Counts Ethernet bad frames (i.e., no Ethernet CRC-32/FCS errors). |
| Reserved | F:A | RSV | | Reserved. Do not modify. |

4.6.2.2.101 PCS Receive XFIO Vendor State 5: Address 3.E864

| Field Name | Bit(s) | Type | Default | Description |
|------------------------|--------|------|---------|---|
| XFIO BER Counter [5:0] | 5:0 | SCT | 0x00 | XFIO BER counter. 10GBASE-R BER Counter[5:0], saturating, clear on read. |
| Reserved | F:6 | RSV | | Reserved. Do not modify. |



4.6.2.2.102 PCS Receive XFIO Vendor State 6: Address 3.E865

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------------|--------|------|---------|---|
| XFIO Errored Block Counter [7:0] | 7:0 | SCT | 0x00 | XFIO errored block counter. 10GBASE-R Errored Block Counter[7:0], saturating, clear on read. |
| Reserved | F:8 | RSV | | Reserved. Do not modify. |

4.6.2.2.103 PCS Receive XFIO Vendor State 7: Address 3.E866

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------------|--------|------|---------|--|
| XFIO Test Pattern Error Counter [F:0] | F:0 | SCT | 0x0000 | XFIO test pattern error counter. 10GBASE-R Test Pattern Error Counter[15:0], saturating, clear on read. |

4.6.2.2.104 PCS Receive XFI 1 Vendor State 1: Address 3.E870

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------------|--------|------|---------|--|
| XF11 Good Frame Counter LSW [F:0] | F:0 | SCTL | 0x0000 | XF11 Good Frame Counter LSW. Counts Ethernet good frames (i.e., no Ethernet CRC-32/FCS errors). |

4.6.2.2.105 PCS Receive XFI 1 Vendor State 2: Address 3.E871

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------------|--------|------|---------|--|
| XF11 Good Frame Counter MSW [9:0] | 9:0 | SCTM | 0x000 | XF11 Good Frame Counter MSW. Counts Ethernet good frames (i.e., no Ethernet CRC-32/FCS errors). |
| Reserved | F:A | RSV | | Reserved. Do not modify. |

4.6.2.2.106 PCS Receive XFI 1 Vendor State 3: Address 3.E872

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------------|--------|------|---------|--|
| XF11 Bad Frame Counter LSW [F:0] | F:0 | SCTL | 0x0000 | XF11 Bad Frame Counter LSW. Counts Ethernet bad frames (i.e., no Ethernet CRC-32/FCS errors). |

4.6.2.2.107 PCS Receive XFI 1 Vendor State 4: Address 3.E873

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------------|--------|------|---------|--|
| XF11 Bad Frame Counter MSW [9:0] | 9:0 | SCTM | 0x000 | XF11 Bad Frame Counter MSW. Counts Ethernet bad frames (i.e., no Ethernet CRC-32/FCS errors). |
| Reserved | F:A | RSV | | Reserved. Do not modify. |



4.6.2.2.108 PCS Receive XFI1 Vendor State 5: Address 3.E874

| Field Name | Bit(s) | Type | Default | Description |
|------------------------|--------|------|---------|---|
| XFI1 BER Counter [5:0] | 5:0 | SCT | 0x00 | XFI1 BER counter. 10GBASE-R BER Counter[5:0], saturating, clear on read. |
| Reserved | F:6 | RSV | | Reserved. Do not modify. |

4.6.2.2.109 PCS Receive XFI1 Vendor State 6: Address 3.E875

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------------|--------|------|---------|---|
| XFI1 Errored Block Counter [7:0] | 7:0 | SCT | 0x00 | XFI1 errored block counter. 10GBASE-R Errored Block Counter[7:0], saturating, clear on read. |
| Reserved | F:8 | RSV | | Reserved. Do not modify. |

4.6.2.2.110 PCS Receive XFI1 Vendor State 7: Address 3.E876

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------------|--------|------|---------|--|
| XFI1 Test Pattern Error Counter [F:0] | F:0 | SCT | 0x0000 | XFI1 test pattern error counter. 10GBASE-R Test Pattern Error Counter[15:0], saturating, clear on read. |

4.6.2.2.111 PCS Receive Vendor Alarms 1: Address 3.EC00

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|---|
| Change in Auxiliary Bit | 0 | LRF | | This bit is set when a change is detected in the auxiliary bit. 1b = Indicates a change in the value of the auxiliary bit. |
| Reserved | 1 | RSV | | Reserved. Do not modify. |
| EEE Rx LPI Received Latched High | 2 | LH | | Indicates LPI ordered-set is detected. 1b = Rx LPI has been detected. |
| EEE Rx LPI Received Latched Low | 3 | LH | | Indicates LPI ordered-set is detected. 1b = Rx LPI has been detected |
| EEE Rx LPI Alert | 4 | LH | | Indicates Rx PCS received alert. 1b = Rx PCS received alert indication. |
| LDPC Consecutive Errored Frame Exceeded | 5 | LH | | Indicates the consecutive LDPC errored frame has exceeded the threshold. 1b = Rx PCS LDPC consecutive errored frame threshold exceeded. |
| EEE Rx LPI Active On | 6 | LH | | 1b = EEE Rx LPI Active On. |
| EEE Rx LPI Active Off | 7 | LH | | 1b = EEE Rx LPI Active Off. |
| Invalid 65B Block | 8 | LH | | This bit is set when an invalid 65B block (but without LDPC frame parity error) has been detected on the received LDPC frame. 1b = Invalid Rx 65B block received in PCS transmission frame |
| 40G BIP Lock | 9 | LH | | Indicates the 40G BIP checker has achieved lock to the alignment marker. 1b = RPL 40G BIP lock. |



| Field Name | Bit(s) | Type | Default | Description |
|---------------------|--------|------|---------|--|
| LOF Detect | A | LH | | LOF Detection Interrupt. 1b = RPL LOF detect. |
| Local Fault Detect | B | LH | | Local_Fault Interrupt. 1b = RPL local fault detect. |
| Reserved | D:C | RSV | | Reserved. Do not modify. |
| LDPC Decode Failure | E | LH | | This bit is set when the LDPC decoder fails to decode an LDPC block. 1b = LDPC decode failure. |
| CRC Error | F | LH | | This bit is set when a CRC-8 error is detected on the receive PCS frame. 1b = Rx CRC Frame error. |

4.6.2.2.112 PCS Receive Vendor Alarms 2: Address 3.EC01

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |

4.6.2.2.113 PCS Receive Vendor Alarms 3: Address 3.EC02

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |

4.6.2.2.114 PCS Receive Vendor Alarms 4: Address 3.EC03

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |

4.6.2.2.115 PCS Receive Vendor Alarms 5: Address 3.EC04

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |

4.6.2.2.116 PCS Receive Vendor Alarms 6: Address 3.EC05

| Field Name | Bit(s) | Type | Default | Description |
|-------------------------------------|--------|------|---------|--|
| Reserved | 2:0 | RSV | | Reserved. Do not modify. |
| XFI0 Invalid 66B Character Received | 3 | LH | | Invalid 66B code error. 1b = XFI1 Receive invalid 66B character received. |
| Reserved | A:4 | RSV | | Reserved. Do not modify. |



| Field Name | Bit(s) | Type | Default | Description |
|-------------------------------------|--------|------|---------|--|
| XFI1 Invalid 66B Character Received | B | LH | | Invalid 66B code error. 1b = XFI1 Receive invalid 66B character received. |
| Reserved | F:C | RSV | | Reserved. Do not modify. |

4.6.2.2.117 PCS Receive Vendor Alarms 7: Address 3.EC06

| Field Name | Bit(s) | Type | Default | Description |
|-------------------------------------|--------|------|---------|--|
| XFI0 Block Lock Status | 0 | LL | | 1b = XFI0 Block Lock condition. |
| XFI0 High BER Status | 1 | LH | | 1b = XFI0 High BER condition. |
| Reserved | 2 | RSV | | Reserved. Do not modify. |
| XFI0 Receive Link Status Latch High | 3 | LH | | Status of the XFI0 receive link. Indicates the status of the XFI0 receive link. |
| XFI1 Block Lock Status | 4 | LL | | 1b = XFI1 Block Lock condition. |
| XFI1 High BER Status | 5 | LH | | 1b = XFI1 High BER condition. |
| Reserved | 6 | RSV | | Reserved. Do not modify. |
| XFI1 Receive Link Status Latch High | 7 | LH | | Status of the XFI1 receive link Indicates the status of the XFI1 receive link. |
| Reserved | F:8 | RSV | | Reserved. Do not modify. |

4.6.2.2.118 PCS Receive Vendor Interrupt Mask 1: Address 3.F400

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|--------|---------|--|
| Change in Auxiliary Bit Mask | 0 | R/W PD | 0b | This bit is set when a change is detected in the auxiliary bit. 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | 1 | RSV | | Reserved. Do not modify. |
| EEE Rx LPI Received Latched High Mask | 2 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| EEE Rx LPI Received Latched Low Mask | 3 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| EEE Rx LPI Alert Mask | 4 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| LDPC Consecutive Errored Frame Exceeded Mask | 5 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| EEE Rx LPI Active On Mask | 6 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| EEE Rx LPI Active Off Mask | 7 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |



| Field Name | Bit(s) | Type | Default | Description |
|--------------------------|--------|--------|---------|--|
| Invalid 65B Block Mask | 8 | R/W PD | 0b | This bit is set when an invalid 65B block (but without LDPC frame parity error) has been detected on the received LDPC frame. 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| 40G BIP Lock Mask | 9 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| LOF Detect Mask | A | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Local Fault Detect Mask | B | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | D:C | RSV | | Reserved. Do not modify. |
| LDPC Decode Failure Mask | E | R/W PD | 0b | This bit is set when the LDPC decoder fails to decode an LDPC block. 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| CRC Error Mask | F | R/W PD | 0b | This bit is set when a CRC-8 error is detected on the receive PCS frame. 0b = Disable interrupt generation. 1b = Enable interrupt generation. |

4.6.2.2.119 PCS Receive Vendor Interrupt Mask 2: Address 3.F401

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |

4.6.2.2.120 PCS Receive Vendor Interrupt Mask 3: Address 3.F402

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |

4.6.2.2.121 PCS Receive Vendor Interrupt Mask 4: Address 3.F403

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |

4.6.2.2.122 PCS Receive Vendor Interrupt Mask 5: Address 3.F404

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |



4.6.2.2.123 PCS Receive Vendor Interrupt Mask 6: Address 3.F405

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|--------|---------|---|
| Reserved | 2:0 | RSV | | Reserved. Do not modify. |
| XFI0 Invalid 66B Character Received Mask | 3 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | A:4 | RSV | | Reserved. Do not modify. |
| XFI1 Invalid 66B Character Received Mask | B | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | F:C | RSV | | Reserved. Do not modify. |

4.6.2.2.124 PCS Receive Vendor Interrupt Mask 7: Address 3.F406

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|--------|---------|---|
| XFI0 Block Lock Status Mask | 0 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| XFI0 High BER Status Mask | 1 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | 2 | RSV | | Reserved. Do not modify. |
| XFI0 Receive Link Status Latch High Mask | 3 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| XFI1 Block Lock Status Mask | 4 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| XFI1 High BER Status Mask | 5 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | 6 | RSV | | Reserved. Do not modify. |
| XFI1 Receive Link Status Latch High Mask | 7 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | F:8 | RSV | | Reserved. Do not modify. |

4.6.2.2.125 PCS Receive Vendor Debug 1: Address 3.F800

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------|--------|--------|---------|--|
| PCS Network Loopback | 0 | R/W PD | 0b | When set to 1b, data after the Rx PCS layer is looped back to the Tx PCS layer and transmitted back towards the network UTP line. |
| Reserved | 1 | R/W PD | 1b | Reserved for future use. |
| Reserved | E:3 | RSV | | Reserved. Do not modify. |
| Reserved | 2 | R/W PD | 1b | If the MAC sends data, it takes priority over the PCS Network Loopback data. The loopback data is dropped. |
| PCS Rx Descrambler Disable | F | R/W PD | 0b | Setting this bit disables the Rx descrambler during regular data transmission (for example, descrambler functionality during training and startup is unmodified). 0b = Normal Operation. 1b = Rx Descrambler Disabled. |



4.6.2.2.126 PCS Vendor Global Interrupt Flags 1: Address 3.FC00

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------------|--------|------|---------|--|
| Reserved | 1:0 | RSV | | Reserved. Do not modify. |
| Vendor Specific Rx Alarms 5 Interrupt | 2 | RO | | An interrupt was generated from status register (Section 4.6.2.2.115, "PCS Receive Vendor Alarms 5: Address 3.EC04") and the corresponding mask register (Section 4.6.2.2.122, "PCS Receive Vendor Interrupt Mask 5: Address 3.F404"). 1b = Interrupt in vendor specific Rx alarms 5. |
| Vendor Specific Rx Alarms 4 Interrupt | 3 | RO | | An interrupt was generated from status register (Section 4.6.2.2.114, "PCS Receive Vendor Alarms 4: Address 3.EC03") and the corresponding mask register (Section 4.6.2.2.121, "PCS Receive Vendor Interrupt Mask 4: Address 3.F403"). 1b = Interrupt in vendor specific Rx alarms 4. |
| Vendor Specific Rx Alarms 3 Interrupt | 4 | RO | | An interrupt was generated from status register (Section 4.6.2.2.113, "PCS Receive Vendor Alarms 3: Address 3.EC02") and the corresponding mask register (Section 4.6.2.2.120, "PCS Receive Vendor Interrupt Mask 3: Address 3.F402"). 1b = Interrupt in vendor specific Rx alarms 3. |
| Vendor Specific Rx Alarms 2 Interrupt | 5 | RO | | An interrupt was generated from status register (Section 4.6.2.2.112, "PCS Receive Vendor Alarms 2: Address 3.EC01") and the corresponding mask register (Section 4.6.2.2.119, "PCS Receive Vendor Interrupt Mask 2: Address 3.F401"). 1b = Interrupt in vendor specific Rx alarms 2. |
| Vendor Specific Rx Alarms 1 Interrupt | 6 | RO | | An interrupt was generated from status register (Section 4.6.2.2.111, "PCS Receive Vendor Alarms 1: Address 3.EC00") and the corresponding mask register (Section 4.6.2.2.118, "PCS Receive Vendor Interrupt Mask 1: Address 3.F400"). 1b = Interrupt in vendor specific Rx alarms 1. |
| Reserved | 8:7 | RSV | | Reserved. Do not modify. |
| Vendor Specific Tx Alarms 3 Interrupt | 9 | RO | | An interrupt was generated from status register (Section 4.6.2.2.60, "PCS Transmit Vendor Alarms 3: Address 3.CC02") and the corresponding mask register (Section 4.6.2.2.67, "PCS Transmit Vendor Interrupt Mask 3: Address 3.D402"). 1b = Interrupt in vendor specific Tx alarms 3. |
| Vendor Specific Tx Alarms 2 Interrupt | A | RO | | An interrupt was generated from status register (Section 4.6.2.2.59, "PCS Transmit Vendor Alarms 2: Address 3.CC01") and the corresponding mask register (Section 4.6.2.2.66, "PCS Transmit Vendor Interrupt Mask 2: Address 3.D401"). 1b = Interrupt in vendor specific Tx alarms 2. |
| Vendor Specific Tx Alarms 1 Interrupt | B | RO | | An interrupt was generated from status register (Section 4.6.2.2.58, "PCS Transmit Vendor Alarms 1: Address 3.CC00") and the corresponding mask register (Section 4.6.2.2.65, "PCS Transmit Vendor Interrupt Mask 1: Address 3.D400"). 1b = Interrupt in vendor specific Tx alarms 1. |
| Reserved | C | RSV | | Reserved. Do not modify. |
| Standard Alarm 3 Interrupt | D | RO | | An interrupt was generated from status register (Section 4.6.2.2.15, "PCS 10G Status 2: Address 3.21") and the corresponding mask register (Section 4.6.2.2.64, "PCS Standard Interrupt Mask 3: Address 3.D002"). 1b = Interrupt in standard alarms 3. |
| Standard Alarm 2 Interrupt | E | RO | | An interrupt was generated from status register (Section 4.6.2.2.9, "PCS Standard Status 2: Address 3.8") and the corresponding mask register (Section 4.6.2.2.63, "PCS Standard Interrupt Mask 2: Address 3.D001"). 1b = Interrupt in standard alarms 2. |



| Field Name | Bit(s) | Type | Default | Description |
|----------------------------|--------|------|---------|--|
| Standard Alarm 1 Interrupt | F | RO | | An interrupt was generated from status register (Section 4.6.2.2.2, "PCS Standard Status 1: Address 3.1") and the corresponding mask register (Section 4.6.2.2.62, "PCS Standard Interrupt Mask 1: Address 3.D000"). 1b = Interrupt in standard alarms 1. |

4.6.2.2.127 PCS Vendor Global Interrupt Flags 3: Address 3.FC02

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------------|--------|------|---------|--|
| Reserved | 5:0 | RSV | | Reserved. Do not modify. |
| Vendor Specific Rx Alarms 7 Interrupt | 6 | RO | | An interrupt was generated from status register (Section 4.6.2.2.116, "PCS Receive Vendor Alarms 6: Address 3.EC05") and the corresponding mask register (Section 4.6.2.2.123, "PCS Receive Vendor Interrupt Mask 6: Address 3.F405"). 1b = Interrupt in vendor specific Rx alarms 6. |
| Vendor Specific Rx Alarms 6 Interrupt | 7 | RO | | An interrupt was generated from status register (Section 4.6.2.2.117, "PCS Receive Vendor Alarms 7: Address 3.EC06") and the corresponding mask register (Section 4.6.2.2.124, "PCS Receive Vendor Interrupt Mask 7: Address 3.F406"). 1b = Interrupt in vendor specific Rx alarms 7. |
| Reserved | F:8 | RSV | | Reserved. Do not modify. |



4.6.2.3 PHY XS Registers

4.6.2.3.1 PHY XS Standard Control 1: Address 4.0

| Field Name | Bit(s) | Type | Default | Description |
|-------------------------|--------|-----------|---------|---|
| Reserved | 1:0 | RSV | | Reserved. Do not modify. |
| Speed Selection 2 [3:0] | 5:2 | ROS | 0x0 | This should always be set to 0x0. 0000b = 10 GbE xxx1b = Reserved xx1xb = Reserved x1xxb = Reserved 1xxxb = Reserved |
| Speed Selection 1 | 6 | ROS | 1b | This should always be set to 1b. 0b = Unspecified 01b = 10 GbE and above. |
| Reserved | 9:7 | RSV | | Reserved. Do not modify. |
| Clock Stop Enable | A | R/W | 0b | 0b = Clock not stoppable. 1b = The PHY XS may stop the clock during LPI. |
| Low Power | B | R/W | 0b | A one written to this register causes the PHY XS to enter low-power mode. If a global chip low-power state is desired, use 1E.0.B (refer to Section 4.6.2.6.1). 0b = Normal operation. 1b = Low-power mode. Note: This is a processor intensive operation. Completion of this operation can be monitored via 1E.C831.F (refer to Section 4.6.2.6.83). |
| Reserved | C | RSV | | Reserved. Do not modify. |
| Speed Selection 0 | D | ROS | 1b | This should always be set to 1b. 0b = Unspecified 01b = 10 GbE and above. |
| Loopback | E | R/W | 0b | Enables network loopback on the designated system interface. 0b = Normal operation. 1b = System Interface Network Loopback. Note: This is a processor intensive operation. Completion of this operation can be monitored via 1E.C831.F (refer to Section 4.6.2.6.83). |
| Reset | F | R/W SC | 1b | Resets the entire PHY. 0b = Normal operation. 1b = PHY XS reset. The reset bit is automatically cleared upon completion of the reset sequence by the microcontroller. This bit is set to 1b during reset. The reset is internally stretched by approximately 1.7 μ s. Therefore the MDIO or uP should allow for 1.7 μ s before writing any PCS registers after this bit is set. |

4.6.2.3.2 PHY XS Standard Status 1: Address 4.1

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | 0 | RSV | | Reserved. Do not modify. |
| Reserved | 1 | ROS | 1b | Reserved. |



| Field Name | Bit(s) | Type | Default | Description |
|--------------------|--------|------|---------|--|
| Reserved | 5:2 | RSV | | Reserved. Do not modify. |
| Clock Stop Capable | 6 | ROS | 0b | 0b = Clock not stoppable. 1b = The attached PHY may stop the clock during LPI. |
| Fault | 7 | RO | | The top-level fault indicator flag for the PHY XS block. 0b = No fault detected. 1b = Fault condition detected. This bit is set if either of the two bits 4.8.B or 4.8.A are set (refer to Section 4.6.2.3.8). |
| Rx LPI Indication | 8 | RO | | 0b = Rx PHY XS is not currently receiving LPI. 1b = Rx PHY XS is currently receiving LPI. |
| Tx LPI Indication | 9 | RO | | 0b = Tx PHY XS is not currently receiving LPI. 1b = Tx PHY XS is currently receiving LPI. |
| Rx LPI Received | A | LH | | 0b = LPI not received. 1b = Rx PHY XS has received LPI. |
| Tx LPI Received | B | LH | | 0b = LPI not received. 1b = Tx PHY XS has received LPI. |
| Reserved | F:C | RSV | | Reserved. Do not modify. |

4.6.2.3.3 PHY XS Standard Device Identifier 1: Address 4.2

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------|--------|------|---------|----------------------------|
| Device ID MSW [1F:10] | F:0 | RO | | Bits [31:16] of Device ID. |

4.6.2.3.4 PHY XS Standard Device Identifier 2: Address 4.3

| Field Name | Bit(s) | Type | Default | Description |
|---------------------|--------|------|---------|---------------------------|
| Device ID LSW [F:0] | F:0 | RO | | Bits [15:0] of Device ID. |

4.6.2.3.5 PHY XS Standard Speed Ability: Address 4.4

| Field Name | Bit(s) | Type | Default | Description |
|-------------|--------|------|---------|---|
| 10G Capable | 0 | ROS | 1b | This is always set to 1b in the X557. 0b = PHY XS is not 10 Gb/s capable. 1b = PHY XS is 10 Gb/s capable. |
| Reserved | F:1 | RSV | | Reserved. Do not modify. |

4.6.2.3.6 PHY XS Standard Devices in Package 1: Address 4.5

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------|--------|------|---------|--|
| Clause 22 Registers Present | 0 | ROS | 0b | This is always set to 0b, as there are no Clause 22 registers in the X557. 0b = Clause 22 registers are not present in package. 1b = Clause 22 registers are present in package. |



| Field Name | Bit(s) | Type | Default | Description |
|--------------------------|--------|------|---------|---|
| PMA Present | 1 | ROS | 1b | This is always set to 1b, as there is PMA functionality in the X557. 0b = PMA is not present. 1b = PMA is present in package. |
| WIS Present | 2 | ROS | 0b | This is always set to 0b, as there is no WIS functionality in the X557. 0b = WIS is not present in package. 1b = WIS is present in package. |
| PCS Present | 3 | ROS | 1b | This is always set to 1b, as there is PCS functionality in the X557. 0b = PCS is not present in package. 1b = PCS is present in package. |
| PHY XS Present | 4 | ROS | 1b | This is always set to 1b, as there is a PHY XS interface in the X557. 0b = PHY XS is not present in package. 1b = PHY XS is present in package. |
| DTE XS Present | 5 | ROS | 0b | This is always set to 0b. |
| TC Present | 6 | ROS | 0b | This is always set to 0b, as there is no TC functionality in the X557. 0b = TC is not present in package. 1b = TC is present in package. |
| Auto-negotiation Present | 7 | ROS | 1b | This is always set to 1b, as there is auto-negotiation in the X557. 0b = Auto-negotiation is not present in package. 1b = Auto-negotiation is present in package. |
| Reserved | F:8 | RSV | | Reserved. Do not modify. |

4.6.2.3.7 PHY XS Standard Devices in Package 2: Address 4.6

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------------|--------|------|---------|---|
| Reserved | C:0 | RSV | | Reserved. Do not modify. |
| Clause 22 Extension Present | D | ROS | 1b | This is always set to 1b, as the X557 utilizes this device for the GbE registers. 0b = Clause 22 Extension is not present in package. 1b = Clause 22 Extension is present in package. |
| Vendor Specific Device #1 Present | E | ROS | 1b | This is always set to 1b, as the X557 utilizes this device for the Global registers. 0b = Device #1 is not present in package. 1b = Device #1 is present in package. |
| Vendor Specific Device #2 Present | F | ROS | 1b | This is always set to 1b, as the X557 utilizes this device for the DSP PMA registers. 0b = Device #2 is not present in package. 1b = Device #2 is present in package. |

4.6.2.3.8 PHY XS Standard Status 2: Address 4.8

| Field Name | Bit(s) | Type | Default | Description |
|---------------|--------|------|---------|---|
| Reserved | 9:0 | RSV | | Reserved. Do not modify. |
| Receive Fault | A | LH | | Indicates whether there is a fault somewhere along the receive path. A fault is indicated if there is a FIFO underflow/overflow error. 0b = No fault condition on receive path. 1b = Fault condition on receive path. |



| Field Name | Bit(s) | Type | Default | Description |
|----------------------|--------|------|---------|--|
| Transmit Fault | B | LH | | Indicates whether there is a fault somewhere along the transmit path. A fault is indicated if there is an alignment fault, a synchronization fault on any lane, or a FIFO underflow/overflow error. 0b = No fault condition on transmit path. 1b = Fault condition on transmit path. |
| Reserved | D:C | RSV | | Reserved. Do not modify. |
| Device Present [1:0] | F:E | ROS | 10b | This field is always set to 10b, as the PHY XS is present in the X557. 00b = No device at this address. 01b = Device present at this address. 10b = No device at this address. 11b = No device at this address. |

4.6.2.3.9 PHY XS Standard Package Identifier 1: Address 4.E

| Field Name | Bit(s) | Type | Default | Description |
|------------------------|--------|------|---------|-----------------------------|
| Package ID MSW [1F:10] | F:0 | RO | | Bits [31:16] of Package ID. |

4.6.2.3.10 PHY XS Standard Package Identifier 2: Address 4.F

| Field Name | Bit(s) | Type | Default | Description |
|----------------------|--------|------|---------|----------------------------|
| Package ID LSW [F:0] | F:0 | RO | | Bits [15:0] of Package ID. |

4.6.2.3.11 PHY XS EEE Capability Register: Address 4.14

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--|
| Reserved | 3:0 | RSV | | Reserved. Do not modify. |
| PHY XS EEE | 4 | ROC | 1b | 0b = EEE is not supported for PHY XS 1b = EEE is supported for PHY XS |
| Reserved | F:5 | RSV | | Reserved. Do not modify. |

4.6.2.3.12 PHY XS EEE Wake Error Counter: Address 4.16

| Field Name | Bit(s) | Type | Default | Description |
|------------------------------|--------|------|---------|---|
| EEE Wake Error Counter [F:0] | F:0 | SCT | 0x0000 | EEE wake error counter. This register is a 16-bit, saturating, clear on read counter. The wake error source is configured with 1E.C4A2.A:8. The default wake error source is from the TX1. |

4.6.2.3.13 PHY XS Standard XGXS Lane Status: Address 4.18

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | 9:0 | RSV | | Reserved. Do not modify. |



| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|---------------------------|
| Reserved | A | ROS | 1b | This is always set to 1b. |
| Reserved | B | ROS | 1b | Reserved. |
| Reserved | C | RO | | Reserved. |
| Reserved | F:D | RSV | | Reserved. Do not modify. |

4.6.2.3.14 PHY XS Standard XGXS Test Control: Address 4.19

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------|--------|--------|---------|--|
| Test-Pattern Select [1:0] | 1:0 | R/W PD | 10b | These test patterns are described in Annex 48A of 802.3ae. The full range of options is described there, but for these functions to correspond to the test-patterns described here, Bits [C:B] must be set to zero. 00b = High-frequency test pattern. 01b = Low-frequency test pattern. 10b = Mixed-frequency test pattern. 11b = Reserved. |
| Reserved | 2 | R/W PD | 0b | Reserved. |
| Reserved | F:3 | RSV | | Reserved. Do not modify. |

4.6.2.3.15 PHY XS SERDES Configuration 1: Address 4.C180

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|--------------------------|
| SERDES Configuration Reserved 1-2 [2:0] | 2:0 | R/W | 000b | Reserved. |
| Reserved | 3 | RSV | | Reserved. Do not modify. |
| SERDES Configuration Reserved 1-1 | 4 | R/W | 0b | Reserved. |
| Reserved | F:5 | RSV | | Reserved. Do not modify. |

4.6.2.3.16 PHY XS SERDES Lane 0 Configuration 1: Address 4.C1C0

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|--------------------------|
| SERDES Lane 0 Configuration Reserved 1 | 0 | R/W | 1b | Reserved. |
| Reserved | F:1 | RSV | | Reserved. Do not modify. |

4.6.2.3.17 PHY XS SERDES Lane 1 Configuration 1: Address 4.C1D0

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|--------------------------|
| SERDES Lane 1 Configuration Reserved 1 | 0 | R/W | 1b | Reserved. |
| Reserved | F:1 | RSV | | Reserved. Do not modify. |



4.6.2.3.18 PHY XS SERDES Lane 2 Configuration 1: Address 4.C1E0

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|--------------------------|
| SERDES Lane 2 Configuration Reserved 1 | 0 | R/W | 1b | Reserved. |
| Reserved | F:1 | RSV | | Reserved. Do not modify. |

4.6.2.3.19 PHY XS SERDES Lane 3 Configuration 1: Address 4.C1F0

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|--------------------------|
| SERDES Lane 3 Configuration Reserved 1 | 0 | R/W | 1b | Reserved. |
| Reserved | F:1 | RSV | | Reserved. Do not modify. |

4.6.2.3.20 PHY XS SERDES LUT 256: Address 4.C200

| Field Name | Bit(s) | Type | Default | Description |
|-------------------------------|--------|------|---------|--------------------------------------|
| SERDES LUT 256 Reserved [7:0] | 7:0 | R/W | 0x00 | Reserved. Spans 0xC200 to 0xC2FF. |
| Reserved | F:8 | RSV | | Reserved. Do not modify. |

4.6.2.3.21 PHY XS Vendor Global Interrupt Flags 1: Address 4.FC00

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------------|--------|------|---------|--|
| Reserved | 0 | RSV | | Reserved. Do not modify. |
| Vendor Specific Rx Alarms 2 Interrupt | 1 | RO | | An interrupt was generated from the status register and the corresponding mask register. 1b = Interrupt in vendor specific Rx alarms 2. |
| Vendor Specific Rx Alarms 1 Interrupt | 2 | RO | | An interrupt was generated from the status register and the corresponding mask register. 1b = Interrupt in vendor specific Rx alarms 1. |
| Reserved | 7:3 | RSV | | Reserved. Do not modify. |
| Vendor Specific Tx Alarms 3 Interrupt | 8 | RO | | An interrupt was generated from the status register and the corresponding mask register. 1b = Interrupt in vendor specific Tx alarms 3. |
| Vendor Specific Tx Alarms 2 Interrupt | 9 | RO | | An interrupt was generated from the status register and the corresponding mask register. 1b = Interrupt in vendor specific Tx alarms 2. |
| Vendor Specific Tx Alarms 1 Interrupt | A | RO | | An interrupt was generated from the status register and the corresponding mask register. 1b = Interrupt in vendor specific Tx alarms 1. |
| Reserved | D:B | RSV | | Reserved. Do not modify. |
| Standard Alarms 2 Interrupt | E | RO | | An interrupt was generated from the status register and the corresponding mask register. 1b = Interrupt in standard alarms 2. |



| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------|--------|------|---------|--|
| Standard Alarms 1 Interrupt | F | RO | | An interrupt was generated from the status register and the corresponding mask register. 1b = Interrupt in standard alarms 1. |

4.6.2.4 Auto-negotiation Registers

4.6.2.4.1 Auto-negotiation Standard Control 1: Address 7.0

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------|--------|--------|---------|--|
| Reserved | 8:0 | RSV | | Reserved. Do not modify. |
| Restart Auto-negotiation | 9 | R/W SC | 0b | 0b = Normal operation. 1b = Restart auto-negotiation process. Note: This is a processor intensive operation. Completion of this operation can be monitored via 1E.C831.F (refer to Section 4.6.2.6.83). |
| Reserved | B:A | RSV | | Reserved. Do not modify. |
| Auto-negotiation Enable | C | R/W PD | 1b | When enabled, auto-negotiation determines the link speed. If this bit is disabled, auto-negotiation is disabled. 0b = Disable auto-negotiation. 1b = Enable auto-negotiation. |
| Extended Next Page Control | D | R/W PD | 1b | This bit is OR'ed with bit 7.10.C (refer to Section 4.6.2.4.10). 0b = Extended next pages are disabled. 1b = Extended next pages are enabled. |
| Reserved | E | RSV | | Reserved. Do not modify. |
| Reset | F | R/W SC | 1b | Resets the entire PHY. 0b = Normal operation. 1b = Auto-negotiation reset. The reset bit is automatically cleared upon completion of the reset sequence by the microcontroller. This bit is set to 1b during reset. The reset is internally stretched by approximately 1.7 us. Therefore the MDIO or uP should allow for 1.7 us before writing any auto-negotiation registers after this bit is set. |

4.6.2.4.2 Auto-negotiation Standard Status 1: Address 7.1

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------------|--------|------|---------|--|
| Link Partner Auto-negotiation Ability | 0 | RO | | 0b = Link Partner not able to perform auto-negotiation. 1b = Link Partner able to perform auto-negotiation. |
| Reserved | 1 | RSV | | Reserved. Do not modify. |
| Link Status | 2 | | | This bit is a duplicate of the PMA link status bit in 1.1.2 (refer to Section 4.6.2.1.2). 0b = Link lost since last read. 1b = Link is up. Note: This is latching low, and can only be used to detect link drops, and not the current status of the link without performing back-to-back reads. |



| Field Name | Bit(s) | Type | Default | Description |
|---------------------------|--------|------|---------|---|
| Auto-negotiation Ability | 3 | ROS | 1b | Always set as 1b, as the local device has auto-negotiation ability. 0b = PHY is not able to perform auto-negotiation. 1b = PHY is able to perform auto-negotiation. |
| Remote Fault | 4 | LH | | Indicates that the remote PHY has a fault. 0b = No remote fault condition detected. 1b = Remote fault condition detected. |
| Auto-negotiation Complete | 5 | RO | | Indicates the status of the auto-negotiation receive link. 0b = Auto-negotiation in process. 1b = Auto-negotiation complete. |
| Page Received | 6 | LH | | Indicates that a page has been received. 0b = A page has not been received. 1b = A page has been received. If a regular page, it is placed in 7.13–7.15. If an extended next page, it is placed in registers 7.19–7.1B |
| Extended Next Page Status | 7 | RO | | Indicates that both the local device and the link partner have indicated support for extended next page. 0b = Extended next page is not used. 1b = Extended next page is used. |
| Reserved | 8 | RSV | | Reserved. Do not modify. |
| Parallel Detection Fault | 9 | LH | | 0b = A fault has not been detected via the parallel detection function. 1b = A fault has been detected via the parallel detection function. |
| Reserved | F:A | RSV | | Reserved. Do not modify. |

4.6.2.4.3 Auto-negotiation Standard Device Identifier 1: Address 7.2

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------|--------|------|---------|----------------------------|
| Device ID MSW [1F:10] | F:0 | RO | | Bits [31:16] of Device ID. |

4.6.2.4.4 Auto-negotiation Standard Device Identifier 2: Address 7.3

| Field Name | Bit(s) | Type | Default | Description |
|---------------------|--------|------|---------|---------------------------|
| Device ID LSW [F:0] | F:0 | RO | | Bits [15:0] of Device ID. |

4.6.2.4.5 Auto-negotiation Standard Devices in Package 1: Address 7.5

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------|--------|------|---------|--|
| Clause 22 Registers Present | 0 | ROS | 0b | Always set to 0b, as there are no Clause 22 registers in the X557. 0b = Clause 22 registers are not present in package. 1b = Clause 22 registers are present in package. |



| Field Name | Bit(s) | Type | Default | Description |
|--------------------------|--------|------|---------|---|
| PMA Present | 1 | ROS | 1b | Always set to 1b, as there is PMA functionality in the X557. 0b = PMA is not present. 1b = PMA is present in package. |
| WIS Present | 2 | ROS | 0b | Always set to 0b, as there is no WIS functionality in the X557. 0b = WIS is not present in package. 1b = WIS is present in package. |
| PCS Present | 3 | ROS | 1b | Always set to 1b, as there is PCS functionality in the X557. 0b = PCS is not present in package. 1b = PCS is present in package. |
| PHY XS Present | 4 | ROS | 1b | Always set to 1b, as there is a PHY XS interface in the X557. 0b = PHY XS is not present in package. 1b = PHY XS is present in package. |
| Reserved | 5 | ROS | 0b | Always set to 0b. |
| TC Present | 6 | ROS | 0b | Always set to 0b, as there is no TC functionality in the X557. 0b = TC is not present in package. 1b = TC is present in package. |
| Auto-negotiation Present | 7 | ROS | 1b | Always set to 1b, as there is auto-negotiation in the X557. 0b = Auto-negotiation is not present in package. 1b = Auto-negotiation is present in package. |
| Reserved | F:8 | RSV | | Reserved. Do not modify. |

4.6.2.4.6 Auto-negotiation Standard Devices in Package 2: Address 7.6

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------------|--------|------|---------|---|
| Reserved | C:0 | RSV | | Reserved. Do not modify. |
| Clause 22 Extension Present | D | ROS | 1b | Always set to 1b, as the X557 utilizes this device for the GbE registers. 0b = Clause 22 Extension is not present in package. 1b = Clause 22 Extension is present in package. |
| Vendor Specific Device #1 Present | E | ROS | 1b | Always set to 1b, as the X557 utilizes this device for the Global registers. 0b = Device #1 is not present in package. 1b = Device #1 is present in package. |
| Vendor Specific Device #2 Present | F | ROS | 1b | Always set to 1b, as the X557 utilizes this device for the DSP PMA registers. 0b = Device #2 is not present in package. 1b = Device #2 is present in package. |

4.6.2.4.7 Auto-negotiation Standard Status 2: Address 7.8

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | D:0 | RSV | | Reserved. Do not modify. |



| Field Name | Bit(s) | Type | Default | Description |
|----------------------|--------|------|---------|---|
| Device Present [1:0] | F:E | ROS | 10b | This field is always set to 10b, as the auto-negotiation resides here in the X557. 00b = No device at this address. 01b = No device at this address. 10b = Device present at this address. 11b = No device at this address. |

4.6.2.4.8 Auto-negotiation Standard Package Identifier 1: Address 7.E

| Field Name | Bit(s) | Type | Default | Description |
|------------------------|--------|------|---------|-----------------------------|
| Package ID MSW [1F:10] | F:0 | RO | | Bits [31:16] of Package ID. |

4.6.2.4.9 Auto-negotiation Standard Package Identifier 2: Address 7.F

| Field Name | Bit(s) | Type | Default | Description |
|----------------------|--------|------|---------|----------------------------|
| Package ID LSW [F:0] | F:0 | RO | | Bits [15:0] of Package ID. |

4.6.2.4.10 Auto-negotiation Advertisement Register: Address 7.10

This register is used in conjunction with bit 7.C400.5 to hard provision the auto-negotiation base page that is sent.

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------------|--------|--------|---------|---|
| Selector Field [4:0] | 4:0 | R/W PD | 0x01 | Defines the device compatibility. 00000b = Reserved 00001b = IEEE 802.3 00010b = IEEE 802.9 ISLAN-16T 00011b = IEEE 802.5 00100b = IEEE 1394 All other values are reserved. This field should always be set to 0x01, as the PHY is only capable of handling 802.3 Ethernet. |
| Technology Ability Field [6:0] | B:5 | R/W PD | 0x00 | The Technology Ability Field contains information indicating supported technologies defined in Annex 28B.2 and Annex 28D. Bit [0] = 10BASE-T Bit [1] = 10BASE-T full duplex Bit [2] = 100BASE-TX Bit [3] = 100BASE-TX full duplex Bit [4] = 100BASE-T4 Bit [5] = PAUSE operation for full duplex links Bit [6] = Asymmetric PAUSE operation for full duplex links Multiple technologies may be advertised in the link code word. A device supports the data service ability for a technology it advertises. Since the PHY does not support 10BASE-T or 100BASE-T4, these bits (0, 1, 4) should always be set to zero. |



| Field Name | Bit(s) | Type | Default | Description |
|----------------------------|--------|--------|---------|---|
| Extended Next Page Ability | C | R/W PD | 1b | The Extended Next Page (XNP) bit indicates that the local device supports transmission of extended next pages when set to 1b, and indicates that the local device does not support extended next pages when set to 0. 0b = Not capable of extended next pages. 1b = Extended next page capable. |
| Advertisement Remote Fault | D | R/W | 0b | The remote fault bit provides a standard transport mechanism for the transmission of simple fault information. When the RF bit in the received base link code word is set to 1b, the RF bit is set to 1b. 1b = Remote fault. Note: The PHY does not support a remote fault sensing function. |
| Reserved | E | RSV | | Reserved. Do not modify. |
| Next page Ability | F | R/W PD | 1b | If a device implements Next Page ability and wishes to engage in Next Page exchange, it sets the NP bit to 1b. A device may implement Next Page ability and choose not to engage in Next Page exchange by setting the NP bit to a 0b. 1b = Next page ability. |

4.6.2.4.11 Auto-negotiation Link Partner Base Page Ability Register: Address 7.13

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|---|
| Link Partner Selector Field [4:0] | 4:0 | RO | | Defines the device compatibility. 00000b = Reserved 00001b = IEEE 802.3 00010b = IEEE 802.9 ISLAN-16T 00011b = IEEE 802.5 00100b = IEEE 1394 All other values are reserved. Selector field encodes 32 possible messages defined in Annex 28A. Combinations not specified are reserved for future use and are not transmitted. |
| Link Partner Technology Ability Field [6:0] | B:5 | RO | | Technology ability field contains information indicating supported technologies defined in Annex 28B.2 and Annex 28D. Bit [0] = 10BASE-T Bit [1] = 10BASE-T full duplex Bit [2] = 100BASE-TX Bit [3] = 100BASE-TX full duplex Bit [4] = 100BASE-T4 Bit [5] = PAUSE operation for full duplex links Bit [6] = Asymmetric PAUSE operation for full duplex links Multiple technologies may be advertised in the link code word. A device supports the data service ability for a technology it advertises. The arbitration function determines the common mode of operation shared by a link partner and resolves the multiple common modes. |
| Link Partner Extended Next Page Ability | C | RO | | The extended next page indicates that the link partner has indicated support for the extended next page when set to 1b. When set to 0b, the link partner does not support extended next page. 0b = Not capable of extended next pages. 1b = Extended next page capable. |
| Link Partner Remote Fault | D | RO | | The remote fault bit provides a standard transport mechanism for the transmission of simple fault information. When the RF bit in the received base link code word is set to 1b, the RF bit is set to 1b. 1b = Remote fault. |



| Field Name | Bit(s) | Type | Default | Description |
|------------------------------------|--------|------|---------|--|
| Link Partner Base Page Acknowledge | E | RO | | The Acknowledge (ACK) is used by the auto-negotiation function to indicate that a device has successfully received its Link Partner's Link Code Word. 1b = Acknowledge |
| Link Partner Next Page Ability | F | RO | | If Next Page ability is not supported, the NP bit is always be set to 0b. If a device implements Next Page ability and wishes to engage in Next Page exchange, it shall set the NP bit to logic 1b. 0b = Next page ability not supported or not engaged. 1b = Next page ability. |

4.6.2.4.12 Auto-negotiation Extended Next Page Transmit Register: Address 7.16

This register is used in conjunction with bit 7.C400.5 and registers 7.17 and 7.18 to hard provision the auto-negotiation extended next page that is sent. Using this it is possible to hard-code the 1 GbE and 10 GbE capabilities, as well as short-reach capability.

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------|--------|--------|---------|---|
| Message Code Field [A:0] | A:0 | R/W PD | 0x001 | Interpreted as message code (see 802.3 Appendix 28C) if Message Page bit is set to one (7.16:1). Otherwise interpreted as an unformatted code field. [A:0] = Message Code Field: 0x0 = Reserved 0x1 = Null message 0x2 = Reserved Expansion message 0x3 = Reserved Expansion message 0x4 = Remote fault details message 0x5 = OUI message 0x6 = PHY ID message 0x7 = 100BASE-T2 message 0x8 = 1000BASE-T message 0x9 = 10GBASE-T message |
| Toggle | B | RO | | Value of toggle bit. Set to opposite of corresponding bit in previous page. |
| Acknowledge 2 | C | R/W | 0b | Acknowledge 2 is used by the next page function to indicate that a device has the ability to comply with the message. 0b = Cannot comply with corresponding message. 1b = Complies with corresponding message. |
| Message Page | D | R/W | 0b | Message page is used by the next page function to differentiate a message page from an unformatted page. 0b = Unformatted page. 1b = Message page. |
| Reserved | E | RSV | | Reserved. Do not modify. |
| Next Page | F | R/W | 0b | Next page is used by the next page function to indicate whether or not this is the last next page to be transmitted. 0b = Last page. 1b = Additional next page follows. |



4.6.2.4.13 Auto-negotiation Extended Next Page Unformatted Code Register 1: Address 7.17

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------------|--------|-----------|---------|---------------------------|
| Unformatted Code Field 1 [1F:10] | F:0 | R/W PD | 0x0000 | Unformatted Code Field 1. |

4.6.2.4.14 Auto-negotiation Extended Next Page Unformatted Code Register 2: Address 7.18

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------------|--------|-----------|---------|---------------------------|
| Unformatted Code Field 2 [2F:20] | F:0 | R/W PD | 0x0000 | Unformatted Code Field 2. |

4.6.2.4.15 Auto-negotiation Link Partner Extended Next Page Ability Register: Address 7.19

This register, along with 7.1A and 7.1B, are used to store the received next pages. If an extended next page is used, it is stored in 7.19—7.1B.

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|---|
| Link Partner Message Code Field [A:0] | A:0 | RO | | Interpreted as message code (see 802.3 Appendix 28C) if Message Page bit is set to one (7.16:1). Otherwise interpreted as an unformatted code field. [A:0] = Message Code Field: 0x0 = Reserved 0x1 = Null message 0x2 = Reserved Expansion message 0x3 = Reserved Expansion message 0x4 = Remote fault details message 0x5 = OUI message 0x6 = PHY ID message 0x7 = 100BASE-T2 message 0x8 = 1000BASE-T message 0x9 = 10GBASE-T message |
| Link Partner Toggle | B | RO | | Value of link partner's toggle bit. Set to opposite of corresponding bit in previous page. |
| Link Partner Acknowledge 2 | C | RO | | 0b = Link partner cannot comply with the current next page. 1b = Link partner acknowledges that they can comply with the current next page. |
| Link Partner Message Page | D | RO | | 0b = Unformatted page. 1b = Message page. |
| Link Partner Extended Next Page Acknowledge | E | RO | | Acknowledge is used by the auto-negotiation function to indicate that a device has successfully received its link partners link code word. 0b = Link Partner acknowledges receipt of corresponding page. |
| Link Partner Next Page | F | RO | | 1b = Next page ability. |



4.6.2.4.16 Auto-negotiation Link Partner Extended Next Page Unformatted Code Register 1: Address 7.1A

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|----------------------------------|
| Link Partner Unformatted Code Field 2 [F:0] | F:0 | RO | | Unformatted Code Field 2 [15:0]. |

4.6.2.4.17 Auto-negotiation Link Partner Extended Next Page Unformatted Code Register 2: Address 7.1B

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|----------------------------------|
| Link Partner Unformatted Code Field 1 [F:0] | F:0 | RO | | Unformatted Code Field 1 [15:0]. |

4.6.2.4.18 Auto-negotiation 10GBASE-T Control Register: Address 7.20

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|--------|---------|---|
| LD Loop Timing Ability | 0 | R/W PD | 1b | 0b = Do not advertise PHY as capable of loop timing. 1b = Advertise PHY as capable of loop timing. |
| LD Fast Retrain Ability | 1 | R/W PD | 0b | 0b = Do not advertise PHY as 10GBASET fast retrain capable. 1b = Advertise PHY as 10GBASE-T fast retrain capable. |
| LD PMA Training | 2 | R/W PD | 0b | 0b = Local device requests that Link Partner run PMA training PRBS continuously. 1b = Local device requests that Link Partner reset PMA training PRBS every frame. |
| Reserved | B:3 | RSV | | Reserved. Do not modify. |
| 10GBASE-T Ability | C | R/W PD | 1b | 0b = Do not advertise PHY as 10GBASET capable. 1b = Advertise PHY as 10GBASE-T capable. |
| Port Type | D | R/W PD | 0b | 0b = Single port device. 1b = Multi-port device. |
| MASTER-SLAVE Configuration | E | R/W PD | 0b | 0b = SLAVE 1b = MASTER |
| MASTER-SLAVE Manual Configuration Enable | F | R/W PD | 0b | 0b = Disable MASTER-SLAVE Manual configuration. 1b = Enable MASTER-SLAVE Manual configuration. |

4.6.2.4.19 Auto-negotiation 10GBASE-T Status Register: Address 7.21

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------------|--------|------|---------|---|
| Reserved | 0 | RSV | | Reserved. Do not modify. |
| Link Partner Fast Retrain Ability | 1 | RO | | 0b = Link partner is not capable of 10GBASE-T fast retrain. 1b = Link partner is capable of 10GBASET fast retrain. |
| Reserved | 8:2 | RSV | | Reserved. Do not modify. |



| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------------|--------|------|---------|---|
| Link Partner Training Reset Request | 9 | RO | | 0b = Link partner has requested that PMA PRBS training run continuously. 1b = Link partner has requested that PMA PRBS training be reset every frame. |
| Link Partner Loop Timing Ability | A | RO | | 0b = Link partner is not capable of loop timing. 1b = Link partner is capable of loop timing. |
| Link Partner 10GBASE-T Ability | B | RO | | This bit is only valid when the Page received bit 7.1.6 is set to 1b (refer to Section 4.6.2.4.2). 0b = Link partner is not 10GBASE-T capable. 1b = Link partner is 10GBASE-T capable. |
| Remote Receiver Status | C | RO | | Set by microcontroller. 0b = Remote receiver not OK. 1b = Remote receiver OK. |
| Local Receiver Status | D | RO | | Set by microcontroller. 0b = Local receiver not OK. 1b = Local receiver OK. |
| MASTER-SLAVE Configuration Resolution | E | RO | | 0b = Local PHY resolved to SLAVE. 1b = Local PHY resolved to MASTER. |
| MASTER-SLAVE Configuration Fault | F | LH | | 1b = MASTER-SLAVE configuration fault. |

4.6.2.4.20 Auto-negotiation EEE Advertisement Register: Address 7.3C

| Field Name | Bit(s) | Type | Default | Description |
|-----------------|--------|------|---------|--|
| Reserved | 0 | RSV | | Reserved. Do not modify. |
| 100BASE-TX EEE | 1 | R/W | 0b | 0b = Do not advertise that the 100BASETX has EEE capability. 1b = Advertise that the 100BASE-TX has EEE capability. |
| 1000BASE-T EEE | 2 | R/W | 1b | 0b = Do not advertise that the 1000BASET has EEE capability. 1b = Advertise that the 1000BASE-T has EEE capability. |
| 10GBASE-T EEE | 3 | R/W | 1b | 0b = Do not advertise that the 10GBASET has EEE capability. 1b = Advertise that the 10GBASE-T has EEE capability. |
| 1000BASE-KX EEE | 4 | R/W | 0b | 0b = Do not advertise that the 1000BASEKX has EEE capability. 1b = Advertise that the 1000BASE-KX has EEE capability. |
| 10GBASE-KX4 EEE | 5 | R/W | 0b | 0b = Do not advertise that the 10GBASEKX4 has EEE capability. 1b = Advertise that the 10GBASE-KX4 has EEE capability. |
| 10GBASE-KR EEE | 6 | R/W | 0b | 0b = Do not advertise that the 10GBASEKR has EEE capability. 1b = Advertise that the 10GBASE-KR has EEE capability. |
| Reserved | F:7 | RSV | | Reserved. Do not modify. |

4.6.2.4.21 Auto-negotiation EEE Link Partner Ability Register: Address 7.3D

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | 0 | RSV | | Reserved. Do not modify. |



| Field Name | Bit(s) | Type | Default | Description |
|------------------------------|--------|------|---------|--|
| Link Partner 100BASE-TX EEE | 1 | RO | | 0b = Link partner is advertising that its 100BASE-TX does not have EEE capability. 1b = Link partner is advertising that its 100BASE-TX has EEE capability. |
| Link Partner 1000BASE-T EEE | 2 | RO | | 0b = Link partner is advertising that its 1000BASE-T does not have EEE capability. 1b = Link partner is advertising that its 1000BASE-T has EEE capability. |
| Link Partner 10GBASE-T EEE | 3 | RO | | 0b = Link partner is advertising that its 10GBASE-T does not have EEE capability. 1b = Link partner is advertising that its 10GBASE-T has EEE capability. |
| Link Partner 1000BASE-KX EEE | 4 | RO | | 0b = Link partner is advertising that its 1000BASE-KX does not have EEE capability. 1b = Link partner is advertising that its 1000BASE-KX has EEE capability. |
| Link Partner 10GBASE-KX4 EEE | 5 | RO | | 0b = Link partner is advertising that its 10GBASE-KX4 does not have EEE capability. 1b = Link partner is advertising that its 10GBASE-KX4 has EEE capability. |
| Link Partner 10GBASE-KR EEE | 6 | RO | | 0b = Link partner is advertising that its 10GBASE-KR does not have EEE capability. 1b = Link partner is advertising that its 10GBASE-KR has EEE capability. |
| Reserved | F:7 | RSV | | Reserved. Do not modify. |

4.6.2.4.22 KR0 Auto-negotiation Control: Address 7.C200

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------|--------|--------|---------|---|
| Reserved 2 [8:0] | 8:0 | R/W PD | 0x000 | Reserved for future use. |
| Auto-negotiation Restart | 9 | R/W SC | 0b | 0b = Normal operation. 1b = Restart auto-negotiation. |
| Reserved 1 [1:0] | B:A | R/W PD | 00b | Reserved for future use. |
| Auto-negotiation Enable | C | R/W PD | 0b | 0b = Disable auto-negotiation. 1b = Enable auto-negotiation. |
| Reserved 0 [1:0] | E:D | R/W PD | 00b | Reserved for future use. |
| Reset | F | R/W SC | 1b | 0b = Normal operation. 1b = Auto-negotiation reset. |

4.6.2.4.23 KR0 Auto-negotiation Status: Address 7.C201

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------------|--------|--------|---------|---|
| Link Partner Auto-negotiation Ability | 0 | ROS | 0b | 0b = Link partner is not able to perform auto-negotiation. 1b = Link partner is able to perform auto-negotiation. |
| Reserved 3 [1:0] | 2:1 | R/W PD | 0x0 | Reserved for future use. |
| Auto-negotiation Ability | 3 | ROS | 1b | Always set as 1b, as the local device has auto-negotiation ability. 0b = PHY is not able to perform auto-negotiation. 1b = PHY is able to perform auto-negotiation. |



| Field Name | Bit(s) | Type | Default | Description |
|---------------------------|--------|--------|---------|--|
| Reserved 2 | 4 | R/W PD | 0b | Reserved for future use. |
| Auto-negotiation Complete | 5 | LH | | 0b = Normal operation. 1b = Auto-negotiation complete. |
| Page Received | 6 | LH | | 0b = Normal operation. 1b = A new DME page has been received. |
| Reserved 1 [1:0] | 8:7 | R/W PD | 0x0 | Reserved for future use. |
| Parallel Detection Fault | 9 | LH | | 0b = No fault detected. 1b = Fault detected. |
| Reserved 0 [5:0] | F:A | R/W PD | 0x00 | Reserved for future use. |

4.6.2.4.24 KR0 Auto-negotiation Advertisement Word 1: Address 7.C210

| Field Name | Bit(s) | Type | Default | Description |
|------------------------|--------|--------|---------|--|
| Selector Field [4:0] | 4:0 | R/W PD | 0x01 | Defines the device compatibility: 00000b = Reserved 00001b = IEEE 802.3 00010b = IEEE 802.9 ISLAN-16T 00011b = IEEE 802.5 00100b = IEEE 1394 All other values are reserved. This field should always be set to 00001b, as the PHY is only capable of handling 802.3 Ethernet. |
| Echoed Nonce [4:0] | 9:5 | R/W PD | 0x00 | Echoed nonce. |
| Pause Capability [1:0] | B:A | R/W PD | 00b | Bit [A] = Asymmetric PAUSE operation for full duplex links. Bit [B] = PAUSE operation for full duplex links. |
| Reserved 0 | C | R/W PD | 0b | Reserved for future use. |
| Remote Fault | D | R/W | 0b | The remote fault bit provides a standard transport mechanism for the transmission of simple fault information. When the RF bit in the received base link code word is set to 1b, the RF bit is set to 1b. 1b = Remote fault |
| Acknowledge | E | R/W PD | 0b | The Acknowledge (Ack) is used by the auto-negotiation function to indicate that a device has successfully received its Link Partner's Link Code Word. 0b = No fault detected 1b = Acknowledge |
| Next Page | F | R/W PD | 0b | 0b = Next page ability not supported or not engaged. 1b = Next page ability. |



4.6.2.4.25 KR0 Auto-negotiation Advertisement Word 2: Address 7.C211

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|--------|---------|--|
| Transmitted Nonce [4:0] | 4:0 | R/W PD | 0x00 | Transmitted nonce. |
| Technology Ability Bit A0 | 5 | R/W PD | 1b | 0b = 10GBASE-KX is not supported. 1b = 10GBASE-KX is supported. |
| Technology Ability Bit A1 | 6 | R/W PD | 0b | 0b = 10GBASE-KX4 is not supported. 1b = 10GBASE-KX4 is supported. |
| Technology Ability Bit A2 | 7 | R/W PD | 1b | 0b = 10GBASE-KR is not supported. 1b = 10GBASE-KR is supported. |
| Technology Ability Bits A3 to A10 [7:0] | F:8 | R/W PD | 0x00 | Reserved for future technology. |

4.6.2.4.26 KR0 Auto-negotiation Advertisement Word 3: Address 7.C212

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|--------|---------|--|
| Technology Ability Bits A11 to A24 [D:0] | D:0 | R/W PD | 0x0000 | Reserved for future technology. |
| FEC Ability | E | R/W PD | 0b | 0b = 10GBASE-KR PHY does not have FEC capability. 1b = 10GBASE-KR PHY has FEC capability. |
| FEC Requested | F | R/W PD | 0b | 0b = Disable 10GBASE-KR FEC ability. 1b = Enable 10GBASE-KR FEC ability. |

4.6.2.4.27 KR0 Link Partner Auto-negotiation Advertisement Word 1: Address 7.C213

| Field Name | Bit(s) | Type | Default | Description |
|-------------------------------------|--------|------|---------|--|
| Link Partner Selector Field [4:0] | 4:0 | RO | | Defines the device compatibility: 00000b = Reserved 00001b = IEEE 802.3 00010b = IEEE 802.9 ISLAN-16T 00011b = IEEE 802.5 00100b = IEEE 1394 All other values are reserved. This field should always be set to 00001b, as the PHY is only capable of handling 802.3 Ethernet. |
| Link Partner Echoed Nonce [4:0] | 9:5 | RO | | Echoed nonce. |
| Link Partner Pause Capability [1:0] | B:A | RO | | Bit [A] = Asymmetric PAUSE operation for full duplex links. Bit [B] = PAUSE operation for full duplex links. |
| Reserved 0 | C | RO | | Reserved for future use. |



| Field Name | Bit(s) | Type | Default | Description |
|---------------------------|--------|------|---------|--|
| Link Partner Remote Fault | D | RO | | The remote fault bit provides a standard transport mechanism for the transmission of simple fault information. When the RF bit in the received base link code word is set to 1b, the RF bit is set to 1b. 1b = Remote fault |
| Link Partner Acknowledge | E | RO | | The Acknowledge (Ack) is used by the auto-negotiation function to indicate that a device has successfully received its Link Partner's Link Code Word. 0b = No fault detected 1b = Acknowledge |
| Link Partner Next Page | F | RO | | 0b = Next page ability not supported or not engaged. 1b = Next page ability. |

4.6.2.4.28 KR0 Link Partner Auto-negotiation Advertisement Word 2: Address 7.C214

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|--|
| Link Partner Transmitted Nonce [4:0] | 4:0 | RO | | Transmitted nonce. |
| Link Partner Technology Ability Bit A0 | 5 | RO | | 0b = 10GBASE-KX is not supported. 1b = 10GBASE-KX is supported. |
| Link Partner Technology Ability Bit A1 | 6 | RO | | 0b = 10GBASE-KX4 is not supported. 1b = 10GBASE-KX4 is supported. |
| Link Partner Technology Ability Bit A2 | 7 | RO | | 0b = 10GBASE-KR is not supported. 1b = 10GBASE-KR is supported. |
| Link Partner Technology Ability Bits A3 to A10 [7:0] | F:8 | RO | | Reserved for future technology. |

4.6.2.4.29 KR0 Link Partner Auto-negotiation Advertisement Word 3: Address 7.C215

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|--|
| Link Partner Technology Ability Bits A11 to A24 [D:0] | D:0 | RO | | Reserved for future technology. |
| Link Partner FEC Ability | E | RO | | 0b = 10GBASE-KR PHY does not have FEC capability. 1b = 10GBASE-KR PHY has FEC capability. |
| Link Partner FEC Requested | F | RO | | 0b = Disable 10GBASE-KR FEC ability. 1b = Enable 10GBASE-KR FEC ability. |

4.6.2.4.30 KR0 Auto-negotiation Extended Next Page Advertisement Word 1: Address 7.C216

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------|--------|--------|---------|---------------------------------|
| Extended Next Page 0 [F:0] | F:0 | R/W PD | 0x0000 | Extended next page, Bits [F:0]. |



4.6.2.4.31 KR0 Auto-negotiation Extended Next Page Advertisement Word 2: Address 7.C217

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------|--------|--------|---------|-----------------------------------|
| Extended Next Page 1 [F:0] | F:0 | R/W PD | 0x0000 | Extended next page, Bits [1F:10]. |

4.6.2.4.32 KR0 Auto-negotiation Extended Next Page Advertisement Word 3: Address 7.C218

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------|--------|--------|---------|-----------------------------------|
| Extended Next Page 2 [F:0] | F:0 | R/W PD | 0x0000 | Extended next page, Bits [2F:20]. |

4.6.2.4.33 KR0 Link Partner Auto-negotiation Extended Next Page Advertisement Word 1: Address 7.C219

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|---------------------------------|
| Link Partner Extended Next Page 0 [F:0] | F:0 | RO | | Extended next page, Bits [F:0]. |

4.6.2.4.34 KR0 Link Partner Auto-negotiation Extended Next Page Advertisement Word 2: Address 7.C21A

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|-----------------------------------|
| Link Partner Extended Next Page 1 [F:0] | F:0 | RO | | Extended next page, Bits [1F:10]. |

4.6.2.4.35 KR0 Link Partner Auto-negotiation Extended Next Page Advertisement Word 3: Address 7.C21B

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|-----------------------------------|
| Link Partner Extended Next Page 2 [F:0] | F:0 | RO | | Extended next page, Bits [2F:20]. |

4.6.2.4.36 KR1 Auto-negotiation Control: Address 7.C300

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------|--------|--------|---------|--|
| Reserved 2 [8:0] | 8:0 | R/W PD | 0x000 | Reserved for future use. |
| Auto-negotiation Restart | 9 | R/W SC | 0b | 0b = Normal operation. 1b = Restart auto-negotiation. |
| Reserved 1 [1:0] | B:A | R/W PD | 00b | Reserved for future use. |



| Field Name | Bit(s) | Type | Default | Description |
|-------------------------|--------|--------|---------|---|
| Auto-negotiation Enable | C | R/W PD | 0b | 0b = Disable auto-negotiation. 1b = Enable auto-negotiation. |
| Reserved 0 [1:0] | E:D | R/W PD | 00b | Reserved for future use. |
| Reset | F | R/W SC | 1b | 0b = Normal operation. 1b = Auto-negotiation reset. |

4.6.2.4.37 KR1 Auto-negotiation Status: Address 7.C301

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------------|--------|--------|---------|---|
| Link Partner Auto-negotiation Ability | 0 | ROS | 0b | 0b = Link partner is not able to perform auto-negotiation. 1b = Link partner is able to perform auto-negotiation. |
| Reserved 3 [1:0] | 2:1 | R/W PD | 0x0 | Reserved for future use. |
| Auto-negotiation Ability | 3 | ROS | 1b | Always set as 1b, as the local device has auto-negotiation ability. 0b = PHY is not able to perform auto-negotiation. 1b = PHY is able to perform auto-negotiation. |
| Reserved 2 | 4 | R/W PD | 0b | Reserved for future use. |
| Auto-negotiation Complete | 5 | LH | | 0b = Normal operation. 1b = Auto-negotiation complete. |
| Page Received | 6 | LH | | 0b = Normal operation. 1b = A new DME page has been received. |
| Reserved 1 [1:0] | 8:7 | R/W PD | 0x0 | Reserved for future use. |
| Parallel Detection Fault | 9 | LH | | 0b = No fault detected. 1b = Fault detected. |
| Reserved 0 [5:0] | F:A | R/W PD | 0x00 | Reserved for future use. |

4.6.2.4.38 KR1 Auto-negotiation Advertisement Word 1: Address 7.C310

| Field Name | Bit(s) | Type | Default | Description |
|----------------------|--------|--------|---------|--|
| Selector Field [4:0] | 4:0 | R/W PD | 0x01 | Defines the device compatibility: 00000b = Reserved 00001b = IEEE 802.3 00010b = IEEE 802.9 ISLAN-16T 00011b = IEEE 802.5 00100b = IEEE 1394 All other values are reserved. This field should always be set to 00001b, as the PHY is only capable of handling 802.3 Ethernet. |
| Echoed Nonce [4:0] | 9:5 | R/W PD | 0x00 | Echoed nonce. |



| Field Name | Bit(s) | Type | Default | Description |
|------------------------|--------|-----------|---------|--|
| Pause Capability [1:0] | B:A | R/W PD | 00b | Bit [A] = Asymmetric PAUSE operation for full duplex links. Bit [B] = PAUSE operation for full duplex links. |
| Reserved 0 | C | R/W PD | 0b | Reserved for future use. |
| Remote Fault | D | R/W | 0b | The remote fault bit provides a standard transport mechanism for the transmission of simple fault information. When the RF bit in the received base link code word is set to 1b, the RF bit is set to 1b. 1b = Remote fault |
| Acknowledge | E | R/W PD | 0b | The Acknowledge (Ack) is used by the auto-negotiation function to indicate that a device has successfully received its Link Partner's Link Code Word. 0b = No fault detected 1b = Acknowledge |
| Next Page | F | R/W PD | 0b | 0b = Next page ability not supported or not engaged. 1b = Next page ability. |

4.6.2.4.39 KR1 Auto-negotiation Advertisement Word 2: Address 7.C311

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|-----------|---------|--|
| Transmitted Nonce [4:0] | 4:0 | R/W PD | 0x00 | Transmitted nonce. |
| Technology Ability Bit A0 | 5 | R/W PD | 1b | 0b = 10GBASE-KX is not supported. 1b = 10GBASE-KX is supported. |
| Technology Ability Bit A1 | 6 | R/W PD | 0b | 0b = 10GBASE-KX4 is not supported. 1b = 10GBASE-KX4 is supported. |
| Technology Ability Bit A2 | 7 | R/W PD | 1b | 0b = 10GBASE-KR is not supported. 1b = 10GBASE-KR is supported. |
| Technology Ability Bits A3 to A10 [7:0] | F:8 | R/W PD | 0x00 | Reserved for future technology. |

4.6.2.4.40 KR1 Auto-negotiation Advertisement Word 3: Address 7.C312

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|-----------|---------|--|
| Technology Ability Bits A11 to A24 [D:0] | D:0 | R/W PD | 0x0000 | Reserved for future technology. |
| FEC Ability | E | R/W PD | 0b | 0b = 10GBASE-KR PHY does not have FEC capability. 1b = 10GBASE-KR PHY has FEC capability. |
| FEC Requested | F | R/W PD | 0b | 0b = Disable 10GBASE-KR FEC ability. 1b = Enable 10GBASE-KR FEC ability. |



4.6.2.4.41 KR1 Link Partner Auto-negotiation Advertisement Word 1: Address 7.C313

| Field Name | Bit(s) | Type | Default | Description |
|-------------------------------------|--------|------|---------|--|
| Link Partner Selector Field [4:0] | 4:0 | RO | | Defines the device compatibility: 00000b = Reserved 00001b = IEEE 802.3 00010b = IEEE 802.9 ISLAN-16T 00011b = IEEE 802.5 00100b = IEEE 1394 All other values are reserved. This field should always be set to 00001b, as the PHY is only capable of handling 802.3 Ethernet. |
| Link Partner Echoed Nonce [4:0] | 9:5 | RO | | Echoed nonce. |
| Link Partner Pause Capability [1:0] | B:A | RO | | Bit [A] = Asymmetric PAUSE operation for full duplex links. Bit [B] = PAUSE operation for full duplex links. |
| Reserved 0 | C | RO | | Reserved for future use. |
| Link Partner Remote Fault | D | RO | | The remote fault bit provides a standard transport mechanism for the transmission of simple fault information. When the RF bit in the received base link code word is set to 1b, the RF bit is set to 1b. 1b = Remote fault |
| Link Partner Acknowledge | E | RO | | The Acknowledge (Ack) is used by the auto-negotiation function to indicate that a device has successfully received its Link Partner's Link Code Word. 0b = No fault detected 1b = Acknowledge |
| Link Partner Next Page | F | RO | | 0b = Next page ability not supported or not engaged. 1b = Next page ability. |

4.6.2.4.42 KR1 Link Partner Auto-negotiation Advertisement Word 2: Address 7.C314

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|--|
| Link Partner Transmitted Nonce [4:0] | 4:0 | RO | | Transmitted nonce. |
| Link Partner Technology Ability Bit A0 | 5 | RO | | 0b = 10GBASE-KX is not supported. 1b = 10GBASE-KX is supported. |
| Link Partner Technology Ability Bit A1 | 6 | RO | | 0b = 10GBASE-KX4 is not supported. 1b = 10GBASE-KX4 is supported. |
| Link Partner Technology Ability Bit A2 | 7 | RO | | 0b = 10GBASE-KR is not supported. 1b = 10GBASE-KR is supported. |
| Link Partner Technology Ability Bits A3 to A10 [7:0] | F:8 | RO | | Reserved for future technology. |



4.6.2.4.43 KR1 Link Partner Auto-negotiation Advertisement Word 3: Address 7.C315

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|--|
| Link Partner Technology Ability Bits A11 to A24 [D:0] | D:0 | RO | | Reserved for future technology. |
| Link Partner FEC Ability | E | RO | | 0b = 10GBASE-KR PHY does not have FEC capability. 1b = 10GBASE-KR PHY has FEC capability. |
| Link Partner FEC Requested | F | RO | | 0b = Disable 10GBASE-KR FEC ability. 1b = Enable 10GBASE-KR FEC ability. |

4.6.2.4.44 KR1 Auto-negotiation Extended Next Page Advertisement Word 1: Address 7.C316

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------|--------|--------|---------|---------------------------------|
| Extended Next Page 0 [F:0] | F:0 | R/W PD | 0x0000 | Extended next page, Bits [F:0]. |

4.6.2.4.45 KR1 Auto-negotiation Extended Next Page Advertisement Word 2: Address 7.C317

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------|--------|--------|---------|-----------------------------------|
| Extended Next Page 1 [F:0] | F:0 | R/W PD | 0x0000 | Extended next page, Bits [1F:10]. |

4.6.2.4.46 KR1 Auto-negotiation Extended Next Page Advertisement Word 3: Address 7.C318

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------|--------|--------|---------|-----------------------------------|
| Extended Next Page 2 [F:0] | F:0 | R/W PD | 0x0000 | Extended next page, Bits [2F:20]. |

4.6.2.4.47 KR1 Link Partner Auto-negotiation Extended Next Page Advertisement Word 1: Address 7.C319

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|---------------------------------|
| Link Partner Extended Next Page 0 [F:0] | F:0 | RO | | Extended next page, Bits [F:0]. |



4.6.2.4.48 KR1 Link Partner Auto-negotiation Extended Next Page Advertisement Word 2: Address 7.C31A

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|-----------------------------------|
| Link Partner Extended Next Page 1 [F:0] | F:0 | RO | | Extended next page, Bits [1F:10]. |

4.6.2.4.49 KR1 Link Partner Auto-negotiation Extended Next Page Advertisement Word 3: Address 7.C31B

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|-----------------------------------|
| Link Partner Extended Next Page 2 [F:0] | F:0 | RO | | Extended next page, Bits [2F:20]. |

4.6.2.4.50 Auto-negotiation Vendor Provisioning 1: Address 7.C400

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------------|--------|--------|---------|---|
| Retry Attempts Before Downshift [3:0] | 3:0 | R/W PD | 0x4 | Number of retry attempts before downshift. If automatic downshifting is enabled, this is the number of retry attempts the PHY makes to connect at the maximum mutually-acceptable rate, before removing this rate from the list and trying the next lower rate. |
| Automatic Downshift Enable | 4 | R/W PD | 1b | 0b = Manual downshift. 1b = Enable automatic downshift. |
| User Provided Auto-negotiation Data | 5 | R/W PD | 0b | If this bit is set, the PHY attempts to use the user-provided auto-negotiation words. If there is a mismatch (such as a legacy 1GBASE-T device attempting connect), the PHY then attempts to construct a new set of auto-negotiation words from the data provided in these words. Otherwise, the PHY constructs the correct auto-negotiation words based on the provisioned values. 0b = Construct the correct auto-negotiation words based on the register settings of 7.10, 7.20, and 7.C400. 1b = User provides the next page or extended next page data directly (7.16 -> 7.18), and the configuration info in 7.20 and 7.C400 is ignored. |
| Exchange PHY ID Information | 6 | R/W PD | 1b | 1b = Exchange PHY ID Information. |
| Reserved1 [2:0] | 9:7 | R/W PD | 000b | Reserved for future use. |
| Reserved | C:A | RSV | | Reserved. Do not modify. |
| Short-Reach | D | R/W PD | 0b | 0b = Do not advertise PHY as operating in short-reach mode. 1b = Advertise PHY as operating in short-reach mode. |
| 1000BASE-T Half Duplex Ability | E | R/W PD | 0b | 0b = Do not advertise PHY as 1000BASE-T Half Duplex capable. 1b = Advertise PHY as 1000BASE-T Half Duplex capable. |
| 1000BASE-T Full Duplex Ability | F | R/W PD | 0b | 0b = Do not advertise PHY as 1000BASE-T Full Duplex capable. 1b = Advertise PHY as 1000BASE-T Full Duplex capable. |



4.6.2.4.51 Auto-negotiation Reserved Vendor Provisioning 1: Address 7.C410

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------------------|--------|--------|---------|--|
| MDI / MDI-X Control [1:0] | 1:0 | R/W PD | 00b | Used to force a manual MDI or MDI-X configuration. 00b = Automatic MDI / MDI-X operation 01b = Manual MDI 10b = Manual MDI-X 11b = Reserved |
| Extra Page Count [3:0] | 5:2 | R/W PD | 0x0 | Number of extra pages to send at end of auto-negotiation sequence when link partner is legacy Gigabit PHY. Intervals between pages for GbE PHYs may be much longer. When this is the case, the link partner may still be in auto-negotiation when the X557 has started training. This may confuse the link partner MDI/MDI-X state machine. Sending extra pages seems to solve this problem. |
| Reserved | 6 | R/W PD | 0b | 1b = Reserved. |
| Reserved | 7 | R/W PD | 0b | 1b = Reserved |
| Semi-Cross Link Attempt Period [2:0] | A:8 | R/W PD | 000b | Number of failed link attempts before trying semi cross. Set to zero to disable semi-cross. Set to 0x7 to always use semi-cross. |
| Reserved Provisioning 0 [1:0] | C:B | R/W PD | 00b | Reserved for future use. |
| SERDES Start-Up Mode [2:0] | F:D | R/W PD | 000b | The state up mode of the MAC interface: 000b = Selected 10G interface on with automatic rate select. 001b = Reserved. 010b = Reserved. 011b = Reserved. 100b = 1000BASE-X on with automatic rate select and no SGMII auto-negotiation. 101b = Reserved. 110b = All interfaces off with automatic rate select. 111b = Reserved. This sets the start-up mode for the MAC interface. In all scenarios, the X557 sets the interface rate based on the auto-negotiated line rate. The interface selection controls are in 4.C441 (refer to Section 4.6.2.3.21). |

4.6.2.4.52 Auto-negotiation Vendor Status 1: Address 7.C800

| Field Name | Bit(s) | Type | Default | Description |
|--------------|--------|------|---------|---|
| Connect Rate | 2:1 | RO | | The rate the PHY connected or attempting to connect at: 0x3 = 10GBASE-T 0x2 = 1000BASE-T 0x1 = 100BASE-TX 0x0 = 10BASE-T This field is used in conjunction with "Connection State" in "Auto-negotiation Reserved Vendor Status 1: Address 7.C810" on page 160 to indicated the duplex method the PHY is connected or attempting to connect at. |



| Field Name | Bit(s) | Type | Default | Description |
|--------------|--------|------|---------|---|
| Connect Type | 0 | RO | | The duplex method the PHY connected or attempting to connect at: 0b = Half-Duplex 1b = Full Duplex This field is used in conjunction with "Connection State" in "Auto-negotiation Reserved Vendor Status 1: Address 7.C810" on page 160 to indicated the duplex method the PHY is connected or attempting to connect at. |
| Reserved | F:1 | RSV | | Reserved. Do not modify. |

4.6.2.4.53 Auto-negotiation Reserved Vendor Status 1: Address 7.C810

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|---|
| Transmit PAUSE Resolution | 0 | RO | | PAUSE resolution from 28B-3. 0b = Transmit PAUSE Disabled. 1b = Transmit PAUSE Enabled. |
| Receive PAUSE Resolution | 1 | RO | | PAUSE resolution from 28B-3. 0b = Receive PAUSE Disabled. 1b = Receive PAUSE Enabled. |
| Reserved Status 1 [6:2] | 6:2 | RO | | Reserved for future use. |
| Duplicate Link Partner Auto-negotiation Ability | 7 | RO | | Link Partner is capable of auto-negotiation. This is a duplicate of the bit at 7.1.0 (refer to Section 4.6.2.4.2). |
| MDI/MDI-X | 8 | RO | | When auto-negotiation is completed, this register indicates whether the connection was made as an MDI or MDI-X connection. 0b = MDI 1b = MDI-X |
| Connection State [4:0] | D:9 | RO | | The current state of the connection: 00000b = Inactive (i.e. high-impedance) 00001b = Cable diagnostics 00010b = Auto-negotiation 00011b = Training (10 GbE and 1GbE only) 00100b = Connected 00101b = Fail (Auto-negotiation Break Link) 00110b = Test Mode 00111b = Loopback Mode 01000b = Low Power Mode 01001b = Connected Wake-On-LAN Mode 01010b = System Calibrating 01011b = Cable Disconnected 11111b = Invalid All other values are reserved Used in conjunction with "Connect Type" in "Auto-negotiation Vendor Status 1: Address 7.C800" on page 159 to indicate the current state of the PHY. |
| Device Present | E | RO | | If true, a far-end Ethernet device exists, as valid link pulses have been detected in the most recent auto-negotiation session, or a valid Ethernet connection has been established. If false, no connection is established, and the most recent attempt at auto-negotiation failed to detect any valid link pulses. Specifically, when MDI/MDI-X resolution has completed, this bit is true. This bit is set false before entering auto-negotiation. 0b = No far-end Ethernet device detected. 1b = Far-end Ethernet device present. |



| Field Name | Bit(s) | Type | Default | Description |
|----------------|--------|------|---------|--|
| Energy On Line | F | RO | | Used to indicate that the PHY has detected energy on the line. Specifically, when MDI/MDI-X resolution has completed, this bit is true. This bit is set false before entering auto-negotiation. 0b = No energy detected on line. 1b = Energy detected on line. |

4.6.2.4.54 Auto-negotiation Reserved Vendor Status 2: Address 7.C811

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------|--------|------|---------|--|
| Auto-negotiation Attempts [F:0] | F:0 | RO | | The number of auto-negotiation attempts since the last successful connection (or power-up). This is a rolling counter (i.e., upon saturation it reverts to zero). It is cleared upon reset, or the completion of a successful connection. |

4.6.2.4.55 Auto-negotiation Reserved Vendor Status 3: Address 7.C812

| Field Name | Bit(s) | Type | Default | Description |
|------------------------|--------|------|---------|--------------------------|
| Reserved State 3 [F:0] | F:0 | RO | | Reserved for future use. |

4.6.2.4.56 Auto-negotiation Reserved Vendor Status 4: Address 7.C813

| Field Name | Bit(s) | Type | Default | Description |
|------------------------|--------|------|---------|--------------------------|
| Reserved State 4 [F:0] | F:0 | RO | | Reserved for future use. |

4.6.2.4.57 Auto-negotiation Reserved Vendor Status 5: Address 7.C814

| Field Name | Bit(s) | Type | Default | Description |
|------------------------|--------|------|---------|--------------------------|
| Reserved State 5 [F:0] | F:0 | RO | | Reserved for future use. |

4.6.2.4.58 Auto-negotiation Transmit Vendor Alarms 1: Address 7.CC00

| Field Name | Bit(s) | Type | Default | Description |
|-------------------------|--------|------|---------|---|
| Connection State Change | 0 | LH | | Indicates a change in "Connection State [D:B]" in "Auto-negotiation Reserved Vendor Status 1: Address 7.C810" on page 160. 1b = The connection state has changed. Note: This indicates any state change, versus 7.CC01.0, which indicates a connect or disconnect event. |



| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|---|
| Automatic Downshift | 1 | LH | | 1b = Automatic downshift has occurred. |
| Auto-negotiation Completed for Supported Rate | 2 | LH | | 1b = Auto-negotiation has completed successfully for a rate that is supported by the X557. |
| Auto-negotiation Completed For Non-supported Rate | 3 | LH | | Indicates that the X557 has completed auto-negotiation, and was unable to agree on a rate that both could operate at. Indication should be ignored in case of Master/Slave resolution fault. 1b = Auto-negotiation has completed for a rate that is not supported by the X557. |
| Reserved | F:4 | RSV | | Reserved. Do not modify. |

4.6.2.4.59 Auto-negotiation Transmit Vendor Alarms 2: Address 7.CC01

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------------|--------|------|---------|---|
| Link Connect/Disconnect | 0 | LH | | Indicates whether the link has achieved a connect state, or was in a connect state and disconnected. 1b = MDI Link has either connected or disconnected. |
| Reserved Vendor Alarms 2 [E:0] | F:1 | LH | | Reserved for future use. |

4.6.2.4.60 Auto-negotiation Standard Interrupt Mask 1: Address 7.D000

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------------|--------|--------|---------|---|
| Reserved | 1:0 | RSV | | Reserved. Do not modify. |
| Parallel Detection Fault Mask | 2 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | 3 | RSV | | Reserved. Do not modify. |
| Extended Next Page Received Mask | 4 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | 5 | RSV | | Reserved. Do not modify. |
| Remote Fault Mask | 6 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | 8:7 | RSV | | Reserved. Do not modify. |
| Link Status Mask | 9 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | F:A | RSV | | Reserved. Do not modify. |

4.6.2.4.61 Auto-negotiation Standard Interrupt Mask 2: Address 7.D001

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | E:0 | RSV | | Reserved. Do not modify. |



| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------------|--------|--------|---------|---|
| MASTER-SLAVE Configuration Fault Mask | F | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |

4.6.2.4.62 Auto-negotiation Transmit Vendor Interrupt Mask 1: Address 7.D400

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|--------|---------|---|
| Connection State Change Mask | 0 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Automatic Downshift Mask | 1 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Auto-negotiation Completed for Supported Rate Mask | 2 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Auto-negotiation Completed For Non-supported Rate Mask | 3 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | F:4 | RSV | | Reserved. Do not modify. |

4.6.2.4.63 Auto-negotiation Transmit Vendor Interrupt Mask 2: Address 7.D401

| Field Name | Bit(s) | Type | Default | Description |
|-------------------------------------|--------|--------|---------|---|
| Link Connect/Disconnect Mask | 0 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved Vendor Alarms 2 Mask [E:0] | F:1 | R/W PD | 0x0000 | Reserved for future use. |

4.6.2.4.64 Auto-negotiation Transmit Vendor Interrupt Mask 3: Address 7.D402

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |

4.6.2.4.65 Auto-negotiation Receive Link Partner Status 1: Address 7.E820

| Field Name | Bit(s) | Type | Default | Description |
|--------------------|--------|------|---------|--|
| Reserved | 1:0 | RSV | | Reserved. Do not modify. |
| Intel Link Partner | 2 | RO | | 0b = Link Partner is not an Intel PHY. 1b = Link Partner is an Intel PHY. |
| Reserved2 [6:0] | 9:3 | RO | | Reserved for future use. |



| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|--|
| Reserved | C:A | RSV | | Reserved. Do not modify. |
| Link Partner Short-Reach | D | RO | | 0b = Link Partner is not operating in short-reach mode. 1b = Link Partner is operating in short-reach mode. |
| Link Partner 1000BASE-T Half Duplex Ability | E | RO | | 0b = Link Partner is not 1000BASE-T Half-Duplex capable. 1b = Link Partner is 1000BASE-T Half-Duplex capable. |
| Link Partner 1000BASE-T Full Duplex Ability | F | RO | | 0b = Link Partner is not 1000BASE-T Full Duplex capable. 1b = Link Partner is 1000BASE-T Full Duplex capable. |

4.6.2.4.66 Auto-negotiation Receive Link Partner Status 2: Address 7.E821

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |

4.6.2.4.67 Auto-negotiation Receive Link Partner Status 3: Address 7.E822

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |

4.6.2.4.68 Auto-negotiation Receive Link Partner Status 4: Address 7.E823

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|---|
| Link Partner Firmware Minor Revision Number [7:0] | 7:0 | RO | | Link partner firmware minor revision number. Only the lower six bits of major and minor firmware revision are exchanged in auto-negotiation when the PHYID message is sent. Consequently the upper 2 bits of the major and minor revision should always be zero. |
| Link Partner Firmware Major Revision Number [7:0] | F:8 | RO | | Link partner firmware major revision number. Only the lower six bits of major and minor firmware revision are exchanged in auto-negotiation when the PHYID message is sent. Consequently the upper 2 bits of the major and minor revision should always be zero. |

4.6.2.4.69 Auto-negotiation Receive Reserved Vendor Status 1: Address 7.E830

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------|--------|------|---------|--------------------------|
| Reserved Receive Status 1 [8:0] | 8:0 | RO | | Reserved for future use. |



| Field Name | Bit(s) | Type | Default | Description |
|----------------------------|--------|------|---------|--|
| Link Partner PHY Tag [2:0] | B:9 | RO | | When the link partner is Intel and PHY ID pages have been exchanged, this field contains the vendor specific link partner PHY tag value. This field is only valid if the link partner is Intel/X540, and PHY ID link pages have been exchanged during auto-negotiation. |
| Link Attempts [3:0] | F:C | RO | | Number of attempts needed to establish current link. Once a link has been established, save the total number of auto-negotiation and training sequence passes. |

4.6.2.4.70 Auto-negotiation Receive Reserved Vendor Status 2: Address 7.E831

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------------|--------|------|---------|---|
| Reserved Receive State 2 [B:0] | B:0 | RO | | State bit associated with "Reserved Receive Vendor Alarms 2 [B:0]" in "Auto-negotiation Receive Vendor Alarms 2: Address 7.EC01" on page 166. Reserved for future use. |
| FLP Idle Error State | C | RO | | State bit associated with "FLP Idle Error" in "Auto-negotiation Receive Vendor Alarms 2: Address 7.EC01" on page 166. 1b = No FLP Burst has been seen for 50 ms, forcing the receive state machine back to the Idle state. |
| Auto-negotiation Protocol Error State | D | RO | | State bit associated with "Auto-negotiation Protocol Error" in "Auto-negotiation Receive Vendor Alarms 2: Address 7.EC01" on page 166. 1b = Link partner has violated the auto-negotiation protocol. |
| Reserved | F:E | RSV | | Reserved. Do not modify. |

4.6.2.4.71 Auto-negotiation Receive Reserved Vendor Status 3: Address 7.E832

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------------|--------|------|---------|---|
| Link Partner AFR Enabled | 0 | RO | | 1b = The link partner has Fast Re-frame capability enabled. |
| Reserved Receive State 3 [E:0] | F:1 | RO | | Reserved for future use. |

4.6.2.4.72 Auto-negotiation Receive Vendor Alarms 1: Address 7.EC00

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |



4.6.2.4.73 Auto-negotiation Receive Vendor Alarms 2: Address 7.EC01

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|--|
| Auto-negotiation Protocol Error | B:0 | LH | | Reserved for future use. |
| FLP Idle Error | C | LH | | Once FLP bursts are detected on any receive channel, they must keep coming. If no burst has been detected for a period of 50 ms, the auto-negotiation process resets itself and goes back to the "break link" state. 1b = No FLP Burst has been seen for 50 ms, forcing the receive state machine back to the Idle state. |
| Reserved Receive Vendor Alarms 2 [B:0] | D | LH | | If the Arbiter state machine detects a protocol violation, the auto-negotiation process resets itself and goes back to the "break link" state. 1b = Link partner has violated the auto-negotiation protocol. |
| Reserved | F:E | RSV | | Reserved. Do not modify. |

4.6.2.4.74 Auto-negotiation Receive Vendor Alarms 3: Address 7.EC02

| Field Name | Bit(s) | Type | Default | Description |
|------------------------|--------|------|---------|---|
| Reserved | 1:0 | RSV | | Reserved. Do not modify. |
| 10BASE-T Device Detect | 2 | LL | | Indicates that the detected far-end device is 10BASE-T when it is 0b. This bit is 1b when link pulses are no longer received. 0b = 10BASE-T device detected. |
| Reserved | F:3 | RSV | | Reserved. Do not modify. |

4.6.2.4.75 Auto-negotiation Receive Vendor Alarms 4: Address 7.EC03

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|--|
| 100BASE-TX Parallel Detect | 0 | LH | | 1b = 100BASE-TX parallel event detection occurred. |
| Reserved Receive Vendor Alarms 4 [E:0] | F:1 | LH | | Reserved for future use. |

4.6.2.4.76 Auto-negotiation Receive Vendor Interrupt Mask 1: Address 7.F400

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|--------|---------|---|
| Reserved Receive Vendor Alarms 1 Mask [F:0] | F:0 | R/W PD | 0x0000 | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |



4.6.2.4.77 Auto-negotiation Receive Vendor Interrupt Mask 2: Address 7.F401

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|--------|---------|---|
| Reserved Receive Vendor Alarms 2 Mask [B:0] | B:0 | R/W PD | 0x000 | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| FLP Idle Error Mask | C | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Auto-negotiation Protocol Error Mask | D | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | F:E | RSV | | Reserved. Do not modify. |

4.6.2.4.78 Auto-negotiation Receive Vendor Interrupt Mask 3: Address 7.F402

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------|--------|--------|---------|---|
| Reserved | 1:0 | RSV | | Reserved. Do not modify. |
| 10BASE-T Device Detect Mask | 2 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | F:3 | RSV | | Reserved. Do not modify. |

4.6.2.4.79 Auto-negotiation Receive Vendor Interrupt Mask 4: Address 7.F403

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|--------|---------|---|
| 100BASE-TX Parallel Detect Mask | 0 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved Receive Vendor Alarms 4 Mask [E:0] | F:1 | R/W PD | 0x0000 | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |

4.6.2.4.80 Auto-negotiation Vendor Global Interrupt Flags 1: Address 7.FC00

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------------|--------|------|---------|--|
| Vendor Specific Rx Alarms 4 Interrupt | 0 | RO | | An interrupt was generated from the status register (" Auto-negotiation Receive Vendor Alarms 4: Address 7.EC03 " on page 166) and the corresponding mask register (" Auto-negotiation Receive Vendor Interrupt Mask 4: Address 7.F403 " on page 167). 1b = Interrupt |
| Vendor Specific Rx Alarms 3 Interrupt | 1 | RO | | An interrupt was generated from the status register (" Auto-negotiation Receive Vendor Alarms 3: Address 7.EC02 " on page 166) and the corresponding mask register (" Auto-negotiation Receive Vendor Interrupt Mask 3: Address 7.F402 " on page 167). 1b = Interrupt |



| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------------|--------|------|---------|--|
| Vendor Specific Rx Alarms 2 Interrupt | 2 | RO | | An interrupt was generated from the status register (" Auto-negotiation Receive Vendor Alarms 2: Address 7.EC01 " on page 166) and the corresponding mask register (" Auto-negotiation Receive Vendor Interrupt Mask 2: Address 7.F401 " on page 167). 1b = Interrupt |
| Vendor Specific Rx Alarms 1 Interrupt | 3 | RO | | An interrupt was generated from the status register (" Auto-negotiation Receive Vendor Alarms 1: Address 7.EC00 " on page 165) and the corresponding mask register (" Auto-negotiation Receive Vendor Interrupt Mask 1: Address 7.F400 " on page 166). 1b = Interrupt |
| Reserved | 8:4 | RSV | | Reserved. Do not modify. |
| Vendor Specific Alarms 2 Interrupt | 9 | RO | | An interrupt was generated from the status register (" Auto-negotiation Transmit Vendor Alarms 2: Address 7.CC01 " on page 162) and the corresponding mask register (" Auto-negotiation Transmit Vendor Interrupt Mask 2: Address 7.D401 " on page 163). 1b = Interrupt |
| Vendor Specific Alarms 1 Interrupt | A | RO | | An interrupt was generated from the status register (" Auto-negotiation Transmit Vendor Alarms 1: Address 7.CC00 " on page 161) and the corresponding mask register (" Auto-negotiation Transmit Vendor Interrupt Mask 1: Address 7.D400 " on page 163). 1b = Interrupt |
| Reserved | D:B | RSV | | Reserved. Do not modify. |
| Standard Alarms 2 Interrupt | E | RO | | An interrupt was generated from the status register (" Auto-negotiation 10GBASE-T Status Register: Address 7.21 " on page 147) and the corresponding mask register (" Auto-negotiation Standard Interrupt Mask 2: Address 7.D001 " on page 162). 1b = Interrupt |
| Standard Alarms 1 Interrupt | F | RO | | An interrupt was generated from the status register (" Auto-negotiation Standard Status 1: Address 7.1 " on page 140) and the corresponding mask register (" Auto-negotiation Standard Interrupt Mask 1: Address 7.D000 " on page 162). 1b = Interrupt |



4.6.2.5 GbE Registers

4.6.2.5.1 GbE Standard Device Identifier 1: Address 1D.2

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------|--------|------|---------|----------------------------|
| Device ID MSW [1F:10] | F:0 | RO | | Bits [31:16] of Device ID. |

4.6.2.5.2 GbE Standard Device Identifier 2: Address 1D.3

| Field Name | Bit(s) | Type | Default | Description |
|---------------------|--------|------|---------|---------------------------|
| Device ID LSW [F:0] | F:0 | RO | | Bits [15:0] of Device ID. |

4.6.2.5.3 GbE Standard Devices in Package 1: Address 1D.5

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------|--------|------|---------|--|
| Clause 22 Registers Present | 0 | ROS | 0b | Always set to 0b, as there are no Clause 22 registers in the X557. 0b = Clause 22 registers are not present in package. 1b = Clause 22 registers are present in package. |
| PMA Present | 1 | ROS | 1b | Always set to 1b, as there is PMA functionality in the X557. 0b = PMA is not present. 1b = PMA is present in package. |
| WIS Present | 2 | ROS | 0b | Always set to 0b, as there is no WIS functionality in the X557. 0b = WIS is not present in package. 1b = WIS is present in package. |
| PCS Present | 3 | ROS | 1b | Always set to 1b, as there is PCS functionality in the X557. 0b = PCS is not present in package. 1b = PCS is present in package. |
| Reserved | 4 | ROS | 1b | Always set to 1b. |
| DTE XS Present | 5 | ROS | 0b | Always set to 0b. |
| TC Present | 6 | ROS | 0b | Always set to 0b, as there is no TC functionality in the X557. 0b = TC is not present in package. 1b = TC is present in package. |
| Auto-negotiation Present | 7 | ROS | 1b | Always set to 1b, as there is auto-negotiation in the X557. 0b = Auto-negotiation is not present in package. 1b = Auto-negotiation is present in package. |
| Reserved | F:8 | RSV | | Reserved. Do not modify. |

4.6.2.5.4 GbE Standard Vendor Devices in Package 2: Address 1D.6

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | C:0 | RSV | | Reserved. Do not modify. |



| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------------|--------|------|---------|---|
| Clause 22 Extension Present | D | ROS | 1b | Always set to 1b, as the X557 utilizes this device for the GbE registers. 0b = Clause 22 Extension is not present in package. 1b = Clause 22 Extension is present in package. |
| Vendor Specific Device #1 Present | E | ROS | 1b | Always set to 1b, as the X557 utilizes this device for the Global registers. 0b = Device #1 is not present in package. 1b = Device #1 is present in package. |
| Vendor Specific Device #2 Present | F | ROS | 1b | Always set to 1b, as the X557 utilizes this device for the DSP PMA registers. 0b = Device #2 is not present in package. 1b = Device #2 is present in package. |

4.6.2.5.5 GbE Standard Status 2: Address 1D.8

| Field Name | Bit(s) | Type | Default | Description |
|----------------------|--------|------|---------|--|
| Reserved | D:0 | RSV | | Reserved. Do not modify. |
| Device Present [1:0] | F:E | ROS | 10b | This field is always set to 10b, as the Control is present in the X557. 00b = No device at this address. 01b = No device at this address. 10b = Device present at this address. 11b = No device at this address. |

4.6.2.5.6 GbE Standard Package Identifier 1: Address 1D.E

| Field Name | Bit(s) | Type | Default | Description |
|------------------------|--------|------|---------|-----------------------------|
| Package ID MSW [1F:10] | F:0 | RO | | Bits [31:16] of Package ID. |

4.6.2.5.7 GbE Standard Package Identifier 2: Address 1D.F

| Field Name | Bit(s) | Type | Default | Description |
|----------------------|--------|------|---------|----------------------------|
| Package ID LSW [F:0] | F:0 | RO | | Bits [15:0] of Package ID. |

4.6.2.5.8 GbE PHY SGMII Test Control: Address 1D.C282

| Field Name | Bit(s) | Type | Default | Description |
|-------------------------------------|--------|------|---------|--|
| SGMII Test Pattern Injection Enable | 0 | R/W | 0b | 0b = Normal mode 1b = Inject test pattern |
| Reserved | F:1 | RSV | | Reserved. Do not modify. |



4.6.2.5.9 GbE Reserved Provisioning 1: Address 1D.C500

| Field Name | Bit(s) | Type | Default | Description |
|-------------------------------|--------|--------|---------|---|
| Reserved Provisioning 1 [D:0] | D:0 | R/W PD | 0x0000 | Reserved for future use. |
| GbE System Loopback | E | R/W PD | 0b | Setting this bit enables the 1 GbE system loopback. 1b = Enable System Loopback. Note: This is a processor intensive operation. Completion of this operation can be monitored via 1E.C831.F (refer to Section 4.6.2.6.83). Note: GbE system loopback is not supported. |
| 100M System Loopback | F | R/W PD | 0b | Setting this bit enables the 100 Mb/s system loopback. 1b = Enable System Loopback. Note: This is a processor intensive operation. Completion of this operation can be monitored via 1E.C831.F (refer to Section 4.6.2.6.83). Note: 100 Mb/s loopback is not supported. |

4.6.2.5.10 GbE Reserved Provisioning 2: Address 1D.C501

| Field Name | Bit(s) | Type | Default | Description |
|-------------------------------|--------|--------|---------|--|
| 100BASE-TX Test Mode [1:0] | 1:0 | R/W | 00b | 100BASE-TX IEEE Test Mode = MLT-3 Idle Sequence. ANSI Jitter Test = FDDI - Clause 9.1.3 Fig. 12. ANSI Droop Test = FDDI - Clause 9.1.8 Fig. 14. 00b = Normal mode 01b = 100BASE-TX IEEE Test Mode 10b = 100BASE-TX ANSI Jitter Test 11b = 100BASE-TX ANSI Droop Test Note: This is a processor intensive operation. Completion of this operation can be monitored via 1E.C831.F (refer to Section 4.6.2.6.83) |
| Reserved Provisioning 2 [A:0] | C:2 | R/W PD | 0x000 | Reserved for future use. |
| Test Mode [2:0] | F:D | R/W | 000b | 000b = Normal mode 001b = Test Mode 1 — Transmit waveform test. 010b = Test Mode 2 — Master transmit jitter test. 011b = Test Mode 3 — Slave transmit jitter test. 100b = Test Mode 4 — Transmitter distortion test. All other values are reserved. Note: This is a processor intensive operation. Completion of this operation can be monitored via 1E.C831.F (refer to Section 4.6.2.6.83) |

4.6.2.5.11 GbE PHY SGMII 1 Rx Status 1: Address 1D.D280

| Field Name | Bit(s) | Type | Default | Description |
|------------------------------|--------|------|---------|--|
| SGMII Rx Link Activity | 0 | LH | | SGMII Start Character K27_7 detected. 1b = SGMII Rx Link Activity. |
| SGMII TX_ER Suppression | 1 | LH | | Indicates TX_ER has been suppressed when TX_EN was not asserted. 1b = TX_ER suppressed. |
| Reserved | 3:2 | RSV | | Reserved. Do not modify. |
| SGMII Idle Deletion Detected | 4 | LH | | 1b = SGMII Idle Deletion Detected. |



| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|-------------------------------------|
| SGMII Idle Insertion Detected | 5 | LH | | 1b = SGMII Idle Insertion Detected. |
| SGMII Loopback Idle Deletion Detected | 6 | LH | | 1b = SGMII Idle Deletion Detected. |
| SGMII Loopback Idle Insertion Detected | 7 | LH | | 1b = SGMII Idle Insertion Detected. |
| SGMII Synchronization Status | 8 | RO | | 1b = SGMII is Synchronized. |
| Reserved | F:9 | RSV | | Reserved. Do not modify. |

4.6.2.5.12 GbE PHY SGMII 1 Rx Status 2: Address 1D.D281

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |

4.6.2.5.13 GbE PHY SGMII 1 Rx Status 3: Address 1D.D282

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------------|--------|------|---------|--|
| SGMII1 Rx Frame Counter LSW [F:0] | F:0 | SCTL | 0x0000 | SGMII1 Rx Good Frame Counter. Counts 100M/GbE Ethernet good frames (i.e., no Ethernet CRC-32/FCS errors). |

4.6.2.5.14 GbE PHY SGMII 1 Rx Status 4: Address 1D.D283

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------------|--------|------|---------|--|
| SGMII1 Rx Frame Counter MSW [9:0] | 9:0 | SCTM | 0x000 | SGMII1 Rx Good Frame Counter. Counts 100M/GbE Ethernet good frames (i.e., no Ethernet CRC-32/FCS errors). |
| Reserved | F:A | RSV | | Reserved. Do not modify. |

4.6.2.5.15 GbE PHY SGMII 1 Rx Status 5: Address 1D.D284

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|--|
| SGMII1 Rx Frame Error Counter LSW [F:0] | F:0 | SCTL | 0x0000 | SGMII1 Rx Bad Frame Counter. Counts 100M/GbE Ethernet frames with a bad FCS (=RC-32). |

4.6.2.5.16 GbE PHY SGMII 1 Rx Status 6: Address 1D.D285

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|--|
| SGMII1 Rx Frame Error Counter MSW [9:0] | 9:0 | SCTL | 0x000 | SGMII1 Rx Bad Frame Counter. counts 100M/GbE Ethernet frames with a bad FCS (=RC-32). |



| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:A | RSV | | Reserved. Do not modify. |

4.6.2.5.17 GbE PHY SGMII 1 Rx Status 7: Address 1D.D286

| Field Name | Bit(s) | Type | Default | Description |
|------------------------|--------|------|---------|---|
| SGMII1 Rx Comma Detect | 0 | LH | | Indicates when SGMII Rx has detected a comma character. 1b = SGMII1 Rx Comma Detected. |
| Reserved | F:1 | RSV | | Reserved. Do not modify. |

4.6.2.5.18 GbE PHY SGMII 1 Rx Status 8: Address 1D.D287

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------------|--------|------|---------|---|
| SGMII1 Rx False Carrier Counter [7:0] | 7:0 | SCT | 0x00 | SGMII1 Rx False Carrier Counter. TSI detects false carrier on the SGMII interface. |
| Reserved | F:8 | RSV | | Reserved. Do not modify. |

4.6.2.5.19 GbE PHY SGMII 1 Rx Status 9: Address 1D.D288

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|---|
| SGMII1 Rx EEE Rx LPI Active State | 0 | RO | | Indicates Rx LPI is in active state. 1b = SGMII1 Rx Rx LPI is in active state. |
| SGMII1 Rx EEE Rx LPI Quiet State | 1 | RO | | Indicates Rx LPI is in quiet state. 1b = SGMII1 Rx Rx LPI is in quiet state. |
| SGMII1 Rx EEE Rx LPI Wake Done State | 2 | RO | | Indicates Rx LPI is in wake done state. 1b = SGMII1 Rx Rx LPI is in wake done state. |
| SGMII1 Rx EEE Rx LPI Wake Timer Fault Error | 3 | LH | | Indicates Rx LPI detected wake timer fault. 1b = SGMII1 Rx Rx LPI detected wake timer fault. |
| SGMII1 Rx EEE Rx LPI Ordered Set Detected | 4 | LH | | Indicates LPI ordered_set is detected. 1b = SGMII1 Rx LPI ordered set detected |
| Reserved | 7:5 | RSV | | Reserved. Do not modify. |
| SGMII1 Rx EEE Rx LPI State Machine [3:0] | B:8 | RO | | SGMII1 Rx EEE Rx LPI state machine. |
| Reserved | F:C | RSV | | Reserved. Do not modify. |

4.6.2.5.20 GbE PHY SGMII 0 Rx Status 1: Address 1D.D290

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------|--------|------|---------|---|
| SGMII0 Rx Rx Link Activity | 0 | LH | | SGMII Start Character K27_7 detected. 1b = SGMII Rx Link Activity. |



| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|--|
| SGMII0 Rx TX_ER Suppression | 1 | LH | | Indicates TX_ER has been suppressed when TX_EN was not asserted. 1b = TX_ER suppressed. |
| Reserved | 3:2 | RSV | | Reserved. Do not modify. |
| SGMII0 Rx Idle Deletion Detected | 4 | LH | | 1b = SGMII0 Rx Idle Deletion Detected. |
| SGMII0 Rx Idle Insertion Detected | 5 | LH | | 1b = SGMII0 Rx Idle Insertion Detected. |
| SGMII0 Rx Loopback Idle Deletion Detected | 6 | LH | | 1b = SGMII0 Rx Idle Deletion Detected. |
| SGMII0 Rx Loopback Idle Insertion Detected | 7 | LH | | 1b = SGMII0 Rx Idle Insertion Detected. |
| SGMII0 Rx Synchronization Status | 8 | RO | | 1b = SGMII0 Rx is Synchronized. |
| Reserved | F:9 | RSV | | Reserved. Do not modify. |

4.6.2.5.21 GbE PHY SGMII0 Rx Status 2: Address 1D.D291

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |

4.6.2.5.22 GbE PHY SGMII0 Rx Status 3: Address 1D.D292

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------------|--------|------|---------|--|
| SGMII0 Rx Frame Counter LSW [F:0] | F:0 | SCTL | 0x0000 | SGMII0 Rx Good Frame Counter. Counts 100M/GbE Ethernet good frames (i.e., no Ethernet CRC-32/FCS errors). |

4.6.2.5.23 GbE PHY SGMII0 Rx Status 4: Address 1D.D293

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------------|--------|------|---------|--|
| SGMII0 Rx Frame Counter MSW [9:0] | 9:0 | SCTM | 0x0000 | SGMII0 Rx Good Frame Counter. Counts 100M/GbE Ethernet good frames (i.e., no Ethernet CRC-32/FCS errors). |
| Reserved | F:A | RSV | | Reserved. Do not modify. |

4.6.2.5.24 GbE PHY SGMII0 Rx Status 5: Address 1D.D294

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|--|
| SGMII0 Rx Frame Error Counter LSW [F:0] | F:0 | SCTL | 0x0000 | SGMII0 Rx Bad Frame Counter. Counts 100M/GbE Ethernet frames with a bad FCS (CRC-32). |



4.6.2.5.25 GbE PHY SGMII0 Rx Status 6: Address 1D.D295

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|---|
| SGMII0 Rx Frame Error Counter MSW [9:0] | 9:0 | STCM | 0x000 | SGMII0 Rx Bad Frame Counter. Counts 100M/GbE Ethernet frames with a bad FCS (CRC-32). |
| Reserved | F:A | RSV | | Reserved. Do not modify. |

4.6.2.5.26 GbE PHY SGMII0 Rx Status 7: Address 1D.D296

| Field Name | Bit(s) | Type | Default | Description |
|------------------------|--------|------|---------|--|
| SGMII0 Rx Comma Detect | 0 | LH | | Indicates when Rx has detected a comma character. 1b = SGMII0 Rx Comma Detected. |
| Reserved | F:1 | RSV | | Reserved. Do not modify. |

4.6.2.5.27 GbE PHY SGMII0 Rx Status 8: Address 1D.D297

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------------|--------|------|---------|--|
| SGMII0 Rx False Carrier Counter [7:0] | 7:0 | SCT | 0x00 | SGMII0 Rx False Carrier Counter. False carrier events on XF10 SGMII interface. |
| Reserved | F:9 | RSV | | Reserved. Do not modify. |

4.6.2.5.28 GbE PHY SGMII0 Rx Status 9: Address 1D.D298

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|--|
| SGMII0 Rx EEE Rx LPI Active State | 0 | RO | | Indicates Rx LPI is in active state. 1b = SGMII0 Rx Rx LPI is in active state. |
| SGMII0 Rx EEE Rx LPI Quiet State | 1 | RO | | Indicates Rx LPI is in quiet state. 1b = SGMII0 Rx Rx LPI is in quiet state. |
| SGMII0 Rx EEE Rx LPI Wake Done State | 2 | RO | | Indicates Rx LPI is in wake done state. 1b = SGMII0 Rx Rx LPI is in wake done state. |
| SGMII0 Rx EEE Rx LPI Wake Timer Fault Error | 3 | LH | | Indicates Rx LPI detected wake timer fault. 1b = SGMII0 Rx Rx LPI detected wake timer fault. |
| SGMII0 Rx EEE Rx LPI Ordered Set Detected | 4 | LH | | Indicates LPI ordered_set is detected. 1b = SGMII0 Rx LPI ordered set detected |
| Reserved | 7:5 | RSV | | Reserved. Do not modify. |
| SGMII0 Rx EEE Rx LPI State Machine [3:0] | B:8 | RO | | SGMII0 Rx EEE Rx LPI state machine. |
| Reserved | F:C | RSV | | Reserved. Do not modify. |



4.6.2.5.29 GbE PHY SGMII 1 Tx Status 1: Address 1D.D303

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------------|--------|------|---------|--|
| SGMII1 Tx Frame Counter LSW [F:0] | F:0 | SCTL | 0x0000 | SGMII1 Tx Good Frame Counter. Counts 100M/GbE Ethernet good frames (i.e., no Ethernet CRC-32/FCS errors). |

4.6.2.5.30 GbE PHY SGMII 1 Tx Status 2: Address 1D.D304

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------------|--------|------|---------|--|
| SGMII1 Tx Frame Counter MSW [9:0] | 9:0 | SCTM | 0x000 | SGMII1 Tx Good Frame Counter. Counts 100M/GbE Ethernet good frames (i.e., no Ethernet CRC-32/FCS errors). |
| Reserved | F:A | RSV | | Reserved. Do not modify. |

4.6.2.5.31 GbE PHY SGMII 1 Tx Status 3: Address 1D.D305

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|--|
| SGMII1 Tx Frame Error Counter LSW [F:0] | F:0 | SCTL | 0x0000 | SGMII1 Tx Bad Frame Error Counter. Frames with CRC error counter. |

4.6.2.5.32 GbE PHY SGMII 1 Tx Status 4: Address 1D.D306

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|--|
| SGMII1 Tx Frame Error Counter MSW [9:0] | 9:0 | SCTM | 0x000 | SGMII1 Tx Bad Frame Error Counter. Frames with CRC error counter. |
| Reserved | F:A | RSV | | Reserved. Do not modify. |

4.6.2.5.33 GbE PHY SGMII 1 Tx Status 5: Address 1D.D307

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------------|--------|------|---------|---|
| SGMII1 Tx False Carrier Counter [7:0] | 7:0 | SCT | 0x00 | SGMII1 Tx False Carrier Counter. SGMII1 Tx detected false carrier event the on the SERDES interface. |
| Reserved | F:8 | RSV | | Reserved. Do not modify. |

4.6.2.5.34 GbE PHY SGMII 1 Tx Status 6: Address 1D.D308

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------------|--------|------|---------|---|
| SGMII1 Tx Collision Counter [7:0] | 7:0 | SCT | 0x00 | SGMII1 Tx Collision Counter. SGMII1 Tx detected a collision on the SERDES interface. |
| Reserved | F:8 | RSV | | Reserved. Do not modify. |



4.6.2.5.35 GbE PHY SGMII 1 Tx Status 7: Address 1D.D309

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|---|
| SGMII1 Tx Line Collision Counter [7:0] | 7:0 | SCT | 0x00 | SGMII1 Tx Line Collision Counter. SGMII1 Tx detects collision on the GMII/MII interface. |
| Reserved | F:8 | RSV | | Reserved. Do not modify. |

4.6.2.5.36 GbE PHY SGMII 1 Tx Status 8: Address 1D.D30A

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|--|
| SGMII1 Tx Frame Alignment Counter [F:0] | F:8 | SCT | 0x0000 | SGMII1 Tx Frame Alignment Counter. SGMII1 Tx Frame Count with alignment error. This is detected by CRC error with an extra nibble on MII interface (100 Mb/s mode) on the GMII/MII interface. |

4.6.2.5.37 GbE PHY SGMII 1 Tx Status 9: Address 1D.D30B

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|--|
| SGMII1 Tx Runt Frame Counter LSW [F:0] | F:0 | SCTL | 0x0000 | SGMII1 Tx Runt Frame Counter. SGMII1 Tx Runt Frame (less than 64 bytes long) Count on the GMII/MII interface. |

4.6.2.5.38 GbE PHY SGMII 1 Tx Status 10: Address 1D.D30C

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|--|
| SGMII1 Tx Runt Frame Counter MSW [5:0] | 5:0 | SCTM | 0x00 | SGMII1 Tx Runt Frame Counter. SGMII1 Tx Runt Frame (less than 64 bytes long) Count on the GMII/MII interface. |
| Reserved | F:6 | RSV | | Reserved. Do not modify. |

4.6.2.5.39 GbE PHY SGMII 0 Tx Status 1: Address 1D.D313

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------------|--------|------|---------|--|
| SGMII0 Tx Frame Counter LSW [F:0] | F:0 | SCTL | 0x0000 | SGMII0 Tx Good Frame Counter. Counts 100M/GbE Ethernet good frames (i.e., no Ethernet CRC-32/FCS errors). |

4.6.2.5.40 GbE PHY SGMII 0 Tx Status 2: Address 1D.D314

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------------|--------|------|---------|--|
| SGMII0 Tx Frame Counter MSW [9:0] | 9:0 | SCTM | 0x0000 | SGMII0 Tx Good Frame Counter. Counts 100M/GbE Ethernet good frames (i.e., no Ethernet CRC-32/FCS errors). |



| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:A | RSV | | Reserved. Do not modify. |

4.6.2.5.41 GbE PHY SGMII0 Tx Status 3: Address 1D.D315

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|---|
| SGMII0 Tx Frame Error Counter LSW [F:0] | F:0 | SCTL | 0x0000 | SGMII0 Tx Bad Frame Error Counter. Counts 100M/GbE Ethernet frames with a bad FCS (CRC-32). |

4.6.2.5.42 GbE PHY SGMII0 Tx Status 4: Address 1D.D316

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|---|
| SGMII0 Tx Frame Error Counter MSW [9:0] | 9:0 | SCTM | 0x000 | SGMII0 Tx Bad Frame Error Counter. Counts 100M/GbE Ethernet frames with a bad FCS (CRC-32). |
| Reserved | F:A | RSV | | Reserved. Do not modify. |

4.6.2.5.43 GbE PHY SGMII0 Tx Status 5: Address 1D.D317

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------------|--------|------|---------|--|
| SGMII0 Tx False Carrier Counter [7:0] | 7:0 | SCT | 0x00 | SGMII0 Tx False Carrier Counter. SGMII0 Tx detected false carrier on the GMII/MII interface. |
| Reserved | F:8 | RSV | | Reserved. Do not modify. |

4.6.2.5.44 GbE PHY SGMII0 Tx Status 6: Address 1D.D318

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------------|--------|------|---------|---|
| SGMII0 Tx Collision Counter [7:0] | 7:0 | SCT | 0x00 | SGMII0 Tx Collision Counter. SGMII0 Tx detected a collision on the SGMII interface. |
| Reserved | F:8 | RSV | | Reserved. Do not modify. |

4.6.2.5.45 GbE PHY SGMII0 Tx Status 7: Address 1D.D319

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|--|
| SGMII0 Tx Line Collision Counter [7:0] | 7:0 | SCT | 0x00 | SGMII0 Tx Line Collision Counter. SGMII0 Tx detects collision on the GMII/MII interface. |
| Reserved | F:8 | RSV | | Reserved. Do not modify. |



4.6.2.5.46 GbE PHY SGMII0 Tx Status 8: Address 1D.D31A

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|--|
| SGMII0 Tx Frame Alignment Counter [F:0] | F:8 | SCT | 0x0000 | SGMII0 Tx Frame Alignment Counter. SGMII0 Tx Frame Count with alignment error. This is detected by CRC error with an extra nibble on MII interface (100 Mb/s mode) on the GMII/MII interface. |

4.6.2.5.47 GbE PHY SGMII0 Tx Status 9: Address 1D.D31B

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|--|
| SGMII0 Tx Runt Frame Counter LSW [F:0] | F:0 | SCTL | 0x0000 | SGMII0 Tx Runt Frame Counter. SGMII0 Tx Runt Frame (less than 64 bytes long) Count on the GMII/MII interface. |

4.6.2.5.48 GbE PHY SGMII0 Tx Status 10: Address 1D.D31C

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|--|
| SGMII0 Tx Runt Frame Counter MSW [5:0] | 5:0 | SCTM | 0x00 | SGMII0 Tx Runt Frame Counter. SGMII0 Tx Runt Frame (less than 64 bytes long) Count on the GMII/MII interface. |
| Reserved | F:6 | RSV | | Reserved. Do not modify. |

4.6.2.5.49 GbE PHY SGMII Rx Alarms 1: Address 1D.EC10

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------------|--------|------|---------|---|
| SGMII1 Rx Code Violation Error | 0 | LH | | 1b = SGMII1 Rx Code Violation Error. |
| SGMII1 Rx Running Disparity Error | 1 | LH | | 1b = SGMII1 Rx Running Disparity Error. |
| SGMII1 Rx Invalid Character Error | 2 | LH | | 1b = SGMII1 Rx Invalid Character Error. |
| SGMII1 Rx Loss of Signal | 3 | LH | | 1b = SGMII1 Loss of Signal. |
| SGMII0 Rx Code Violation Error | 4 | LH | | 1b = SGMII0 Rx Code Violation Error. |
| SGMII0 Rx Running Disparity Error | 5 | LH | | 1b = SGMII0 Rx Running Disparity Error. |
| SGMII0 Rx Invalid Character Error | 6 | LH | | 1b = SGMII0 Rx Invalid Character Error. |
| SGMII0 Rx Loss of Signal | 7 | LH | | 1b = SGMII0 Loss of Signal. |
| Reserved | F:8 | RSV | | Reserved. Do not modify. |

4.6.2.5.50 GbE PHY SGMII Tx Alarms 1: Address 1D.EC20

| Field Name | Bit(s) | Type | Default | Description |
|------------------------------------|--------|------|---------|--|
| SGMII1 Wake Up Frame Detected | 0 | LH | | 1b = SGMII1 Wake Up Frame Detected. |
| SGMII1 Magic Packet Frame Detected | 1 | LH | | 1b = SGMII1 Magic Packet Frame Detected. |



| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|---|
| SGMII1 Tx Invalid GMII Character Detected | 2 | LH | | 1b = SGMII1 Tx Invalid GMII Character Detected. |
| Reserved | 3 | RSV | | Reserved. Do not modify. |
| SGMII0 Wake Up Frame Detected | 4 | LH | | 1b = SGMII0 Wake Up Frame Detected. |
| SGMII0 Magic Packet Frame Detected | 5 | LH | | 1b = SGMII0 Magic Packet Frame Detected. |
| SGMII0 Tx Invalid GMII Character Detected | 6 | LH | | 1b = SGMII0 Tx Invalid GMII Character Detected. |
| Reserved | 7 | RSV | | Reserved. Do not modify. |
| SGMII Wake Up Frame Detected | 8 | LH | | 1b = SGMII Wake Up Frame Detected. |
| SGMII Magic Packet Frame Detected | 9 | LH | | 1b = SGMII Magic Packet Frame Detected. |
| Reserved | F:A | RSV | | Reserved. Do not modify. |

4.6.2.5.51 GbE PHY SGMII Rx Interrupt Mask 1: Address 1D.F410

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|--------|---------|---|
| SGMII1 Rx Code Violation Error Mask | 0 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| SGMII1 Rx Running Disparity Error Mask | 1 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| SGMII1 Rx Invalid Character Error Mask | 2 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| SGMII1 Rx Loss of Signal Mask | 3 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| SGMII0 Rx Code Violation Error Mask | 4 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| SGMII0 Rx Running Disparity Error Mask | 5 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| SGMII0 Rx Invalid Character Error Mask | 6 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| SGMII0 Rx Loss of Signal Mask | 7 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | F:8 | RSV | | Reserved. Do not modify. |

4.6.2.5.52 GbE PHY SGMII Tx Interrupt Mask 1: Address 1D.F420

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|--------|---------|---|
| SGMII1 Wake Up Frame Detected Mask | 0 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| SGMII1 Magic Packet Frame Detected Mask | 1 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| SGMII1 Tx Invalid GMII Character Detected Mask | 2 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | 3 | RSV | | Reserved. Do not modify. |



| Field Name | Bit(s) | Type | Default | Description |
|--|--------|--------|---------|---|
| SGMII0 Wake Up Frame Detected Mask | 4 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| SGMII0 Magic Packet Frame Detected Mask | 5 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| SGMII0 Tx Invalid GMII Character Detected Mask | 6 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | 7 | RSV | | Reserved. Do not modify. |
| SGMII Wake Up Frame Detected Mask | 8 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| SGMII Magic Packet Frame Detected Mask | 9 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | F:A | RSV | | Reserved. Do not modify. |

4.6.2.5.53 GbE PHY Vendor Global Interrupt Flags 1: Address 1D.FC00

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|--|
| Reserved | 0 | RSV | | Reserved. Do not modify. |
| Vendor Specific SGMII Rx Alarms 2 Interrupt | 1 | RO | | An interrupt was generated from the status register and the corresponding mask register. 1b = Interrupt in vendor specific SGMII Tx Alarms 2. |
| Vendor Specific SGMII Rx Alarms 1 Interrupt | 2 | RO | | An interrupt was generated from the status register and the corresponding mask register. 1b = Interrupt in vendor specific SGMII Tx Alarms 1. |
| Vendor Specific SGMII Tx Alarms 2 Interrupt | 3 | RO | | An interrupt was generated from the status register and the corresponding mask register. 1b = Interrupt in vendor specific SGMII Tx Alarms 2. |
| Vendor Specific SGMII Tx Alarms 1 Interrupt | 4 | RO | | An interrupt was generated from the status register and the corresponding mask register. 1b = Interrupt in vendor specific SGMII Tx Alarms 1. |
| Reserved | F:5 | RSV | | Reserved. Do not modify. |



4.6.2.6 Global Registers

4.6.2.6.1 Global Standard Control 1: Address 1E.0

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|--------|---------|---|
| Reserved | A:0 | RSV | | Reserved. Do not modify. |
| Low Power | B | R/W PD | 0b | A one written to this register causes the chip to enter low-power mode. 0b = Normal operation 1b = Low-power mode This bit puts the entire chip in low-power mode, with only the MDIO and microprocessor functioning, and turns off the analog front-end (i.e., places it in high-impedance mode). Setting this bit also sets all of the Low Power bits in the other MMDs. |
| Reserved | E:C | RSV | | Reserved. Do not modify. |
| Soft Reset | F | R/W SC | 1b | Resets the entire PHY. 0b = Normal operation 1b = Global soft reset Setting this bit initiates a global soft reset on all of the digital logic not including the microprocessor (i.e., microprocessor is not reset). Upon completion of the reset sequence, this bit is set back to 0b by the microprocessor. Note: This bit is OR'ed with the individual MMD resets. This bit should be set to 0b before setting the individual MMD resets. |

4.6.2.6.2 Global Standard Device Identifier 1: Address 1E.2

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------|--------|------|---------|----------------------------|
| Device ID MSW [1F:10] | F:0 | RO | | Bits [31:16] of Device ID. |

4.6.2.6.3 Global Standard Device Identifier 2: Address 1E.3

| Field Name | Bit(s) | Type | Default | Description |
|---------------------|--------|------|---------|---------------------------|
| Device ID LSW [F:0] | F:0 | RO | | Bits [15:0] of Device ID. |

4.6.2.6.4 Global Standard Devices in Package 1: Address 1E.5

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------|--------|------|---------|--|
| Clause 22 Registers Present | 0 | ROS | 0b | Always set to 0b, as there are no Clause 22 registers in the X557. 0b = Clause 22 registers are not present in package. 1b = Clause 22 registers are present in package. |
| PMA Present | 1 | ROS | 1b | Always set to 1b, as there is PMA functionality in the X557. 0b = PMA is not present. 1b = PMA is present in package. |
| WIS Present | 2 | ROS | 0b | Always set to 0b, as there is no WIS functionality in the X557. 0b = WIS is not present in package. 1b = WIS is present in package. |



| Field Name | Bit(s) | Type | Default | Description |
|--------------------------|--------|------|---------|---|
| PCS Present | 3 | ROS | 1b | Always set to 1b, as there is PCS functionality in the X557. 0b = PCS is not present in package. 1b = PCS is present in package. |
| PHY XS Present | 4 | ROS | 1b | Always set to 1b, as there is a PHY XS interface in the X557. 0b = PHY XS is not present in package. 1b = PHY XS is present in package. |
| Reserved | 5 | ROS | 0b | Always set to 0b. |
| TC Present | 6 | ROS | 0b | Always set to 0b, as there is no TC functionality in the X557. 0b = TC is not present in package. 1b = TC is present in package. |
| Auto-negotiation Present | 7 | ROS | 1b | Always set to 1b, as there is auto-negotiation in the X557. 0b = Auto-negotiation is not present in package. 1b = Auto-negotiation is present in package. |
| Reserved | F:8 | RSV | | Reserved. Do not modify. |

4.6.2.6.5 Global Standard Vendor Devices in Package 2: Address 1E.6

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------------|--------|------|---------|---|
| Reserved | C:0 | RSV | | Reserved. Do not modify. |
| Clause 22 Extension Present | D | ROS | 1b | Always set to 1b, as the X557 utilizes this device for the GbE registers. 0b = Clause 22 Extension is not present in package. 1b = Clause 22 Extension is present in package. |
| Vendor Specific Device #1 Present | E | ROS | 1b | Always set to 1b, as the X557 utilizes this device for the Global registers. 0b = Device #1 is not present in package. 1b = Device #1 is present in package. |
| Vendor Specific Device #2 Present | F | ROS | 1b | Always set to 1b, as the X557 utilizes this device for the DSP PMA registers. 0b = Device #2 is not present in package. 1b = Device #2 is present in package. |

4.6.2.6.6 Global Standard Status 2: Address 1E.8

| Field Name | Bit(s) | Type | Default | Description |
|----------------------|--------|------|---------|---|
| Reserved | D:0 | RSV | | Reserved. Do not modify. |
| Device Present [1:0] | F:E | ROS | 10b | This field is always set to 10b, as the Global MMD resides here in the X557. 00b = No device at this address. 01b = No device at this address. 10b = Device present at this address. 11b = No device at this address. |



4.6.2.6.7 Global Standard Package Identifier 1: Address 1E.E

| Field Name | Bit(s) | Type | Default | Description |
|------------------------|--------|------|---------|-----------------------------|
| Package ID MSW [1F:10] | F:0 | RO | | Bits [31:16] of Package ID. |

4.6.2.6.8 Global Standard Package Identifier 2: Address 1E.F

| Field Name | Bit(s) | Type | Default | Description |
|----------------------|--------|------|---------|----------------------------|
| Package ID LSW [F:0] | F:0 | RO | | Bits [15:0] of Package ID. |

4.6.2.6.9 Global Firmware ID: Address 1E.20

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------------------|--------|------|---------|---|
| Firmware Minor Revision Number [7:0] | 7:0 | RO | | Minor revision number. The lower six bits of major and minor firmware revision are exchanged in auto-negotiation when the PHYID message is sent. |
| Firmware Major Revision Number [7:0] | F:8 | RO | | Major revision number. The lower six bits of major and minor firmware revision are exchanged in auto-negotiation when the PHYID message is sent. |

4.6.2.6.10 Global Chip Identification: Address 1E.21

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------|--------|------|---------|---|
| Chip Identification [F:0] | F:0 | RO | | Hardware Chip ID. This value is the chip ID. |

4.6.2.6.11 Global Chip Revision: Address 1E.22

| Field Name | Bit(s) | Type | Default | Description |
|---------------------|--------|------|---------|---|
| Chip Revision [F:0] | F:0 | RO | | Hardware Chip Revision. This value is the chip revision. |

4.6.2.6.12 Global FW Image Identification 1: Address 1E.28

| Field Name | Bit(s) | Type | Default | Description |
|--------------------|--------|------|---------|---------------|
| Image ID MSW [F:0] | F:0 | RO | | Image ID MSW. |



4.6.2.6.13 Global FW Image Identification 2: Address 1E.29

| Field Name | Bit(s) | Type | Default | Description |
|--------------------|--------|------|---------|---------------|
| Image ID LSW [F:0] | F:0 | RO | | Image ID LSW. |

4.6.2.6.14 Global NVR Interface 1: Address 1E.100

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------|--------|-----------|---------|---|
| NVR Opcode [7:0] | 7:0 | R/W | 0x03 | NVR instruction opcode. |
| NVR Busy | 8 | RO | | When set to 1b, the NVR is busy. A new NVR operation should not occur until this bit is 0b. If the NVR clock is greater than 64/63 of the MDIO clock, this bit never needs to be polled when operating over the MDIO. 0b = NVR is ready. 1b = NVR is busy. |
| Reserved | 9 | RSV | | Reserved. Do not modify. |
| NVR Burst | A | R/W | 0b | When this bit is set, the operation is a burst operation where more than 32 bits is read from the NVR or written to the NVR. This bit should be set to one until the last burst in the read or write operation, when it should be set to zero. It operates by gating the SPI clock, and not restarting it until new data is ready to be written, or the previous contents have been read. Each burst of data requires the NVR Execute Operation bit to be set to initiate the next phase. 0b = Single read or write operation of up to 4 bytes. 1b = Burst operation. |
| Reserved | B | RSV | | Reserved. Do not modify. |
| Reset NVR CRC | C | R/W SC | 0b | To prevent an erroneous answer, this bit should not be set at the same time the "NVR Execute Operation" bit (Bit [0]) is set. 1b = Reset NVR Mailbox CRC calculation register. |
| Freeze NVR CRC | D | R/W | 0b | To prevent an erroneous answer, this bit should not be set at the same time the "NVR Execute Operation" bit (Bit [0]) is set. 1b = Freeze NVR Mailbox CRC calculation register. |
| NVR Write Mode | E | R/W | 0b | 0b = Read from NVR. 1b = Write to NVR. |
| NVR Execute Operation | F | R/W SC | 0b | When set to 1b, the NVR operation begins. Ensure that the uP is stalled using the "uP Run Stall" bit to ensure no NVR contention. 1b = Start NVR Operation |

4.6.2.6.15 Global NVR Interface 2: Address 1E.101

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------|--------|------|---------|--|
| NVR Mailbox CRC [F:0] | F:0 | RO | | The running CRC-16 of everything passing through the NVR interface. The CRC-16 over all data written or read through the NVR interface. The CRC-16 is calculated by dividing the data by: $x^{16} + x^{12} + x^5 + 1$ |



4.6.2.6.16 Global NVR Interface 3: Address 1E.102

| Field Name | Bit(s) | Type | Default | Description |
|-------------------------|--------|------|---------|--|
| NVR Address MSW [17:10] | 7:0 | R/W | 0x00 | NVR address MSW, Bits [17:10]. The address of where to read and write from in the NVR. This is self-incrementing and automatically increments after each read or write operation. The increment amount is based on the data length (i.e., increments by 4 if the data length is 4 bytes). |
| Reserved | F:8 | RSV | | Reserved. Do not modify. |

4.6.2.6.17 Global NVR Interface 4: Address 1E.103

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------|--------|------|---------|--|
| NVR Address LSW [F:0] | F:0 | R/W | 0x0000 | NVR address LSW, Bits [F:0]. The address of where to read and write from in the NVR. This is self-incrementing and automatically increments after each read or write operation. |

4.6.2.6.18 Global NVR Interface 5: Address 1E.104

| Field Name | Bit(s) | Type | Default | Description |
|----------------------|--------|------|---------|---|
| NVR Data MSW [1F:10] | F:0 | R/W | 0x0000 | NVR data MSW, Bits [1F:10]. Data is stored and read-out from these registers in little-endian format for operations such as FLASH device ID, and for programming the processor. For instance, the 64-K Atmel device code reads out as two bytes 0x651F into the LSW register, whereas the datasheet indicates that 1F is the first byte read, followed by 65 as the second byte. To burst read and write these 4 bytes in the correct order (where DD is written to address x), they should be stored as: <ul style="list-style-type: none">• AA BB in the MSW.• CC DD in the LSW. |

4.6.2.6.19 Global NVR Interface 6: Address 1E.105

| Field Name | Bit(s) | Type | Default | Description |
|--------------------|--------|------|---------|---|
| NVR Data LSW [F:0] | F:0 | R/W | 0x0000 | NVR data LSW, Bits [F:0]. Data is stored and read-out from these registers in little-endian format for operations such as FLASH device ID, and for programming the processor. For instance, the 64-K Atmel device code reads out as two bytes 0x651F into the LSW register, whereas the datasheet indicates that 1F is the first byte read, followed by 65 as the second byte. To burst read and write these 4 bytes in the correct order (where DD is written to address x), they should be stored as: <ul style="list-style-type: none">• AA BB in the MSW.• CC DD in the LSW. |



4.6.2.6.20 Global Mailbox Interface 1: Address 1E.200

| Field Name | Bit(s) | Type | Default | Description |
|------------------------------|--------|--------|---------|---|
| Reserved | 7:0 | RSV | | Reserved. Do not modify. |
| uP Mailbox Busy | 8 | RO | | In general, the uP responds within a few processor cycles to any PIF slave request, much faster than the MDIO. If the busy is asserted over multiple MDIO polling cycles, then a H/W error may have occurred and a Global S/W reset or uP reset is required. 0b = uP mailbox ready. 1b = uP mailbox busy. |
| Reserved | B:9 | RSV | | Reserved. Do not modify. |
| Reset uP Mailbox CRC | C | R/W SC | 0b | 1b = Reset uP mailbox CRC calculation register. |
| Reserved | D | RSV | | Reserved. Do not modify. |
| uP Mailbox Write Mode | E | R/W | 0b | Mailbox direction. 0b = Read 1b = Write |
| uP Mailbox Execute Operation | F | R/W SC | 0b | Indicates mailbox is loaded and ready. 1b = Start of mailbox Operation. |

4.6.2.6.21 Global Mailbox Interface 2: Address 1E.201

| Field Name | Bit(s) | Type | Default | Description |
|----------------------|--------|------|---------|---|
| uP Mailbox CRC [F:0] | F:0 | RO | | The running CRC-16 of everything passing through the mailbox interface. |

4.6.2.6.22 Global Mailbox Interface 3: Address 1E.202

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------------|--------|------|---------|--|
| uP Mailbox Address MSW [1F:10] | F:0 | R/W | 0x0000 | uP Mailbox MSW address. The address of where to read and write from in the Microcontroller Mailbox. This is self-incrementing and automatically increments after each read and write operation. |

4.6.2.6.23 Global Mailbox Interface 4: Address 1E.203

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|--|
| uP Mailbox Address LSW Don't Care [1:0] | 1:0 | RO | | Least significant uP LSW Mailbox address, Bits [1:0]. These bits are always set to 00b since each memory access is on a 4-byte boundary. |
| uP Mailbox Address LSW [F:2] | F:2 | R/W | 0x0000 | uP LSW Mailbox address [F:2]. The address of where to read and write from in the Microcontroller Mailbox. This is self-incrementing and automatically increments after each read and write operation. |



4.6.2.6.24 Global Mailbox Interface 5: Address 1E.204

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------|--------|------|---------|----------------------|
| uP Mailbox Data MSW [1F:10] | F:0 | R/W | 0x0000 | uP Mailbox data MSW. |

4.6.2.6.25 Global Mailbox Interface 6: Address 1E.205

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------|--------|------|---------|----------------------|
| uP Mailbox Data LSW [F:0] | F:0 | R/W | 0x0000 | uP Mailbox data LSW. |

4.6.2.6.26 Global Mailbox Interface 7: Address 1E.206

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------|--------|------|---------|------------------------------------|
| Reserved | 0 | RSV | | Reserved. Do not modify. |
| uP Mailbox CRC Read Enable | 1 | R/W | 0b | 1b = Update uP mailbox CRC on read |
| Reserved | F:2 | RSV | | Reserved. Do not modify. |

4.6.2.6.27 Global Microprocessor Scratch Pad 1: Address 1E.300

| Field Name | Bit(s) | Type | Default | Description |
|---------------------|--------|------|---------|------------------------------|
| Scratch Pad 1 [F:0] | F:0 | R/W | 0x0000 | General Purpose Scratch Pad. |

4.6.2.6.28 Global Microprocessor Scratch Pad 2: Address 1E.301

| Field Name | Bit(s) | Type | Default | Description |
|---------------------|--------|------|---------|------------------------------|
| Scratch Pad 2 [F:0] | F:0 | R/W | 0x0000 | General Purpose Scratch Pad. |

4.6.2.6.29 Global Control 1: Address 1E.C000

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |

4.6.2.6.30 Global Control 2: Address 1E.C001

| Field Name | Bit(s) | Type | Default | Description |
|--------------|--------|------|---------|---|
| uP Run Stall | 0 | R/W | 0b | Deactivates the uP. 0b = uP normal mode. 1b = uP Run Stall. |
| Reserved | 5:1 | RSV | | Reserved. Do not modify. |



| Field Name | Bit(s) | Type | Default | Description |
|-----------------------|--------|------|---------|--|
| uP Run Stall Override | 6 | R/W | 0b | Selects the uP Run Stall from the "uP Run Stall" bit (Bit [0]). Pin no longer brought out as deprecated. 0b = Reserved. 1b = uP Run Stall from "uP Run Stall" bit (Bit [0]). |
| Reserved | E:7 | RSV | | Reserved. Do not modify. |
| uP Reset | F | R/W | 0b | Resets the uP and the PIF master and slave bus. Is active for a minimum of 100 μ s. 1b = Reset |

4.6.2.6.31 Global Reset Control: Address 1E.C006

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------|--------|-----------|---------|--|
| Reserved | D:0 | RSV | | Reserved. Do not modify. |
| Global MMD Reset Disable | E | R/W PD | 0b | Setting this bit prevents a Global S/W reset or Global S/W reset from resetting the Global MMD registers. 0b = Enable the S/W reset to the Global MMD registers. 1b = Disable the S/W reset to the Global MMD registers. |
| Reserved | F | RSV | | Reserved. Do not modify. |

4.6.2.6.32 Global Diagnostic Provisioning: Address 1E.C400

| Field Name | Bit(s) | Type | Default | Description |
|--------------------|--------|-----------|---------|---|
| Reserved | E:0 | RSV | | Reserved. Do not modify. |
| Enable Diagnostics | F | R/W PD | 1b | 1b = Chip performs diagnostics on power-up. |

4.6.2.6.33 Global Thermal Provisioning 1: Address 1E.C420

| Field Name | Bit(s) | Type | Default | Description |
|------------------|--------|-----------|---------|-----------------------------------|
| Reserved 0 [F:0] | R:0 | R/W PD | 0x0000 | Internal reserved. Do not modify. |

4.6.2.6.34 Global Thermal Provisioning 2: Address 1E.C421

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------------|--------|-----------|---------|---|
| High Temp Failure Threshold [F:0] | F:0 | R/W PD | 0x4600 | Bits [F:0] of high temperature failure threshold. 2's complement value with the LSB representing 1/256 of a degree Celsius. This corresponds to -40 $^{\circ}$ C = 0xD800. Default is 70 $^{\circ}$ C. Note: All Thresholds are orthogonal and can be set to any value regardless of the value of the other thresholds (for example, High-Temperature-Warning (1E.C423) could be higher than High-Temperature-Failure. |



4.6.2.6.35 Global Thermal Provisioning 3: Address 1E.C422

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------------|--------|--------|---------|--|
| Low Temp Failure Threshold [F:0] | F:0 | R/W PD | 0x0000 | <p>Bits [F:0] of low temperature failure threshold.</p> <p>2's complement value with the LSB representing 1/256 of a degree Celsius. This corresponds to -40 °C = 0xD800. Default is 0 °C.</p> <p>Note: All Thresholds are orthogonal and can be set to any value regardless of the value of the other thresholds (for example, Low-Temperature-Warning (1E.C424) could be lower than Low-Temperature-Failure).</p> |

4.6.2.6.36 Global Thermal Provisioning 4: Address 1E.C423

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------------|--------|--------|---------|---|
| High Temp Warning Threshold [F:0] | F:0 | R/W PD | 0x3C00 | <p>Bits [F:0] of high temperature warning threshold.</p> <p>2's complement value with the LSB representing 1/256 of a degree Celsius. This corresponds to -40 °C = 0xD800. Default is 60 °C.</p> <p>Note: All Thresholds are orthogonal and can be set to any value regardless of the value of the other thresholds (for example, High-Temperature-Warning could be higher than High-Temperature-Failure (1E.C421)).</p> |

4.6.2.6.37 Global Thermal Provisioning 5: Address 1E.C424

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------------|--------|--------|---------|---|
| Low Temp Warning Threshold [F:0] | F:0 | R/W PD | 0x0A00 | <p>Bits [F:0] of low temperature warning threshold.</p> <p>2's complement value with the LSB representing 1/256 of a degree Celsius. This corresponds to -40 °C = 0xD800. Default is 10 °C.</p> <p>Note: All Thresholds are orthogonal and can be set to any value regardless of the value of the other thresholds (for example, Low-Temperature-Warning could be lower than Low-Temperature-Failure (1E.C422)).</p> |

4.6.2.6.38 Global LED Provisioning 1: Address 1E.C430

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------------|--------|--------|---------|--|
| LED #0 Activity Stretch [1:0] | 1:0 | R/W PD | 11b | <p>00b = No stretching.</p> <p>01b = Stretch activity by 28 ms.</p> <p>10b = Stretch activity by 60 ms.</p> <p>11b = Stretch activity by 100 ms.</p> |
| LED #0 Transmit Activity | 2 | R/W PD | 0b | 1b = LED toggles on transmit activity. |
| LED #0 Receive Activity | 3 | R/W PD | 0b | 1b = LED toggles on receive activity. |
| LED #0 Connecting | 4 | R/W PD | 0b | 1b = LED is on when attempting to connect. |
| LED #0 100 Mb/ s Link Established | 5 | R/W PD | 0b | 1b = LED is on when link connects at 100 Mb/s. |
| LED #0 1 Gb/s Link Established | 6 | R/W PD | 0b | 1b = LED is on when link connects at 1 GbE. |



| Field Name | Bit(s) | Type | Default | Description |
|----------------------------------|--------|--------|---------|--|
| LED #0 10 Gb/s Link Established | 7 | R/W PD | 0b | 1b = LED is on when link connects at 10 GbE. |
| LED #0 Manual Set | 8 | R/W PD | 0b | 1b = LED On. |
| Reserved Provisioning C430 [4:0] | D:9 | R/W PD | 0x00 | Reserved for future use. |
| Reserved | F:E | RSV | | Reserved. Do not modify. |

4.6.2.6.39 Global LED Provisioning 2: Address 1E.C431

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------------|--------|--------|---------|---|
| LED #1 Activity Stretch [1:0] | 1:0 | R/W PD | 11b | 00b = No stretching. 01b = Stretch activity by 28 ms. 10b = Stretch activity by 60 ms. 11b = Stretch activity by 100 ms. |
| LED #1 Transmit Activity | 2 | R/W PD | 0b | 1b = LED toggles on transmit activity. |
| LED #1 Receive Activity | 3 | R/W PD | 0b | 1b = LED toggles on receive activity. |
| LED #1 Connecting | 4 | R/W PD | 0b | 1b = LED is on when attempting to connect. |
| LED #1 100 Mb/ s Link Established | 5 | R/W PD | 0b | 1b = LED is on when link connects at 100 Mb/s. |
| LED #1 1 Gb/s Link Established | 6 | R/W PD | 0b | 1b = LED is on when link connects at 1 GbE. |
| LED #1 10 Gb/s Link Established | 7 | R/W PD | 0b | 1b = LED is on when link connects at 10 GbE. |
| LED #1 Manual Set | 8 | R/W PD | 0b | 1b = LED On. |
| Reserved Provisioning C431 [4:0] | D:9 | R/W PD | 0x00 | Reserved for future use. |
| Reserved | F:E | RSV | | Reserved. Do not modify. |

4.6.2.6.40 Global LED Provisioning 3: Address 1E.C432

| Field Name | Bit(s) | Type | Default | Description |
|-------------------------------|--------|--------|---------|---|
| LED #2 Activity Stretch [1:0] | 1:0 | R/W PD | 11b | 00b = No stretching. 01b = Stretch activity by 28 ms. 10b = Stretch activity by 60 ms. 11b = Stretch activity by 100 ms. |
| LED #2 Transmit Activity | 2 | R/W PD | 0b | 1b = LED toggles on transmit activity. |
| LED #2 Receive Activity | 3 | R/W PD | 0b | 1b = LED toggles on receive activity. |
| LED #2 Connecting | 4 | R/W PD | 0b | 1b = LED is on when attempting to connect. |



| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------------|--------|--------|---------|--|
| LED #2 100 Mb/ s Link Established | 5 | R/W PD | 0b | 1b = LED is on when link connects at 100 Mb/s. |
| LED #2 1 Gb/s Link Established | 6 | R/W PD | 0b | 1b = LED is on when link connects at 1 GbE. |
| LED #2 10 Gb/s Link Established | 7 | R/W PD | 0b | 1b = LED is on when link connects at 10 GbE. |
| LED #2 Manual Set | 8 | R/W PD | 0b | 1b = LED On. |
| Reserved Provisioning C431 [4:0] | D:9 | R/W PD | 0x00 | Reserved for future use. |
| Reserved | F:E | RSV | | Reserved. Do not modify. |

4.6.2.6.41 Global LED Provisioning 4: Address 1E.C433

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |

4.6.2.6.42 Global LED Provisioning 5: Address 1E.C434

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |

4.6.2.6.43 Global LED Provisioning 6: Address 1E.C435

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |

4.6.2.6.44 Global LED Provisioning 7: Address 1E.C436

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |

4.6.2.6.45 Global LED Provisioning 8: Address 1E.C437

| Field Name | Bit(s) | Type | Default | Description |
|--------------------|--------|--------|---------|--|
| LED Operation Mode | 0 | R/W PD | 0b | LED blinking rate is based on Mode #2 algorithm or classic Intel algorithm. 0b = LED link activity in Intel classic mode. 1b = LED link activity in Mode #2. |
| Reserved | F:1 | RSV | | Reserved. Do not modify. |



4.6.2.6.46 Global LED Provisioning 15: Address 1E.C43E

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |

4.6.2.6.47 Global General Provisioning 1: Address 1E.C440

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |

4.6.2.6.48 Global General Provisioning 2: Address 1E.C441

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------|--------|--------|---------|--|
| Reserved | 2:0 | RSV | | Reserved. Do not modify. |
| MDIO Preamble Detection Disable | 3 | R/W PD | 0b | 0b = Enable preamble detection on MDIO. 1b = Suppress preamble detection on MDIO. |
| MDIO Drive Configuration | 4 | R/W PD | 0b | When the MDIO driver is in open drain mode during a read cycle, "0" data is actively driven out of the MDIO, "1" data sets the MDIO driver in high impedance state, and an external pull-up is set the MDIO line to "1". The Turn-Around "0" is also actively driven out of the MDIO. Therefore, in open drain mode, the Turn-Around is still "0". 0b = MDIO driver is in normal mode. 1b = MDIO driver is in open drain mode. |
| Reserved | C:5 | RSV | | Reserved. Do not modify. |
| MDIO Read MSW First Enable | D | R/W PD | 0b | This bit configures whether the MSW or LSW must be read first for counters greater than 16 bits. 0b = LSW of counter must be read first. 1b = MSW of counter must be read first. |
| MDIO Broadcast Mode Enable | E | R/W PD | 0b | When enabled, writes and load MMD address opcodes are supported. Read opcodes are ignored. 0b = Disable broadcast on n address set in 1E.C446 (refer to Section 4.6.2.6.53). 1b = Enable broadcast on address set in 1E.C446 (refer to Section 4.6.2.6.53). |
| Reserved | F | RSV | | Reserved. Do not modify. |

4.6.2.6.49 Global General Provisioning 3: Address 1E.C442

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | R/W | 0b | | Reserved. |
| Reserved | F:1 | RSV | | Reserved. Do not modify. |



4.6.2.6.50 Global General Provisioning 4: Address 1E.C443

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |

4.6.2.6.51 Global General Provisioning 5: Address 1E.C444

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |

4.6.2.6.52 Global General Provisioning 6: Address 1E.C445

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |

4.6.2.6.53 Global General Provisioning 7: Address 1E.C446

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |

4.6.2.6.54 Global General Provisioning 8: Address 1E.C447

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|--------|---------|---|
| MDIO Broadcast Address Configuration [4:0] | 4:0 | R/W PD | 0x1F | Broadcast address. Allows setting the broadcast address. |
| Reserved | F:5 | RSV | | Reserved. Do not modify. |

4.6.2.6.55 Global General Provisioning 9: Address 1E.C448

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |

4.6.2.6.56 Global General Provisioning 10: Address 1E.C449

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------|--------|------|---------|--------------------------|
| MDIO Preamble Length [6:0] | 6:0 | R/W | 0x02 | MDIO Preamble Length. |
| Reserved | F:7 | RSV | | Reserved. Do not modify. |



4.6.2.6.57 Global NVR Provisioning 1: Address 1E.C450

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------|--------|--------|---------|---|
| NVR Address Length [1:0] | 1:0 | R/W PD | 10b | NVR address length ranges from 0 bytes up to 3 bytes. Sets the length of the address field used in read and write operations. Use of this field is enabled via Bit 8 of "Global NVR Provisioning 2: Address 1E.C451" on page 195. |
| Reserved | 3:2 | RSV | | Reserved. Do not modify. |
| NVR Dummy Length [2:0] | 6:4 | R/W PD | 000b | NVR dummy length ranges from 0 bytes to 4 bytes. Sets the length of the dummy field used in some manufacturer's read status and write status operations. |
| Reserved | 7 | RSV | | Reserved. Do not modify. |
| NVR Data Length [2:0] | A:8 | R/W PD | 100b | NVR data length ranges from 0 bytes to 4 bytes. Sets the length of the data burst used in read and write operations. |
| Reserved | F:B | RSV | | Reserved. Do not modify. |

4.6.2.6.58 Global NVR Provisioning 2: Address 1E.C451

| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------|--------|--------|---------|---|
| NVR Clock Divide [7:0] | 7:0 | R/W PD | 0xA0 | NVR clock divide. Clock frequency is divided by the NVR clock divide + 1. |
| NVR Address Length Override | 8 | R/W PD | 0b | When this bit = 0 and NVR_SIZE pin = 0, the NVR address length is 2 bytes. When this bit = 0 and the NVR_SIZE pin = 1, the NVR address length is 3 bytes. When this bit = 1 the NVR address length is from the "NVR Address Length [1:0]". 0b = NVR address length is based on the "NVR_SIZE" pin. 1b = NVR address length is based on the "NVR Address Length [1:0]" register. |
| Reserved | F:9 | RSV | | Reserved. Do not modify. |

4.6.2.6.59 Global NVR Provisioning 3: Address 1E.C452

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | 0 | R/W | 0b | Reserved |
| Reserved | 1 | R/W | 0b | Reserved |
| Reserved | F:2 | RSV | | Reserved. Do not modify. |

4.6.2.6.60 Global NVR Provisioning 4: Address 1E.C453

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | 3:0 | RSV | | Reserved. Do not modify. |
| NVR Reset | 4 | R/W | 0b | 1b = Reset SPI |
| Reserved | F:5 | RSV | | Reserved. Do not modify. |



4.6.2.6.61 Global Reserved Provisioning 1: Address 1E.C470

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------------|--------|--------|---------|--|
| Reserved | 3:0 | RSV | | Reserved. Do not modify. |
| Initiate Cable Diagnostics | 4 | R/W SC | 0b | <p>Perform cable diagnostics regardless of link state. If link is up, setting this bit causes the link to drop while diagnostics are performed. This bit is self-clearing upon completion of the cable diagnostics.</p> <p>1b = Perform cable diagnostics.</p> <p>Note: This is a processor intensive operation. Completion of this operation can also be monitored via 1E.C831.F (refer to Section 4.6.2.6.83).</p> |
| Reserved | C:5 | RSV | | Reserved. Do not modify. |
| Extended MDI Diagnostics Select [1:0] | E:D | R/W PD | 00b | <p>These bits select what sort of cable diagnostics to perform.</p> <p>00b = TDR Data 01b = RFI Channel PSD 10b = Noise PSD while the local Tx is Off 11b = Noise PSD while the local Tx is On</p> <p>For regular cable diagnostics, Bit [F] is set to 0b, and the diagnostics are triggered by setting Bit [4].</p> <p>For extended diagnostics, Bit [F] is set to 1b, and the desired extended diagnostics are selected by Bits [E:D]. The routine is then triggered by setting Bit [4].</p> <p>Each of the extended diagnostic routines present data for all for MDI pairs (A, B, C, D) consecutively, and after the data for each channel is gathered Bits [F:D] are reset. To get the data for the next pair, Bits [F:D] must be set back to the desired value (which must be the same as the initial channel). This continues until the data for all channels has been gathered. The address in memory where the data is stored is given in 1E.C802 and 1E.C804 (refer to Section 4.6.2.6.74 and Section 4.6.2.6.76, respectively).</p> <p>For the case of PSD, the structure is as follows:</p> <pre>Int32 info Int16 data[Len] Info = Len << 16 TxEnable << 8 Pair (0 = A, etc.)</pre> <p>For TDR:</p> <pre>Int32 info Int16 tdr_A[Len] Int16 tdr_B[Len] Int16 tdr_C[Len] Int16 tdr_D[Len] Info = Len << 16 Channel</pre> <p>TDR data is from the current pair to all other pairs.</p> <p>At the end of retrieving extended MDI diag data, the part is reset. Conversely, the only way to exit this routine once it starts is to issue a PMA reset.</p> |
| Diagnostics Select | F | R/W PD | 0b | <p>0b = Provide normal cable diagnostics. 1b = Provide Extended MDI Diagnostics Information.</p> |

4.6.2.6.62 Global Reserved Provisioning 2: Address 1E.C471

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|--------|---------|-------------|
| Reserved | 5:0 | R/W uP | 0x00 | Reserved |



| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|-----------|---------|--------------------------|
| Reserved | 6 | R/W uP | 0b | Reserved |
| Reserved | F:7 | RSV | | Reserved. Do not modify. |

4.6.2.6.63 Global Reserved Provisioning 3: Address 1E.C472

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|-----------------|---------|---|
| Enable 5th Channel RFI Cancellation | 0 | R/W PD uP | 0b | 0b = 5th channel AFE is powered down, 5th channel digital is clock gated, RFI cancelers are disabled. 1b = 5th channel and RFI cancelers operation enabled. Note: The value of this bit at the time of auto-negotiation sets the local PHY behavior until the next time auto-negotiation occurs. |
| Reserved | 1 | R/W PD uP | 0b | Reserved. |
| External VDD Change Request [3:0] | 5:2 | R/W PD | 0x0 | The amount of VDD change requested by firmware, in mV (2's complement value). |
| Tunable External VDD Power Supply Present | 6 | R/W PD | 0b | This bit must be set if tuning of external power supply is desired. 0b = No tunable external VDD power supply present. 1b = Tunable external VDD power supply present. |
| Reserved | D:7 | RSV | | Reserved. Do not modify. |
| Enable VDD Power Supply Tuning | E | R/W PD | 0b | Controls whether the PHY attempts to tune the external VDD power supply via the SMBus. 0b = Disable external VDD power supply tuning is disabled. 1b = Enable external VDD power supply tuning. This bit is only operational if the external supply is present. Refer to 1E.C472.6 in Section 4.6.2.6.63 . |
| Reserved | F | RSV | | Reserved. Do not modify. |

4.6.2.6.64 Global Reserved Provisioning 4: Address 1E.C473

| Field Name | Bit(s) | Type | Default | Description |
|--------------------|--------|-----------|---------|---|
| Training SNR [7:0] | 7:0 | R/W PD | 0x00 | SNR during 10G training on the worst channel. SNR is in steps of 0.1 dB The SNR margin that is enjoyed by the worst channel, over and above the minimum SNR required to operate at a BER of 10-12. It is reported with 0.1 dB of resolution to an accuracy of 0.5 dB within the range of -12.7 dB to 12.7 dB. The number is in offset binary, with 0.0 dB represented by 0x8000. |
| Reserved | F:8 | RSV | | Reserved. Do not modify. |

4.6.2.6.65 Global Reserved Provisioning 5: Address 1E.C474

| Field Name | Bit(s) | Type | Default | Description |
|-------------------------------|--------|-----------|---------|--------------------------|
| Reserved | 0 | R/W | 0b | Reserved |
| Reserved Provisioning 5 [F:1] | F:1 | R/W PD | 0x0000 | Reserved for future use. |



4.6.2.6.66 Global Reserved Provisioning 6: Address 1E.C475

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------|--------|--------|---------|---|
| Reserved | 1:0 | RSV | | Reserved. Do not modify. |
| Smart Power-Down Enable | 2 | R/W PD | 0b | Smart power down (SPD) is the lowest power mode at which PHY is able to auto-negotiate. SPD can be enabled with bit 1E.C475.2 (refer to Section 4.6.2.6.66). 0b = Smart power-down mode disabled. 1b = Enable smart power down mode. |
| Deadlock Avoidance Enable | 3 | R/W PD | 0b | 0b = SPD without deadlock avoidance: PHY transmitter is shut down, no auto-negotiation pulses are sent on the line but the receiver is active and able to detect the pulses 1b = SPD with deadlock avoidance: PHY transmits auto-negotiation pulses (FLPs) at a slower rate (~ 1 FLP / 100 ms) than specified by auto-negotiation standard (~1 FLP / 8.25 ms). Receiver is active and able to detect the pulses. |
| CFR Support | 4 | R/W PD | 0b | 0b = Local PHY does not support Cisco Fast Retrain. 1b = Local PHY supports Cisco Fast Retrain. |
| CFR THP | 5 | R/W PD | 0b | 0b = Local PHY does not require local PHY to enable THP. 1b = Local PHY requires local PHY to enable THP. |
| CFR Extended Maxwait | 6 | R/W PD | 0b | 0b = Local PHY does not require extended maxwait. 1b = Local PHY requires extended maxwait. |
| CFR Disable Timer | 7 | R/W PD | 0b | 0b = Local PHY does not require cfr_disable timer. 1b = Local PHY requires cfr_disable timer. |
| CFR LP Support | 8 | R/W PD | 0b | 0b = Link partner does not support Cisco Fast Retrain. 1b = Link partner supports Cisco Fast Retrain. |
| CFR LP THP | 9 | R/W PD | 0b | 0b = Link partner does not require local PHY to enable THP. 1b = Link partner requires local PHY to enable THP. |
| CFR LP Extended Maxwait | A | R/W PD | 0b | 0b = Link partner does not require extended maxwait. 1b = Link partner requires extended maxwait. |
| CFR LP Disable Timer | B | R/W PD | 0b | 0b = Link partner does not require cfr_disable timer. 1b = Link partner requires cfr_disable timer. |
| Reserved Provisioning 6 | C | R/W PD | 0b | Internal reserved. Do not modify |
| Smart Power-Down Status | D | R/W PD | 0b | 0b = Smart Power-Down Inactive. 1b = Smart Power-Down Active. |
| Reserved | F:E | RSV | | Reserved. Do not modify. |

4.6.2.6.67 Global Reserved Provisioning 9: Address 1E.C478

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------------|--------|--------|---------|--|
| Reserved Provisioning 9 [A:0] | A:0 | R/W PD | 0x000 | Reserved for future use |
| DTE Drop Reporting Timer [3:0] | E:B | R/W PD | 0x0 | Number of seconds between loss of link partner filter and assertion of no-power-needed state, in 5 second increments (e.g., 0x4 = 20 seconds). These bits are used to set how long the PHY waits after it no longer detects the link partner filter before declaring that power is not needed. |
| DTE Enable | F | R/W PD | 0b | 0b = Disable DTE 1b = Enable DTE |



4.6.2.6.68 Global Reserved Provisioning 10: Address 1E.C479

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------------|--------|--------|---------|--|
| Reserved Provisioning 10 [E:0] | E:0 | R/W PD | 0x0000 | Reserved for future use. |
| Power Up Stall | F | R/W PD | 0b | This bit needs to be provisioned in Power Up Init for firmware to stall. 0b = Unstall the FW. 1b = Stall FW at Power Up. |

4.6.2.6.69 Global SMBus 0 Provisioning 6: Address 1E.C485

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------|--------|------|---------|----------------------------------|
| Reserved | 0 | RSV | | Reserved. Do not modify. |
| SMB 0 Slave Address [7:1] | 7:1 | R/W | 0x00 | SMB slave address configuration. |
| Reserved | F:8 | RSV | | Reserved. Do not modify. |

4.6.2.6.70 Global SMBus 1 Provisioning 6: Address 1E.C495

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------|--------|------|---------|----------------------------------|
| Reserved | 0 | RSV | | Reserved. Do not modify. |
| SMB 1 Slave Address [7:1] | 7:1 | R/W | 0x00 | SMB slave address configuration. |
| Reserved | F:8 | RSV | | Reserved. Do not modify. |

4.6.2.6.71 Global EEE Provisioning 1: Address 1E.C4A0

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|--------|---------|---|
| EEE Mode | 0 | R/W PD | 0b | EEE mode of operation. 0b = Disable 1b = Enable |
| Reserved | F:1 | RSV | | Reserved. Do not modify. |



4.6.2.6.72 Global Cable Diagnostic Status 1: Address 1E.C800

| Field Name | Bit(s) | Type | Default | Description |
|---------------------|--------|------|---------|---|
| Pair D Status [2:0] | 2:0 | RO | | Summarizes the worst impairment on Pair D. [6:4]: 000b = OK 001b = Connected to Pair A 010b = Connected to Pair B 011b = Connected to Pair C 100b = Short Circuit (< 30 Ω) 101b = Low Mismatch (< 85 Ω) 110b = High Mismatch (> 115 Ω) 111b = Open Circuit (> 300 Ω) |
| Reserved | 3 | RSV | | Reserved. Do not modify. |
| Pair C Status [2:0] | 6:4 | RO | | Summarizes the worst impairment on Pair C. [9:7]: 000b = OK 001b = Connected to Pair D 010b = Connected to Pair A 011b = Connected to Pair B 100b = Short Circuit (< 30 Ω) 101b = Low Mismatch (< 85 Ω) 110b = High Mismatch (> 115 Ω) 111b = Open Circuit (> 300 Ω) |
| Reserved | 7 | RSV | | Reserved. Do not modify. |
| Pair B Status [2:0] | A:8 | RO | | Summarizes the worst impairment on Pair B. [C:A]: 000b = OK 001b = Connected to Pair C 010b = Connected to Pair D 011b = Connected to Pair A 100b = Short Circuit (< 30 Ω) 101b = Low Mismatch (< 85 Ω) 110b = High Mismatch (> 115 Ω) 111b = Open Circuit (> 300 Ω) |
| Reserved | B | RSV | | Reserved. Do not modify. |
| Pair A Status [2:0] | E:C | RO | | Summarizes the worst impairment on Pair A. [F:D]: 000b = OK 001b = Connected to Pair B 010b = Connected to Pair C 011b = Connected to Pair D 100b = Short Circuit (< 30 Ω) 101b = Low Mismatch (< 85 Ω) 110b = High Mismatch (> 115 Ω) 111b = Open Circuit (> 300 Ω) |
| Reserved | F | RSV | | Reserved. Do not modify. |



4.6.2.6.73 Global Cable Diagnostic Status 2: Address 1E.C801

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------|--------|------|---------|---|
| Pair A Reflection #2 [7:0] | 7:0 | RO | | The distance in meters, accurate to ± 1 m, of the second of the four worst reflections seen by the PHY on Pair A. The distance to this reflection is given in "Global Cable Diagnostic Impedance 1: Address 1E.C880" on page 205. A value of zero indicates that this reflection does not exist or was not computed. |
| Pair A Reflection #1 [7:0] | F:8 | RO | | The distance in meters, accurate to ± 1 m, of the first of the four worst reflections seen by the PHY on Pair A. The distance to this reflection is given in "Global Cable Diagnostic Impedance 1: Address 1E.C880" on page 205. A value of zero indicates that this reflection does not exist or was not computed. |

4.6.2.6.74 Global Cable Diagnostic Status 3: Address 1E.C802

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------|--------|------|---------|---|
| Impulse Response MSW [F:0] | F:0 | RO | | The MSW of the memory location that contains the start of the impulse response data for the Extended Diagnostic type in 1E.C470.E:D. Refer to Section 4.6.2.6.61 for more information. |

4.6.2.6.75 Global Cable Diagnostic Status 4: Address 1E.C803

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------|--------|------|---------|---|
| Pair B Reflection #2 [7:0] | 7:0 | RO | | The distance in meters, accurate to ± 1 m, of the second of the four worst reflections seen by the PHY on Pair B. The distance to this reflection is given in "Global Cable Diagnostic Impedance 2: Address 1E.C881" on page 206. A value of zero indicates that this reflection does not exist or was not computed. |
| Pair B Reflection #1 [7:0] | F:8 | RO | | The distance in meters, accurate to ± 1 m, of the first of the four worst reflections seen by the PHY on Pair B. The distance to this reflection is given in "Global Cable Diagnostic Impedance 2: Address 1E.C881" on page 206. A value of zero indicates that this reflection does not exist or was not computed. |

4.6.2.6.76 Global Cable Diagnostic Status 5: Address 1E.C804

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------|--------|------|---------|---|
| Impulse Response LSW [F:0] | F:0 | RO | | The LSW of the memory location that contains the start of the impulse response data for the Extended Diagnostic type in 1E.C470.E:D. Refer to Section 4.6.2.6.61 for more information. |



4.6.2.6.77 Global Cable Diagnostic Status 6: Address 1E.C805

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------|--------|------|---------|---|
| Pair C Reflection #2 [7:0] | 7:0 | RO | | The distance in meters, accurate to ± 1 m, of the second of the four worst reflections seen by the PHY on Pair C. The distance to this reflection is given in "Global Cable Diagnostic Impedance 3: Address 1E.C882" on page 207. A value of zero indicates that this reflection does not exist or was not computed. |
| Pair C Reflection #1 [7:0] | F:8 | RO | | The distance in meters, accurate to ± 1 m, of the first of the four worst reflections seen by the PHY on Pair C. The distance to this reflection is given in "Global Cable Diagnostic Impedance 3: Address 1E.C882" on page 207. A value of zero indicates that this reflection does not exist or was not computed. |

4.6.2.6.78 Global Cable Diagnostic Status 7: Address 1E.C806

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | F:0 | RSV | | Reserved. Do not modify. |

4.6.2.6.79 Global Cable Diagnostic Status 8: Address 1E.C807

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------|--------|------|---------|---|
| Pair D Reflection #2 [7:0] | 7:0 | RO | | The distance in meters, accurate to ± 1 m, of the second of the four worst reflections seen by the PHY on Pair D. The distance to this reflection is given in "Global Cable Diagnostic Impedance 4: Address 1E.C883" on page 208. A value of zero indicates that this reflection does not exist or was not computed. |
| Pair D Reflection #1 [7:0] | F:8 | RO | | The distance in meters, accurate to ± 1 m, of the first of the four worst reflections seen by the PHY on Pair D. The distance to this reflection is given in "Global Cable Diagnostic Impedance 4: Address 1E.C883" on page 208. A value of zero indicates that this reflection does not exist or was not computed. |

4.6.2.6.80 Global Thermal Status 1: Address 1E.C820

| Field Name | Bit(s) | Type | Default | Description |
|-------------------|--------|------|---------|---|
| Temperature [F:0] | F:0 | RO | | Bit [F:0] of temperature. 2's complement value with the LSB representing 1/256 of a degree Celsius. This corresponds to -40 °C = 0xD800. Default is 70 °C. |

4.6.2.6.81 Global Thermal Status 2: Address 1E.C821

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | 0 | RO | | Reserved. |
| Reserved | F:1 | RSV | | Reserved. Do not modify. |



4.6.2.6.82 Global General Status 1: Address 1E.C830

| Field Name | Bit(s) | Type | Default | Description |
|------------|--------|------|---------|--------------------------|
| Reserved | A:0 | RSV | | Reserved. Do not modify. |
| Reserved | B | RO | | Reserved. Do not modify. |
| Reserved | C | RO | | Reserved. Do not modify. |
| Reserved | D | RO | | Reserved. Do not modify. |
| Reserved | E | RO | | Reserved. Do not modify. |
| Reserved | F | RSV | | Reserved. Do not modify. |

4.6.2.6.83 Global General Status 2: Address 1E.C831

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|--|
| Reserved | E:0 | RSV | | Reserved. Do not modify. |
| Processor Intensive MDIO Operation In- Progress | F | RO | | <p>This bit may be used with certain processor-intensive MDIO commands (such as Loopbacks, Test Modes, Low power modes, Tx-Disable, Restart auto-negotiation, Cable Diagnostics, etc.) that take longer than an MDIO cycle to complete.</p> <p>0b = Processor-intensive MDIO operation completed. 1b = PHY microprocessor is busy with a processor-intensive MDIO operation.</p> <p>Upon receiving an MDIO command that involves the PHY's microprocessor, this bit is set, and when the command is completed, this bit is cleared.</p> <p>Note: This bit should be checked only after 1 ms of issuing a processor-intensive MDIO operation.</p> <p>The list of operations that set this bit are as follows:</p> <ul style="list-style-type: none"> • 1.0.0, PMA Loopback • 1.0.B, Low power mode • 1.9.4:0, Tx Disable • 1.84, 10G Test modes • 1.E400.F, External loopback • 3.0.B, Low power mode • 3.0.E, System PCS loopback • 3.C471.5, PRBS Test • 3.C471.6, PRBS Test • 3.E471.5, PRBS Test • 3.E471.6, PRBS Test • 4.0.B, Low power mode • 4.0.E, PHY-XS network loopback • 4.C440, Output clock control, Load SERDES parameters • 4.F802.E, System loopback • 4.C444.F:B, Loopback Control • 4.C444.4:2, Packet generation • 4.C445.C, SERDES calibration • 7.0.9, Restart auto-negotiation • 1D.C280, 1G/100M Network loopback • 1D.C500, 1G System loopback • 1D.C501, 1G / 100M Test modes • 1E.C470.4, Cable diagnostics |



4.6.2.6.84 Global Pin Status: Address 1E.C840

| Field Name | Bit(s) | Type | Default | Description |
|------------------------|--------|------|---------|---|
| LED Pullup State [5:0] | 5:0 | RO | | 0b = LED output pin is pulled low. 1b = LED output pin is pulled high. |
| Reserved | 6 | RSV | | Reserved. Do not modify. |
| Tx Enable | 7 | RO | | Current Value of Tx Enable pin. 0b = Disable Transmitter. |
| Reserved | 8 | RSV | | Reserved. Do not modify. |
| Package Connectivity | 9 | RO | | Value of the package connection pin. |
| Reserved | C:A | RSV | | Reserved. Do not modify. |
| Reserved | D | RO | | Reserved |
| Reserved | F:E | RSV | | Reserved. Do not modify. |

4.6.2.6.85 Global Fault Message: Address 1E.C850

| Field Name | Bit(s) | Type | Default | Description |
|---------------|--------|------|---------|---|
| Message [F:0] | F:0 | RO | | <p>Error code describing fault.</p> <p>Code # Description</p> <p>0x8001 = Firmware not compatible with chip architecture. This fault occurs when firmware compiled for a different microprocessor core is loaded.</p> <p>0x8002 = VCO calibration failed. This occurs when the main PLLs on chip fail to lock. This is not possible to trigger.</p> <p>0x8003 = Reserved.</p> <p>0x8005 = Unexpected device ID. This occurs if the device ID programmed into the internal E-Fuse registers is not valid. This is not possible to trigger.</p> <p>0x8006 = Computed checksum does not match expected checksum. This occurs when the FLASH checksum check performed at boot time fails. This only occurs when the system boots from FLASH.</p> <p>0x8007 = Detected a bit error in static memory. To trigger, corrupt one of the static regions.</p> <p>0xC001 = Illegal Instruction exception. This occurs when the processor attempts to execute an illegal instruction. To trigger this, write an illegal instruction to program memory. It is possible that the bit error check triggers before the illegal instruction is executed.</p> <p>0xC002 = Instruction Fetch Error. Internal physical address or a data error during instruction fetch. This is not possible to trigger.</p> <p>0xC003 = Load Store Error. Internal physical address or data error during load store operation. This is not possible to trigger.</p> <p>0xC004 = Privileged Instruction. Attempt to execute a privileged operation without sufficient privilege. This is not possible to trigger.</p> <p>0xC005 = Unaligned Load or Store. Attempt to load or store data at an address which cannot be handled due to alignment. This is not possible to trigger.</p> <p>0xC006 = Instruction fetch from prohibited space. This is not possible to trigger.</p> <p>0xC007 = Data load from prohibited space. This is not possible to trigger.</p> <p>0xC008 = Data store into prohibited space. This is not possible to trigger.</p> |



4.6.2.6.86 Global Cable Diagnostic Impedance 1: Address 1E.C880

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------|--------|------|---------|---|
| Pair A Reflection #4 [2:0] | 2:0 | RO | | The impedance of the fourth worst reflection on Pair A. The corresponding length of this reflection from the PHY is given in "Global Cable Diagnostic Status 1: Address 1E.C800" on page 200. 0xb = No information available 100b = Short Circuit (< 30 Ω) 101b = Low Mismatch (< 85 Ω) 110b = High Mismatch (> 115 Ω) 111b = Open Circuit (> 300 Ω) |
| Reserved 4 | 3 | RO | | Reserved. Do not modify. |
| Pair A Reflection #3 [2:0] | 6:4 | RO | | The impedance of the third worst reflection on Pair A. The corresponding length of this reflection from the PHY is given in "Global Cable Diagnostic Status 1: Address 1E.C800" on page 200. 0xb = No information available 100b = Short Circuit (< 30 Ω) 101b = Low Mismatch (< 85 Ω) 110b = High Mismatch (> 115 Ω) 111b = Open Circuit (> 300 Ω) |
| Reserved 3 | 7 | RO | | Reserved. Do not modify. |
| Pair A Reflection #2 [2:0] | A:8 | RO | | The impedance of the second worst reflection on Pair A. The corresponding length of this reflection from the PHY is given in "Global Cable Diagnostic Status 1: Address 1E.C800" on page 200. 0xb = No information available 100b = Short Circuit (< 30 Ω) 101b = Low Mismatch (< 85 Ω) 110b = High Mismatch (> 115 Ω) 111b = Open Circuit (> 300 Ω) |
| Reserved 2 | B | RO | | Reserved. Do not modify. |
| Pair A Reflection #1 [2:0] | E:C | RO | | The impedance of the first worst reflection on Pair A. The corresponding length of this reflection from the PHY is given in "Global Cable Diagnostic Status 1: Address 1E.C800" on page 200. 0xb = No information available 100b = Short Circuit (< 30 Ω) 101b = Low Mismatch (< 85 Ω) 110b = High Mismatch (> 115 Ω) 111b = Open Circuit (> 300 Ω) |
| Reserved 1 | F | RO | | Reserved. Do not modify. |



4.6.2.6.87 Global Cable Diagnostic Impedance 2: Address 1E.C881

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------|--------|------|---------|---|
| Pair B Reflection #4 [2:0] | 2:0 | RO | | The impedance of the fourth worst reflection on Pair B. The corresponding length of this reflection from the PHY is given in "Global Cable Diagnostic Status 2: Address 1E.C801" on page 201. 0xb = No information available 100b = Short Circuit (< 30 Ω) 101b = Low Mismatch (< 85 Ω) 110b = High Mismatch (> 115 Ω) 111b = Open Circuit (> 300 Ω) |
| Reserved 4 | 3 | RO | | Reserved. Do not modify. |
| Pair B Reflection #3 [2:0] | 6:4 | RO | | The impedance of the third worst reflection on Pair B. The corresponding length of this reflection from the PHY is given in "Global Cable Diagnostic Status 2: Address 1E.C801" on page 201. 0xb = No information available 100b = Short Circuit (< 30 Ω) 101b = Low Mismatch (< 85 Ω) 110b = High Mismatch (> 115 Ω) 111b = Open Circuit (> 300 Ω) |
| Reserved 3 | 7 | RO | | Reserved. Do not modify. |
| Pair B Reflection #2 [2:0] | A:8 | RO | | The impedance of the second worst reflection on Pair B. The corresponding length of this reflection from the PHY is given in "Global Cable Diagnostic Status 2: Address 1E.C801" on page 201. 0xb = No information available 100b = Short Circuit (< 30 Ω) 101b = Low Mismatch (< 85 Ω) 110b = High Mismatch (> 115 Ω) 111b = Open Circuit (> 300 Ω) |
| Reserved 2 | B | RO | | Reserved. Do not modify. |
| Pair B Reflection #1 [2:0] | E:C | RO | | The impedance of the first worst reflection on Pair B. The corresponding length of this reflection from the PHY is given in "Global Cable Diagnostic Status 2: Address 1E.C801" on page 201. 0xb = No information available 100b = Short Circuit (< 30 Ω) 101b = Low Mismatch (< 85 Ω) 110b = High Mismatch (> 115 Ω) 111b = Open Circuit (> 300 Ω) |
| Reserved 1 | F | RO | | Reserved. Do not modify. |



4.6.2.6.88 Global Cable Diagnostic Impedance 3: Address 1E.C882

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------|--------|------|---------|---|
| Pair C Reflection #4 [2:0] | 2:0 | RO | | The impedance of the fourth worst reflection on Pair C. The corresponding length of this reflection from the PHY is given in "Global Cable Diagnostic Status 3: Address 1E.C802" on page 201. 0xb = No information available 100b = Short Circuit (< 30 Ω) 101b = Low Mismatch (< 85 Ω) 110b = High Mismatch (> 115 Ω) 111b = Open Circuit (> 300 Ω) |
| Reserved 4 | 3 | RO | | Reserved. Do not modify. |
| Pair C Reflection #3 [2:0] | 6:4 | RO | | The impedance of the third worst reflection on Pair C. The corresponding length of this reflection from the PHY is given in "Global Cable Diagnostic Status 3: Address 1E.C802" on page 201. 0xb = No information available 100b = Short Circuit (< 30 Ω) 101b = Low Mismatch (< 85 Ω) 110b = High Mismatch (> 115 Ω) 111b = Open Circuit (> 300 Ω) |
| Reserved 3 | 7 | RO | | Reserved. Do not modify. |
| Pair C Reflection #2 [2:0] | A:8 | RO | | The impedance of the second worst reflection on Pair C. The corresponding length of this reflection from the PHY is given in "Global Cable Diagnostic Status 3: Address 1E.C802" on page 201. 0xb = No information available 100b = Short Circuit (< 30 Ω) 101b = Low Mismatch (< 85 Ω) 110b = High Mismatch (> 115 Ω) 111b = Open Circuit (> 300 Ω) |
| Reserved 2 | B | RO | | Reserved. Do not modify. |
| Pair C Reflection #1 [2:0] | E:C | RO | | The impedance of the first worst reflection on Pair C. The corresponding length of this reflection from the PHY is given in "Global Cable Diagnostic Status 3: Address 1E.C802" on page 201. 0xb = No information available 100b = Short Circuit (< 30 Ω) 101b = Low Mismatch (< 85 Ω) 110b = High Mismatch (> 115 Ω) 111b = Open Circuit (> 300 Ω) |
| Reserved 1 | F | RO | | Reserved. Do not modify. |



4.6.2.6.89 Global Cable Diagnostic Impedance 4: Address 1E.C883

| Field Name | Bit(s) | Type | Default | Description |
|----------------------------|--------|------|---------|---|
| Pair D Reflection #4 [2:0] | 2:0 | RO | | The impedance of the fourth worst reflection on Pair D. The corresponding length of this reflection from the PHY is given in "Global Cable Diagnostic Status 4: Address 1E.C803" on page 201. 0xb = No information available 100b = Short Circuit (< 30 Ω) 101b = Low Mismatch (< 85 Ω) 110b = High Mismatch (> 115 Ω) 111b = Open Circuit (> 300 Ω) |
| Reserved 4 | 3 | RO | | Reserved. Do not modify. |
| Pair D Reflection #3 [2:0] | 6:4 | RO | | The impedance of the third worst reflection on Pair D. The corresponding length of this reflection from the PHY is given in "Global Cable Diagnostic Status 4: Address 1E.C803" on page 201. 0xb = No information available 100b = Short Circuit (< 30 Ω) 101b = Low Mismatch (< 85 Ω) 110b = High Mismatch (> 115 Ω) 111b = Open Circuit (> 300 Ω) |
| Reserved 3 | 7 | RO | | Reserved. Do not modify. |
| Pair D Reflection #2 [2:0] | A:8 | RO | | The impedance of the second worst reflection on Pair D. The corresponding length of this reflection from the PHY is given in "Global Cable Diagnostic Status 4: Address 1E.C803" on page 201. 0xb = No information available 100b = Short Circuit (< 30 Ω) 101b = Low Mismatch (< 85 Ω) 110b = High Mismatch (> 115 Ω) 111b = Open Circuit (> 300 Ω) |
| Reserved 2 | B | RO | | Reserved. Do not modify. |
| Pair D Reflection #1 [2:0] | E:C | RO | | The impedance of the first worst reflection on Pair D. The corresponding length of this reflection from the PHY is given in "Global Cable Diagnostic Status 4: Address 1E.C803" on page 201. 0xb = No information available 100b = Short Circuit (< 30 Ω) 101b = Low Mismatch (< 85 Ω) 110b = High Mismatch (> 115 Ω) 111b = Open Circuit (> 300 Ω) |
| Reserved 1 | F | RO | | Reserved. Do not modify. |

4.6.2.6.90 Global Status: Address 1E.C884

| Field Name | Bit(s) | Type | Default | Description |
|-------------------------|--------|------|---------|--|
| Cable Length [7:0] | 7:0 | RO | | The estimated length of the cable in meters. The length of the cable shown here is estimated from the cable diagnostic engine and should be accurate to ±1 m. |
| Reserved Status 0 [7:0] | F:8 | RO | | Reserved. |



4.6.2.6.91 Global Reserved Status 1: Address 1E.C885

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------|--------|-----------|---------|---|
| ROM Revision [7:0] | 7:0 | ROS PD | 0x00 | ROM Revision Number. Customers may receive multiple ROM images that differ only in their provisioning. This field is used to differentiate those images. This field is used in conjunction with the firmware major and minor revision numbers to uniquely identify ROM images. |
| Reserved | 9:8 | ROS PD | 00b | Reserved. |
| Nearly Seconds MSW [5:0] | F:A | RO | | Bits [16:21] of the 22-bit "Nearly Seconds" uptime counter. The counter is incremented every 1024 ms. |

4.6.2.6.92 Global Reserved Status 2: Address 1E.C886

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------|--------|------|---------|---|
| Nearly Seconds LSW [F:0] | F:0 | RO | | Bits [0:15] of the 22-bit "Nearly Seconds" uptime counter. The counter is incremented every 1024 ms. |

4.6.2.6.93 Global Reserved Status 3: Address 1E.C887

| Field Name | Bit(s) | Type | Default | Description |
|-------------------------|--------|------|---------|--|
| Reserved Status 3 [D:0] | D:0 | RO | | Reserved for future use |
| Power Up Stall Status | E | ROS | 0b | 0b = Firmware is unstalled. 1b = FW is stalled at power up. |
| DTE Status | F | ROS | 0b | 0b = Don't need power. 1b = Need power. |

4.6.2.6.94 Global Alarms 1: Address 1E.CC00

| Field Name | Bit(s) | Type | Default | Description |
|------------------|--------|------|---------|--|
| Reserved Alarm D | 0 | LH | | Reserved for future use. |
| Reserved Alarm C | 1 | LH | | Reserved for future use. |
| Reserved Alarm B | 2 | LH | | Reserved for future use. |
| Reserved Alarm A | 3 | LH | | Reserved for future use. |
| Device Fault | 4 | LH | | When set, a fault has been detected by the uP and the associated 16-bit error code is visible in 1E.C850 (refer to Section 4.6.2.6.85). 1b = Fault |
| Reserved | 5 | RSV | | Reserved. Do not modify. |
| Reset completed | 6 | LH | | This bit is set by the microprocessor when it has completed its initialization sequence. This bit is mirrored in 1.CC02.0 (refer to Section 4.6.2.1.38). 1b = Chip wide reset completed. |
| Reserved | A:7 | RSV | | Reserved. Do not modify. |



| Field Name | Bit(s) | Type | Default | Description |
|--------------------------|--------|------|---------|---|
| Low Temperature Warning | B | LH | | This bit mirrors the matching bit in 1.A070 and 1.A074. This bit is driven by Bits [B] in "Global General Status 1: Address 1E.C830" on page 203. 1b = Low temperature warning threshold has been exceeded. |
| High Temperature Warning | C | LH | | This bit mirrors the matching bit in 1.A070 and 1.A074. This bit is driven by Bits [C] in "Global General Status 1: Address 1E.C830" on page 203. 1b = High temperature warning threshold has been exceeded. |
| Low Temperature Failure | D | LH | | This bit mirrors the matching bit in 1.A070 and 1.A074. This bit is driven by Bits [D] in "Global General Status 1: Address 1E.C830" on page 203. 1b = Low temperature failure threshold has been exceeded. |
| High Temperature Failure | E | LH | | This bit mirrors the matching bit in 1.A070 and 1.A074. This bit is driven by Bits [E] in "Global General Status 1: Address 1E.C830" on page 203. 1b = High temperature failure threshold has been exceeded. |
| Reserved | F | RSV | | Reserved. Do not modify. |

4.6.2.6.95 Global Alarms 2: Address 1E.CC01

| Field Name | Bit(s) | Type | Default | Description |
|--------------------------------|--------|------|---------|--|
| Reserved | 6:0 | RSV | | Reserved. Do not modify. |
| MDIO Command Handling Overflow | 7 | LH | | Assertion of this bit means that more MDIO commands were issued than FW could handle. 1b = PHY was issued more MDIO requests than it could service in its request buffer. |
| Reserved Alarms [2:0] | A:8 | LH | | Reserved. |
| DTE Status Change | B | LH | | Change in 1E.C887.F (refer to Section 4.6.2.6.93). 1b = DTE status change |
| IP Phone Detect | C | LH | | Assertion of this bit means that the presence of an IP Phone has been detected. 1b = IP Phone Detect |
| Reserved | D | RO | | Reserved. |
| Smart Power-Down Entered | E | LH | | When this bit is set, it indicates that the Smart Power-Down state was entered. 1b = Smart Power-Down State Entered. |
| Reserved | F | RSV | | Reserved. Do not modify. |

4.6.2.6.96 Global Alarms 3: Address 1E.CC02

| Field Name | Bit(s) | Type | Default | Description |
|------------------------|--------|------|---------|------------------------------------|
| Watchdog Timer Alarm | 0 | LH | | 1b = Watchdog timer alarm. |
| MDIO Timeout Error | 1 | LH | | 1b = MDIO timeout detected. |
| MDIO MMD Error | 2 | LH | | 1b = Invalid MMD address detected. |
| Reserved | 4:3 | RSV | | Reserved. Do not modify. |
| Tx Enable State Change | 5 | LRF | | 1b = TX_EN pin has changed state. |
| Reserved | 7:6 | RSV | | Reserved. Do not modify. |



| Field Name | Bit(s) | Type | Default | Description |
|----------------------------|--------|------|---------|--|
| uP IRAM Parity Error [1:0] | 9:8 | LH | | Bit [0] indicates a parity error was detected in the uP IRAM but was corrected. Bit [1] indicates a multiple parity errors were detected in the uP IRAM and could not be corrected. The uP IRAM is protected with ECC. 1b = Parity error detected in the uP IRAM. |
| uP DRAM Parity Error | A | LH | | 1b = Parity error detected in the uP DRAM. |
| Reserved | D:B | RSV | | Reserved. Do not modify. |
| Mailbox Operation Complete | E | LH | | Mailbox interface is ready interrupt for registers Global Mailbox Interface 1: Address 1E.200 — Global Mailbox Interface 5: Address 1E.204 . 1b = Mailbox operation is complete. |
| NVR Operation Complete | F | LH | | NVR interface is ready interrupt for registers Global NVR Interface 1: Address 1E.100 — Global NVR Interface 5: Address 1E.104 . 1b = NVR operation is complete. |

4.6.2.6.97 Global Interrupt Mask 1: Address 1E.D400

| Field Name | Bit(s) | Type | Default | Description |
|-------------------------------|--------|-----------|---------|---|
| Reserved Alarm D Mask | 0 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved Alarm C Mask | 1 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved Alarm B Mask | 2 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved Alarm A Mask | 3 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Device Fault Mask | 4 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | 5 | RSV | | Reserved. Do not modify. |
| Reset completed Mask | 6 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | A:7 | RSV | | Reserved. Do not modify. |
| Low Temperature Warning Mask | B | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| High Temperature Warning Mask | C | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Low Temperature Failure Mask | D | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| High Temperature Failure Mask | E | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | F | RSV | | Reserved. Do not modify. |



4.6.2.6.98 Global Interrupt Mask 2: Address 1E.D401

| Field Name | Bit(s) | Type | Default | Description |
|-------------------------------------|--------|--------|---------|---|
| Diagnostic Alarm Mask | 0 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | 6:1 | RSV | | Reserved. Do not modify. |
| MDIO Command Handling Overflow Mask | 7 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved Alarms Mask [2:0] | A:8 | R/W PD | 000b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| DTE Status Change Mask | B | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| IP Phone Detect Mask | C | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | D | R/W PD | 0b | Reserved. |
| Smart Power-Down Entered Mask | E | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | F | RSV | | Reserved. Do not modify. |

4.6.2.6.99 Global Interrupt Mask 3: Address 1E.D402

| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------|--------|--------|---------|---|
| Watchdog Timer Alarm Mask | 0 | R/W PD | 1b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| MDIO Timeout Error Mask | 1 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| MDIO MMD Error Mask | 2 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | 4:3 | RSV | | Reserved. Do not modify. |
| Tx Enable State Change Mask | 5 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | 7:6 | RSV | | Reserved. Do not modify. |
| uP IRAM Parity Error Mask [1:0] | 9:8 | R/W PD | 00b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| uP DRAM Parity Error Mask | A | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | D:B | RSV | | Reserved. Do not modify. |
| Mailbox Operation Complete Mask | E | R/W PD | 0b | Mailbox interface is ready interrupt for registers Global Mailbox Interface 1: Address 1E.200 — Global Mailbox Interface 5: Address 1E.204 . 0b = Disable interrupt generation. 1b = Enable interrupt generation. |



| Field Name | Bit(s) | Type | Default | Description |
|-----------------------------|--------|-----------|---------|---|
| NVR Operation Complete Mask | F | R/W PD | 0b | NVR interface is ready interrupt for registers Global NVR Interface 1: Address 1E.100 — Global NVR Interface 5: Address 1E.104 0b = Disable interrupt generation. 1b = Enable interrupt generation. |

4.6.2.6.100 Global Chip-Wide Standard Interrupt Flags: Address 1E.FC00

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|------|---------|---|
| All Vendor Alarms Interrupt | 0 | RO | | An interrupt was generated from status register "Global Chip-Wide Vendor Interrupt Flags: Address 1E.FC01" on page 214, and the corresponding mask register "Global Interrupt Chip-Wide Vendor Mask: Address 1E.FF01" on page 215 1b = Interrupt in all vendor alarms. |
| Reserved | 5:1 | RSV | | Reserved. Do not modify. |
| GbE Standard Alarms Interrupt | 6 | RO | | An interrupt was generated from the TGE core. 1b = Interrupt in GbE standard alarms. |
| Auto-negotiation Standard Alarms 2 Interrupt | 7 | RO | | An interrupt was generated from status register "Auto-negotiation 10GBASE-T Status Register: Address 7.21" on page 147, and the corresponding mask register "Auto-negotiation Standard Interrupt Mask 2: Address 7.D001" on page 162 1b = Interrupt in auto-negotiation standard alarms 2. |
| Auto-negotiation Standard Alarms 1 Interrupt | 8 | RO | | An interrupt was generated from status register "Auto-negotiation Standard Status 1: Address 7.1" on page 140, and the corresponding mask register "Auto-negotiation Standard Interrupt Mask 1: Address 7.D000" on page 162 1b = Interrupt in auto-negotiation standard alarms 1. |
| PHY XS Standard Alarms 2 Interrupt | 9 | RO | | An interrupt was generated from status register "PHY XS Standard Status 2: Address 4.8" on page 136, and the corresponding mask register "PHY XS Vendor Global Interrupt Flags 1: Address 4.FC00" on page 139 1b = Interrupt in PHY XS standard alarms 2. |
| PHY XS Standard Alarms 1 Interrupt | A | RO | | An interrupt was generated from status register "PHY XS Standard Status 1: Address 4.1" on page 134, and the corresponding mask register "PHY XS Vendor Global Interrupt Flags 1: Address 4.FC00" on page 139 1b = Interrupt in PHY XS standard alarms 1. |
| PCS Standard Alarm 3 Interrupt | B | RO | | An interrupt was generated from status register "PCS 10G Status 2: Address 3.21" on page 105, and the corresponding mask register "PCS Standard Interrupt Mask 3: Address 3.D002" on page 116 1b = Interrupt in PCS standard alarms 3. |
| PCS Standard Alarm 2 Interrupt | C | RO | | An interrupt was generated from status register "PCS Standard Status 2: Address 3.8" on page 103, and the corresponding mask register "PCS Standard Interrupt Mask 2: Address 3.D001" on page 116 1b = Interrupt in PCS standard alarms 2. |
| PCS Standard Alarm 1 Interrupt | D | RO | | An interrupt was generated from status register "PCS Standard Status 1: Address 3.1" on page 101, and the corresponding mask register "PCS Standard Interrupt Mask 1: Address 3.D000" on page 116 1b = Interrupt in PCS standard alarms 1. |



| Field Name | Bit(s) | Type | Default | Description |
|--------------------------------|--------|------|---------|--|
| PMA Standard Alarm 2 Interrupt | E | RO | | An interrupt was generated from either bit 1.8.B or 1.8.A. An interrupt was generated from status register "PMA Standard Status 2: Address 1.8" on page 85, and the corresponding mask register "PMA Transmit Standard Interrupt Mask 2: Address 1.D001" on page 96 1b = Interrupt in PMA standard alarms 2. |
| PMA Standard Alarm 1 Interrupt | F | RO | | An interrupt was generated from bit 1.1.2. An interrupt was generated from status register "PMA Standard Status 1: Address 1.1" on page 83, and the corresponding mask register "PMA Transmit Standard Interrupt Mask 1: Address 1.D000" on page 96. 1b = Interrupt in PMA standard alarms 1. |

4.6.2.6.101 Global Chip-Wide Vendor Interrupt Flags: Address 1E.FC01

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|------|---------|---|
| Global Alarms 3 Interrupt | 0 | RO | | An interrupt was generated from status register "Global Alarms 3: Address 1E.CC02" on page 210, and the corresponding mask register "Global Interrupt Mask 3: Address 1E.D402" on page 212. 1b = Interrupt in Global alarms 3. |
| Global Alarms 2 Interrupt | 1 | RO | | An interrupt was generated from status register "Global Alarms 2: Address 1E.CC01" on page 210, and the corresponding mask register "Global Interrupt Mask 2: Address 1E.D401" on page 212. 1b = Interrupt in Global alarms 2. |
| Global Alarms 1 Interrupt | 2 | RO | | An interrupt was generated from status register "Global Alarms 1: Address 1E.CC00" on page 209, and the corresponding mask register "Global Interrupt Mask 1: Address 1E.D400" on page 211. 1b = Interrupt in Global alarms 1. |
| Reserved | A:3 | RSV | | Reserved. Do not modify. |
| GbE Vendor Alarm Interrupt | B | RO | | A GbE alarm was generated. Refer to "GbE PHY Vendor Global Interrupt Flags 1: Address 1D.FC00" on page 181. 1b = Interrupt in GbE vendor specific alarm. |
| Auto-negotiation Vendor Alarm Interrupt | C | RO | | An auto-negotiation alarm was generated. Refer to "Auto-negotiation Vendor Global Interrupt Flags 1: Address 7.FC00" on page 167. 1b = Interrupt in auto-negotiation vendor specific alarm. |
| PHY XS Vendor Alarm Interrupt | D | RO | | A PHY XS alarm was generated. Refer to "PHY XS Vendor Global Interrupt Flags 1: Address 4.FC00" on page 139. 1b = Interrupt in PHY XS vendor specific alarm. |
| PCS Vendor Alarm Interrupt | E | RO | | A PCS alarm was generated. Refer to "PCS Vendor Global Interrupt Flags 1: Address 3.FC00" on page 132. 1b = Interrupt in PCS vendor specific alarm. |
| PMA Vendor Alarm Interrupt | F | RO | | A PMA alarm was generated. Refer to "PMA Vendor Global Interrupt Flags 1: Address 1.FC00" on page 98. 1b = Interrupt in PMA vendor specific alarm. |

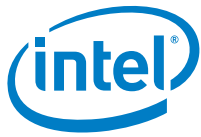


4.6.2.6.102 Global Interrupt Chip-Wide Standard Mask: Address 1E.FF00

| Field Name | Bit(s) | Type | Default | Description |
|---|--------|-----------|---------|---|
| All Vendor Alarms Interrupt Mask | 0 | R/W PD | 1b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | 5:1 | RSV | | Reserved. Do not modify. |
| GbE Standard Alarms Interrupt Mask | 6 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Auto-negotiation Standard Alarms 2 Interrupt Mask | 7 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Auto-negotiation Standard Alarms 1 Interrupt Mask | 8 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| PHY XS Standard Alarms 2 Interrupt Mask | 9 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| PHY XS Standard Alarms 1 Interrupt Mask | A | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| PCS Standard Alarm 3 Interrupt Mask | B | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| PCS Standard Alarm 2 Interrupt Mask | C | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| PCS Standard Alarm 1 Interrupt Mask | D | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| PMA Standard Alarm 2 Interrupt Mask | E | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| PMA Standard Alarm 1 Interrupt Mask | F | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |

4.6.2.6.103 Global Interrupt Chip-Wide Vendor Mask: Address 1E.FF01

| Field Name | Bit(s) | Type | Default | Description |
|--|--------|-----------|---------|---|
| Global Alarms 3 Interrupt Mask | 0 | R/W PD | 1b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Global Alarms 2 Interrupt Mask | 1 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Global Alarms 1 Interrupt Mask | 2 | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Reserved | A:3 | RSV | | Reserved. Do not modify. |
| GbE Vendor Alarm Interrupt Mask | B | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| Auto-negotiation Vendor Alarm Interrupt Mask | C | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| PHY XS Vendor Alarm Interrupt Mask | D | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |



| Field Name | Bit(s) | Type | Default | Description |
|---------------------------------|--------|-----------|---------|---|
| PCS Vendor Alarm Interrupt Mask | E | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |
| PMA Vendor Alarm Interrupt Mask | F | R/W PD | 0b | 0b = Disable interrupt generation. 1b = Enable interrupt generation. |



5.0 Timing

5.1 MDIO

Data is sampled on the rising edge of MDC at the PHY and at STA.

Table 5-1 MDIO Timing

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|-----------------|------------------|----------------|-----|-----|-----|-------|
| f_{MDC} | MDC Frequency | – | 0 | – | 18 | MHz |
| t_L | MDC Low Time | – | 20 | – | – | ns |
| t_H | MDC High Time | – | 20 | – | – | ns |
| t_{SETUP} | Input Setup Time | – | 8 | – | – | ns |
| t_{HOLD_IN} | Input Hold Time | – | 10 | – | – | ns |
| t_{HOLD_OUT} | Output Hold Time | – | 29 | – | 38 | ns |

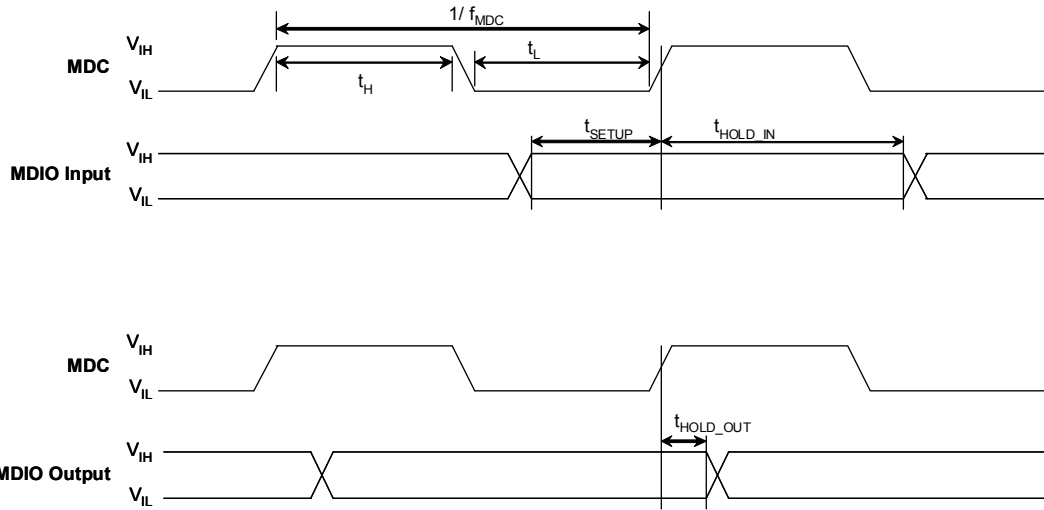


Figure 5-1 MDIO Setup and Hold Times

5.2 Interrupt

Table 5-2 Interrupt Timing

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|-----------|----------------|----------------|------------------|-----|-----|-------|
| t_F | Fall Time | - | 1 | - | - | ns |
| t_R | Rise Time | - | 1 | - | - | ns |
| t_{INT} | Interrupt Time | - | n/a ¹ | - | - | ns |

1. INT* stays low until the interrupt is serviced.

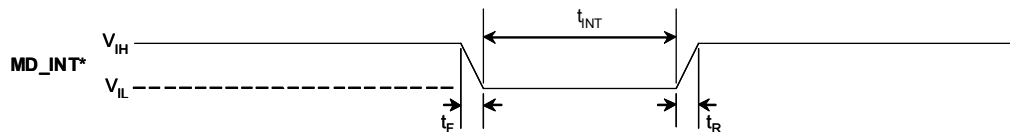


Figure 5-2 Interrupt Timing Diagram



5.3 Reset

Table 5-3 Reset Timing

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|-------------------------|----------------|------------------------------------|-----|-----|-----|-------|
| t_{RESET} | Reset Time | - | 100 | - | - | ms |
| t_{F} | Fall Time | - | 1 | - | - | ns |
| t_{R} | Rise Time | - | 1 | - | - | ns |
| $t_{\text{RESET_OUT}}$ | Reset Out Time | $f_{\text{C}} = 50.00 \text{ MHz}$ | 20 | - | - | ms |

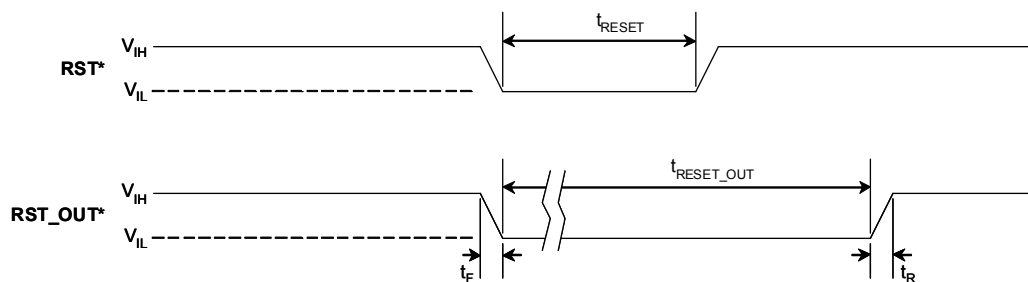


Figure 5-3 Reset Timing Diagram

5.4 SPI

Table 5-4 SPI Timing

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|------------|-----------------------------------|-----------------|-----|-----|------|-------|
| f_{SCLK} | SCLK Clock Frequency ¹ | - | 0 | - | 50.0 | MHz |
| t_H | SCLK High Time | - | 12 | - | - | ns |
| t_L | SCLK Low Time | - | 12 | - | - | ns |
| t_{CE} | CE* High Time | - | 50 | - | - | ns |
| t_{CES} | CE* Setup Time | - | 25 | - | - | ns |
| t_{CEH} | CE* Hold Time | - | 25 | - | - | ns |
| t_{SU} | S _{IN} Setup Time | - | 14 | - | - | ns |
| t_{HI} | S _{IN} Hold Time | - | -4 | - | - | ns |
| t_V | S _{OUT} Output Valid | - | - | - | 4 | ns |
| t_{HO} | S _{OUT} Hold Time | - | -4 | - | - | ns |

1. An attached FLASH device which supports 40 MHz operation, must have a t_V (output valid time) of less than 12.5 ns.

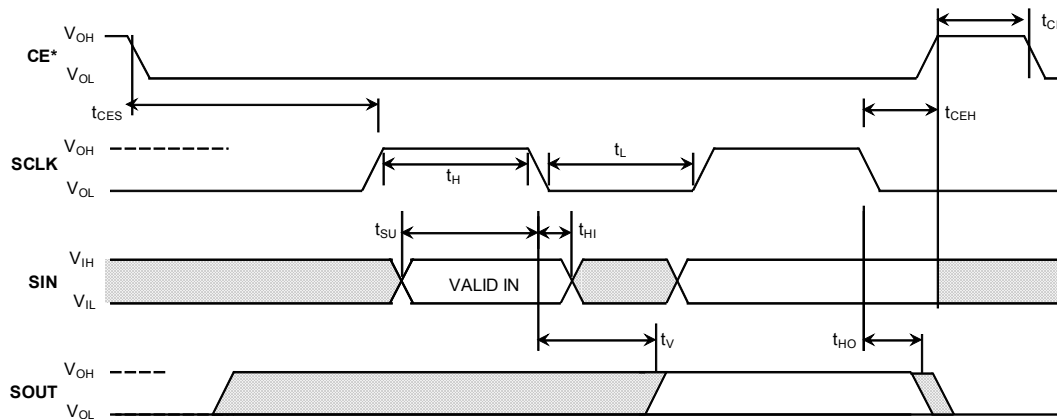


Figure 5-4 SPI Timing Diagram



5.5 SerDes

The measurement BW for these specs is from $\frac{f_{\text{SYMBOL}}}{1667}$ to ∞ , as the tracking bandwidth of the PLL

for the SerDes is up to. For instance, for KR, the symbol rate is 10.3125 GHz,

so $\frac{f_{\text{SYMBOL}}}{1667} \cong 6 \text{ MHz}$. Thus the measurement BW for the integrated jitter is from roughly 6 MHz to infinity.

Table 5-5 SerDes Receiver Jitter Tolerance Specifications

| Maximum Total Jitter (TJ_{MAX}) | Maximum Random Jitter (RJ_{MAX}) | Maximum Data Dependent Jitter (DDJ_{MAX}) | Maximum Deterministic Jitter (DJ_{MAX}) | Maximum Periodic Jitter (PJ_{MAX}) | Units |
|--|---|--|--|---|-------|
| 1.00 | 0.25 | 0.55 | 0.10 | 0.10 | UIpp |

Table 5-6 SerDes Transmit Jitter Tolerance Specifications

| Maximum Total Jitter (TJ_{MAX}) | Maximum Random Jitter (RJ_{MAX}) | Maximum Deterministic Jitter (DJ_{MAX}) | Maximum Periodic Jitter (PJ_{MAX}) | Units |
|--|---|--|---|-------|
| 0.25 | 0.15 | 0.05 | 0.05 | UIpp |

5.6 SGMII Transmit

Table 5-7 SGMII Transmit Timing

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|--------|-------------|----------------|-----|------|-----|-------|
| f_s | Symbol Rate | - | - | 1.25 | - | GS/s |

5.7 SGMII Receive

Table 5-8 SGMII Receive Timing

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|------------|---------------------|----------------|------|------|-----|-------|
| f_{RX} | Receive Symbol Rate | - | - | 1.25 | - | GS/s |
| Δf | Frequency Tolerance | - | -300 | - | 300 | ppm |

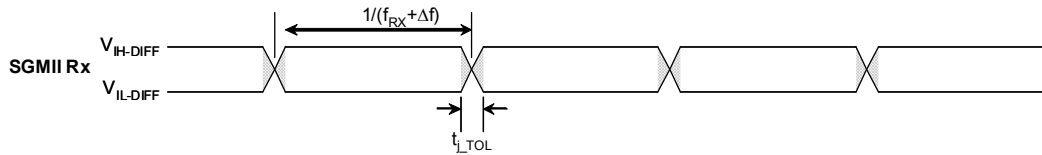


Figure 5-5 SGMII Receive Timing Diagram

5.8 KR Transmit

Figure 5-6 KR Transmit Timing

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|--------|-------------|----------------|-----|---------|-----|-------|
| f_S | Symbol Rate | - | - | 10.3125 | - | GS/s |

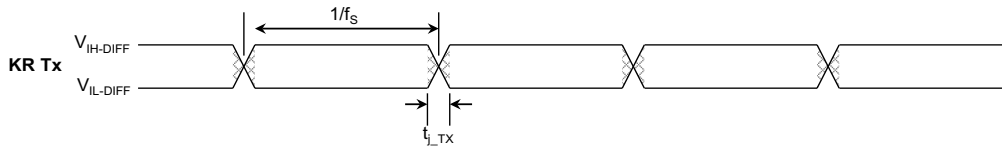


Figure 5-7 KR Transmit Timing Diagram



5.9 KR Receive

Table 5-9 KR Receive Timing

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|------------|---------------------|----------------|-----|---------|-----|-------|
| f_{RX} | Receive Symbol Rate | - | - | 10.3125 | - | GS/s |
| Δf | Frequency Tolerance | - | -50 | - | 50 | ppm |

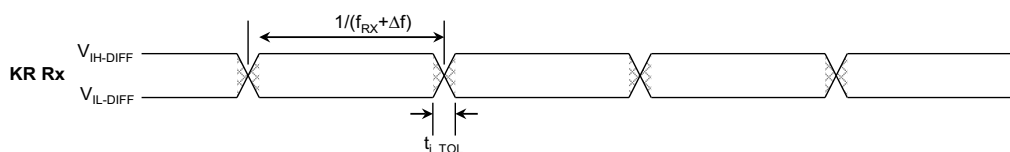


Table 5-10 KR Receive Timing Diagram

5.10 Clocks

5.10.1 Input

Table 5-11 Clocks 50 MHz Input Timing

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|------------|--------------------------------|-----------------|-----|------|-----|-------|
| f_C | Clock Frequency | - | - | 50.0 | - | MHz |
| Δf | Frequency Tolerance | - | -50 | - | 50 | ppm |
| t_j | RMS Period Jitter ¹ | 12 kHz - 20 MHz | - | - | 1.0 | ps |
| DC | Duty Cycle | - | 45 | - | 55 | % |

1. This includes all period jitter and tones.

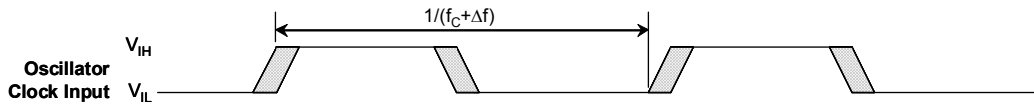


Figure 5-8 Clocks 50 MHz Input Timing Diagram

The phase noise of the 50 MHz input clock should be at least as good as the mask as shown.

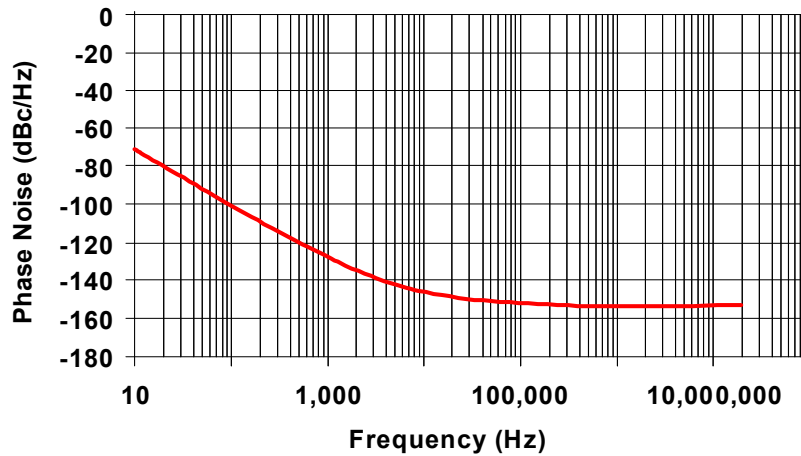


Figure 5-9 50.000 MHz Phase Noise Mask

5.11 JTAG

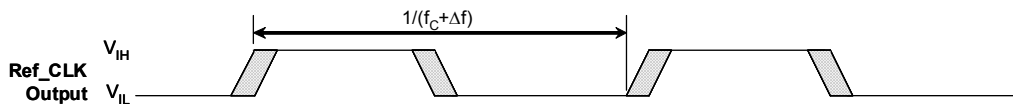
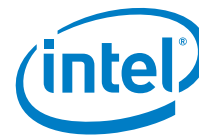


Table 5-12 JTAG Timing

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|-------------|------------------|----------------|-----|-----|-----|-------|
| f_{TCK} | Clock Frequency | – | – | – | 20 | MHz |
| t_L | Clock Low Time | – | 20 | – | – | ns |
| t_H | Clock High Time | – | 20 | – | – | ns |
| t_{SETUP} | Input Setup Time | – | 5 | – | – | ns |



| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|------------------------|------------------|----------------|-----|-----|-----|-------|
| $t_{\text{HOLD_IN}}$ | Input Hold Time | - | 15 | - | - | ns |
| $t_{\text{HOLD_OUT}}$ | Output Hold Time | - | 10 | - | 22 | ns |

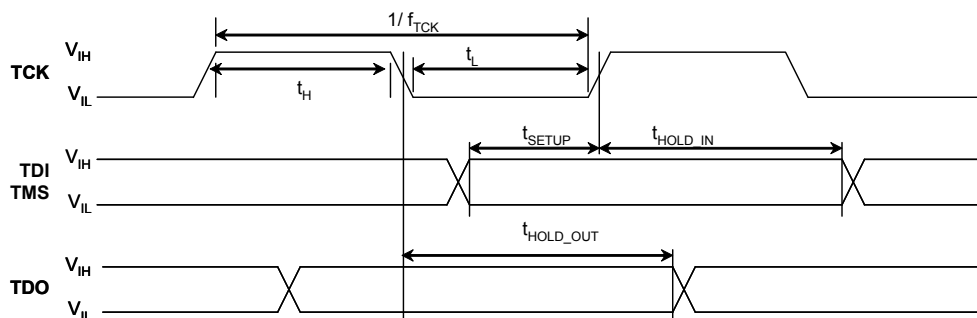


Figure 5-10 JTAG Timing Diagram



NOTE: *This page intentionally left blank.*



6.0 Electrical Specifications

6.1 Absolute Maximum Ratings

| Symbol | Parameter | Test Condition | Min | Max | Units |
|--------------------|-----------------------------|----------------|------|------|-------|
| VDD | 0.83V Digital Supply | - | -0.5 | 1.19 | V |
| VA12 | 1.2V Analog Supply | - | -0.5 | 1.32 | V |
| VA21 | 2.1V Analog Supply | - | -0.5 | 2.32 | V |
| VDD_IO | 2.5V VDD General I/O Supply | - | -0.5 | 2.75 | V |
| VDD_FLASH | 2.5V FLASH I/O Supply | - | -0.5 | 2.75 | V |
| V _{ESD} | ESD on all pins except Line | HBM | - | 2 | kV |
| | | CDM | - | 500 | V |
| | | MM | - | 200 | V |
| V _{CO} | Cable discharge on Line | 100 m cable | - | 2 | kV |
| T _{STORE} | Storage Temperature | - | -50 | 150 | °C |

Note: Stresses above those listed in the previous table can cause permanent device damage. These values should not be used as limits for normal device operation. Exposure to absolute maximum rating conditions for an extended period of time can affect device reliability.



6.2 Recommended Operating Conditions

| Symbol | Parameter | Test Condition | Min | Max | Units |
|----------------|----------------------|----------------|-----|-----|-------|
| T _j | Junction Temperature | - | 0 | 105 | °C |

6.3 Power Delivery

This section describes the power delivery specifications for the X557.

- DC Voltage Regulation - DC accuracy with respect to the nominal voltage specification. Includes controller feedback accuracy and resistive losses in the power distribution network.
- AC Voltage Regulation - Minimum/maximum noise voltage based on mid-to-high frequency (~1-20 MHz) AC load currents (excluding ripple voltage). Note that this specification is met by following the system design recommendations/considerations related to the recommended decoupling design ([Section 9.0](#)).
- Total Line Regulation - The sum of DC and AC voltage regulation.

6.3.1 Power Supply Specifications

| Description | Parameter |
|--------------------------------|---|
| VDDIO 2.5V | |
| Nominal Voltage | 2.5V |
| DE Voltage Regulation | ± 2% DC Regulation |
| AC Voltage Regulation | ± 3% AC Regulation (75 mV peak-to-peak) |
| Total Line Regulation | ± 5% |
| VCC21 | |
| Nominal Voltage | 2.1V |
| DC Voltage Regulation | ± 3% DC Regulation |
| AC Voltage Regulation | ± 0.6% AC Regulation (13 mV peak-to-peak) |
| Total DC/AC Voltage Regulation | ± 3.6% |
| Step Load Size | 64mA |
| Step Load Slew Rate di/dt | 200mA/ 1 μs |



| | |
|-----------------------------------|---|
| Maximum Step Load Slew Rate di/dt | |
| VCC1P2 | |
| Nominal Voltage | 1.2V |
| DC Voltage Regulation | ± 3% DC Regulation |
| AC Voltage Regulation | ± 2% AC Regulation (48 mV peak-to-peak) |
| Total DC/AC Voltage Regulation | ± 5% |
| Step Load Size | 125mA |
| Step Load Slew Rate di/dt | 125mA/ 1 μs |
| VCCOP83 | |
| Nominal Voltage | 0.83V |
| DC Voltage Regulation | ± 3% DC Regulation |
| AC Voltage Regulation | ± 2% AC Regulation (25.5 mV peak-to-peak) |
| Total DC/AC Voltage Regulation | ± 5% |
| Step Load Size | 2A |
| Step Load Slew Rate di/dt | 587mA/1 μs |

6.3.2 VDD_IO 2.5V External Power Supply Specification (2.5V)

| Parameter | Description | Min | Max | Units |
|----------------------------------|---|------|-------|-------|
| Rise Time | Time from 10% to 90% mark | 1 | 5 | ms |
| Monotonicity | Voltage dip allowed in ramp | N/A | 0 | mV |
| Slope | Ramp rate at any given time between 10% and 90% Min: $0.8 \cdot V(\text{min}) / \text{rise time}(\text{max})$ Max: $0.8 \cdot V(\text{max}) / \text{rise time}(\text{min})$ | 380 | 21000 | V/S |
| Operational Range | Voltage range for normal operating conditions | 2.38 | 2.63 | V |
| Overshoot | Maximum overshoot allowed | N/A | 100 | mV |
| Overshoot Settling Time | Maximum overshoot allowed duration (At that time delta voltage should be lower than 5 mV from steady state voltage) | N/A | 0.1 | ms |
| Suggested Decoupling Capacitance | Capacitance range | 100 | - | μF |



6.3.3 VCC2P1 External Power Supply Specification (2.1V)

| Title | Description | Min | Max | Units |
|----------------------------------|---|-------|-------|---------------|
| Rise Time | Time from 10% to 90% mark | 1 | 5 | ms |
| Monotonicity | Voltage dip allowed in ramp | - | 0 | mV |
| Slope | Ramp rate at any given time between 10% and 90% Min: $0.8 \cdot V(\text{min}) / \text{rise time}(\text{max})$ Max: $0.8 \cdot V(\text{max}) / \text{rise time}(\text{min})$ | 334 | 18480 | V/S |
| Operational Range | Voltage range for normal operating conditions | 1.995 | 2.205 | V |
| Overshoot | Maximum overshoot allowed | - | 100 | mV |
| Overshoot Settling Time | Maximum overshoot allowed duration. (At that time delta voltage should be lower than 5 mV from steady state voltage) | - | 0.1 | ms |
| Suggested Decoupling Capacitance | Capacitance range | 174 | - | μF |

6.3.4 VCC1P2 External Power Supply Specification (1.2V)

| Title | Description | Min | Max | Units |
|----------------------------------|---|------|-------|---------------|
| Rise Time | Time from 10% to 90% mark | 1 | 5 | ms |
| Monotonicity | Voltage dip allowed in ramp | - | 0 | mV |
| Slope | Ramp rate at any given time between 10% and 90% Min: $0.8 \cdot V(\text{min}) / \text{rise time}(\text{max})$ Max: $0.8 \cdot V(\text{max}) / \text{rise time}(\text{min})$ | 182 | 10080 | V/S |
| Operational Range | Voltage range for normal operating conditions | 1.14 | 1.26 | V |
| Overshoot | Maximum overshoot allowed | - | 60 | mV |
| Overshoot Duration | Maximum overshoot allowed duration. (At that time delta voltage should be lower than 5 mV from steady state voltage) | 0.0 | 0.05 | ms |
| Suggested Decoupling Capacitance | Capacitance range | 98 | - | μF |



6.3.5 VCCOP83 External Power Supply Specification (0.83V)

| Title | Description | Min | Max | Units |
|----------------------------------|---|------|------|---------------|
| Rise Time | Time from 10% to 90% mark | 1 | 5 | ms |
| Monotonicity | Voltage dip allowed in ramp | - | 0 | mV |
| Slope | Ramp rate at any given time between 10% and 90% Min: $0.8 * V(\text{min}) / \text{rise time}(\text{max})$ Max: $0.8 * V(\text{max}) / \text{rise time}(\text{min})$ | 129 | 7140 | V/S |
| Operational Range | Voltage range for normal operating conditions | 0.76 | 0.85 | V |
| Overshoot | Maximum overshoot allowed | - | 40 | mV |
| Overshoot Duration | Maximum overshoot allowed duration. (At that time delta voltage should be lower than 5 mV from steady state voltage) | - | 0.05 | ms |
| Suggested Decoupling Capacitance | Capacitance range | 174 | - | μF |

6.3.6 Power On/Off Sequence

The following power-up sequence is recommended for the X557.

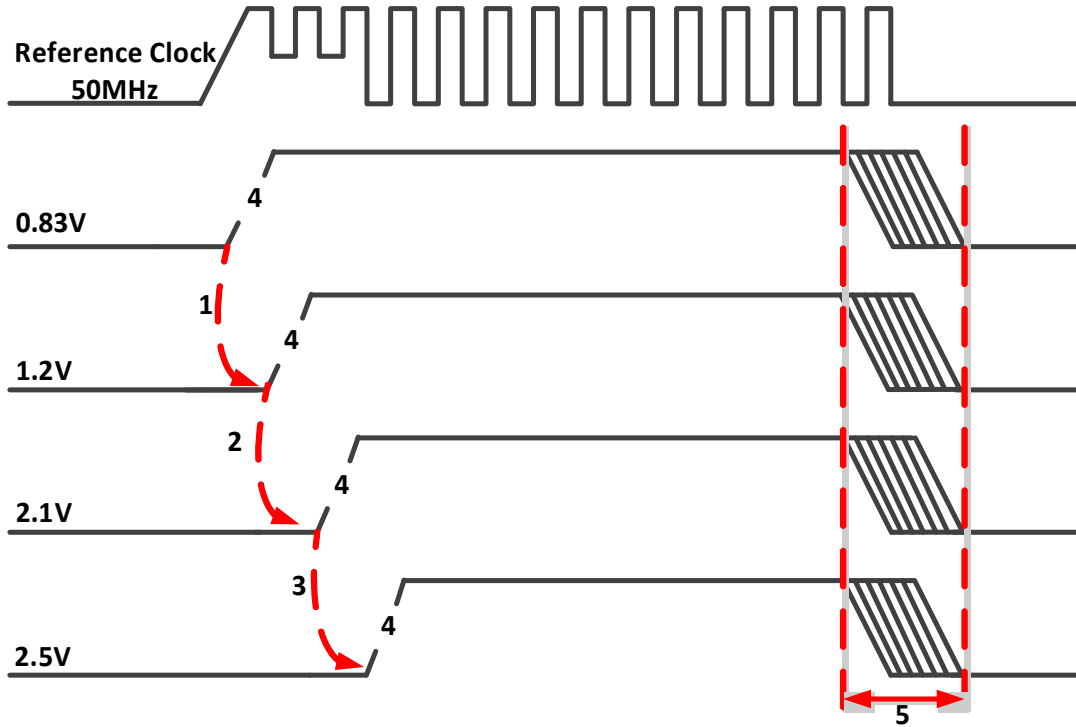


Figure 6.1. Power On/Off Sequence Flow

Table 6-1 Notes for Power On/Off Sequence Diagram

| Note | Description |
|------|--|
| 1 | The 1.2V rail does not start to ramp before the 0.83 rail is 80% of its final value. Tmax(0.83V to 1.2V) should be less than 5 ms. |
| 2 | The 2.1V rail does not start to ramp before the 1.2V rail is 80% of its final value. Tmax(1.2V to 2.1V) should be less than 5 ms. |
| 3 | The 2.5V rail does not start to ramp before the 2.1V rail is 80% of its final value. Tmax(2.1V to 2.5V) should be less than 5 ms. |
| 4 | Tramp for each power rail. |
| 5 | When powering off, all power rails must get to a 0V level within 20 ms from the point the first power rail starts powering off. |

Note: Stresses above those listed in Table 6-1 can cause permanent device damage. These values should not be used as limits for normal device operation. Exposure to absolute maximum rating conditions for an extended period of time can affect device reliability.



6.3.7 Power-on Reset

The X557 internal power-on reset circuitry initiates a full-chip reset when voltage levels of power supplies reach certain thresholds at power up.

| Symbol | Parameter | Specification | | | Units |
|--------|--|---------------|-----|------|-------|
| | | Min | Typ | Max | |
| 2.1V | Threshold for 2.1V supply in power-up | 1.7 | - | 1.8 | V dc |
| 1.2V | Threshold for 1.2V supply in power-up | 0.9 | - | 1 | V dc |
| 0.83V | Threshold for 0.8 Vdc supply in power-up | 0.56 | - | 0.6 | V dc |
| RST_N | High-threshold (VIH) | 0.83 | - | 2.5 | V dc |
| RST_N | Low-threshold (VIL) | 0.3 | - | 0.36 | V dc |

6.4 Operating Modes

The Intel® X557-AT/AT2/AT4 10 GbE PHY has several different operating regimes that each use different amounts of power. These regimes are listed below, and power consumption for each of these regimes is given in [Table 6-2](#).

1. **Low power (LP)**: In this mode, everything is shut off except the internal microprocessor and the MDIO interface. It is designed for out-of-service ports, and is the lowest power operating mode.
1. **Auto-negotiation (ANEG)**: In this mode, the Intel® X557-AT/AT2/AT4 10 GbE PHY is attempting to auto-negotiate with the far-end PHY and is sending and trying to receive link pulses. This is the second lower operating power mode, and usually last between 1.6 and 1.8 seconds¹.
2. **10 GbE Training (TRNG)**: This is the highest power mode, and occurs at the beginning of a 10GBASE-T session. This training mode lasts for a maximum of 2 seconds. This sets the maximum requirements for the 1.2V, 2.1V, and 0.83V power supplies.
3. **10 GbE Steady-state Operation (10GSS)**: This is the second highest power mode, and occurs during normal 10GBASE-T operation. This sets the maximum requirements for the thermal design, and the maximum for the VDD power supply.
4. **1 GbE Steady-state Operation (1GSS)**: This is the power seen during normal 1000BASE-T operation.
5. **100 Mb/s Steady-state Operation (100MSS)**: This is the power seen during normal 100BASE-TX operation.

1. This auto-negotiation time assumes that an active link-partner is present. If one is not present, the Intel® X557-AT/AT2/AT4 10 GbE PHY will continue attempting to auto-negotiate until a PHY is connected.



An example of the power consumption versus time for some of these modes in 10 GbE operation is shown in this figure, the device starts off in low-power mode, and then at time t, the X557-AT2 is enabled, and auto-negotiation begins. After 10GBASE-T is agreed on as the connection rate, 10GBASE-T training starts, and then after 2 seconds, 10GBASE-T steady-state is entered into.

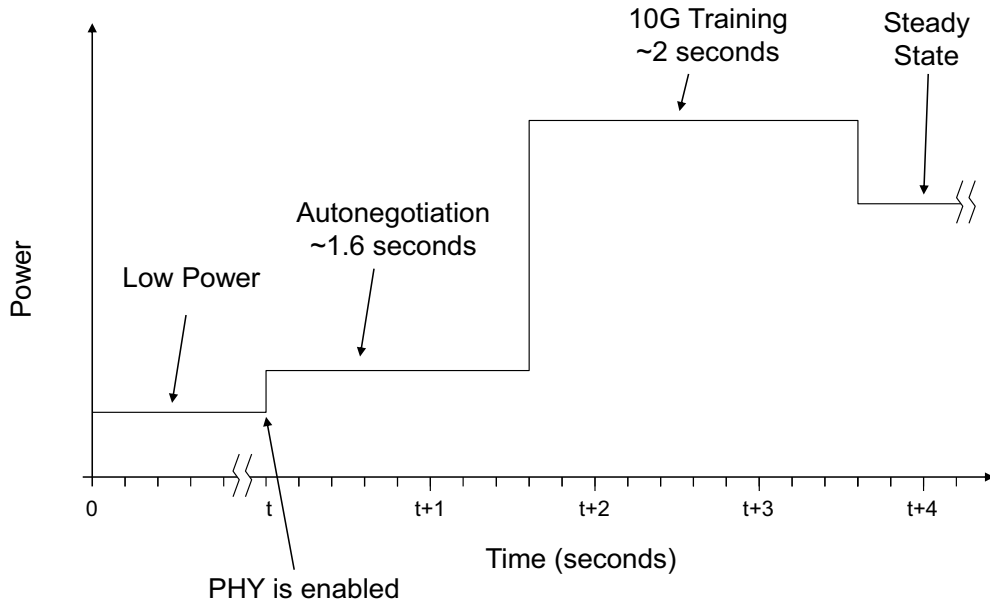


Figure 6-1 Power Versus Time

6.4.1 Power Consumption

Power numbers are based on estimation data and related to a single, dual, or quad PHY.

- Maximum power mode: FAST material, Vnom, Tj-max (85 °C).
- Other operational modes: Typical material, Vnom, Tj-max (80 °C).

6.4.1.1 X557-AT

| X557-AT | Device Total Power (W) |
|-----------------------|------------------------|
| 10 GbE Max Active | 3.4 |
| 10 GbE Max 30 m Reach | 3 |
| 1 GbE Active | 1.8 |



| X557-AT | Device Total Power (W) |
|-------------------------|------------------------|
| 100 Mb/s Active | 1.4 |
| Low Power Mode (no WoL) | 1.3 |

6.4.1.2 X557-AT Peak Current (WoL Mode)

FAST material, Vnom, Tj-max (80 °C).

| 2.5V | 2.1V | 1.2V | 0.83V |
|--------|--------|--------|--------|
| 0.17 A | 0.72 A | 0.33 A | 0.39 A |

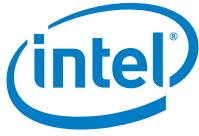
6.4.1.3 X557-AT 10 Gb/s Peak Current Consumption During 10GBASE-T Training

FAST material, Vnom, Tj-max (80 °C).

| 2.5V | 2.1V | 1.2V | 0.83V |
|-------|-------|-------|-------|
| 0.1 A | 0.5 A | 0.3 A | 4.0 A |

6.4.1.4 X557-AT2

| X557-AT2 | Device Total Power (W) |
|---|------------------------|
| 10 GbE Max Active | 6.8 |
| 10 GbE Max 30 m Reach | 6 |
| 1 GbE Active | 3.6 |
| 100 Mb/s Active | 2.8 |
| Low Power Mode (no WoL) | 2.6 |
| Low Power Mode (WoL - only one port active at 1 GbE) | 3.1 |
| Low Power Mode (WoL - only one port active at 100 Mb/s) | 2.7 |



6.4.1.5 X557-AT2 Peak Current (WoL Mode; All Ports Enabled)

FAST material, Vnom, Tj-max (80 °C).

| | | | |
|-------|--------|-------|-------|
| 2.5V | 2.1V | 1.2V | 0.83V |
| 0.2 A | 1.45 A | 0.7 A | 0.8 A |

6.4.1.6 X557-AT2 10 Gb/s Peak Current Consumption During 10GBASE-T Training

FAST material, Vnom, Tj-max (80 °C).

| | | | |
|-------|-------|-------|-------|
| 2.5V | 2.1V | 1.2V | 0.83V |
| 0.2 A | 1.0 A | 0.6 A | 8.0 A |

6.4.1.7 X557-AT4

| X557-AT4 | Device Total Power (W) |
|---|------------------------|
| 10 GbE Max Active | 13.6 |
| 10 GbE Max 30 m Reach | 12 |
| 1 GbE Active | 7.2 |
| 100 Mb/s Active | 5.6 |
| Low Power Mode (no WoL) | 5.2 |
| Low Power Mode (WoL - only one port active at 1 GbE) | 5.7 |
| Low Power Mode (WoL - only one port active at 100 Mb/s) | 5.3 |



6.4.1.8 X557-AT4 Peak Current (WoL Mode; All Ports Enabled)

FAST material, Vnom, Tj-max (80 °C).

| 2.5V | 2.1V | 1.2V | 0.83V |
|--------|--------|--------|--------|
| 0.28 A | 2.25 A | 1.22 A | 1.29 A |

6.4.1.9 X557-AT4 Peak Current - (WoL Mode; Only One Port Enabled)

FAST material, Vnom, Tj-max (80 °C).

| 2.5V | 2.1V | 1.2V | 0.83V |
|--------|--------|--------|--------|
| 0.28 A | 1.02 A | 0.79 A | 1.27 A |

6.4.1.10 X557-AT4 10 Gb/s Peak Current Consumption During 10GBASE-T Training

FAST material, Vnom, Tj-max (80 °C).

| 2.5V | 2.1V | 1.2V | 0.83V |
|-------|-------|-------|--------|
| 0.4 A | 2.0 A | 1.2 A | 16.0 A |

6.5 Management Interface

The management interface includes the following signals:

1. MDC
2. MDIO
3. TX_EN
4. RST_N



Table 6-2 1.2V Mode MDIO Electrical Interface Characteristics

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|------------------------------|-------------------------|--|------|-----|------|-------|
| V _{IL} | Input low voltage | - | - | - | 0.36 | V |
| V _{IH} | Input high voltage | - | 0.84 | - | - | V |
| V _{OL} | Output low voltage | I _{OL} = -4 mA | 0.0 | - | 0.2 | V |
| V _{OH} | Output high voltage | I _{OH} = 0 mA | 1.0 | - | 1.5 | V |
| | | I _{OH} = 10 mA | 0.96 | - | 1.5 | V |
| | | I _{OH} = 20 mA | 0.9 | - | 1.5 | V |
| I _{OL} | Output low current | V _{OL} = 0.2 V | 4 | - | - | mA |
| I _{OH} ¹ | Output high current | V _{OH} = 1.0 V | - | - | 0 | mA |
| I _{LKG} | Tristate Leakage | V _{IN} = 0 V or V _{CC} | -10 | - | 10 | μA |
| C _i | Input capacitance | - | - | - | 10 | pF |
| C _L | Maximum capacitive load | - | - | - | 470 | pF |

1. I_{OH} parameter is not applicable to open drain drivers (i.e. MDIO data line).

Table 6-3 70% / 30% VDD_IO Mode MDIO Electrical Interface Characteristics

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|------------------------------|-------------------------|--|-----|-----|-----|---------|
| V _{IL} | Input low voltage | - | - | - | 30 | %VDD_IO |
| V _{IH} | Input high voltage | - | 70 | - | N/A | %VDD_IO |
| V _{OL} | Output low voltage | I _{OL} = -4 mA | 0 | - | 20 | %VDD_IO |
| V _{OH} | Output high voltage | I _{OH} = 0 mA | 80 | - | 120 | %VDD_IO |
| | | I _{OH} = 20 mA | 80 | - | 120 | %VDD_IO |
| I _{OL} | Output low current | V _{OL} = 20% VDD_IO | 4 | - | N/A | mA |
| I _{OH} ¹ | Output high current | V _{OH} = 80% VDD_IO | - | - | 0 | mA |
| I _{LKG} | Tristate Leakage | V _{IN} = 0 V or V _{CC} | -10 | - | 10 | μA |
| C _i | Input capacitance | - | - | - | 10 | pF |
| C _L | Maximum capacitive load | - | - | - | 120 | pF |



1. I_{OH} parameter is not applicable to open drain drivers (i.e. MDIO data line).

6.6 I/O

All of the non-management interface I/O on the Intel® X557-AT/AT2/AT4 10 GbE PHY run from either VDD_IO or VDD_FLASH and use the same I/O cell that has the following characteristics.

Table 6-4 I/O Pin Electrical Parameters

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|------------|-------------------------|---------------------------------|-----|-----|-----|---------|
| V_{IL} | Input low voltage | - | - | - | 30 | %VDD_IO |
| V_{IH} | Input high voltage | - | 70 | - | | %VDD_IO |
| V_{OL} | Output low voltage | $I_{OL} = -4$ mA | 0 | - | 20 | %VDD_IO |
| V_{OH} | Output high voltage | $I_{OH} = 0$ mA | 80 | - | 120 | %VDD_IO |
| | | $I_{OH} = 20$ mA | 80 | - | 120 | %VDD_IO |
| I_{OL} | Output low current | $V_{OL} = 20\%$ V_{DD_IO} | 4 | - | - | mA |
| I_{OH}^1 | Output high current | $V_{OH} = 80\%$ V_{DD_IO} | - | - | 0 | mA |
| I_{LKG} | Tristate Leakage | $V_{IN} = 0$ V or V_{CC} | -10 | - | 10 | μ A |
| C_i | Input capacitance | - | - | - | 10 | pF |
| C_L | Maximum capacitive load | - | - | - | 120 | pF |

1. I_{OH} parameter is not applicable to open drain drivers (i.e. MDIO data line).

6.7 Serial Flash

Note: The SPI interface is 2.5 V tolerant.

Table 6-5 SPI Pin Capacitance

| Symbol | Parameter | Test Condition | Max | Units |
|-----------|--------------------------------------|-----------------|-----|-------|
| C_{OUT} | Output Capacitance (SCLK, CS*, SOUT) | $V_{OUT} = 0$ V | 5 | pF |
| C_{IN} | Input Capacitance (SIN) | $V_{IN} = 0$ V | 5 | pF |



Table 6-6 SPI DC Pin Capacitance

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|-----------|---------------------|---------------------------------|-----|-----|-----|---------------|
| I_{LKG} | Tristate Leakage | $V_{IN} = 0\text{ V or }V_{CC}$ | -10 | | 10 | μA |
| V_{IL} | Input Low Voltage | | - | - | 20 | %VDD_FLASH |
| V_{IH} | Input High Voltage | | 80 | - | - | %VDD_FLASH |
| V_{OL} | Output Low Voltage | | | | 20 | %VDD_FLASH |
| V_{OH} | Output High Voltage | | | | | |
| I_{OL} | Output low current | | 4 | - | - | mA |
| I_{OH} | Output high current | | - | - | -4 | mA |

6.8 SerDes

Table 6-7 SerDes Transmitter Characteristics

| Parameter | Test Condition | Min | Typ | Max | Units |
|-------------------------------|---------------------------|-----|-----|------|----------|
| Output Voltage ¹ | Peak-to-peak differential | 400 | - | 1500 | mV |
| Transmit Common Mode Voltage | - | 200 | - | 700 | mV |
| Differential Output Impedance | Programmable | 80 | 100 | 120 | Ω |
| Common Mode Output Impedance | - | 20 | 25 | 30 | Ω |

1. Near end programmable output range.

Table 6-8 SerDes Receiver Characteristics

| Parameter | Test Condition | Min | Typ | Max | Units |
|---|---------------------------|-----|-----|------|----------|
| Input Voltage | Peak-to-peak differential | 50 | - | 2000 | mV |
| Input Common Mode Voltage | Peak-to-peak differential | 650 | - | 1000 | mV |
| Input Loss of Signal Voltage | Peak-to-peak differential | 75 | 120 | 175 | mV |
| Differential Input Impedance ¹ | Programmable | 80 | - | 120 | Ω |
| Common Mode Input Impedance | - | 20 | 25 | 27.5 | Ω |



| Parameter | Test Condition | Min | Typ | Max | Units |
|-----------------------------------|----------------|-----|-----|-----|-------|
| Receiver Differential Return Loss | DC | -20 | - | - | dB |
| | 5 GHz | -5 | - | - | dB |
| Receiver Common-Mode Return Loss | DC | -10 | - | - | dB |
| | 5 GHz | -6 | - | - | dB |

1. This is programmable to $\pm 10\%$.

6.9 Line (MDI)

The X557 uses a voltage-mode driver to drive the MDI, so only decoupling is required on the transformer center-tap.

Table 6-9 MDI Electrical Parameters

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|---------------|-----------------------------|----------------|-----|-----|-----|-------------|
| $V_{OH-DIFF}$ | Differential Output Voltage | - | - | - | 2.0 | V_{pk-pk} |
| C_{IN} | Input Capacitance | - | - | - | 2.5 | pF |
| R_{IN} | Input Resistance | - | 48 | 50 | 52 | Ω |

6.10 Reference Clock

6.10.1 Input Clock Pins CLK_P and CLK_N - LVDS

Table 6-10 LVDS 50 MHz Input Electrical Parameters

| Symbol | Parameter | Min | Typ | Max | Units |
|--------------|----------------------------------|-----|-------|-----|-------|
| V_{SWING} | Single-Ended Input Voltage Swing | - | 0.35 | - | V |
| V_{COMMON} | Common-Mode Voltage Level | - | 1.2 | - | V |
| V_{IH} | Input High | - | 1.375 | - | V |
| V_{IL} | Input Low | - | 1.025 | - | V |



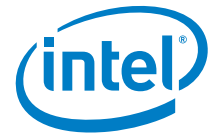
| Symbol | Parameter | Min | Typ | Max | Units |
|---------------|-------------------|-----|-----|-----|----------|
| C_{IN} | Input Capacitance | - | - | 1 | pF |
| $Z_{IN-DIFF}$ | Input Impedance | - | 100 | - | Ω |
| $R_{IN-DIFF}$ | Input Termination | - | 100 | - | Ω |

6.11 Crystal (X557-AT Use Only)

Note: Either a 50 MHz crystal or a 50 MHz oscillator can be implemented with the X557-AT (single port) device (crystal mode or oscillator mode, XTAL_SELECT_N = 0b or XTAL_SELECT_N = 1b). However, a 50 MHz oscillator must be implemented for use with the X557-AT2 (dual port) and X557-AT4 (quad port) devices (LVDS oscillator mode, XTAL_SELECT_N = 1b).

Table 6-11 Recommended Crystal Specifications

| Symbol | Parameter | Recommended Value | Comments |
|------------------|------------------------------|-------------------|--|
| F_c | Operating frequency | 50 MHz | |
| | Vibration mode | Fundamental | |
| | Cut | AT | |
| C_o | Shunt capacitance | < 5 pF | Includes capacitance of crystal electrodes, holder and leads |
| C_{L1}, C_{L2} | Load capacitance | 18 pF each | Includes capacitance of chip package and routing traces |
| R_I | Equivalent series resistance | < 50 Ohm | Value of R_I at series resonance |



6.12 Reference Resistors

Table 6-12 Bandgap Reference Resistor Electrical Parameters

| Parameter | Test Condition | Min | Typ | Max | Units |
|-----------------------|----------------|-----|------|-----|-------------------|
| Reference Resistance | Tied to 0V | - | 2.00 | - | K Ω |
| Resistor Accuracy | - | - | N/A | 1 | % |
| Maximum Power | - | - | N/A | 5 | M Ω |
| Temperature Variation | - | - | 50 | - | ppm/ $^{\circ}$ C |



NOTE: *This page intentionally left blank.*



7.0 Package

7.1 Mechanical (X557-AT/X557-AT2)

The X557-AT/X557-AT2 is packaged in a 19 mm x 19 mm flip-chip 324 pin FCBGA (18 rows x 18 rows) with a thermal heat spreader as shown in Figure 7-1.

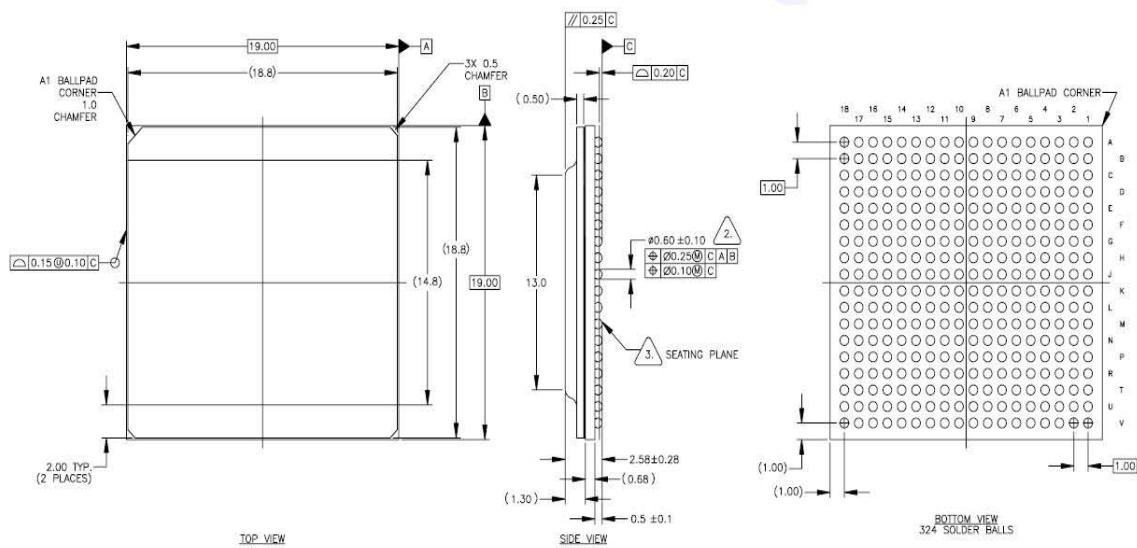


Figure 7-1 X557-AT/X557-AT2 Package Drawing

7.2 Mechanical (X557-AT4)

The X557-AT4 is packaged in a 25 mm x 25 mm flip-chip 576 pin FCBGA (24 rows x 24 rows) with a thermal heat spreader as shown in Figure 7-2

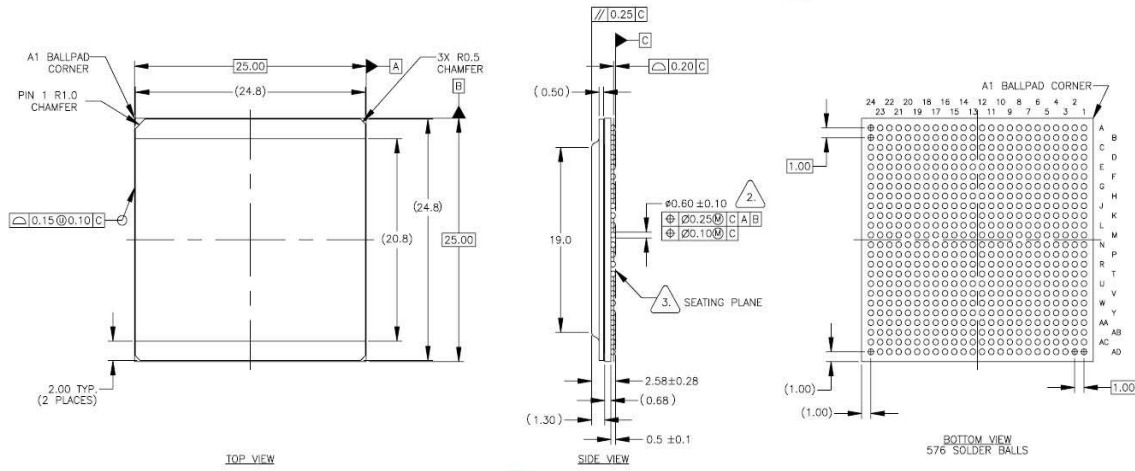


Figure 7-2 X557-AT4 Package Drawing



8.0 Thermal

8.1 Theta J

The X557 uses an copper heat spreader that is directly attached to the back of the die with thermal epoxy. The result is a low θ_{JC} path to the top of the package and a relatively low θ_{JB} to the board. The values of θ_j are listed in the tables that follow.

Table 8-1 X557-AT Thermals

| Name | Thermal Coefficient | Test Condition | Value | Units |
|---------------------------|---------------------|-------------------------|-------|-------|
| Theta Junction to Ambient | θ_{JA} | Still air at 55°C | 15.36 | °C/W |
| Theta Junction to Ambient | θ_{JA} | Still air at 55°C | 13.4 | °C/W |
| Theta Junction to Board | θ_{JB} | JEDEC 2s2p ¹ | 5.1 | °C/W |
| Theta Junction to Case | θ_{JC} | MIL STD 883e | 0.42 | °C/W |

1. Top/bottom trace 2 oz. copper
 Middle planes 1 oz. copper
 Equivalent 20% 2 oz. copper coverage adjacent to package
 Bottom copper 2 oz. 20% coverage



Table 8-2 X557-AT2 Thermals

| Name | Thermal Coefficient | Test Condition | Value | Units |
|---------------------------|---------------------|-------------------------|-------|-------|
| Theta Junction to Ambient | θ_{JA} | Still air at 55°C | 13.4 | °C/W |
| Theta Junction to Ambient | θ_{JA} | Still air at 55°C | 11.9 | °C/W |
| Theta Junction to Board | θ_{JB} | JEDEC 2s2p ¹ | 4.8 | °C/W |
| Theta Junction to Case | θ_{JC} | MIL STD 883e | 0.42 | °C/W |

1. Top/bottom trace 2 oz. copper
Middle planes 1 oz. copper
Equivalent 20% 2 oz. copper coverage adjacent to package
Bottom copper 2 oz. 20% coverage

Table 8-3 X557-AT4 Thermals

| Name | Thermal Coefficient | Test Condition | Value | Units |
|---------------------------|---------------------|-------------------------|-------|-------|
| Theta Junction to Ambient | θ_{JA} | Still air at 55°C | 11.1 | °C/W |
| Theta Junction to Ambient | θ_{JA} | Still air at 55°C | 9.98 | °C/W |
| Theta Junction to Board | θ_{JB} | JEDEC 2s2p ¹ | 4.69 | °C/W |
| Theta Junction to Case | θ_{JC} | MIL STD 883e | 0.42 | °C/W |

1. Top/bottom trace 2 oz. copper
Middle planes 1 oz. copper
Equivalent 20% 2 oz. copper coverage adjacent to package
Bottom copper 2 oz. 20% coverage

8.2 Thermal Model

Intel supplies a Flotherm® PDML model for the X557.



9.0 Design Considerations and Guidelines

This section provides guidelines for selecting components, connecting interfaces, using special pins, and layout guidance.

Unused interfaces should be terminated with pull-up or pull-down resistors. These are indicated in [Section 2.0](#), [Section 3.0](#) or reference schematics. There are reserved pins, identified as RSVD_NC and RSVD_VSS. The X557 might enter special test modes unless these strapping resistors are in place.

Some unused interfaces must be left open. Do not attach pull-up or pull-down resistors to any balls identified as No Connect or Reserved No Connect.

9.1 Connecting the 10GBASE-T MDI Interfaces

In 10GBASE-T mode, the line interface on the X557 is capable of driving up to 100 meters of CAT-6a unshielded twisted pair or 100 meters of CAT-7 shield cable (100 Ω differential impedance). It can also drive 55 meters of CAT-6 cable. In 1GBASE-T and 100MBASE-TX modes, it can drive 130 meters of CAT-5e (or better) cable. It is designed to drive this via a quad, 50 Ω center tapped 1:1 transformer connected to an RJ-45 PCB-mount jack. Solutions that combine the transformer and RJ-45 jack into a single device are also supported.

The line interface on the X557 supports automatic A/B and C/D pair swaps and inversions (MDI-X). It also supports provisioned ABCD to DCBA pair reversal for ease of routing with stack-jacks via an NVM setting, which sets this configuration at power up.

Note: This reversal does not swap polarities thus A+ maps to D+, etc.

9.1.1 MDI Circuit Guidelines

The MDI discrete design and integrated magnetic components were chosen for inclusion in the reference design. These components are capable of delivering the performance required for this demanding application.



9.1.2 Magnetics Module

The magnetics module has a critical effect on overall IEEE and emissions conformance. The X557 should meet the performance required for a design with reasonable margin to allow for manufacturing variation. Carefully qualifying new magnetics modules prevents problems that might arise because of interactions with other components or the Printed Circuit Board (PCB) itself. The magnetics specified should comply with the specifications listed in the Intel® 10-GBASE-T Magnetic Specification Electrical/Mechanical Requirements for 10GBASE-T Magnetic Components, which includes separate specifications for discrete and integrated magnetics modules.

These have five channels of 3-wire choke / transformer pairs in them, with four facing the choke towards the line (RJ45), and one facing the choke towards the X557.

The steps involved in magnetics module qualification are:

1. Verify that the vendor's published specifications in the component datasheet meet or exceed the required IEEE 802.3an specifications and the internal specifications listed in the Intel® 10-GBASE-T Magnetic Specification Electrical/Mechanical Requirements for 10GBASE-T Magnetic Components.
2. Independently measure the component's electrical parameters on a test bench, checking samples from multiple lots. Check that the measured behavior is consistent from sample-to-sample and that measurements meet the published specifications.
3. Perform physical layer conformance testing and EMC (FCC and EN) testing in real systems. Vary temperature and voltage while performing system level tests.

Magnetics modules for 10GBASE-T Ethernet as used by the X557 are similar to those designed for 1GBASE-T, except that the electrical requirements for the board layout and magnetics are more stringent. Refer to [Section 6.0](#) for specific electrical requirements that the magnetics need to meet in the Intel® 10-GBASE-T Magnetic Specification Electrical/Mechanical Requirements for 10GBASE-T Magnetic Components.

9.1.3 5th Channel

In order to sense and cancel common-mode noise, the X557 provides a 5th channel designed for this purpose. It is very similar to the receivers on Pairs A - D, with the exception that it does not have a driver and only receives. Its input impedance is 100 Ω .

When discrete magnetics are in use, this channel should be connected to a common-mode sense point. In this design, the common-mode sense point is the Bob Smith termination of Pair D. This sense point is run through a transformer to convert the signal to differential for pick-up by the 5th channel receiver. In order to match the 100 Ω impedance of the receiver input with the required 75 Ω Bob Smith termination, a 300 Ω parallel resistor is used.

Integrated magnetics perform the required termination internally. As a result, the Bob Smith termination used in the discrete case is not necessary.

9.1.4 External 5th Channel Filtering

5th channel filtering is integrated into the X557. There is no need for an on-board filter circuit.



9.1.5 Board Noise Cancellation

An advantage of the 5th channel is that in addition to canceling received common-mode interference from the line, it also cancels noise picked up on the PCB. This is especially important if the RJ-45 is located any significant distance from the X557. Consequently, every effort should be made to route the 5th channel traces along the same path as the other four MDI traces.

9.1.6 MDI Layout Guidance

The MDI that was chosen for the X557 designs consist of an RJ-45 right-angle PCB jack, Bob Smith termination, discrete magnetics, and a filter (see [Figure 9-1](#)). The magnetics can be implemented either as a discrete module or an integrated solution combining the magnetics and the RJ-45 jack.

Minimizing the amount of space needed for the PHY is important because other interfaces compete for physical space on a Network Interface Card (NIC) or LAN on Motherboard (LOM) near the connector. The PHY circuits need to be as close as possible to the connector.

[Figure 9-1](#) illustrates some basic placement distance guidelines. It shows four differential pairs and the layout can be generalized for a 10 GbE system with four analog pairs. The ideal placement for the X557 is approximately two inches behind the magnetics module for both the discrete and integrated solutions.

9.1.6.1 Discrete Magnetics

The X557 uses a common-mode sensing circuit on the MDI of each channel to cancel in-band common-mode interference that couples into the differential receive signals. This common-mode sense circuitry is referred to as the 5th channel. This is where the sense circuitry sits in series with the Bob Smith termination for Channel D. The signal runs through a transformer to perform the common-to-differential conversion where it is followed by the X557-facing common-mode choke. This provides isolation from board noise being radiated on Channel D. In addition, the impedance of the Bob Smith termination is $75\ \Omega$ Channel A, B, C and $300\ \Omega$ Channel D, whereas the PHY input impedance is $100\ \Omega$.

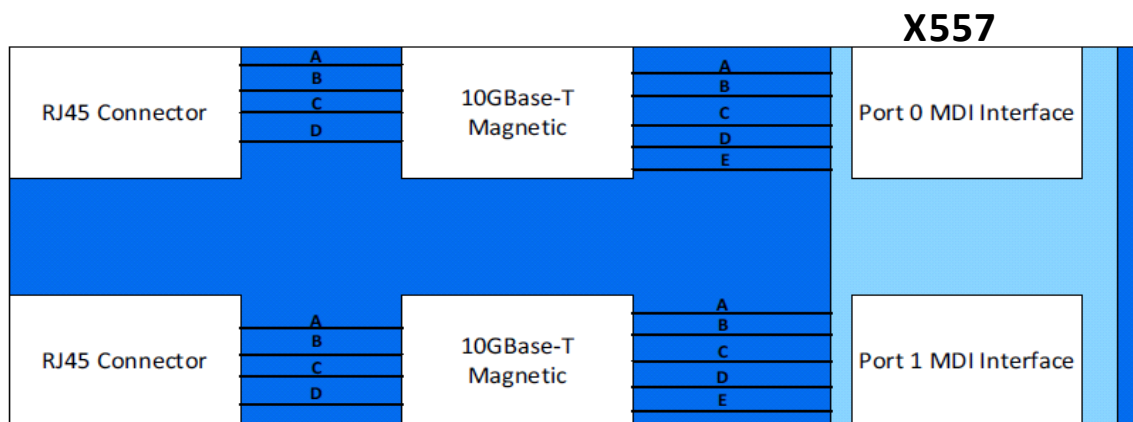


Figure 9-1 Basic MDI Placement Guidelines

The X557, referred as a LAN silicon in [Figure 9-3](#) and [Figure 9-2](#), must be at least one inch from the I/O back panel. To help reduce EMI, the following recommendations should be followed:

- Minimize the length of the MDI interface.
- Place the MDI traces no closer than 0.5 inch (1.3 cm) from the board edge.

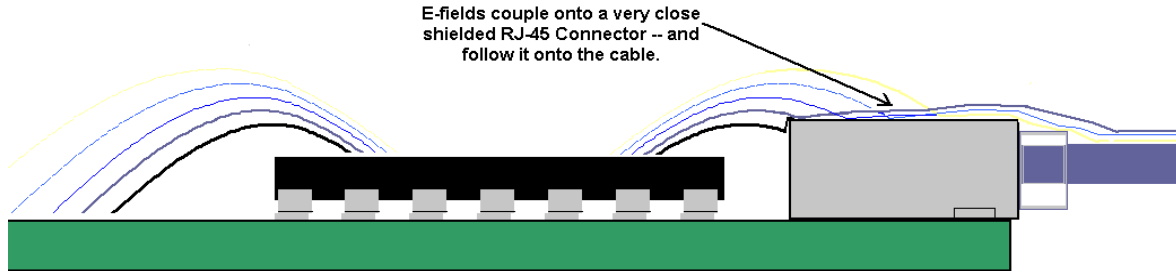


Figure 9-2 Effect of Device Placed Less Than One Inch from the RJ-45 Connector

The associated grounding scheme (blue) with the front-end of the chip is shown in the microstrip traces between the transformer and the RJ-45 (see [Figure 9-3](#)).

From these figures the following should be noted:

1. The ground is split underneath the magnetics, with the chassis ground being present under the front-end ([Figure 9-3](#)), and the circuit ground under the X557 side of the magnetics. Thus, the MDI traces on the line side are referenced to chassis ground.

The magnetic module is used with the common mode choke facing the X557. This enables a Bob Smith termination to be implemented from the line side transformer center taps to chassis ground.

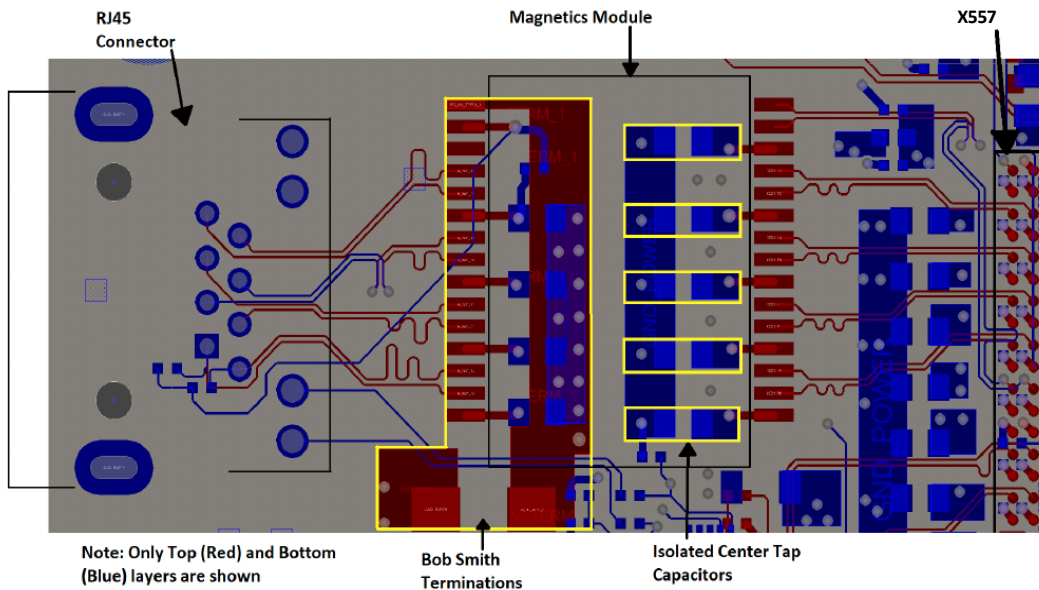


Figure 9-3 Transformer Bypass Components

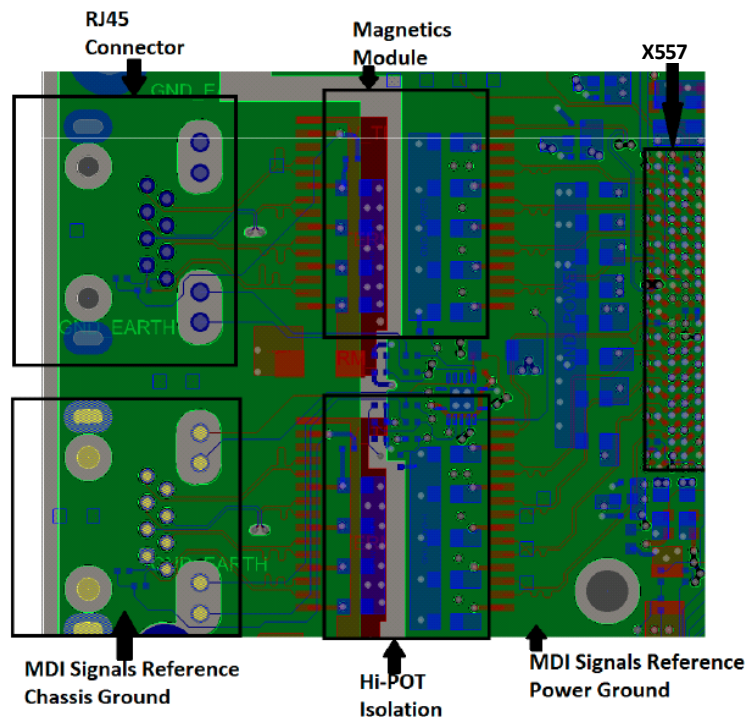


Figure 9-4 MDI Grounds

- Bob Smith termination and the shield of the RJ-45 jack are both connected to chassis ground, which are the two large circular metalizations in the MDI (see [Figure 9-4](#)).
- The resistors in the Bob Smith termination are required to be 0805s to handle the cable discharge voltages.
- Similarly, the magnetics should be placed as close as possible to the RJ-45 jack.
- In [Figure 9-3](#), the Hi-POT clearance for cable discharge is shown and designed with ≥ 80 mils of clearance from the ground. Note that the breakdown voltage in FR-4 is lowest in the x-y axes planar to the PCB and highest in the z-axis between layers.

9.1.6.2 Integrated Magnetics

The 5th MDI channel previously described in discrete magnetics implementation is still realized when using integrated magnetics, with some notable exceptions (see [Figure 9-5](#)). The required termination, reference ground-plane division, and 5th channel wiring to the 4th channel center-tap occur within the integrated magnetics module. The guidance on MDI trace implementation between the X557 and the integrated module remains the same as with discrete magnetics, including length requirements and target impedance.

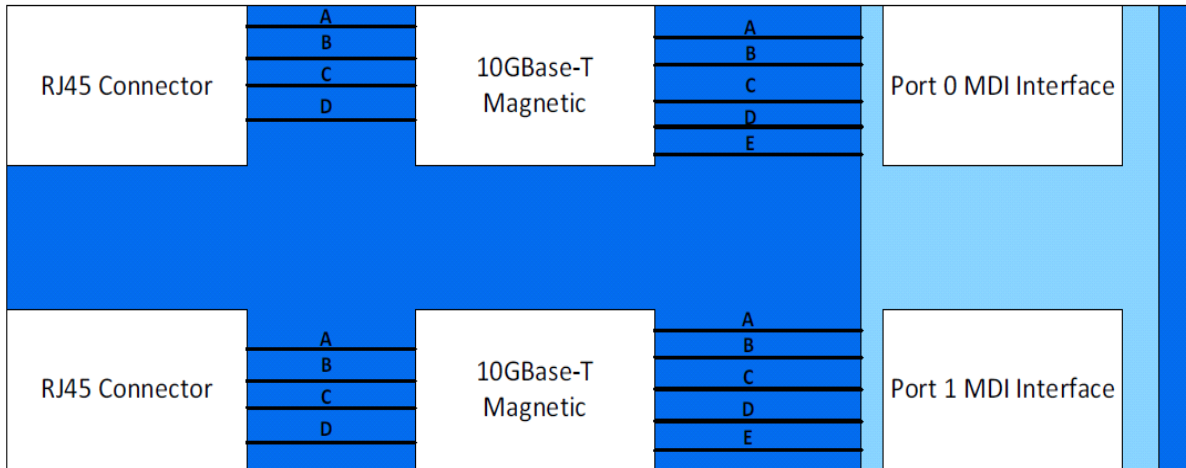


Figure 9-5 Basic MDI Placement Guidelines

Note: The RJ-45 jack and 10GBase-T Magnetics (red outline) are included in the integrated magnetics module.

The differences between the discrete and integrated magnetics implementations are as follows:

1. The ground split that occurs underneath discrete magnetics modules is performed internally when using integrated magnetics. As a result, this ground split does not need to be addressed.
2. The required Bob Smith termination is implemented internally when using integrated magnetics.

9.1.6.3 MDI Differential Pair Trace Routing for LAN Design

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes.

9.1.6.4 Signal Trace Geometry

One of the key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the reference plane. To minimize trace inductance, high-speed signals and signal layers that are close to a reference or power plane should be as short and wide as practical. Ideally, the trace-width to trace-height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the neighboring planes.

Each pair of signals should target a differential impedance of $100 \Omega \pm 15\%$.

A set of trace length calculation tools are made available from Intel to aid with MDI topology design. Contact your Intel representative for tool availability.



When designing a board layout, the automatic router feature of the CAD tool must not route the differential pairs without intervention. In most cases, the differential pairs require manual routing.

Note: Measuring trace impedance for layout designs targeting 100 Ω often results in lower actual impedance due to over-etching. Designers should verify actual trace impedance and adjust the layout accordingly. If the actual impedance is consistently low, a target of 105 Ω to 110 Ω should compensate for over-etching.

9.1.6.4.1 Matching Traces Within a Pair (P and N)

P and N for each MDI pair should be matched to within 5 mils on the PCB to prevent common-to-differential and differential-to-common conversion due to the length mismatch.

If in-pair length matching is not possible using bends or small loops, serpentine routing (zig zag of a shorter trace) is acceptable if only one to three meanders are routed within 200 mils of the source of the skew or the end(s) of any otherwise unmatched lengths of a differential trace segment. For example, near device pins and/or at or near the connector pins and possibly at differential signal vias. Refer to the Intel® Ethernet Controller 10 GbE X557 Controller Checklists for more details.

Table 9-1 MDI Routing Summary

| Parameter | Main Route Guidelines | Breakout Guidelines ¹ | Notes |
|---|---|----------------------------------|-----------------|
| Signal group | MDI_P[3:0] MDI_N[3:0] | | |
| Microstrip*/Stripline* uncoupled single-ended impedance specification | 50 Ω \pm 10% | | |
| Microstrip/Stripline uncoupled differential impedance specification | 100 Ω \pm 15% | | ^{2, 3} |
| Microstrip nominal trace width | Design dependent | Design dependent | |
| Microstrip nominal trace space | Design dependent | Design dependent | ³ |
| Microstrip/Stripline trace length | <8 inches | | Table 9-2 |
| Microstrip/Stripline pair-to-pair space (edge-to-edge) | \geq 7 times the dielectric thickness | | |
| Microstrip/Stripline bus-to-bus spacing | \geq 7 times the dielectric thickness | | |
| Matching traces within a pair (P and N) | <5 mils | | |
| Keep pair-to-pair length differences | <2 inches | | |

1. Pair-to-pair spacing \geq 7 times the dielectric thickness for a maximum distance of 500 mils from the pin. The phase tolerance between MDI_P and MDI_N is <5mils.
2. Board designers should ideally target 100 Ω \pm 10%. If it's not feasible (due to board stackup) it is recommended that board designers use a 95 Ω \pm 10% target differential impedance for MDI with the expectation that the center of the impedance is always targeted at 95 Ω . The \pm 10% tolerance is provided to allow for board manufacturing process variations and not lower target impedances. The minimum value of impedance cannot be lower than 90 Ω .
3. Simulation shows 80 Ω differential trace impedances degrade MDI return loss measurements by approximately 1 dB from that of 90 Ω .

**Table 9-2 Maximum Trace Lengths Based on Trace Geometry and Board Stackup**

| Dielectric Thickness (mils) | Dielectric Constant (DK) at 1 MHz | Width / Space / Width (mils) | Pair-to-Pair Space (mils) | Nominal Impedance (Ω) | Impedance Tolerance (+/-%) | Maximum Trace Length (inches) ¹ |
|-----------------------------|-----------------------------------|------------------------------|---------------------------|--------------------------------|----------------------------|--|
| 2.7 | 4.05 | 4/10/4 | 19 | 95 ² | 17 ² | 3.5 |
| 2.7 | 4.05 | 4/10/4 | 19 | 95 ² | 15 ² | 4 |
| 2.7 | 4.05 | 4/10/4 | 19 | 95 | 10 | 5 |
| 3.3 | 4.1 | 4.2/9/4.2 | 23 | 100 ² | 17 ² | 4 |
| 3.3 | 4.1 | 4.2/9/4.2 | 23 | 100 | 15 | 4.6 |
| 3.3 | 4.1 | 4.2/9/4.2 | 23 | 100 | 10 | 6 |
| 4 | 4.2 | 5/9/5 | 28 | 100 ² | 17 ² | 4.5 |
| 4 | 4.2 | 5/9/5 | 28 | 100 | 15 | 5.3 |
| 4 | 4.2 | 5/9/5 | 28 | 100 | 10 | 7 |

1. Longer MDI trace lengths can be achievable, but might make it more difficult to achieve IEEE conformance. Simulations have shown deviations are possible if traces are kept short. Longer traces are possible; use cost considerations and stackup tolerance for differential pairs to determine length requirements.
2. Deviations from 100 Ω nominal and/or tolerances greater than 15% decrease the maximum length for IEEE conformance.

Note: Use the MDI Differential Trace Calculator to determine the maximum MDI trace length for your trace geometry and board stackup. Contact your Intel representative for access.

The following factors can limit the maximum MDI differential trace lengths for IEEE conformance:

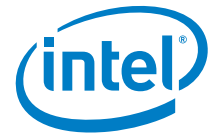
- Dielectric thickness
- Dielectric constant
- Nominal differential trace impedance
- Trace impedance tolerance
- Copper trace losses
- Additional devices, such as switches, in the MDI path might impact IEEE conformance.

Board geometry should also be factored in when setting trace length.

9.1.6.5 Ground Planes Under a Magnetics Module

The magnetics module chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum. Splitting the ground planes beneath the transformer minimizes noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the magnetics. This arrangement also improves the common mode choke functionality of magnetics module.

Integrated magnetics perform this ground plane separation internally. As a result, the ground plane split previously described is not needed when using integrated magnetics.



9.1.7 PHY MDI Lane Swap Configuration

The X557 provides flexible MDI LAN swaps for MDI board routing (see Figure 9-6) via an NVM setting.

- Default configuration - 0, 1, 2, 3 <-> A, B, C, D
- MDI swap configuration - 3, 2, 1, 0 <-> A, B, C, D
- 5th channel swap not supported (AFE_LINE_4P and AFE_LINE_4N)

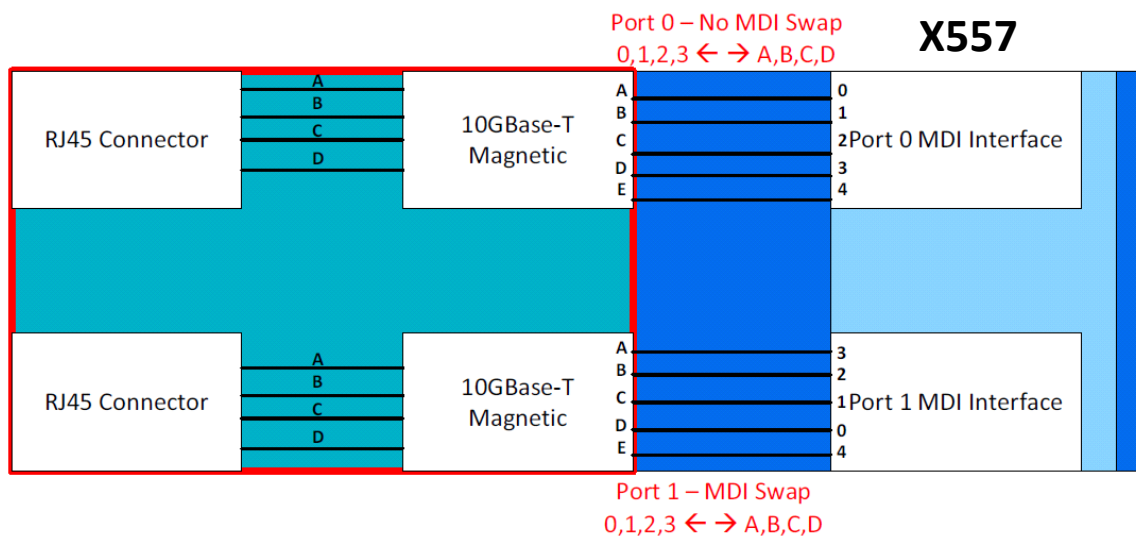


Figure 9-6 PHY AFE_LINE Lane Swap Configuration

9.1.8 Center Tap Connection Via Capacitors to Ground

The X557 has a voltage-mode driver. When using it in 10GBASE-T applications, it is required that a center tap be decoupled to ground. When using an integrated magnetic, four capacitors of 0.1 μ F should be connected to each center tap pin to ground.

When using a discrete magnetic, add a 0.1 μ F capacitor to each center tap pin for a total of five capacitors as previously described.



9.2 Connecting the JTAG Port

The X557 contains a test access port (3.3 V only) conforming to the IEEE 1149.1-2001 Edition (JTAG) specification. To use the test access port, connect these balls to pads accessible by specific test equipment.

For proper operation, a pull-down resistor should be connected to the JTCK and JRST_N signals and pull up resistors to the JTDO, JTMS and JTDI signals.

A Boundary Scan Definition Language (BSDL) file describing the X557 is available for use in specific test environment.

9.3 PCB Guidelines

This section describes the general PCB design guidance targeted as supplementary information in addition to the specific requirements and recommendations for individual interfaces. For items not directly covered in the specific interface sections, these guidance recommendations apply to the design.

9.3.1 Board Stack-Up Example

PCBs for these designs typically have six, eight, or more layers. Although, the X557-AT does not dictate stackup, the following examples show typical stack-up options.

Microstrip Example:

- Layer 1 is a signal layer.
- Layer 2 is a ground layer.
- Layer 3 is used for power planes.
- Layer 4 is a signal layer. Careful routing is necessary to prevent crosstalk with layer 5.
- Layer 5 is a signal layer. Careful routing is necessary to prevent crosstalk with layer 4.
- Layer 6 is used for power planes.
- Layer 7 is a signal ground layer.
- Layer 8 is a signal layer.

Note: Layers 4 and 5 should be used mostly for low-speed signals because they are referenced to potentially noisy power planes that might also be slotted.

Stripline Example:

- Layer 1 is a signal layer.
- Layer 2 is a ground layer.
- Layer 3 is a signal layer.
- Layer 4 is used for power planes.
- Layer 5 is used for power planes.



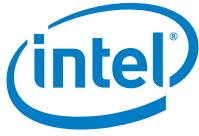
- Layer 6 is a signal layer.
- Layer 7 is a signal ground layer.
- Layer 8 is a signal layer.

Note: To avoid the effect of the potentially noisy power planes on the high-speed signals, use offset stripline topology. The dielectric distance between the power plane and signal layer should be three times the distance between ground and signal layer.

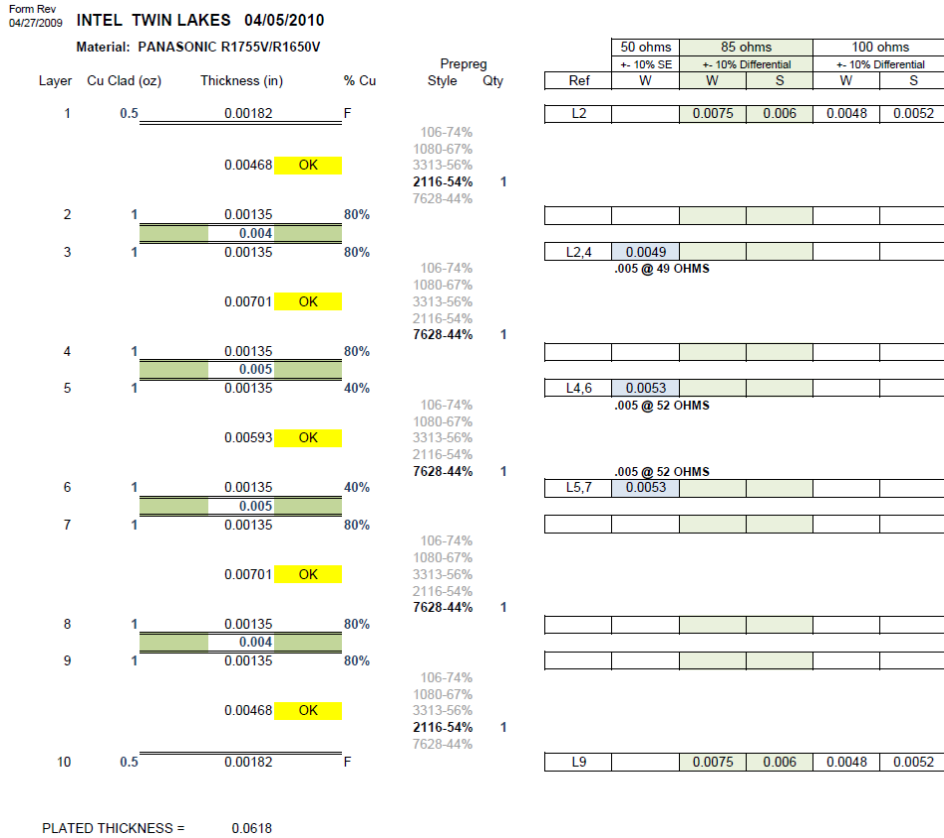
This board stack-up configuration can be adjusted to conform to company-specific design rules.

9.3.2 Customer Reference Board Stack-Up Example

| Layer Name | Plane Description | Layer Thickness (mil) | Copper Weight (oz) | Dielectric eR |
|------------|------------------------|-----------------------|--------------------|---------------|
| | solder mask | 0.5 | | 3.8 |
| Signal 1 | SIGNAL | 1.9 | 1.5 | |
| | 1080-prepreg | 2.7 | | 4.0 |
| Plane 2 | GND DDR PWR GND | 1.3 | 1.0 | |
| | core | 4.0 | | 4.1 |
| Signal 3 | SIGNAL | 1.3 | 1.0 | |
| | prepreg | 12.0 | | 4.0 |
| Plane 4 | POWER (Vddq, GND, Vtt) | 2.6 | 2.0 | |
| | core | 4.0 | | 4.1 |
| Plane 5 | POWER (12V input) | 2.6 | 2.0 | |
| | prepreg | 6.0 | | 4.0 |
| Plane 6 | POWER (PLL, VSA, | 2.6 | 2.0 | |
| | core | 4.0 | | 4.1 |
| Plane 7 | GND | 2.6 | 2.0 | |
| | prepreg | 12.0 | | 4.0 |
| Signal 8 | SIGNAL | 1.3 | 1.0 | |
| | core | 4.0 | | 4.1 |
| Plane 9 | GND DDR PWR GND | 1.3 | 1.0 | |
| | 1080-prepreg | 2.7 | | 4.0 |
| Signal 10 | SIGNAL | 1.9 | 1.5 | |
| | solder mask | 0.5 | | 3.8 |
| | | 71.8 | | |



9.3.3 Intel Reference Board Stack-Up Example



INSTRUCTIONS - EACH LAYER MUST HAVE CU THICKNESS AS "0" OR .5, 1, 2, 3 ETC
 EACH DIELECTRIC SPACE MUST HAVE # PLYS EACH STYLE AT "0" OR 1,2,3, ETC
 EACH CORE LAYER MUST HAVE CORE NOMINAL WITHOUT CU - .010, .0102, .0052 ETC
 CORE TOLERANCE IS NOT CALCULATED AND NEEDS TO BE CONSIDERED

9.3.4 Via Usage

Use vias to optimize signal integrity. Figure 9-7 shows correct via usage. Figure 9-8 shows the type of topology that should be avoided.

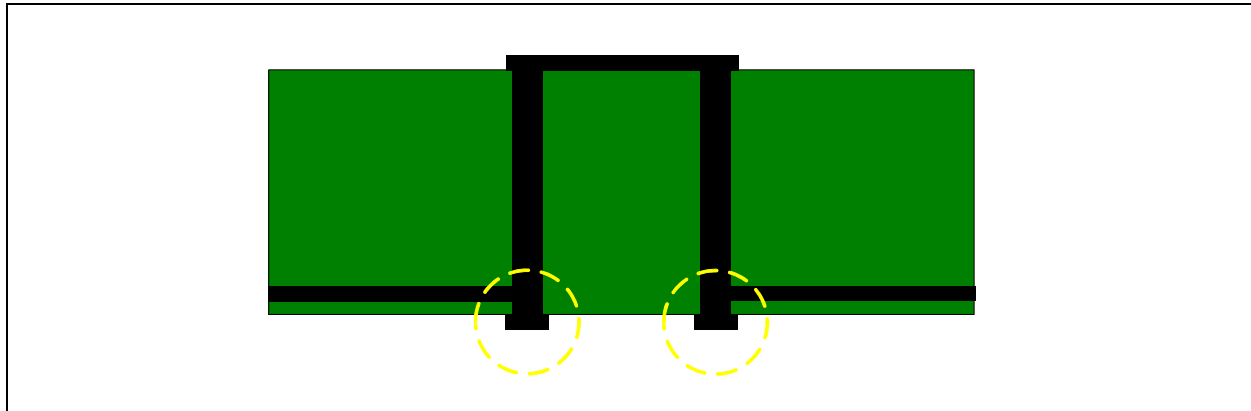


Figure 9-7 Correct Via Usage

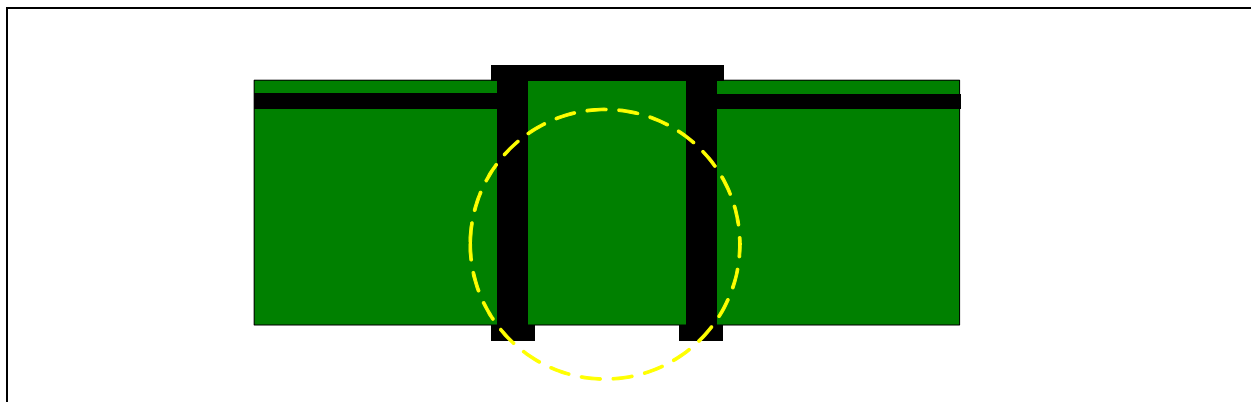


Figure 9-8 Incorrect Via Usage

Any via stubs on the MDI differential signal traces must be less than 35 mils in length. Keeping MDI signal via stubs less than or equal to 20 mils is preferable.

Place ground vias adjacent to signal vias used for the MDI interface. DO NOT embed vias between the high-speed signals, but place them adjacent to the signal vias. This helps to create a better ground path for the return current of the AC signals, which also helps address impedance mismatches and EMC performance.

It is recommend that, in the breakout region between the via and the capacitor pad, target a Z0 for the via to capacitor trace equal to 50 Ω . This minimizes impedance imbalance.

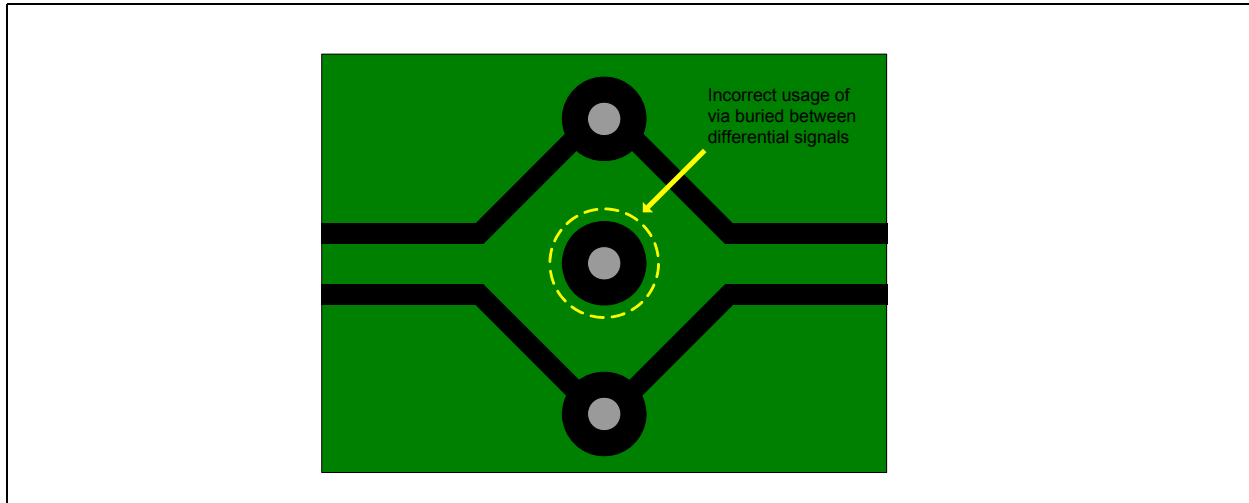


Figure 9-9 No Vias Between High-Speed Traces in the Same Differential Pair

9.3.5 Reference Planes

Do not cross plane splits with the MDI high-speed differential signals. This causes impedance mismatches and negatively affects the return current paths for the board design and layout. Refer to Figure 9-10.

Traces should not cross power or ground plane splits if at all possible. Traces should stay seven times the dielectric height away from plane splits or voids. If traces must cross splits, capacitive coupling should be added to stitch the two planes together in order to provide a better AC return path for the high-speed signals. To be effective, the capacitors should be have low ESR and low equivalent series inductance.

Note: Even with plane split stitching capacitors, crossing plane splits is extremely high risk for 10GBASE-T designs.

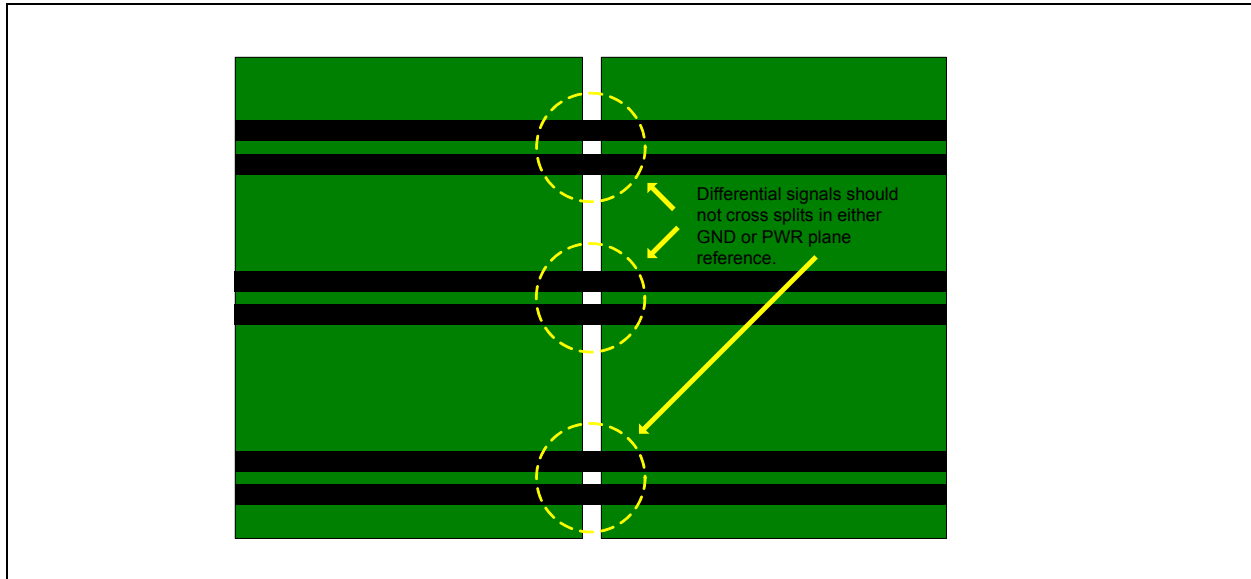


Figure 9-10 Do Not Cross Plane Splits

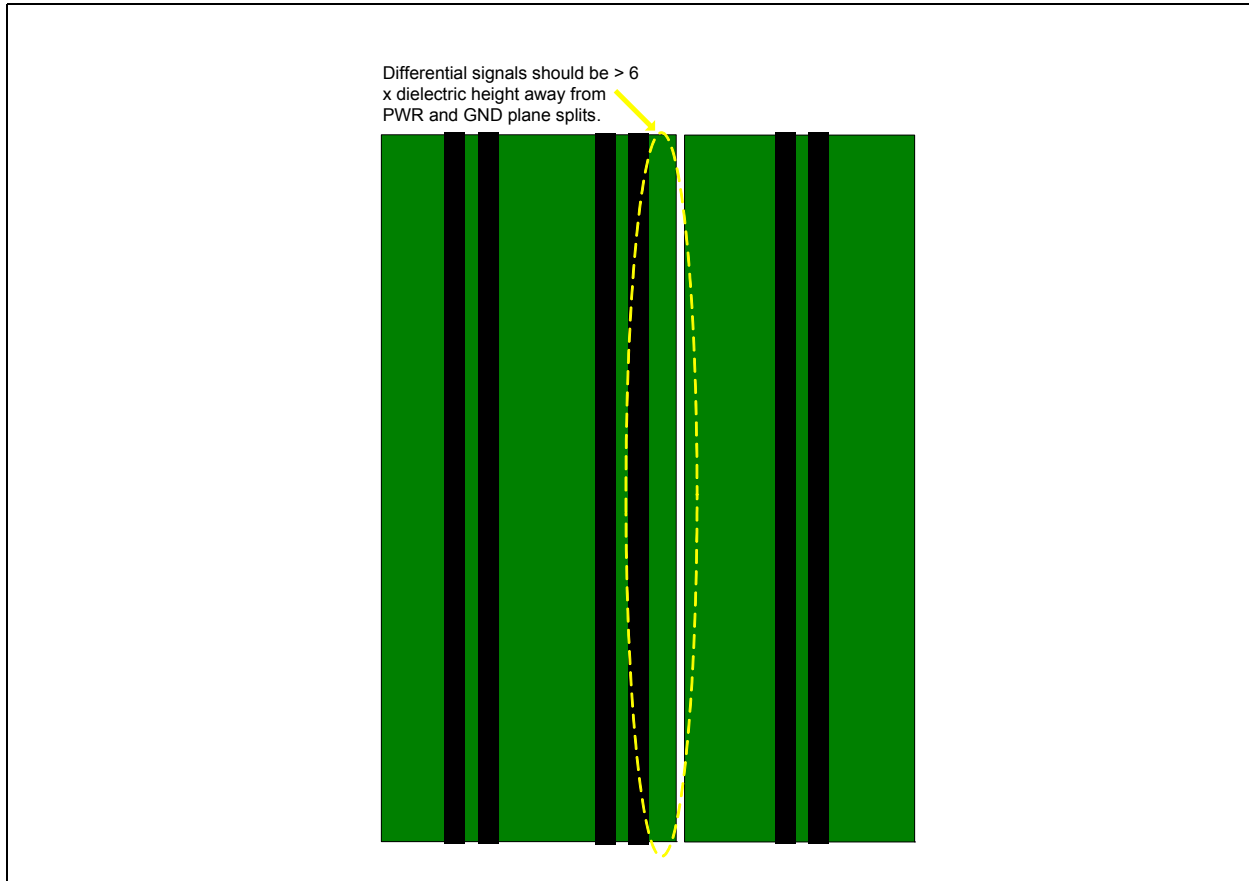


Figure 9-11 Traces Should Stay Seven Times the Dielectric Height Away From Plane Splits Or Voids

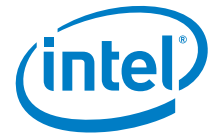
It is recommended that the MDI signals stay at least seven times the dielectric height away from any power or ground plane split. This improves impedance balance and return current paths.

If a high-speed signal needs to reference a power plane, then ensure that the height of the secondary (power) reference plane is at least 3 x the height of the primary (ground) reference plane.

9.3.6 Reducing Circuit Inductance

Traces should be routed over a continuous reference plane with no interruptions. If there are vacant areas on a reference or power plane, the signal conductors should not cross the vacant area. Routing over a void in the reference plane causes impedance mismatches and usually increases radiated noise levels. Noisy logic grounds should NOT be located near or under high-speed signals or near sensitive analog pin regions of the LAN silicon. If a noisy ground area must be near these sensitive signals or IC pins, ensure sufficient decoupling and bulk capacitance in these areas. Noisy logic and switching power supply grounds can sometimes affect sensitive DC subsystems such as analog to digital conversion, operational amplifiers, etc.

All ground vias should be connected to every ground plane; and similarly, every power via should be equally potential power planes. This helps reduce circuit inductance. Another recommendation is to



physically locate grounds to minimize the loop area between a signal path and its return path. Rise and fall times should be as slow as possible while still meeting the relevant electrical requirements because signals with fast rise and fall times contain many high frequency harmonics, which can radiate significantly. The most sensitive signal returns closest to the chassis ground should be connected together. This results in a smaller loop area and reduces the likelihood of crosstalk. The effect of different configurations on the amount of crosstalk can be studied using electronics modeling and simulation software.

9.3.7 Signal Isolation

To maintain the best signal integrity, keep digital signals far away from the analog traces. A good rule to follow is no digital signal should be within 7x to 10x dielectric height of the differential pairs. If digital signals on other board layers cannot be separated by a ground plane, they should be routed at a right angle (90 degrees) to the differential signal traces. If there is another Ethernet controller on the board, take care to keep the differential pairs away from that circuit. The same thing applies to switching regulator traces.

Rules to follow for signal isolation:

- Separate and group signals by function on separate board layers if possible. Maintain a separation that is at least seven times the thinnest adjacent dielectric height between all differential pairs (Ethernet) and other nets, but group associated differential pairs together.
- Over the length of the trace run, each differential pair should be at least seven times the thinnest adjacent dielectric height away from any parallel signal traces.
- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate other I/O signals from high-speed signals to minimize crosstalk. Crosstalk can increase radiated EMI and can also increase susceptibility to EMI from other signals.
- Avoid routing high-speed LAN traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices.

9.3.8 Traces for Decoupling Capacitors

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and reduce the intended effect of decoupling capacitors. Also, for similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance. Refer to [Section 6.0](#) for the PHY in regards to actual placement requirements of the capacitors.

9.3.9 Power and Ground Planes

Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and locating decoupling capacitors at or near power inputs to bypass to the signal return. This significantly reduces EMI radiation.

These guidelines reduce circuit inductance in NICs and LOMs:



- Route traces over a continuous plane with no interruptions. Do not route over a split power or ground plane. If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. Routing signals over power or ground voids increases inductance and increases radiated EMI levels.
- Use distance and/or extra decoupling capacitors to separate noisy digital grounds from analog grounds to reduce coupling. Noisy digital grounds can affect sensitive DC subsystems.
- All ground vias should be connected to every ground plane, and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This minimizes the loop area.
- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high frequency harmonics, which can radiate EMI.
- Do not route high-speed signals near switching regulator circuits.
- It's acceptable to put ground fill or thieving on the trace layers, but preferably not closer than 50 mils to the differential traces and the connector pins.
- If differential traces must be routed on another layer, then the signal vias should carry the signal to the opposite side of the PCB (to be near the top of the PCB), AND if the high-speed signals are being routed between two connectors on the same board, then before the signal traces reach the second connector, they must return to the original signal layer (before reaching the connector pin). This strategy keeps via stubs short without requiring back drilling.
- Each time differential traces make a layer transition (pass through a pair of signal vias), there must be at least one ground via located near each signal via. Two ground vias near each signal via is better. See [Figure 9-12](#) and [Figure 9-13](#).

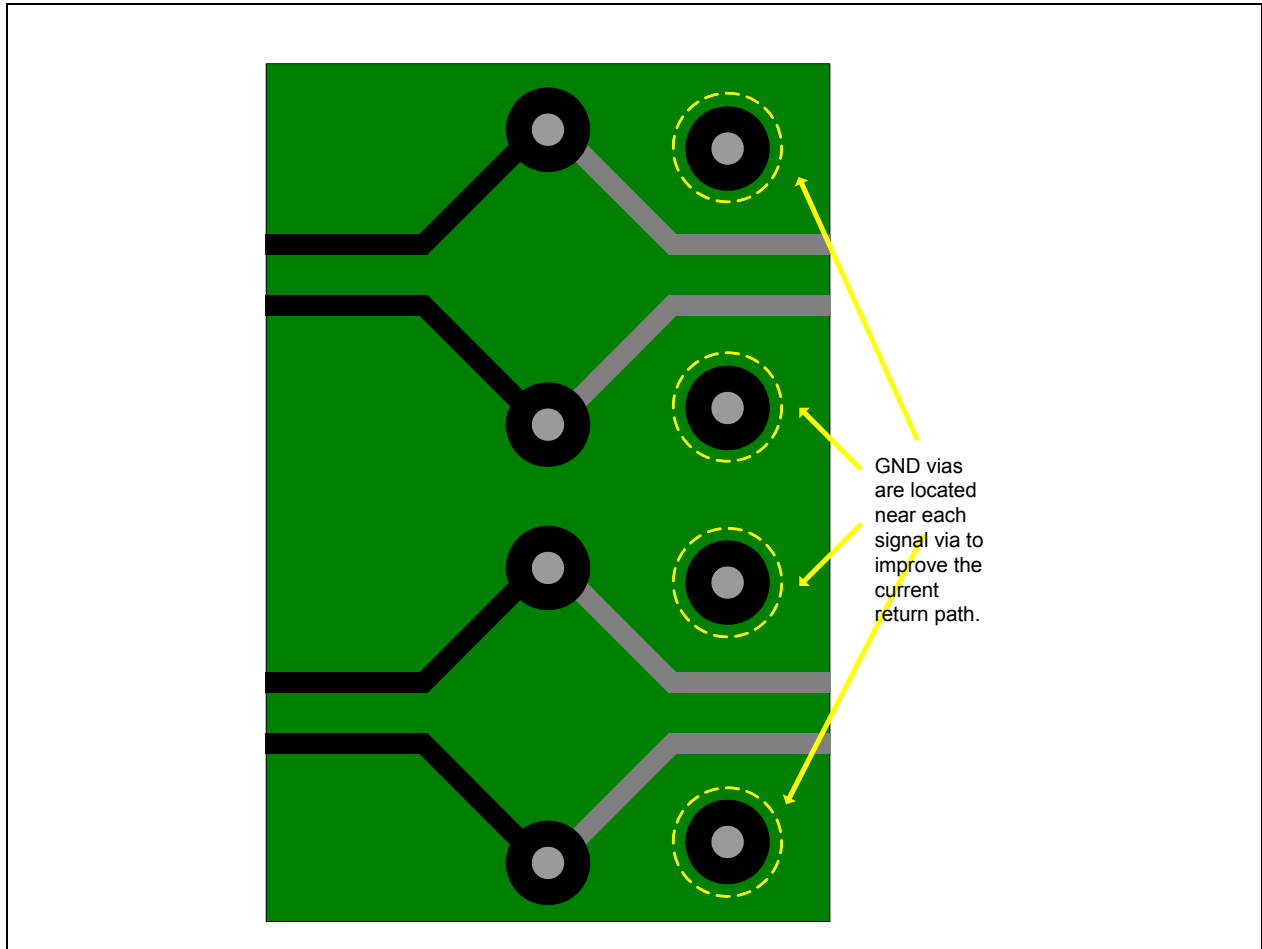


Figure 9-12 Good Ground Vias for Signal Return Paths – One Return Path Via Per Signal Via

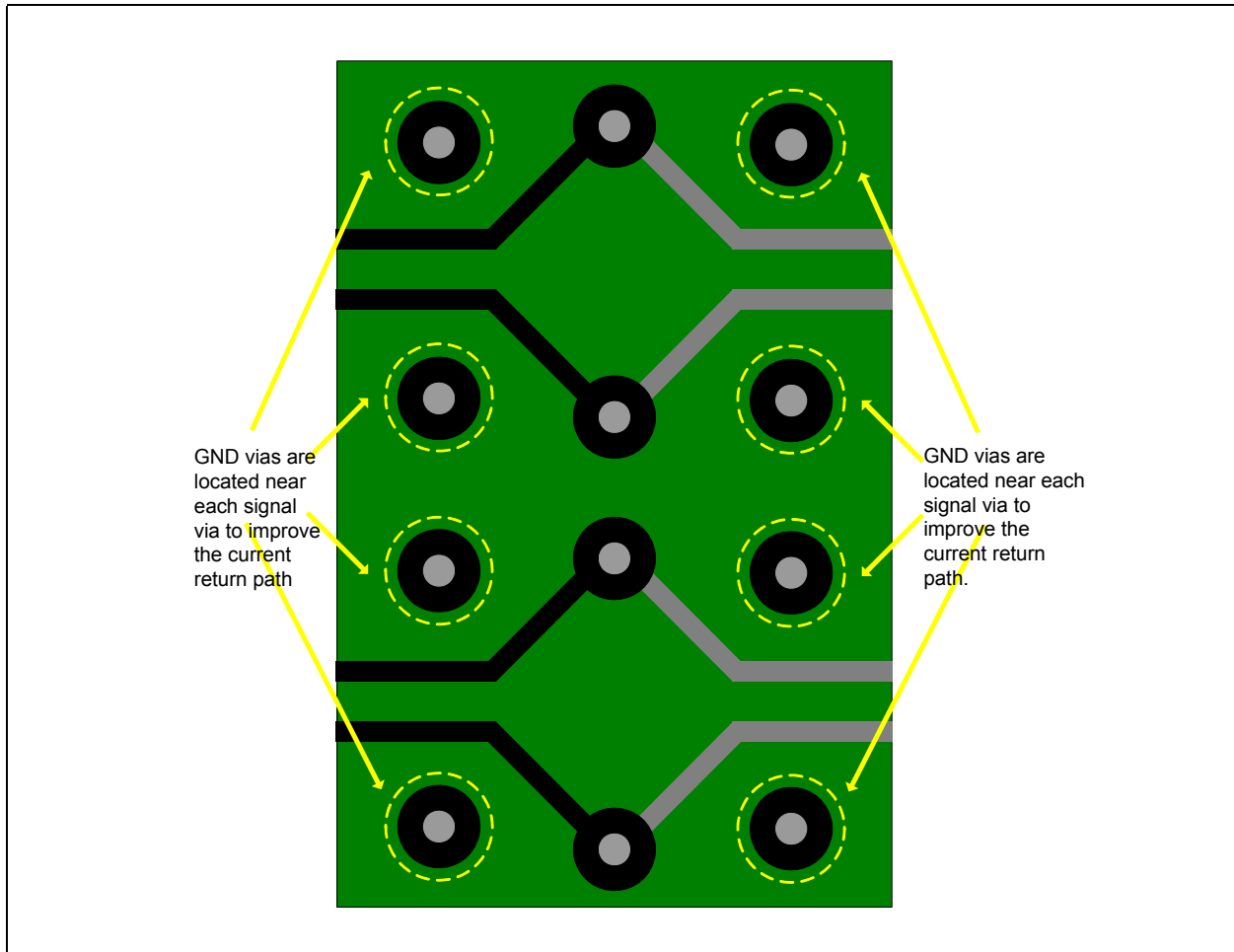


Figure 9-13 Better Ground Vias for Signal Return Paths – Two Return Path Vias Per Signal Via (Less Reflection)

If the PCB fabrication process permits it, it's best to remove signal via pads on unconnected metal layers. See [Figure 9-14](#) and [Figure 9-15](#).

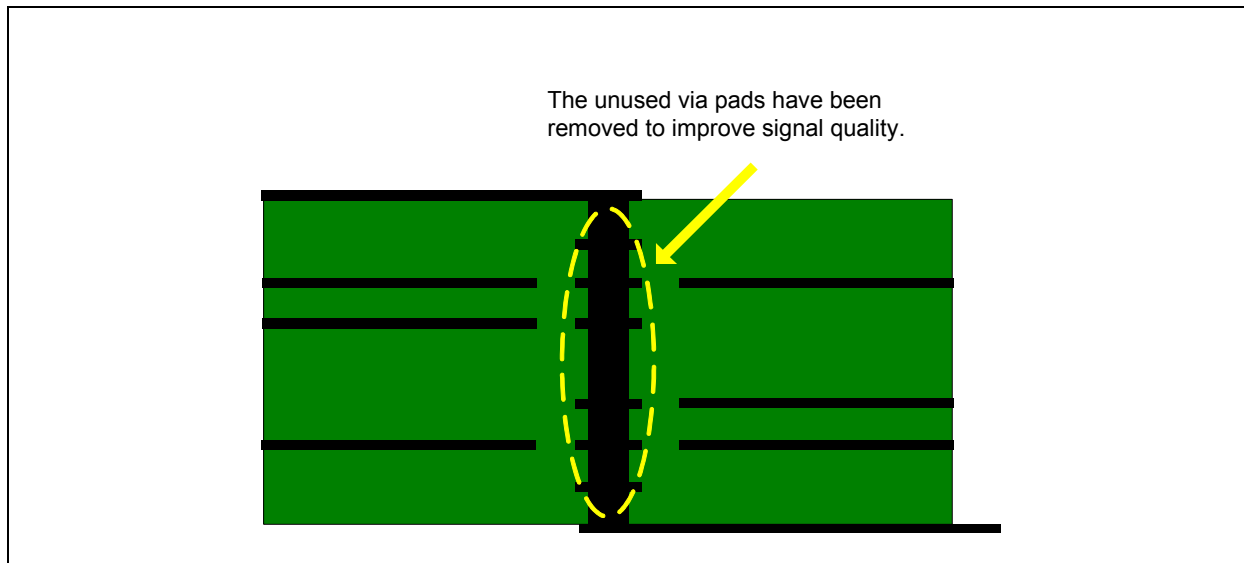
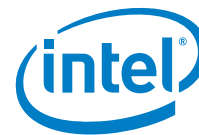


Figure 9-14 Undesirable: For Signal Vias to Have Pads on the Unused Metal Layers

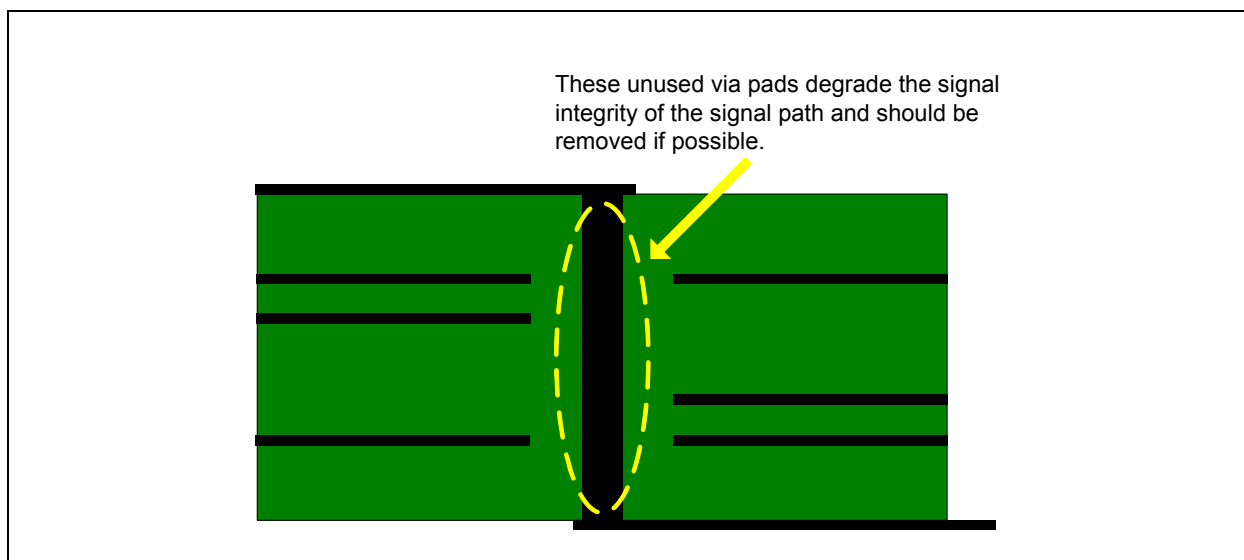


Figure 9-15 Signal Via Improved by Removing Unused Metal Layer Pads

On metal layers where signal vias need to have via pads, it is desirable to reduce capacitance between the signal vias and ground-plane layers. The anti-pad diameters should be up to 20 mils larger than the via pad diameters. See [Figure 9-16](#). Clearance between the pad and the surrounding metal should be ≥ 10 mils.

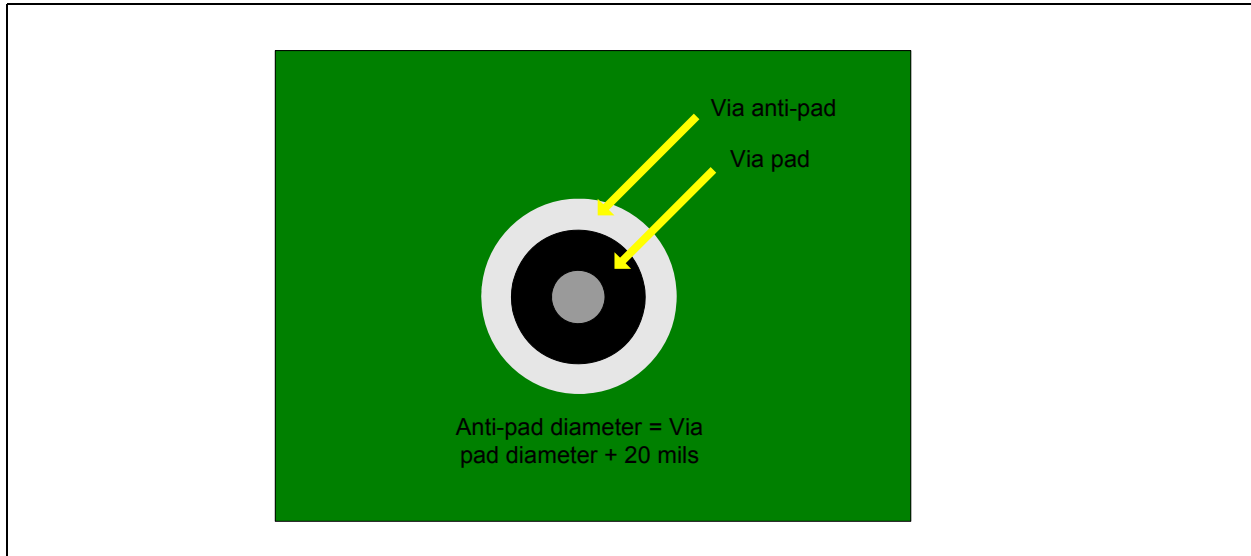


Figure 9-16 Increase Anti-Pad Diameter To Reduce Shunt Capacitance

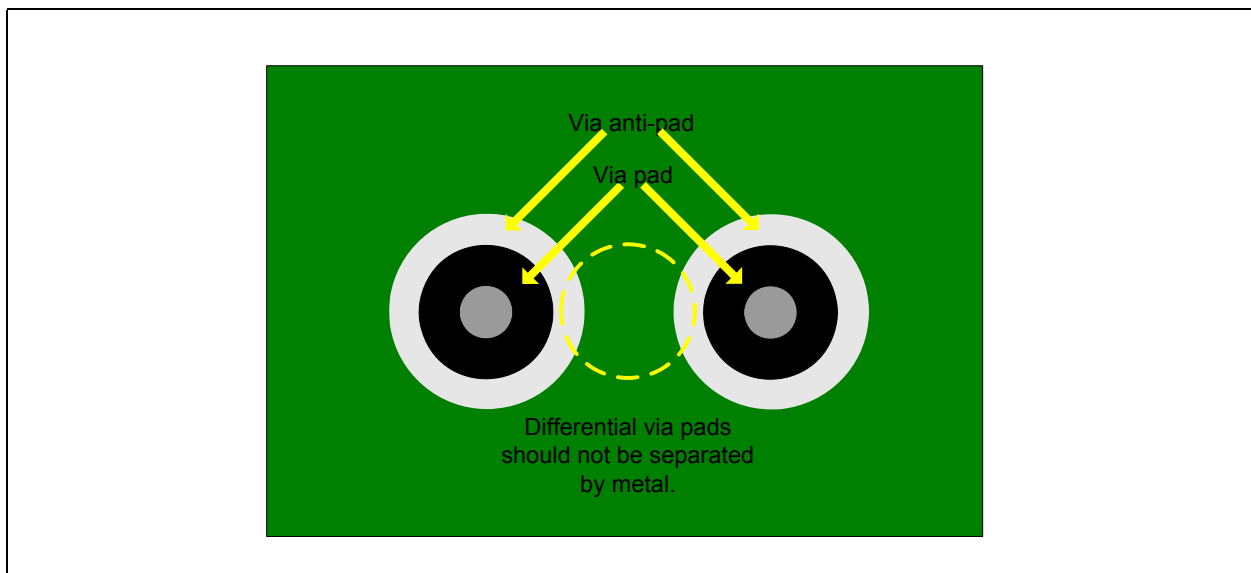


Figure 9-17 Differential Signal Via Pads Should Not Be Separated By Metal

Each time differential signal vias pass through a plane layer, within each differential pair, the anti-pads should overlap. See [Figure 9-18](#) and [Figure 9-19](#).

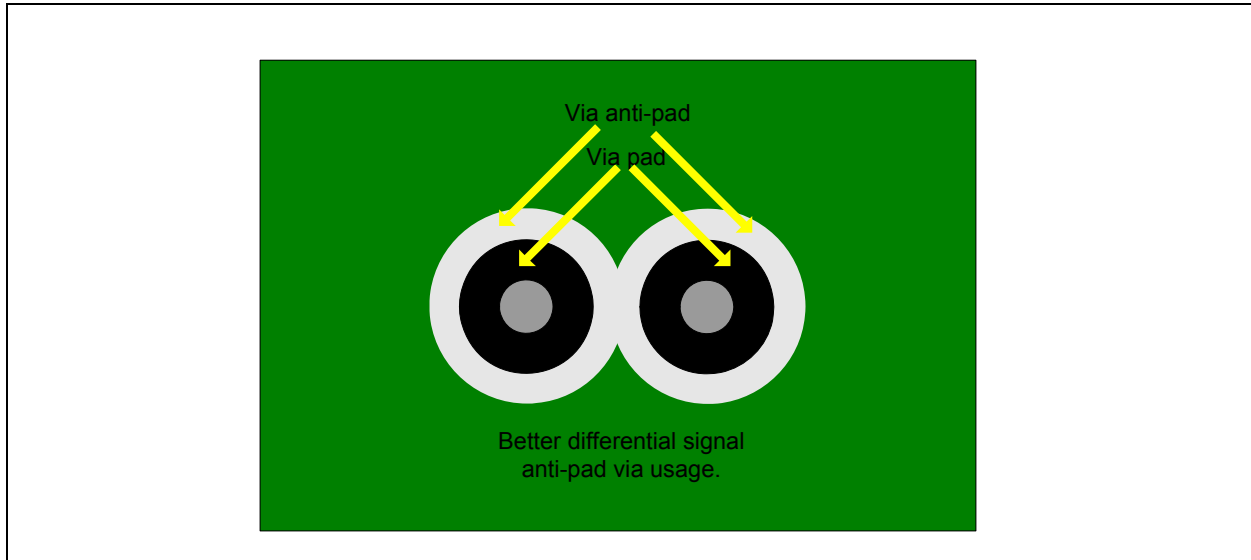


Figure 9-18 Better Differential Signals Via Anti-pads

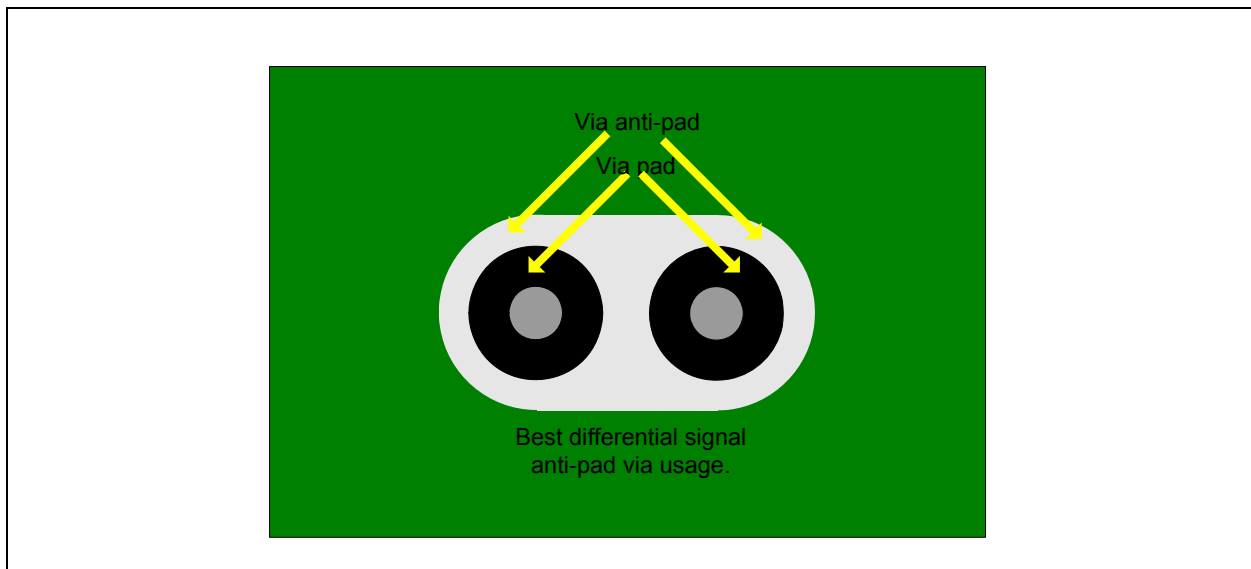


Figure 9-19 Best Differential Signals Via Anti-Pads



9.3.10 Recommended Simulations

10GBASE-T signaling frequencies have frequency content in the range of 800 MHz and below so relatively short stubs, small discontinuities, and fairly small in-pair trace length differences can cause an undesirable increase in bit errors. Before ordering PCBs, verify that:

- Planned 10GBASE-T signal trace routing on the PCB complies with the interconnect characteristics recommended in IEEE 802.3an.
- With sufficient advance notice, Intel engineers can provide assistance under these conditions:
 - Trace routing should be optimized prior to the next steps – request a layout review (must be willing to provide board stack-up information and the MDI traces CAD artwork).
 - After MDI traces have been optimized, if the IEEE recommended electrical characteristics are still not being met, then end-to-end MDI board channels S-parameter models should be extracted (preferably in Touchstone* S4p format) for additional investigative simulations by Intel signal integrity engineers. Please request the required S-parameter frequency range, step size, etc., before extracting Touchstone S-parameter models.

9.4 Bill Of Material (BOM)

Table 9-1 lists the BOM materials for all X557 LAN on Motherboard (LOM) designs.

Table 9-1. X557 LOMs

| Component | Manufacturer | Manufacturer Part Number | Quantity |
|-----------------------------|---|--|---|
| Crystal (X557-AT Only) | TXC* MMD* Rami*/Raltron* | 7A50020001 – 50 MHz V16DB1-50.000 MHz H130A-50.000-16-F-1010-TR-NS1 | 1 |
| LVDS Oscillator | TXC PERICOM* NDK* | BE50020001 PX5000010 7311S-DG-505P 50MIND3072A | 1 |
| Discrete Magnetic | Bel-Fuse* Pulse* | S558-10GB-10 H7137NL | 1 for X557-AT 2 for X557-AT2 4 for X557-AT4 |
| RJ45 | Lotes* Bel-Fuse | ABA-JKM-002-Y02/ABA-JKM-002-Y03 SS60300-010 (No LED) | 1 for X557-AT 2 for X557-AT2 4 for X557-AT4 |
| Integrated Magnetic (1 x 1) | Bel-Fuse Bel-Fuse Bel-Fuse Pulse Tyco* (TE) Delta* Foxconn* | G13-152T-038 G17-188T-038 (Light-pipe) G12-1JJT-038 JT4-1108HL 1840497-1 RJTGE1G4172J JFM5801J-710G-4F | 1 for X557-AT 2 for X557-AT2 4 for X557-AT4 |



| Component | Manufacturer | Manufacturer Part Number | Quantity |
|-----------------------------|--|--|----------------------------------|
| Integrated Magnetic (2 x 1) | Bel-Fuse Foxconn | G23-21YR-083E JFM58A3Y-T19G-4F | 1 for X557-AT2 2 for X557-AT4 |
| Integrated Magnetic (2 x 2) | Bel-Fuse | G18-48NE-083E | 1 for X557-AT4 |
| Flash (2.3V - 3.6V) | Atmel* MXIC* ¹ Micron* Adesto* | AT45DB041E MX25V4006E M25PX16 AT25SF041 | 1 1 1 1 |

1. Macronix International Co., Ltd.



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