

MAX12934/MAX12935

Two-Channel, Fast, Low-Power, 5kV_{RMS} Digital Isolators

General Description

The MAX12934/MAX12935 are the fastest, lowest power, 2-channel digital galvanic isolators on the market today, using Maxim's proprietary process technology. These devices transfer digital signals between circuits with different power domains while using as little as 0.65mW per channel at 1Mbps with a 1.8V supply.

The two channels of the MAX12935 transfer data in opposite directions, making the MAX12935 ideal for isolating the TX and RX lines of a transceiver. The two channels of the MAX12934 transfer data in the same direction.

The MAX12934/MAX12935 have an isolation rating of 5kV_{RMS} for 60 seconds. Both devices are available with a maximum data rate of either 25Mbps or 200Mbps and with outputs that are either default-high or default-low. The default is the state the output assumes when the input is not powered or if the input is open-circuit. See the [Ordering Information](#) for suffixes associated with each option. Independent 1.71V to 5.5V supplies on each side of the isolator also make the devices suitable for use as level translators.

The MAX12934/MAX12935 are available in a 16-pin, wide-body SOIC package. The package material has a minimum comparative tracking index (CTI) of 600V, which gives it a group 1 rating in creepage tables. All devices are rated for operation at ambient temperatures of -40°C to +125°C.

[Ordering Information](#) appears at end of data sheet.

Benefits and Features

- Robust Galvanic Isolation for Fast Digital Signals
 - 200 Mbps Data Rate
 - Withstands 5kV_{RMS} for 60s (VISO)
 - Continuously Withstands 848V_{RMS} (VIOWM)
 - Withstands ±10kV Surge Between GNDA and GNDB with 1.2/50μs Waveform
 - High CMTI (50kV/μs Typical)
- Low Power Consumption
 - 1.3mW per Channel at 2Mbps with V_{DD} = 3.3V
 - 3.3mW per Channel at 100Mbps with V_{DD} = 1.8V
- Options to Support a Broad Range of Applications
 - 2 Data Rates (25Mbps/200Mbps)
 - 2 Channel Direction Configurations
 - 2 Output Default States (High or Low)

Applications

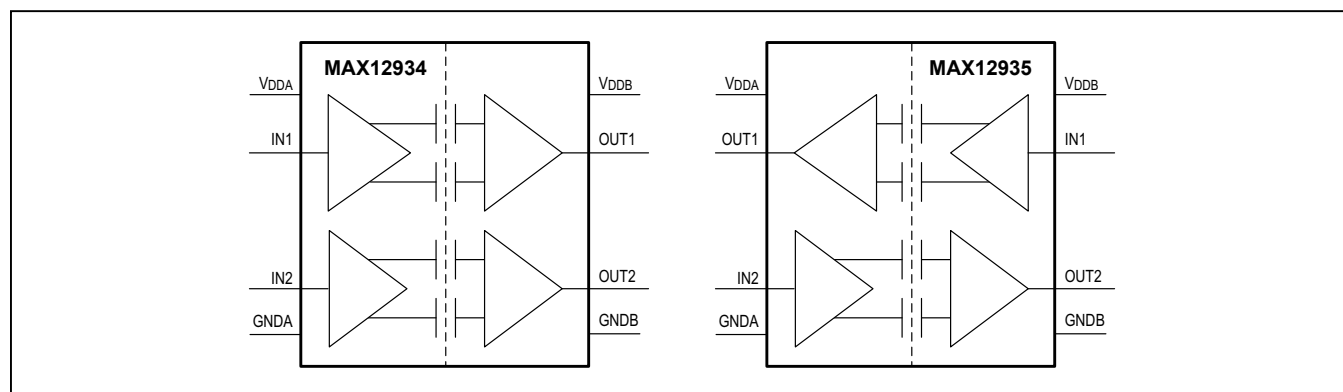
- Fieldbus Communications for Industrial Automation
- Isolated RS232, RS-485/RS-422, CAN
- General Isolation Application
- Battery Management
- Medical Systems

Safety Regulatory Approvals

(see [Safety Regulatory Approvals](#))

- UL According to UL1577
- cUL According to CSA Bulletin 5A

Functional Diagrams



Absolute Maximum Ratings

V _{DDA} to GNDA.....	-0.3V to +6V
V _{DDB} to GNDB.....	-0.3V to +6V
IN_ on Side A to GNDA.....	-0.3V to +6V
IN_ on Side B to GNDB.....	-0.3V to +6V
OUT_ on Side A to GNDA.....	-0.3V to (V _{DDA} + 0.3V)
OUT_ on Side B to GNDB.....	-0.3V to (V _{DDA} + 0.3V)
Short-Circuit Duration	
OUT_ on side A to GNDA,	
OUT_ on side B to GNDB.....	Continuous

Continuous Power Dissipation (T _A = +70°C)	
Wide SOIC (derate 14.1mW/°C above +70°C)	1126.8mW
Operating Temperature Range	-40°C to +125°C
Maximum Junction Temperature	+150°C
Storage Temperature Range	-60°C to +150°C
Soldering Temperature (reflow)	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

Wide SOIC

Junction-to-Ambient Thermal Resistance (θ _{JA})	71°C/W
Junction-to-Case Thermal Resistance (θ _{JC})	23°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

DC Electrical Characteristics

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, GNDA = GNDB, T_A = 25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage	V _{DDA}	Relative to GNDA	1.71		5.5	V
	V _{DDB}	Relative to GNDB	1.71		5.5	
Undervoltage-Lockout Threshold	V _{UVLO_}	V _{DD_} rising	1.5	1.6	1.66	V
Undervoltage-Lockout Threshold Hysteresis	V _{UVLO_HYST}			45		mV

DC Electrical Characteristics (continued)

($V_{DDA} - V_{GNDA} = 1.71V$ to $5.5V$, $V_{DDB} - V_{GNDB} = 1.71V$ to $5.5V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted. Typical values are at $V_{DDA} - V_{GNDA} = 3.3V$, $V_{DDB} - V_{GNDB} = 3.3V$, $G_NDA = G_NDB$, $T_A = 25^{\circ}C$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current (MAX12934_) (Note 3)	I_{DDA}	1MHz square wave, $C_L = 0pF$	$V_{DDA} = 5V$		0.32	0.58	mA
			$V_{DDA} = 3.3V$		0.31	0.54	
			$V_{DDA} = 2.5V$		0.3	0.53	
			$V_{DDA} = 1.8V$		0.29	0.39	
		12.5MHz square wave, $C_L = 0pF$	$V_{DDA} = 5V$		0.81	1.26	
			$V_{DDA} = 3.3V$		0.8	1.20	
			$V_{DDA} = 2.5V$		0.78	1.18	
			$V_{DDA} = 1.8V$		0.77	1.01	
		50MHz square wave, $C_L = 0pF$	$V_{DDA} = 5V$		2.15	3.00	
			$V_{DDA} = 3.3V$		2.09	2.91	
			$V_{DDA} = 2.5V$		2.06	2.88	
			$V_{DDA} = 1.8V$		2	2.62	
	I_{DDB}	1MHz square wave, $C_L = 0pF$	$V_{DDB} = 5V$		0.5	0.83	mA
			$V_{DDB} = 3.3V$		0.47	0.79	
			$V_{DDB} = 2.5V$		0.45	0.76	
			$V_{DDB} = 1.8V$		0.4	0.67	
		12.5MHz square wave, $C_L = 0pF$	$V_{DDB} = 5V$		1.37	1.83	
			$V_{DDB} = 3.3V$		1.02	1.40	
			$V_{DDB} = 2.5V$		0.87	1.22	
			$V_{DDB} = 1.8V$		0.71	1.00	
		50MHz square wave, $C_L = 0pF$	$V_{DDB} = 5V$		4.21	4.99	
			$V_{DDB} = 3.3V$		2.81	3.39	
			$V_{DDB} = 2.5V$		2.21	2.69	
			$V_{DDB} = 1.8V$		1.69	2.04	

DC Electrical Characteristics (continued)

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, G_{NDA} = G_{NDB}, T_A = 25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current (MAX12935_) (Note 3)	I _{DDA}	1MHz square wave, C _L = 0pF	V _{DDA} = 5V		0.42	0.70	mA
			V _{DDA} = 3.3V		0.39	0.67	
			V _{DDA} = 2.5V		0.38	0.64	
			V _{DDA} = 1.8V		0.36	0.56	
		12.5MHz square wave, C _L = 0pF	V _{DDA} = 5V		1.07	1.52	
			V _{DDA} = 3.3V		0.89	1.29	
			V _{DDA} = 2.5V		0.81	1.19	
			V _{DDA} = 1.8V		0.73	1.03	
		50MHz square wave, C _L = 0pF	V _{DDA} = 5V		3.06	3.87	
			V _{DDA} = 3.3V		2.37	3.06	
			V _{DDA} = 2.5V		2.08	2.72	
			V _{DDA} = 1.8V		1.82	2.33	
	I _{DDB}	1MHz square wave, C _L = 0pF	V _{DDB} = 5V		0.42	0.70	mA
			V _{DDB} = 3.3V		0.39	0.67	
			V _{DDB} = 2.5V		0.38	0.64	
			V _{DDB} = 1.8V		0.36	0.56	
		12.5MHz square wave, C _L = 0pF	V _{DDB} = 5V		1.07	1.52	
			V _{DDB} = 3.3V		0.89	1.29	
			V _{DDB} = 2.5V		0.81	1.19	
			V _{DDB} = 1.8V		0.73	1.03	
		50MHz square wave, C _L = 0pF	V _{DDB} = 5V		3.06	3.87	
			V _{DDB} = 3.3V		2.37	3.06	
			V _{DDB} = 2.5V		2.08	2.72	
			V _{DDB} = 1.8V		1.82	2.33	
LOGIC INPUTS AND OUTPUTS							
Input High Voltage	V _{IH}	2.25V ≤ V _{DD_} ≤ 5.5V		0.7 x V _{DD_}		V	
		1.71V ≤ V _{DD_} < 2.25V		0.75 x V _{DD_}			
Input Low Voltage	V _{IL}	2.25V ≤ V _{DD_} ≤ 5.5V		0.8		V	
		1.71V ≤ V _{DD_} < 2.25V		0.7			
Input Hysteresis	V _{HYS}	MAX1293_B/E		410		mV	
		MAX1293_C/F		80			
Input Pullup Current (Note 4)	I _{PU}	IN_, MAX1293_B/C		-10	-5	-1.5	μA
Input Pulldown Current (Note 4)	I _{PD}	IN_, MAX1293_E/F		1.5	5	10	μA
Input Capacitance	C _{IN}	IN_, f _{SW} = 1MHz		2			pF

DC Electrical Characteristics (continued)

($V_{DDA} - V_{GNDA} = 1.71V$ to $5.5V$, $V_{DDB} - V_{GNDB} = 1.71V$ to $5.5V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted. Typical values are at $V_{DDA} - V_{GNDA} = 3.3V$, $V_{DDB} - V_{GNDB} = 3.3V$, $GNDA = GNDB$, $T_A = 25^{\circ}C$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage High (Note 4)	V_{OH}	$I_{OUT} = 4mA$ source	$V_{DD_} - 0.4$			V
Output Voltage Low (Note 4)	V_{OL}	$I_{OUT} = 4mA$ sink			0.4	V

Dynamic Characteristics MAX1293_B/E

($V_{DDA} - V_{GNDA} = 1.71V$ to $5.5V$, $V_{DDB} - V_{GNDB} = 1.71V$ to $5.5V$, $C_L = 15pF$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted. Typical values are at $V_{DDA} - V_{GNDA} = 3.3V$, $V_{DDB} - V_{GNDB} = 3.3V$, $GNDA = GNDB$, $T_A = 25^{\circ}C$, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Common-Mode Transient Immunity	CMTI	$IN_ = GND_$ or $V_{DD_}$ (Note 5)		50		kV/ μs
Maximum Data Rate	DR_{MAX}		25			Mbps
Minimum Pulse Width	PW_{MIN}				40	ns
Glitch Rejection			10	17	29	ns
Propagation Delay (Figure 1)	t_{PLH}	$4.5V \leq V_{DD_} \leq 5.5V$	17.4	23.9	32.5	ns
		$3.0V \leq V_{DD_} \leq 3.6V$	17.6	24.4	33.7	
		$2.25V \leq V_{DD_} \leq 2.75V$	18.3	25.8	36.7	
		$1.71V \leq V_{DD_} \leq 1.89V$	20.7	29.6	43.5	
	t_{PHL}	$4.5V \leq V_{DD_} \leq 5.5V$	16.9	23.4	33.6	
		$3.0V \leq V_{DD_} \leq 3.6V$	17.2	24.2	35.1	
		$2.25V \leq V_{DD_} \leq 2.75V$	17.8	25.4	38.2	
		$1.71V \leq V_{DD_} \leq 1.89V$	19.8	29.3	45.8	
Pulse Width Distortion	PWD			0.4	4	ns
Propagation Delay Skew Part-to-Part (same channel)	t_{SPLH}	$4.5V \leq V_{DD_} \leq 5.5V$			15.1	ns
		$3.0V \leq V_{DD_} \leq 3.6V$			15	
		$2.25V \leq V_{DD_} \leq 2.75V$			15.4	
		$1.71V \leq V_{DD_} \leq 1.89V$			20.5	
	t_{SPHL}	$4.5V \leq V_{DD_} \leq 5.5V$			13.9	
		$3.0V \leq V_{DD_} \leq 3.6V$			14.2	
		$2.25V \leq V_{DD_} \leq 2.75V$			16	
		$1.71V \leq V_{DD_} \leq 1.89V$			21.8	
Propagation Delay Skew Channel-to-Channel (Same Direction) MAX12934 only	t_{SCSLH}				2	ns
	t_{SCSHL}				2	

Dynamic Characteristics MAX1293_B/E (continued)

($V_{DDA} - V_{GNDA} = 1.71V$ to $5.5V$, $V_{DDB} - V_{GNDB} = 1.71V$ to $5.5V$, $C_L = 15pF$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted. Typical values are at $V_{DDA} - V_{GNDA} = 3.3V$, $V_{DDB} - V_{GNDB} = 3.3V$, $GNDA = GNDB$, $T_A = 25^{\circ}C$, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Skew Channel-to-Channel (Opposite Direction) MAX12935 Only	t_{SCOLH}				2	ns
	t_{SCOHL}				2	
Peak Eye Diagram Jitter	$T_{JIT(PK)}$	25Mbps		250		ps
Rise Time	t_R	$4.5V \leq V_{DD_} \leq 5.5V$			1.6	ns
		$3.0V \leq V_{DD_} \leq 3.6V$			2.2	
		$2.25V \leq V_{DD_} \leq 2.75V$			3	
		$1.71V \leq V_{DD_} \leq 1.89V$			4.5	
Fall Time	t_F	$4.5V \leq V_{DD_} \leq 5.5V$			1.4	ns
		$3.0V \leq V_{DD_} \leq 3.6V$			2	
		$2.25V \leq V_{DD_} \leq 2.75V$			2.8	
		$1.71V \leq V_{DD_} \leq 1.89V$			5.1	

Dynamic Characteristics MAX1293_C/F

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, G_{NDA} = G_{NDB}, T_A = 25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Common-Mode Transient Immunity	CMTI	IN ₋ = GND ₋ or V _{DD-} (Note 5)		50		kV/μs
Maximum Data Rate	DR _{MAX}	2.25V ≤ V _{DD-} ≤ 5.5V	200			Mbps
		1.71V ≤ V _{DD-} ≤ 1.89V	150			
Minimum Pulse Width	PW _{MIN}	2.25V ≤ V _{DD-} ≤ 5.5V			5	ns
		1.71V ≤ V _{DD-} ≤ 1.89V			6.67	
Propagation Delay (Figure 1)	t _{PLH}	4.5V ≤ V _{DD-} ≤ 5.5V	4.1	5.4	9.2	ns
		3.0V ≤ V _{DD-} ≤ 3.6V	4.2	5.9	10.2	
		2.25V ≤ V _{DD-} ≤ 2.75V	4.9	7.1	13.4	
		1.71V ≤ V _{DD-} ≤ 1.89V	7.1	10.9	20.3	
	t _{PHL}	4.5V ≤ V _{DD-} ≤ 5.5V	4.3	5.6	9.4	
		3.0V ≤ V _{DD-} ≤ 3.6V	4.4	6.2	10.5	
		2.25V ≤ V _{DD-} ≤ 2.75V	5.1	7.3	14.1	
		1.71V ≤ V _{DD-} ≤ 1.89V	7.2	10.9	21.7	
Pulse Width Distortion	PWD			0.3	2	ns
Propagation Delay Skew Part-to-Part (Same Channel)	t _{SPLH}	4.5V ≤ V _{DD-} ≤ 5.5V			3.7	ns
		3.0V ≤ V _{DD-} ≤ 3.6V			4.3	
		2.25V ≤ V _{DD-} ≤ 2.75V			6	
		1.71V ≤ V _{DD-} ≤ 1.89V			10.3	
	t _{SPHL}	4.5V ≤ V _{DD-} ≤ 5.5V			3.8	
		3.0V ≤ V _{DD-} ≤ 3.6V			4.7	
		2.25V ≤ V _{DD-} ≤ 2.75V			6.5	
		1.71V ≤ V _{DD-} ≤ 1.89V			11.5	
Propagation Delay Skew Channel-to-Channel (Same Direction) MAX12934 Only	t _{SCSLH}				2	ns
	t _{SCSHL}				2	
Propagation Delay Skew Channel-to-Channel (Opposite Direction) MAX12935 Only	t _{SCOLH}				2	ns
	t _{SCOHL}				2	
Peak Eye Diagram Jitter	T _{JIT(PK)}	200Mbps		90		ps
Clock Jitter RMS	T _{JCLK(RMS)}	500kHz Clock Input Rising/Falling Edges		6.5		ps

Dynamic Characteristics MAX1293_C/F (continued)

($V_{DDA} - V_{GNDA} = 1.71V$ to $5.5V$, $V_{DDB} - V_{GNDB} = 1.71V$ to $5.5V$, $C_L = 15pF$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted. Typical values are at $V_{DDA} - V_{GNDA} = 3.3V$, $V_{DDB} - V_{GNDB} = 3.3V$, $GNDA = GNDB$, $T_A = 25^{\circ}C$, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time	t_R	$4.5V \leq V_{DD_} \leq 5.5V$			1.6	ns
		$3.0V \leq V_{DD_} \leq 3.6V$			2.2	
		$2.25V \leq V_{DD_} \leq 2.75V$			3	
		$1.71V \leq V_{DD_} \leq 1.89V$			4.5	
Fall Time	t_F	$4.5V \leq V_{DD_} \leq 5.5V$			1.4	ns
		$3.0V \leq V_{DD_} \leq 3.6V$			2	
		$2.25V \leq V_{DD_} \leq 2.75V$			2.8	
		$1.71V \leq V_{DD_} \leq 1.89V$			5.1	

Note 2: All devices are 100% production tested at $T_A = +25^{\circ}C$. Specifications over temperature are guaranteed by design.

Note 3: Not production tested. Guaranteed by design and characterization.

Note 4: All currents into the device are positive. All currents out of the device are negative. All voltages are referenced to their respective ground (GNDA or GNDB), unless otherwise noted.

Note 5: CMTI is the maximum sustainable common-mode voltage slew rate while maintaining the correct output. CMTI applies to both rising and falling common-mode voltage edges. Tested with the transient generator connected between GNDA and GNDB ($V_{CM} = 1000V$).

ESD Protection

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ESD		Human Body Model, all pins		± 3		kV

Safety Regulatory Approvals

UL
The MAX12934–MAX12935 wide-body SOIC are certified under UL1577. For more details, refer to file E351759.
Rated up to 5000V _{RMS} isolation voltage for single protection.
cUL (Equivalent to CSA notice 5A)
The MAX12934/MAX12935 wide-body SOIC are certified up to 5000V _{RMS} for single protection. For more details, refer to file E351759.

Table 1. Insulation Characteristics

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Partial Discharge Test Voltage	V _{PR}	Method B1 = V _{IORM} × 1.875 (t = 1s, partial discharge < 5pC)	2250	V _P
Maximum Repetitive Peak Isolation Voltage	V _{IORM}	(Note 6)	1200	V _P
Maximum Working Isolation Voltage	V _{IOWM}	Continuous RMS voltage (Note 6)	848	V _{RMS}
Maximum Transient Isolation Voltage	V _{IOTM}	t = 1s	8400	V _P
Maximum Withstand Isolation Voltage	V _{ISO}	f _{SW} = 60Hz, duration = 60s (Note 7)	5000	V _{RMS}
Maximum Surge Isolation Voltage	V _{IOSM}	Basic Insulation, 1.2/50μs pulse per IEC61000-4-5	10	kV
Insulation Resistance	R _S	V _{IO} = 500V	>10 ⁹	Ω
Barrier Capacitance Side A to Side B	C _{IO}	f _{SW} = 1MHz (Note 8)	2	pF
Minimum Creepage Distance	CPG		8	mm
Minimum Clearance Distance	CLR		8	mm
Internal Clearance		Distance through insulation	0.015	mm
Comparative Tracking Index	CTI	Material Group I (IEC60112)	>600	
Climate Category			40/125/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	

Note 6: V_{ISO}, V_{IOWM} and V_{IORM} are defined by the IEC 60747-5-5 standard.

Note 7: Product is qualified at V_{ISO} for 60s and 100% production tested at 120% of V_{ISO} for 1s.

Note 8: Capacitance is measured with all pins on side A and side B tied together.

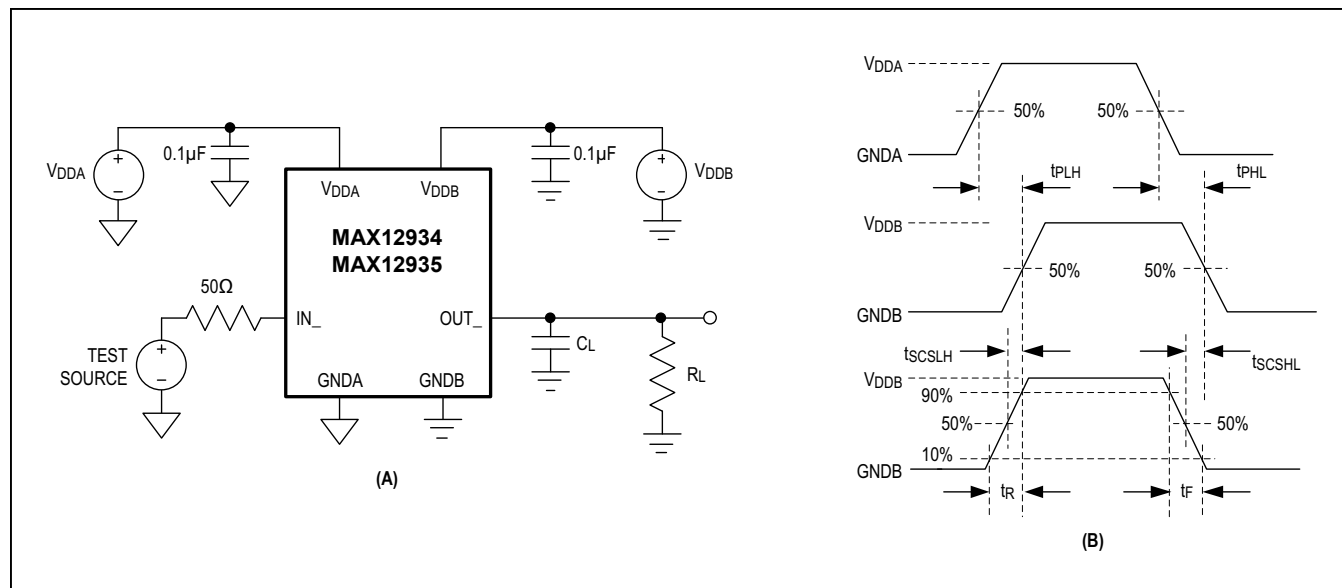
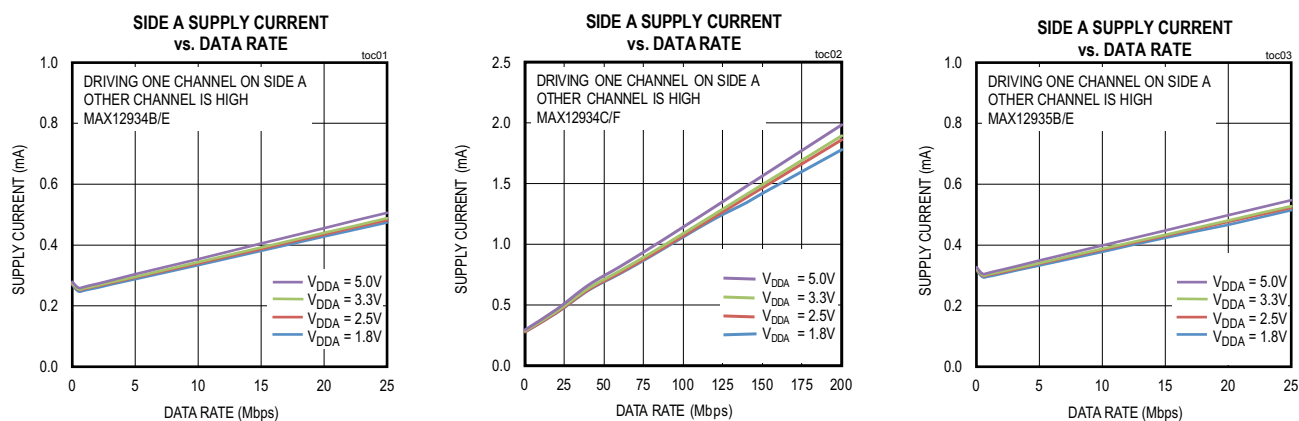


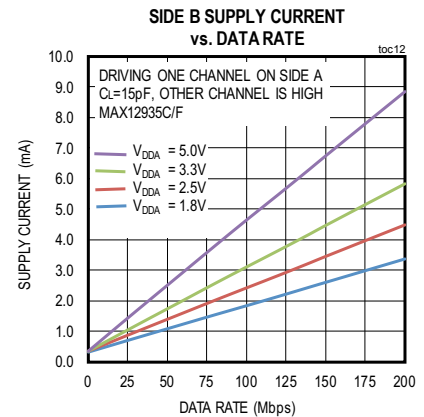
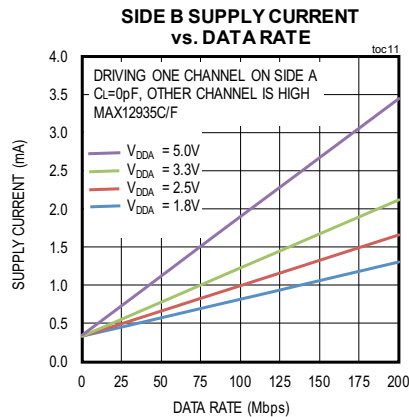
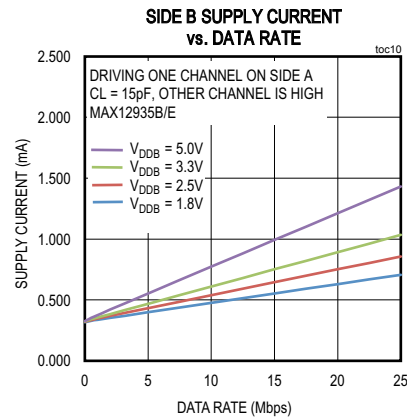
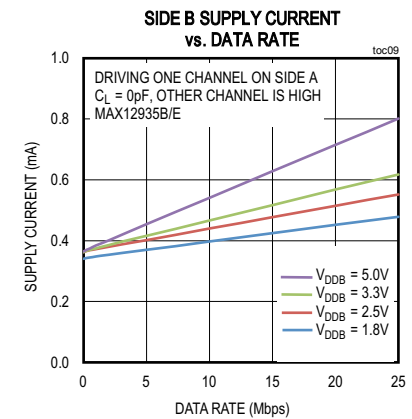
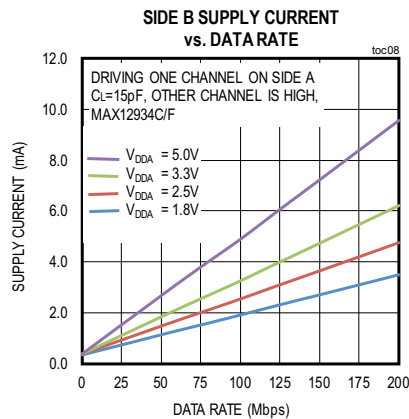
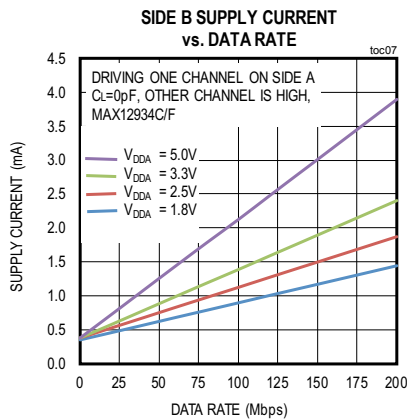
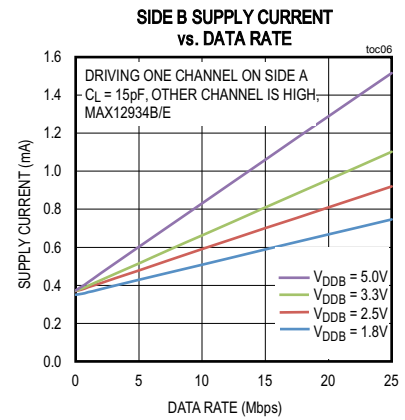
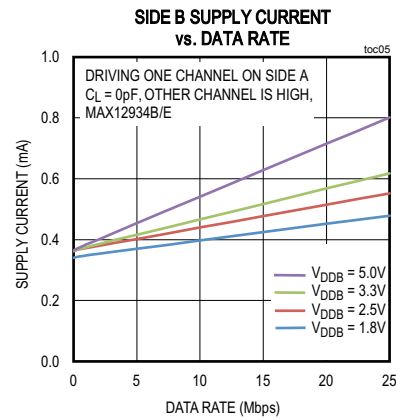
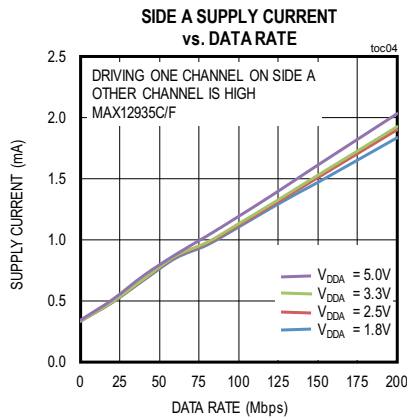
Figure 1. Test Circuit (A) and Timing Diagram (B)

Typical Operating Characteristics

(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, G_{NDA} = G_{NDB}, T_A = +25°C, unless otherwise noted.)

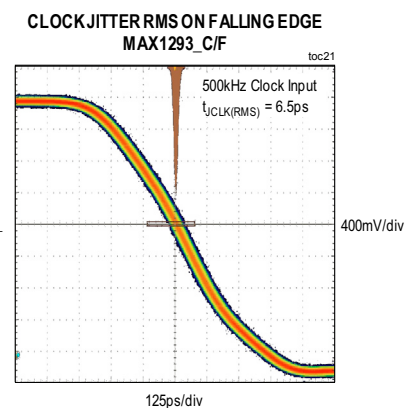
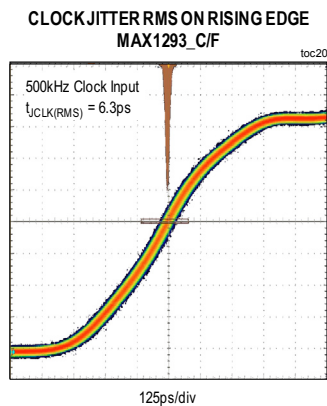
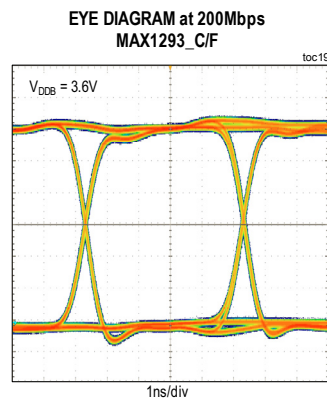
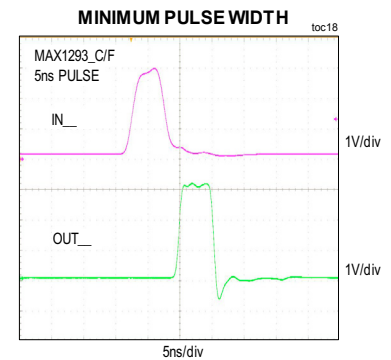
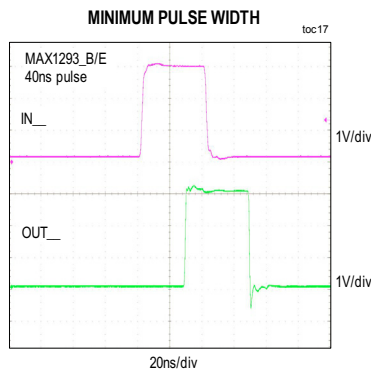
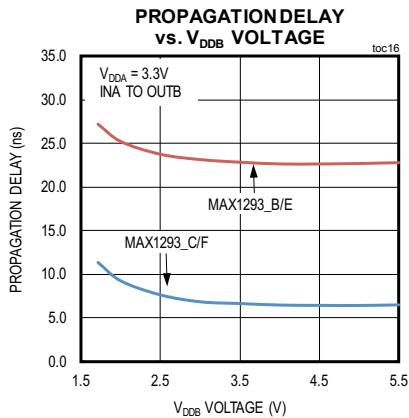
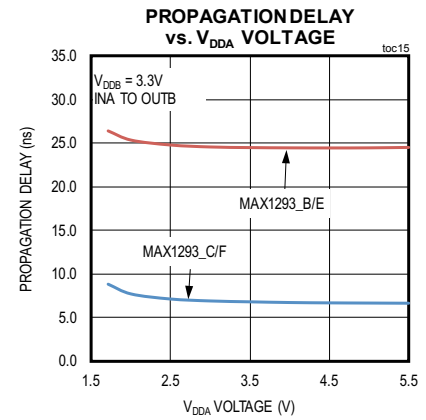
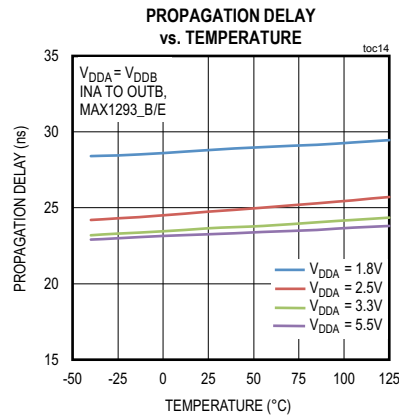
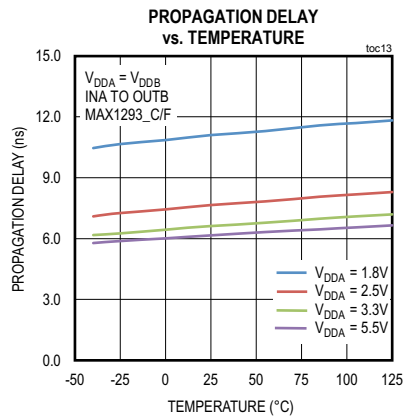


Typical Operating Characteristics (continued)

(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, G_{NDA} = G_{NDB}, T_A = +25°C, unless otherwise noted.)

Typical Operating Characteristics (continued)

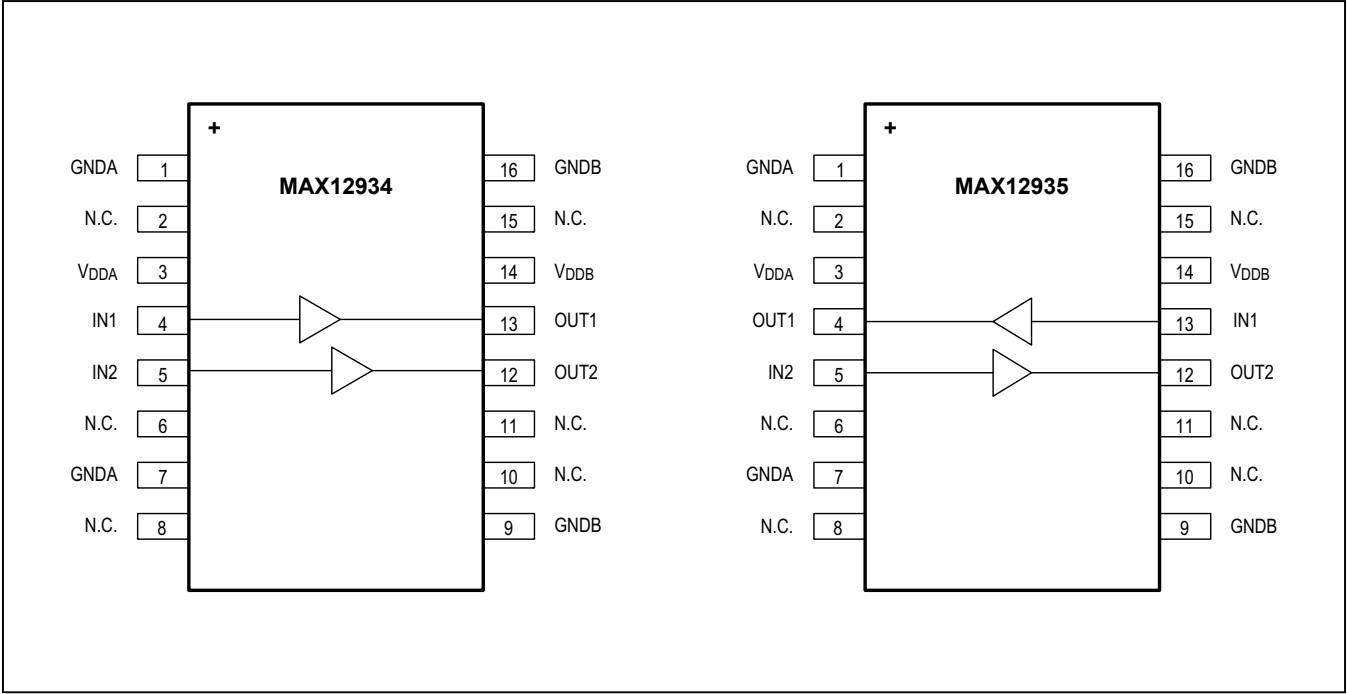
($V_{DDA} - V_{GNDA} = +3.3V$, $V_{DDB} - V_{GNDB} = +3.3V$, $GNDA = GNDB$, $T_A = +25^\circ C$, unless otherwise noted.)



MAX12934/MAX12935

Two-Channel, Fast, Low-Power,
5kV_{RMS} Digital Isolators

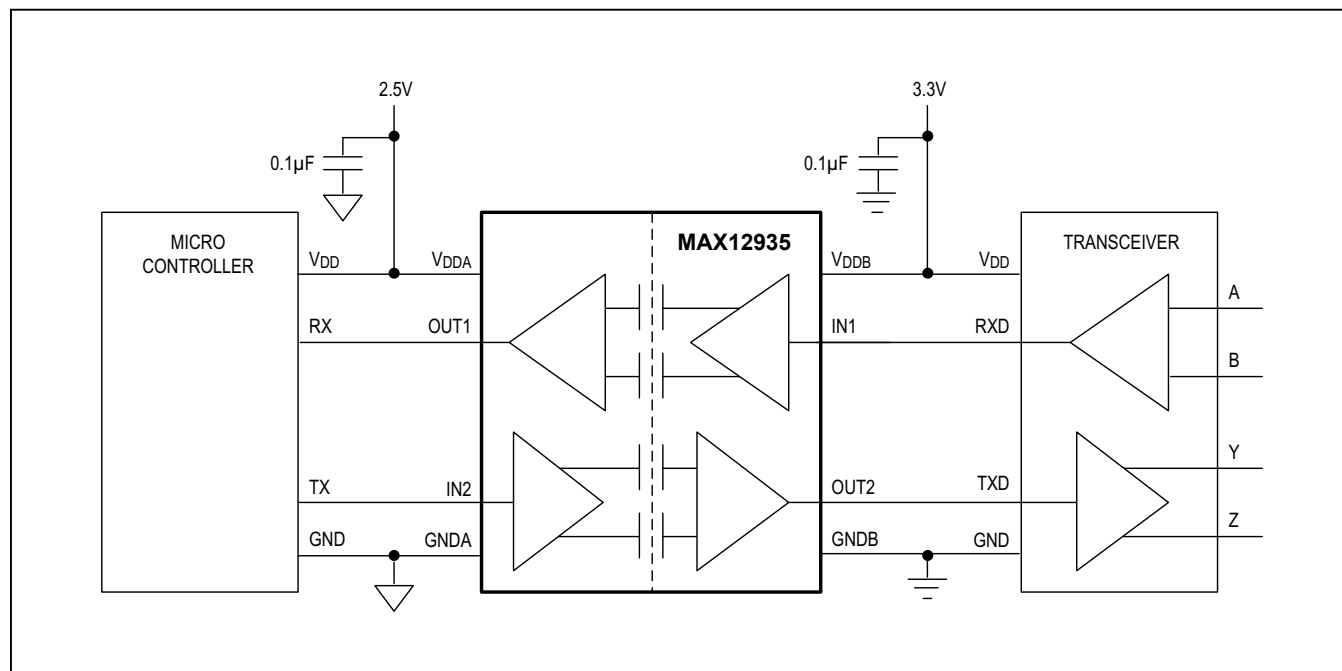
Pin Configurations



Pin Description

PIN		NAME	FUNCTION	REFERENCE
MAX12934	MAX12935			
3	3	V _{DDA}	Power Supply for side A. Bypass V _{DDA} with a 0.1μF ceramic capacitor to GNDA.	GNDA
4	—	IN1	Logic input for channel 1	GNDA
—	4	OUT1	Logic output of channel 1	GNDA
5	5	IN2	Logic input for channel 2	GNDA
1, 7	1, 7	GNDA	Ground reference for side A	—
9, 16	9, 16	GNDB	Ground reference for side B	—
12	12	OUT2	Logic output of channel 2	GNDB
13	—	OUT1	Logic output of channel 1	GNDB
—	13	IN1	Logic input for channel 1	GNDB
14	14	V _{ddb}	Power Supply for side B. Bypass V _{ddb} with a 0.1μF ceramic capacitor to GNDB.	GNDB
2, 6, 8, 10, 11, 15	2, 6, 8, 10, 11, 15	N.C.	Not internally connected	—

Typical Operating Circuit



Detailed Description

The MAX12934/MAX12935 are a family of 2-channel digital isolators. The MAX12934 transfers digital signals between circuits with different power domain in one direction, which is convenient for applications such as digital I/O. The MAX12935 transfers digital signals in opposite directions, which is necessary for isolated RS-485 or other UART applications.

Devices are available in the 16-pin wide body SOIC package and are rated for up to 5kV_{RMS} isolation voltage for 60 seconds. This family of digital isolators offers low-power operation, high electromagnetic interference (EMI) immunity, and stable temperature performance through Maxim's proprietary process technology. The devices isolate different ground domains and block high-voltage/high-current transients from sensitive or human interface circuitry.

Devices are available with data rates from DC to 25Mbps (B/E versions) or 200Mbps (C/F versions). Each device can be ordered with default-high or default-low outputs. The default is the state the output assumes when the input is not powered or if the input is open circuit.

The devices have two supply inputs (V_{DDA} and V_{ddb}) that independently set the logic levels on either side of device. V_{DDA} and V_{ddb} are referenced to $GNDA$ and $GNDB$, respectively. The MAX12934/MAX12935 family also features a refresh circuit to ensure output accuracy when an input remains in the same state indefinitely.

Digital Isolation

The device family provides galvanic isolation for digital signals that are transmitted between two ground domains. The devices withstand differences of up to 5kV_{RMS} for up to 60 seconds, and up to 1200V_{PEAK} of continuous isolation.

Level-Shifting

The wide supply voltage range of both V_{DDA} and V_{ddb} allows the MAX12934/MAX12935 family to be used for level translation in addition to isolation. V_{DDA} and V_{ddb} can be independently set to any voltage from 1.71V to 5.5V. The supply voltage sets the logic level on the corresponding side of the isolator.

Unidirectional Channels

Each channel of the MAX12934/MAX12935 is unidirectional; it only passes data in one direction, as indicated in the functional diagram. Each device features two unidirectional channels that operate independently with guaranteed data rates from DC up to 25Mbps (B/E versions), or DC to 200Mbps (C/F versions). The output driver of each channel is push-pull, eliminating the need for pullup resistors. The outputs are able to drive both TTL and CMOS logic inputs.

Startup and Undervoltage Lockout

The V_{DDA} and V_{ddb} supplies are both internally monitored for undervoltage conditions. Undervoltage events can occur during power-up, power-down, or during normal operation due to a sagging supply voltage. When an undervoltage condition is detected on either supply, all outputs go to their default states regardless of the state of the inputs (Table 2). Figure 2 through Figure 5 show the behavior of the outputs during power-up and power-down.

Table 2. Output Behavior During Undervoltage Conditions

V _{IN_}	V _{VDDA}	V _{Vddb}	V _{OUTA_}	V _{OUTB_}
1	Powered	Powered	1	1
0	Powered	Powered	0	0
X	Undervoltage	Powered	Default	Default
X	Powered	Undervoltage	Default	Default

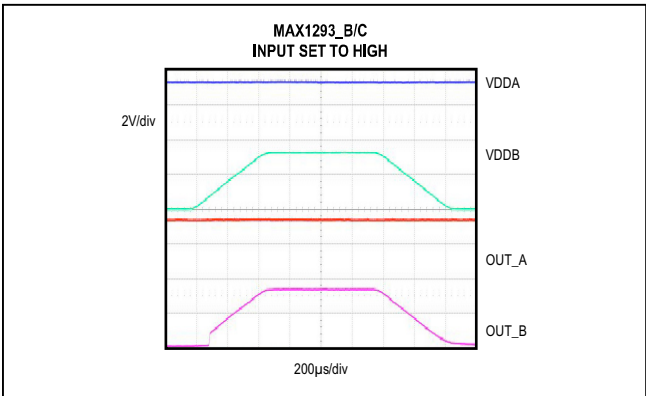


Figure 2. Undervoltage Lockout Behavior (MAX1293_B/C High)

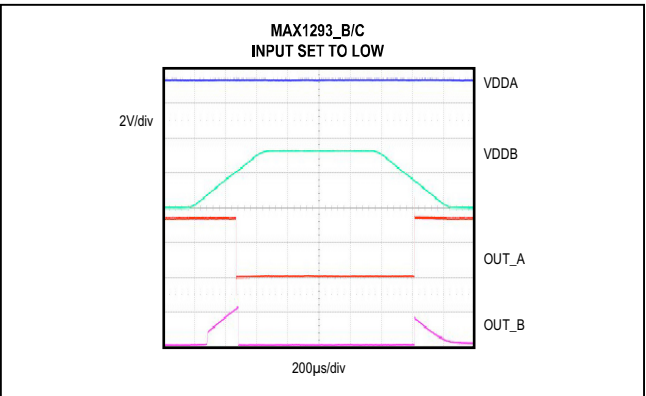


Figure 3. Undervoltage Lockout Behavior (MAX1293_B/C Low)

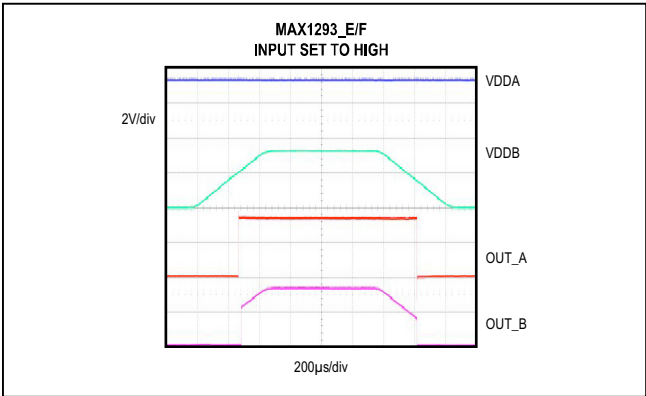


Figure 4. Undervoltage Lockout Behavior (MAX1293_E/F High)

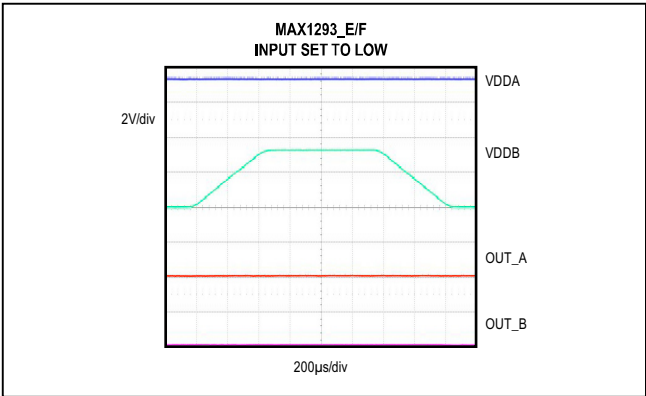


Figure 5. Undervoltage Lockout Behavior (MAX1293_E/F Low)

Application Information

Power-Supply Sequencing

The MAX12934/MAX12935 do not require special power supply sequencing. The logic levels are set independently on either side by V_{DDA} and V_{DDB} . Each supply can be present over the entire specified range regardless of the level or presence of the other supply.

Power-Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass V_{DDA} and V_{DDB} with 0.1μF low-ESR ceramic capacitors to GNDA and GNDB, respectively. Place the bypass capacitors as close to the power supply input pins as possible.

Layout Considerations

The PCB designer should follow some critical recommendation in order to get the best performance from the design.

- Keep the input/output traces as short as possible. Avoid using vias to make low-inductance paths for the signals.
- Have a solid ground plane underneath the high-speed signal layer.
- Keep the area underneath the MAX12934/MAX12935 free from ground and signal planes. Any galvanic or metallic connection between the field-side and logic-side defeats the isolation.

Calculating Power Dissipation

The required current for a given supply (V_{DDA} or V_{DDB}) can be estimated by summing the current required for each channel. The supply current for a channel depends on whether the channel is an input or an output, the channel's data rate, and the capacitive or resistive load if it is an output. The typical current for an input or output at any data rate can be estimated from the graphs in [Figure 6](#) and [Figure 7](#). Please note that the data in [Figure 6](#) and [Figure 7](#) are extrapolated from the supply current measurements in a typical operating condition.

The total current for a single channel is the sum of the “no load” current (shown in [Figure 6](#) and [Figure 7](#)) which is a function of Voltage and Data Rate, and the “load current” which depends upon the type of load. Current into a capacitive load is a function of the load capacitance, the switching frequency, and the supply voltage.

$$I_{CL} = C_L \times f_{SW} \times V_{DD}$$

where

I_{CL} is the current required to drive the capacitive load.

C_L is the load capacitance on the isolator's output pin.

f_{SW} is the switching frequency (bits per second/2).

V_{DD} is the supply voltage on the output side of the isolator.

Current into a resistive load depends on the load resistance, the supply voltage and the average duty cycle of the data waveform. The DC load current can be conservatively estimated by assuming the output is always high.

$$I_{RL} = V_{DD} \div R_L$$

where

I_{RL} is the current required to drive the resistive load.

V_{DD} is the supply voltage on the output side of the isolator.

R_L is the load resistance on the isolator's output pin.

Example (shown in [Figure 8](#)): A MAX12935F is operating with $V_{DDA} = 2.5V$, $V_{DDB} = 3.3V$, channel 1 operating at 100Mbps with a 15pF capacitive load, and channel 2 operating at 20Mbps with a 10pF capacitive load. Refer to [Table 3](#) and [Table 4](#) for V_{DDA} and V_{DDB} supply current calculation worksheets.

V_{DDA} must supply:

Channel 1 is an output channel operating at 2.5V and 100Mbps, consuming 1.02mA, estimated from [Figure 7](#). Channel 2 is an input channel operating at 2.5V and 20Mbps, consuming 0.33mA, estimated from [Figure 6](#). I_{CL} on channel 1 for 15pF capacitor at 2.5V and 100Mbps is 1.875mA.

Total current for side A = 1.02 + 0.33 + 1.875 = 3.225mA, typical

V_{DDB} must supply:

Channel 1 is an input channel operating at 3.3V and 100Mbps, consuming 1.13mA, estimated from [Figure 6](#). Channel 2 is an output channel operating at 3.3V and 20Mbps, consuming 0.42mA, estimated from [Figure 7](#). I_{CL} on channel 2 for 10pF capacitor at 3.3V and 20Mbps is 0.33mA.

Total current for side B = 1.13 + 0.42 + 0.33 = 1.88mA, typical

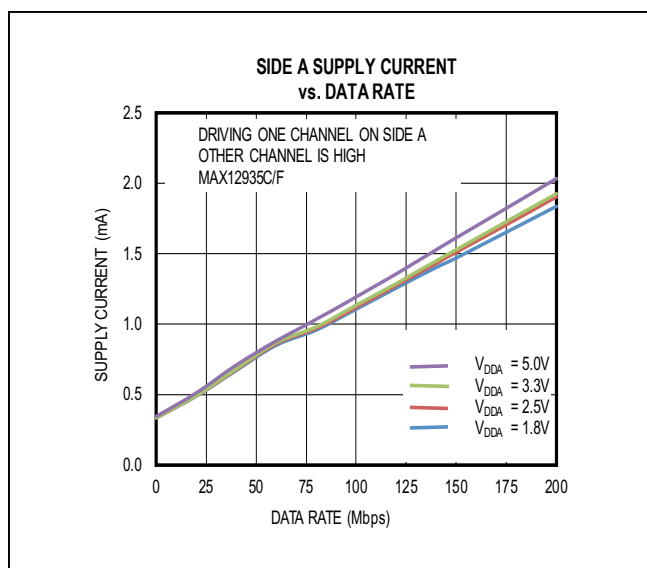


Figure 6. Supply Current per Input Channel Versus Data Rate

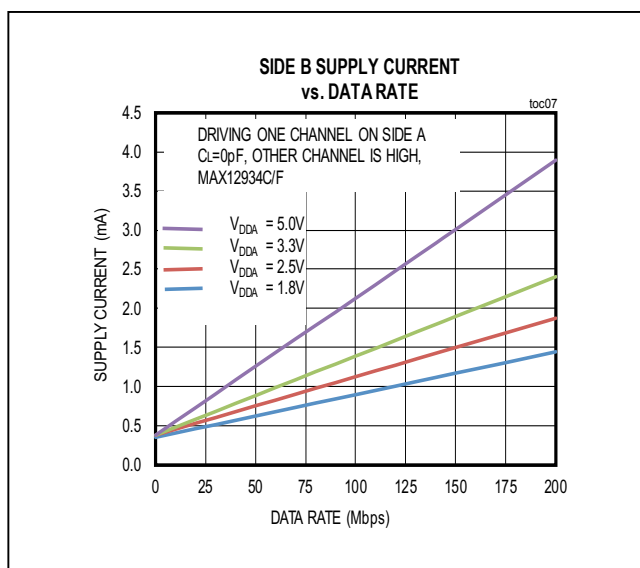


Figure 7. Supply Current per Output Channel Versus Data Rate

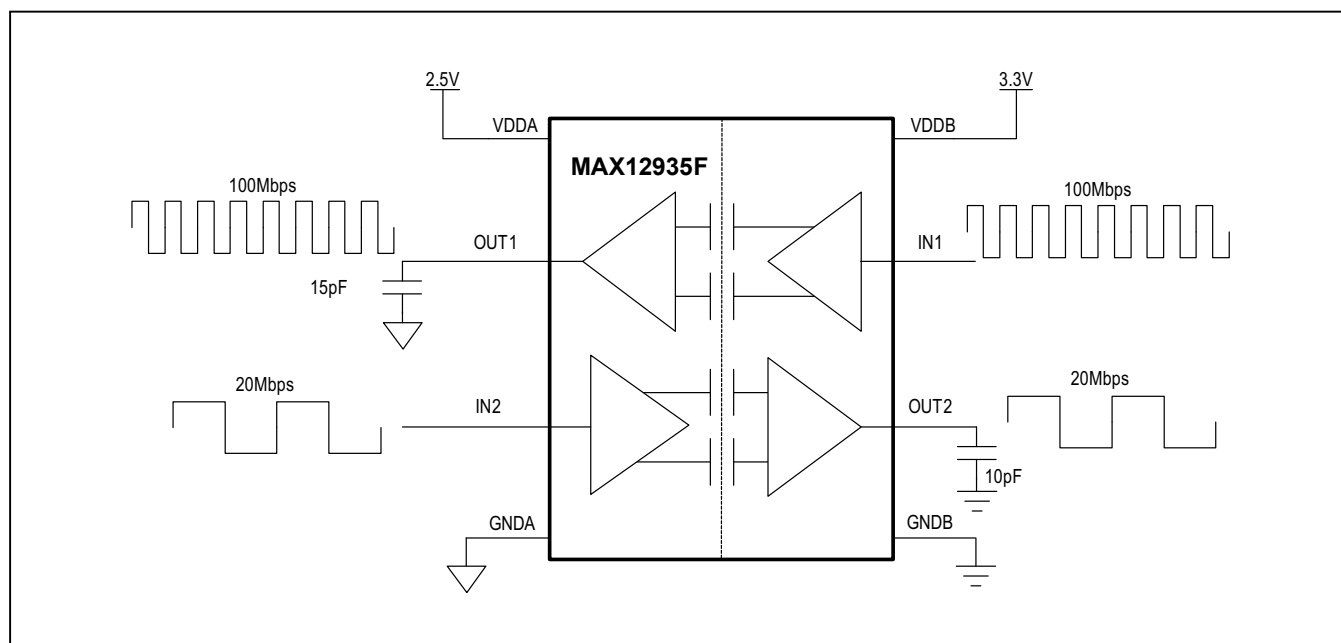


Figure 8. Example Circuit for Supply Current Calculation

Table 3. Side A Supply Current Calculation Worksheet

SIDE A		V _{DDA} = 2.5V				
CHANNEL	IN/OUT	FREQUENCY (Mbps)	LOAD TYPE	LOAD	“NO LOAD” CURRENT (mA)	LOAD CURRENT (mA)
1	OUT	100	Capacitive	15pF	1.02	2.5V x 50MHz x 15pF = 1.875mA
2	IN	20			0.33	
Total:					3.225mA	

Table 4. Side B Supply Current Calculation Worksheet

SIDE B		V _{ddb} = 3.3V				
CHANNEL	IN/OUT	FREQUENCY (Mbps)	LOAD TYPE	LOAD	“NO LOAD” CURRENT (mA)	LOAD CURRENT (mA)
1	IN	100			1.13	
2	OUT	20	Capacitive	10pF	0.42	3.3V x 10MHz x 10pF = 0.33mA
Total:					1.88mA	

Ordering Information

PART	CHANNEL CONFIGURATION	DATA RATE (Mbps)	DEFAULT OUTPUT	ISOLATION VOLTAGE (KV _{RMS})	TEMP RANGE	PIN-PACKAGE
MAX12934 BAWE+*	2/0	25	High	5	-40°C to 125°C	16 Wide SOIC
MAX12934CAWE+*	2/0	200	High	5	-40°C to 125°C	16 Wide SOIC
MAX12934EAW+*	2/0	25	Low	5	-40°C to 125°C	16 Wide SOIC
MAX12934FAWE+*	2/0	200	Low	5	-40°C to 125°C	16 Wide SOIC
MAX12935 BAWE+	1/1	25	High	5	-40°C to 125°C	16 Wide SOIC
MAX12935CAWE+*	1/1	200	High	5	-40°C to 125°C	16 Wide SOIC
MAX12935EAW+*	1/1	25	Low	5	-40°C to 125°C	16 Wide SOIC
MAX12935FAWE+*	1/1	200	Low	5	-40°C to 125°C	16 Wide SOIC

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 Wide SOIC	W16MS-11	21-0042	90-0107

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/17	Initial release	—

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