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FDC602P

P-Channel 2.5V PowerTrench^O Specified MOSFET

General Description

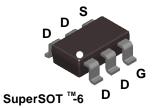
This P-Channel 2.5V specified MOSFET uses a rugged gate version of Fairchild's advanced PowerTrench process. It has been optimized for power management applications with a wide range of gate drive voltage (2.5V – 12V).

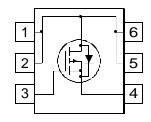
Applications

- Battery management
- · Load switch
- · Battery protection

Features

- -5.5 A, -20 V $R_{DS(ON)} = 35 \text{ m}\Omega$ @ $V_{GS} = -4.5 \text{ V}$ $R_{DS(ON)} = 50 \text{ m}\Omega$ @ $V_{GS} = -2.5 \text{ V}$
- · Fast switching speed
- High performance trench technology for extremely low $R_{\mbox{\scriptsize DS(ON)}}$





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V _{DSS}	Drain-Source Voltage		-20	V
V _{GSS}	Gate-Source Voltage		±12	V
I _D	Drain Current - Continuous	(Note 1a)	-5.5	Α
	- Pulsed		-20	
P _D	Maximum Power Dissipation	(Note 1a)	1.6	W
		(Note 1b)	0.8	
T _J , T _{STG}	Operating and Storage Junction Temperature Range		−55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	30	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.602	FDC602P	7"	8mm	3000 units

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Char	acteristics			ı	I	
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = -250 \mu\text{A}$	-20			V
<u>ΔBV_{DSS}</u> ΔT _J	Breakdown Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$, Referenced to 25°C		-14		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$			-1	μΑ
GSSF	Gate-Body Leakage, Forward	$V_{GS} = 12 \text{ V}, V_{DS} = 0 \text{ V}$			100	nA
I _{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = -12 \text{ V}, V_{DS} = 0 \text{ V}$			-100	nA
On Char	acteristics (Note 2)					
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu\text{A}$	-0.6	-0.9	-1.5	V
ΔV _{GS(th)} ΔT _J	Gate Threshold Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$, Referenced to 25°C		3		mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	$V_{GS} = -4.5 \text{ V}, I_D = -5.5 \text{ A}$ $V_{GS} = -2.5 \text{ V}, I_D = -4.5 \text{ A}$ $V_{GS} = -4.5 \text{ V}, I_D = -5.5 \text{AT}_J = 125^{\circ}\text{C}$		27 38 38	35 50 53	mΩ
I _{D(on)}	On-State Drain Current	$V_{GS} = -4.5 \text{ V}, V_{DS} = -5 \text{ V}$	-20			Α
g fs	Forward Transconductance	$V_{DS} = -5 \text{ V}, \qquad I_{D} = -5.5 \text{ A}$		19		S
Dynamic	Characteristics	,		•	•	
Ciss	Input Capacitance	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V},$		1456		pF
Coss	Output Capacitance	f = 1.0 MHz		300		pF
C _{rss}	Reverse Transfer Capacitance]		150		pF
Switchin	g Characteristics (Note 2)					
t _{d(on)}	Turn-On Delay Time	$V_{DD} = -10 \text{ V}, \qquad I_D = -1 \text{ A},$		15	27	ns
t _r	Turn-On Rise Time	$V_{GS} = -4.5 \text{ V}, \qquad R_{GEN} = 6 \Omega$		11	20	ns
t _{d(off)}	Turn-Off Delay Time	1		57	91	ns
t _f	Turn-Off Fall Time	1		37	59	ns
Qg	Total Gate Charge	$V_{DS} = -10 \text{ V}, I_{D} = -5.5 \text{ A},$		14	20	nC
Q _{gs}	Gate-Source Charge	$V_{GS} = -4.5 \text{ V}$		3		nC
Q _{gd}	Gate-Drain Charge			5		nC
Drain-Se	ource Diode Characteristics	and Maximum Ratings				
ls	Maximum Continuous Drain-Source	Diode Forward Current			-1.3	Α
V _{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = -1.3 \text{ A} \text{(Note 2)}$		-0.7	-1.2	V

Notes:

^{1.} $R_{0,N}$ is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{0,N}$ is guaranteed by design while $R_{0,N}$ is determined by the user's board design.

a. 78°C/W when mounted on a 1in² pad of 2oz copper on FR-4 board.

b. 156°C/W when mounted on a minimum pad.

^{2.} Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2.0%

Typical Characteristics

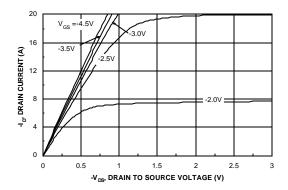


Figure 1. On-Region Characteristics.

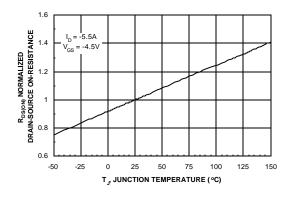


Figure 3. On-Resistance Variation with Temperature.

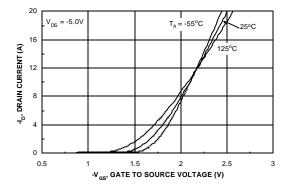


Figure 5. Transfer Characteristics.

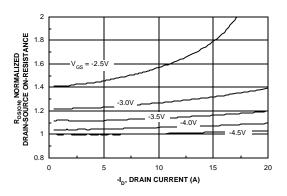


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

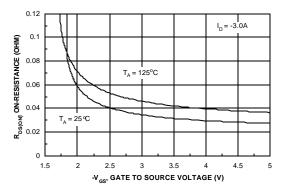


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

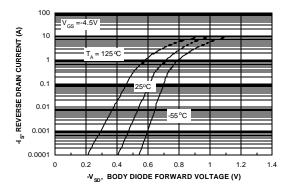
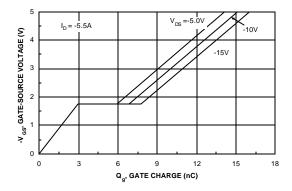


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics



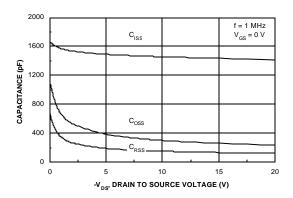
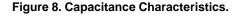
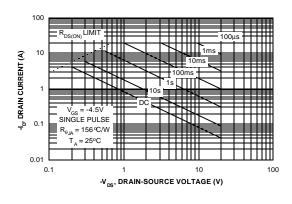


Figure 7. Gate Charge Characteristics.





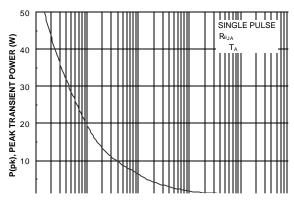


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

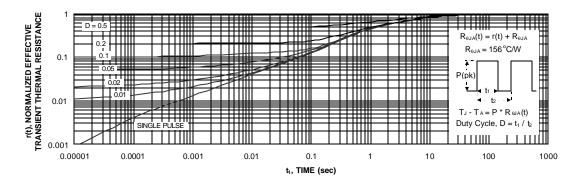


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

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