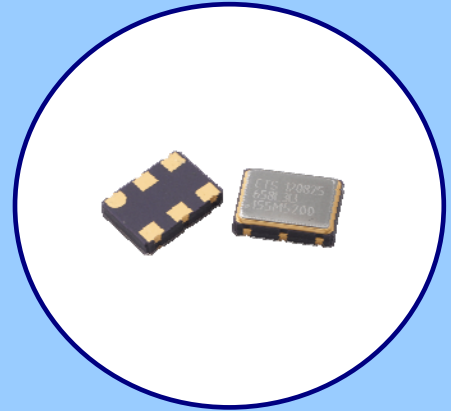


#### FEATURES

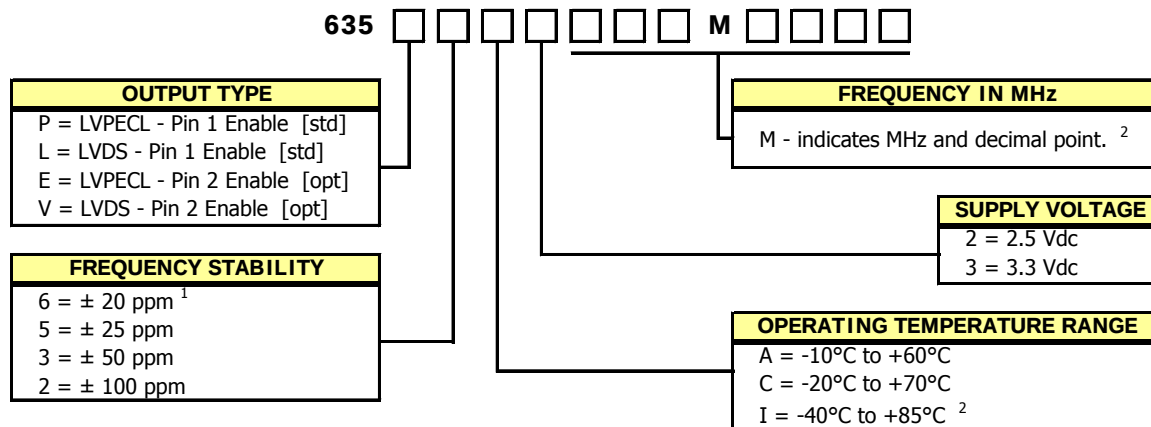
- Standard 7.0mm x 5.0mm, 6-Pad Surface Mount Package
- Low Phase Jitter, 0.7ps RMS Maximum
- LVPECL or LVDS Output
- Fundamental and 3<sup>rd</sup> Overtone Crystal Designs
- Frequency Range 10 – 320 MHz
- Frequency Stability  $\pm 50$  ppm Standard
- Operating Voltages +2.5Vdc or +3.3Vdc
- Operating Temperature to -40°C to +85°C
- Output Enable Standard
- Tape & Reel Packaging Standard, EIA-418
- RoHS/Green Compliant [6/6]



#### APPLICATIONS

Model 635 is ideal for applications such as broadband access, SerDes, Ethernet/Gigabit Ethernet, SONET/SDH and optical networking.

#### ORDERING INFORMATION



1] Consult factory for availability of 6I Stability/Temperature combination.

2] Frequency is recorded with 3 significant digits before the 'M' and 4 significant digits after the 'M' (including zeros).

See Table I for part number frequency codes that exceed 4 significant digits.

[Ex. XXXMXXXX (008M0000), XXXMXXXX (049M1520), XXXMXXXX (122M8800)]

**Not all performance combinations and frequencies may be available.  
Contact your local CTS Representative or CTS Customer Service for availability.**

#### PACKAGING INFORMATION [reference]

Device quantity is 1k pcs. maximum per 180mm reel.

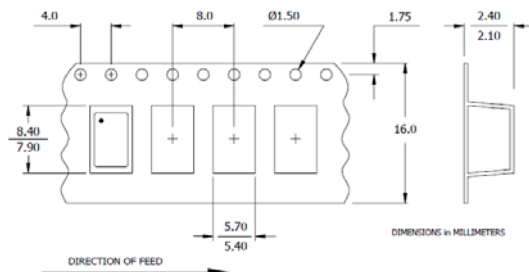


Table I

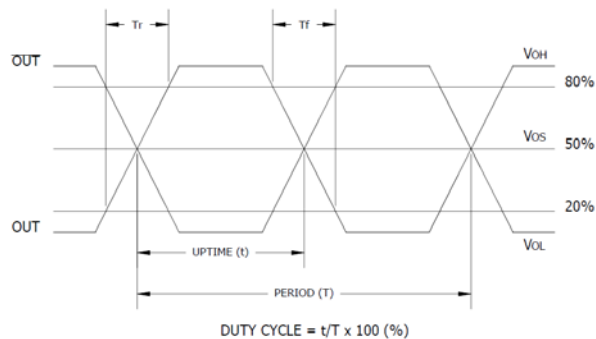
| NOMINAL FREQUENCY [MHz] | CTS PART NUMBER FREQUENCY CODE |
|-------------------------|--------------------------------|
| 025.000625              | 025M0006                       |
| 101.575694              | 101M5756                       |
| 125.009375              | 125M0093                       |
| 148.351648              | 148M351A                       |
| 153.600770              | 153M6007                       |
| 156.253906              | 156M2539                       |
| 178.018970              | 178M0189                       |

**ELECTRICAL CHARACTERISTICS**

| ELECTRICAL PARAMETERS | PARAMETER                   | SYMBOL         | CONDITIONS                                   | MIN                | TYP        | MAX                  | UNIT      |
|-----------------------|-----------------------------|----------------|----------------------------------------------|--------------------|------------|----------------------|-----------|
|                       | Maximum Supply Voltage      | $V_{CC}$       | -                                            | -0.5               | -          | 5.0                  | V         |
|                       | Storage Temperature         | $T_{STG}$      | -                                            | -40                | -          | +100                 | °C        |
|                       | Frequency Range             | $f_0$          | -                                            | 10.00              | -          | 320                  | MHz       |
|                       | LVPECL                      |                |                                              | 80.00              | -          | 320                  |           |
|                       | Frequency Stability         | $\Delta f/f_0$ | All Inclusive, see Note 1.<br>1st year aging | -                  | -          | 20, 25, 50, 100<br>3 | $\pm$ ppm |
|                       | Operating Temperature       | $T_A$          | -                                            | -20                | 25         | +70                  | °C        |
|                       | Commercial                  |                |                                              | -40                |            | +85                  |           |
|                       | Industrial                  |                |                                              |                    |            |                      |           |
|                       | Supply Voltage              | $V_{CC}$       | $\pm 5\%$                                    | 2.38<br>3.14       | 2.5<br>3.3 | 2.63<br>3.47         | V         |
|                       | Supply Current              | $I_{CC}$       | Maximum Load                                 | -                  | -          | 88                   | mA        |
|                       | LVPECL                      |                |                                              | -                  | -          | 65                   |           |
|                       | LVDS                        |                |                                              |                    |            |                      |           |
|                       | Start Up Time               | $T_S$          | Application of $V_{CC}$                      | -                  | 2          | 5                    | ms        |
|                       | Phase Jitter                | $t_{jrms}$     | Bandwidth 12 kHz - 20 MHz                    | -                  | 0.3        | 0.7                  | ps        |
|                       | Period Jitter RMS           | $p_{jrms}$     | -                                            | -                  | 2.6        | -                    |           |
|                       | Period Jitter Pk-Pk         |                | -                                            | -                  | 25         | -                    |           |
|                       | Enable Function             |                | Standby                                      |                    |            |                      | V         |
|                       | Enable Input Voltage        | $V_{IH}$       | Pin 1 or 2 Logic '1', Output Enabled         | $0.7 \cdot V_{CC}$ | -          | -                    |           |
|                       | Disable Input Voltage       | $V_{IL}$       | Pin 1 or 2 Logic '0', Output Disabled        | -                  | -          | $0.3 \cdot V_{CC}$   |           |
|                       | Disable Time                | $T_{PLZ}$      | Pin 1 or 2 Logic '0', Output Disabled        | -                  | -          | 200                  | ns        |
|                       | Enable Time                 | $T_{PLZ}$      | Pin 1 or 2 Logic '1', Output Enabled         | -                  | -          | 2                    | ms        |
|                       | <b>LVPECL WAVEFORM</b>      |                |                                              |                    |            |                      |           |
|                       | Output Load                 | $R_L$          | Terminated to $V_{CC} - 2.0V$                | -                  | 50         | -                    | Ohms      |
|                       | Output Duty Cycle           | SYM            | @ $V_{CC} - 1.3V$                            | 45                 | -          | 55                   | %         |
|                       | Output Voltage Levels       |                |                                              |                    |            |                      | V         |
|                       | Logic '1' Level             | $V_{OH}$       | PECL Load, -20°C to +70°C                    | $V_{CC} - 1.025$   | -          | $V_{CC} - 0.880$     |           |
|                       | Logic '0' Level             | $V_{OL}$       | PECL Load, -20°C to +70°C                    | $V_{CC} - 1.810$   | -          | $V_{CC} - 1.620$     | V         |
|                       | Logic '1' Level             | $V_{OH}$       | PECL Load, -40°C to +85°C                    | $V_{CC} - 1.085$   | -          | $V_{CC} - 0.880$     |           |
|                       | Logic '0' Level             | $V_{OL}$       | PECL Load, -40°C to +85°C                    | $V_{CC} - 1.830$   | -          | $V_{CC} - 1.555$     |           |
|                       | Rise and Fall Time          | $T_R, T_F$     | @ 20% - 80% Levels                           | -                  | 0.3        | 0.7                  | ns        |
|                       | <b>LVDS WAVEFORM</b>        |                |                                              |                    |            |                      |           |
|                       | Output Load                 | $R_L$          | Between Outputs                              | -                  | 100        | -                    | Ohms      |
|                       | Output Duty Cycle           | SYM            | @ 1.25V                                      | 45                 | -          | 55                   | %         |
|                       | Differential Output Voltage | $V_{OD}$       | $R_L = 100$ Ohms                             | 247                | 350        | 454                  | mV        |
|                       | Offset Voltage              | $V_{OS}$       | LVDS Load                                    | 1.125              | 1.25       | 1.375                | V         |
|                       | Output Voltage Levels       |                |                                              |                    |            |                      | V         |
|                       | Logic '1' Level             | $V_{OH}$       | LVDS Load                                    | -                  | 1.43       | 1.60                 |           |
|                       | Logic '0' Level             | $V_{OL}$       | LVDS Load                                    | 0.90               | 1.10       | -                    |           |
|                       | Rise and Fall Time          | $T_R, T_F$     | @ 20% - 80% Levels                           | -                  | 0.4        | 0.7                  | ns        |

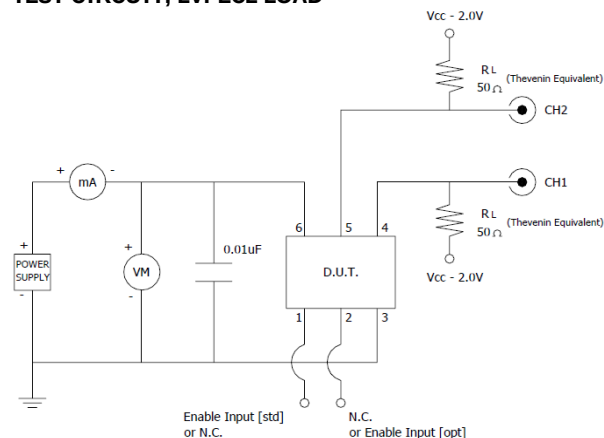
Notes:

- Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 1st year aging.

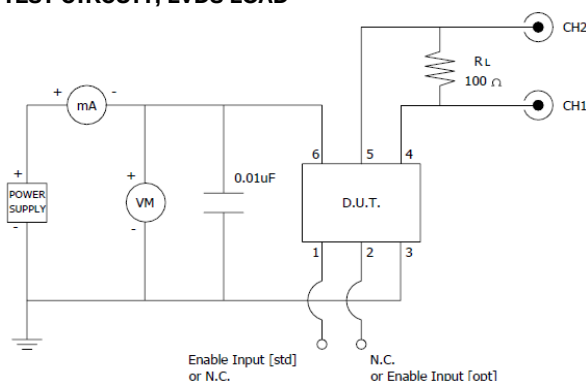
**LVPECL/LVDS OUTPUT WAVEFORM**

**ENABLE TRUTH TABLE**

| PIN 1 or Pin 2 | PIN 4 & 5 |
|----------------|-----------|
| Logic '1'      | Output    |
| Open           | Output    |
| Logic '0'      | High Z    |

**TEST CIRCUIT, LVPECL LOAD**

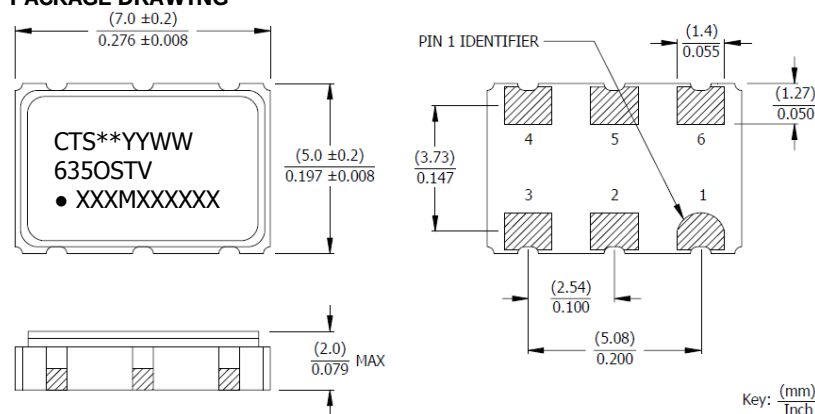


**TEST CIRCUIT, LVDS LOAD**



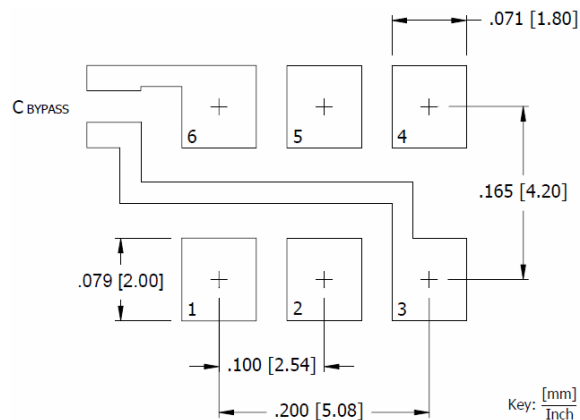
## MECHANICAL SPECIFICATIONS

### PACKAGE DRAWING



### SUGGESTED SOLDER PAD GEOMETRY

C<sub>BYPASS</sub> should be ≥ 0.01 uF.



### MARKING INFORMATION

1. \*\* - Manufacturing Site Code.
2. YYWW - Date code, YY - year, WW - week.
3. O - Output Type. P or E = LVPECL, L or V = LVDS.
4. ST - Frequency stability/temperature code. [Refer to Ordering Information.]
5. V - Voltage code. 3 = 3.3V, 2 = 2.5V
6. XXXMXXXXXX - Frequency is marked with only leading significant digits before the 'M' and 4 - 6 digits after the 'M' (including zeros).  
Ex. XXXMXXXX [19M4400]  
XXXXMXXXX [153M60077]  
XXXXMXXXX [148M351648]

### NOTES

1. Complete CTS part number, frequency value and date code information must appear on reel and carton labels.
2. Termination pads [e4]. Barrier-plating is nickel [Ni] with gold [Au] flash plate.
3. Reflow conditions per JEDEC J-STD-020; 260°C maximum, 20 seconds.
4. MSL = 1.

### D.U.T. PIN ASSIGNMENTS

| PIN | SYMBOL          | DESCRIPTION                |
|-----|-----------------|----------------------------|
| 1   | EOH or N.C.     | Enable [std] or No Connect |
| 2   | N.C. or EOH     | No Connect or Enable [opt] |
| 3   | GND             | Circuit & Package Ground   |
| 4   | Output          | RF Output                  |
| 5   | Output          | Complimentary RF Output    |
| 6   | V <sub>CC</sub> | Supply Voltage             |

## Данный компонент на территории Российской Федерации

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<http://moschip.ru/get-element>

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Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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