

Description

The 74LVC240A provides two 4-bit buffers/drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The device is designed for operation with a power supply range of 1.65V to 3.6V.

The inputs are tolerant to 5.5V allowing this device to be used in a mixed voltage environment. The device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output preventing damaging current backflow when the device is powered down.

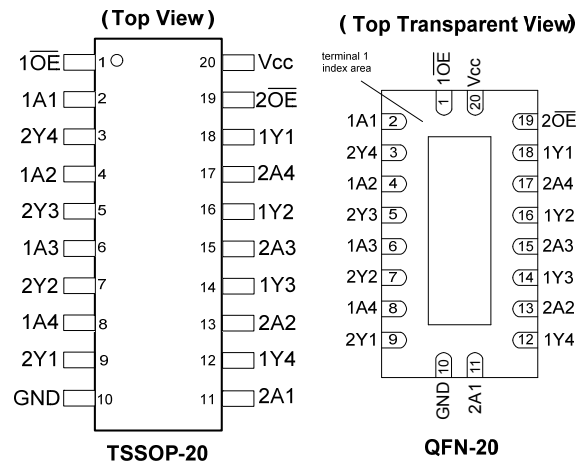
Features

- Supply Voltage Range from 1.65V to 3.6V
- Sinks or Sources 24 ma at $V_{CC} = 3V$
- CMOS Low Power Consumption
- I_{OFF} Supports Partial -Power Down Operation
- Inputs or Outputs Accept up to 5.5V
- Inputs Can Be Driven by 3.3V or 5V Allowing for Mixed Voltage Applications
- Schmitt Trigger Action at All Inputs
- Typical V_{OLP} (Quiet Output Ground Bounce) Less than 0.8V with $V_{CC} = 3.3V$ and $T_A = +25^\circ C$
- Typical V_{OHV} (Quiet Output dynamic VOH) Greater than 2.0V with $V_{CC} = 3.3V$ and $T_A = +25^\circ C$
- ESD Protection Tested per JESD 22
 - Exceeds 200-V Machine Model (A115)
 - Exceeds 2000-V Human Body Model (A114)
 - Exceeds 1000-V Charged Device Model (C101)
- Latch-Up Exceeds 250mA per JESD 78, Class I
- All devices are:
 - **Totally Lead-Free & Fully RoHS compliant (Notes 1 & 2)**
 - **Halogen and Antimony Free. "Green" Device (Note 3)**

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen and Antimony free, "Green" and Lead-Free.
3. Halogen and Antimony free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

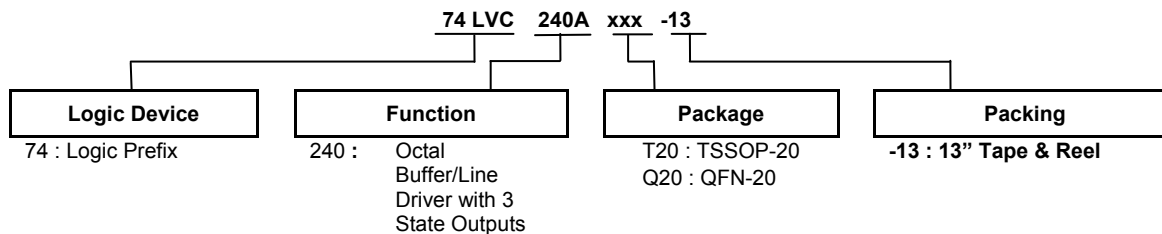
Pin Assignments



Applications

- General Purpose Logic
- Bus Driving
- Power Down Signal Isolation
- Wide Array of Products Such as:
 - PCs, Notebooks, Netbooks, Ultrabooks
 - Networking Computer Peripherals, Hard Drives, CD/DVD ROM
 - TV, DVD, DVR, Set Top Box

Ordering Information



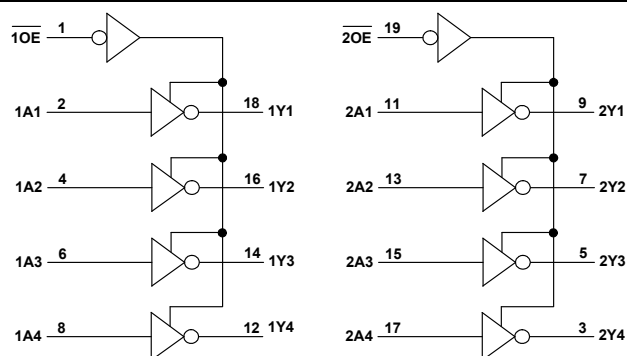
Part Number	Package Code	Package (Note 4 & 5)	Package Size	13" Tape and Reel	
				Quantity	Part Number Suffix
74LVC240AT20-13	T20	TSSOP-20	6.4mm X 6.5mm X 1.2mm 0.65 mm lead pitch	2500/Tape & Reel	-13
74LVC240AQ20-13	Q20	V-QFN4525-20	2.5mm X 4.5mm X 0.95mm 0.50 mm lead pitch	2500/Tape & Reel	-13

Notes: 4. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at <http://www.diodes.com/datasheets/ap02001.pdf>.
 5. V-QFN4525-20 is a JEDEC recognized naming convention that specifies the package thickness category as V and the number 4525 describes the package as 4.5mm X 2.5mm.

Pin Descriptions

Pin Number	Pin Name	Description
1	$\overline{1OE}$	Output Enable 1
2	1A1	Data Input
3	2Y4	Data Output
4	1A2	Data Input
5	2Y3	Data Output
6	1A3	Data Input
7	2Y2	Data Output
8	1A4	Data Input
9	2Y1	Data Output
10	GND	Ground
11	2A1	Data Input
12	1Y4	Data Output
13	2A2	Data Input
14	1Y3	Data Output
15	2A3	Data Input
16	1Y2	Data Output
17	2A4	Data Input
18	1Y1	Data Output
19	$\overline{2OE}$	Output Enable 2
20	Vcc	Supply Voltage

Logic Diagram



Function Table

(Each 4-Bit Buffer)		
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

Absolute Maximum Ratings (Notes 6 & 7)

Symbol	Description	Rating	Unit
ESD HBM	Human Body Model ESD Protection	2	kV
ESD CDM	Charged Device Model ESD Protection	1	kV
ESD MM	Machine Model ESD Protection	200	V
V _{CC}	Supply Voltage Range	-0.5 to +7.0	V
V _I	Input Voltage Range note 3	-0.5 to +7.0	V
I _{IK}	Input Clamp Current V _I < 0V	-20	mA
I _{OK}	Output Clamp Current V _O < 0V	-50	mA
I _O	Continuous output current - 0.5V < V _O V _{CC} + 0.5V	±50	mA
I _{CC}	Continuous current through V _{CC}	100	mA
I _{GND}	Continuous current through GND	-100	mA
T _J	Operating Junction Temperature	-40 to +150	°C
T _{STG}	Storage Temperature	-65 to +150	°C
P _{TOT}	Total Power Dissipation	500	mW

- Notes:
- Stresses beyond the absolute maximum may result in immediate failure or reduced reliability. These are stress values and device operation should be within recommend values.
 - Forcing the maximum allowed voltage could cause a condition exceeding the maximum current or conversely forcing the maximum current could cause a condition exceeding the maximum voltage. The ratings of both current and voltage must be maintained within the controlled range.

Recommended Operating Conditions (Note 8)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Supply Voltage	Operating	1.65	3.6	V
		Data Retention Only	1.5	—	V
V _I	Input Voltage	—	0	5.5	V
V _O	Output Voltage	—	0	V _{CC}	V
I _{OH}	High-Level Output Current	V _{CC} = 1.65V	—	-4	mA
		V _{CC} = 2.3V	—	-8	
		V _{CC} = 2.7V	—	-12	
		V _{CC} = 3.0V	—	-24	
I _{OL}	Low-Level Output Current	V _{CC} = 1.65V	—	4	mA
		V _{CC} = 2.3V	—	8	
		V _{CC} = 2.7V	—	12	
		V _{CC} = 3.0V	—	24	
Δt/ΔV	Input Transition Rise or Fall Rate		—	10	ns/V
T _A	Operating Free-Air Temperature		-40	+125	°C

- Note:
- Unused inputs should be held at V_{CC} or Ground.

Electrical Characteristics

Symbol	Parameter	Test Conditions		V _{CC}	T _A = -40°C to +85°C		T _A = -40°C to +125°C		Unit
					Min	Max	Min	Max	
V _{IH}	High-Level Input Voltage			1.65V to 1.95V	V _{CC} X 0.65	—	V _{CC} X 0.65	—	V
				2.3V to 2.7V	1.7	—	1.7	—	
				3.0V to 3.6V	2	—	2	—	
V _{IL}	Low-Level input voltage			1.65V to 1.95V	—	V _{CC} X 0.35	—	V _{CC} X 0.35	V
				2.3V to 2.7V	—	0.7	—	0.7	
				3.0V to 3.6V	—	0.8	—	0.8	
V _{OH}	High-Level Output Voltage	I _{OH} = -50 μA		1.65V to 3.6V	V _{CC} -0.2	—	V _{CC} -0.3	—	V
		I _{OH} = -4 mA		1.65V	1.2	—	1.05	—	
		I _{OH} = -8 mA		2.3V	1.7	—	1.65	—	
		I _{OH} = -12 mA		2.7V	2.2	—	2.05	—	
				3.0V	2.4	—	2.48	—	
		I _{OH} = -24 mA		3.0V	2.3	—	2.0	—	
V _{OL}	Low-Level Output Voltage	I _{OL} = 100 μA		1.65V to 3.6V	—	0.2	—	0.3	V
		I _{OL} = 4 mA		1.65V	—	0.45	—	0.65	
		I _{OL} = 8 mA		2.3V	—	0.60	—	0.80	
		I _{OL} = 12 mA		2.7V	—	0.40	—	0.60	
		I _{OL} = 24 mA		3.0V	—	0.55	—	0.80	
I _{OFF}	Power Down Leakage Current	V _I or V _O = 0 or 5.5V		0V	—	±10	—	20	μA
I _I	Input Current Control Pins	V _I =GND or 5.5V		0 to 3.6V	—	±5	—	± 20	μA
I _{oz}	Z-state Current Including Input Current I/O Pins	V _I =GND or 5.5V V _O = 0 to 5.5V		3.6V	—	±5	—	± 20	uA
I _{CC}	Supply Current	V _I = GND or V _{CC} , I _o =0		3.6V	—	10	—	40	μA
ΔI _{CC}	Additional Supply Current	One input at V _{cc} -0.6V I _o = 0A		2.7V to 3.6V	—	500	—	5000	μA
C _i	Input Capacitance	Control Pins	V _I = GND or V _{CC}	0V to 3.6V	4.0 typical		4.0 typical		pF
		I/O Pins			5.5 typical		5.5 typical		

Switching Characteristics

Symbol	Parameter	Test Conditions	V _{CC}	T _A = +25°C			-40°C to +85°C		-40°C to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t _{PD}	Propagation Delay A _N to Y _N	Figure 1	1.8V± 0.15V	1.0	6.0	12.2	1.0	13.1	1.0	16.9	ns
			2.5V± 0.2V	1.0	3.9	7.8	1.0	8.4	1.0	8.9	
			2.7V	1.0	4.2	8.1	1.0	8.9	1.0	9.0	
			3.3V± 0.3V	1.5	3.8	7.6	1.5	8.1	1.5	8.3	
t _{EN}	Enable Time $\overline{\text{OE}}$ to Y _N	Figure 1	1.8V± 0.15V	1.0	7.0	14.8	1.0	15.3	1.0	22.5	ns
			2.5V± 0.2V	1.0	4.5	10.0	1.0	10.5	1.0	12.4	
			2.7V	1.0	5.4	8.5	1.0	9.5	1.0	11.0	
			3.3 ± 0.3V	1.5	4.4	7.0	1.5	8.5	1.5	9.0	
t _{DIS}	Disable Time $\overline{\text{OE}}$ to Y _N	Figure 1	1.8V± 0.15V	1.0	7.8	16.5	1.0	17.0	1.0	18.2	ns
			2.5V± 0.2V	1.0	4.0	9.0	1.0	9.5	1.0	10.7	
			2.7V	1.0	4.3	7.5	1.0	8.5	1.0	10.0	
			3.3V± 0.3V	1.7	4.0	6.0	1.7	7.5	1.7	9.0	
t _{sk(0)}	Output Skew Time		3.3V± 0.3V	—	—	1.0	—	—	—	1.5	ns

Operating Characteristics

 $T_A = +25^{\circ}\text{C}$

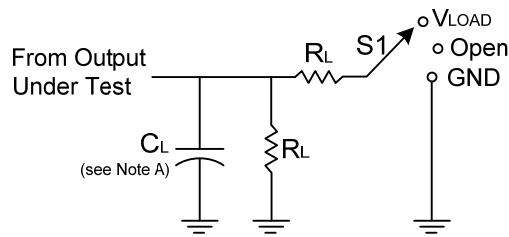
Symbol	Parameter	Test Conditions	V _{CC}	Typ	Unit
C _{pd}	Power Dissipation Capacitance per Gate	F = 10 MHz Outputs Enabled	1.8V ± 0.15V	9.9	pF
			2.5V ± 0.2V	10.2	
			3.3V ± 0.3V	10.6	

Package Characteristics

Symbol	Parameter	Package	Test Conditions	Min	Typ	Max	Unit
θ_{JA}	Thermal Resistance Junction-to-Ambient	TSSOP-20	(Note 9)	—	74	—	°C/W
θ_{JC}	Thermal Resistance Junction-to-Case	TSSOP-20	(Note 9)	—	15	—	°C/W
θ_{JA}	Thermal Resistance Junction-to-Ambient	V-QFN4525-20	(Note 9)	—	67	—	°C/W
θ_{JC}	Thermal Resistance Junction-to-Case	V-QFN4525-20	(Note 9)	—	20	—	°C/W

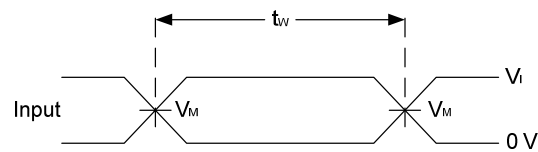
Note: 9. Test conditions for TSSOP-20 and V-QFN4525-20: Devices mounted on 4 layer FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout per JESD 51-7.

Parameter Measurement Information

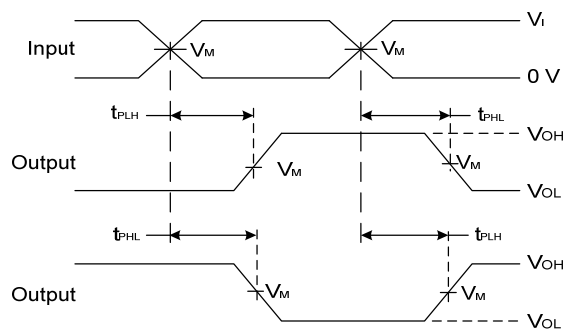


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

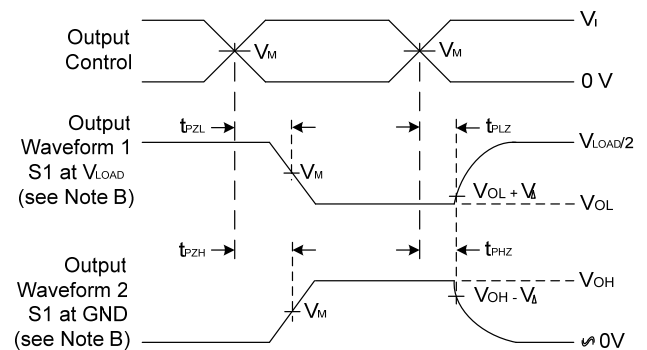
V_{CC}	Inputs		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	2 x V_{CC}	30pF	1KΩ	0.15V
2.5V±0.2V	V_{CC}	≤2ns	$V_{CC}/2$	2 x V_{CC}	30pF	500Ω	0.15V
2.7V	2.7V	≤2.5ns	1.5V	6V	50pF	500Ω	0.3V
3.3V±0.3V	2.7V	≤2.5ns	1.5V	6V	50pF	500Ω	0.3V



Voltage Waveform Pulse Duration



Voltage Waveform Propagation Delay Times
Inverting and Non Inverting Outputs



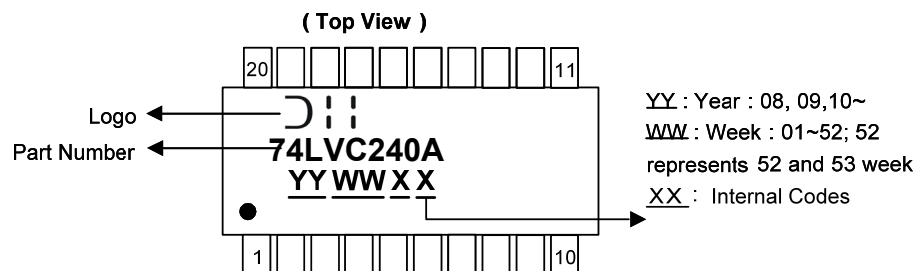
Voltage Waveform Enable and Disable Times
Low and High Level Enabling

- Notes:
- A. Includes test lead and test apparatus capacitance.
 - B. All pulses are supplied at pulse repetition rate ≤ 10 MHz.
 - C. Inputs are measured separately one transition per measurement.
 - D. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - E. t_{PZL} and t_{PZH} are the same as t_{EN0} .
 - F. t_{PLH} and t_{PHL} are the same as t_{PD} .

Figure 1 Load Circuit and Voltage Waveforms

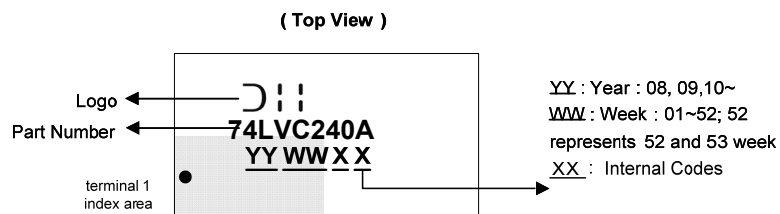
Marking Information

(1) TSSOP20



Part Number	Package
74LVC240AT20	TSSOP-20

(2) QFN-20 (V-QFN4525-20)

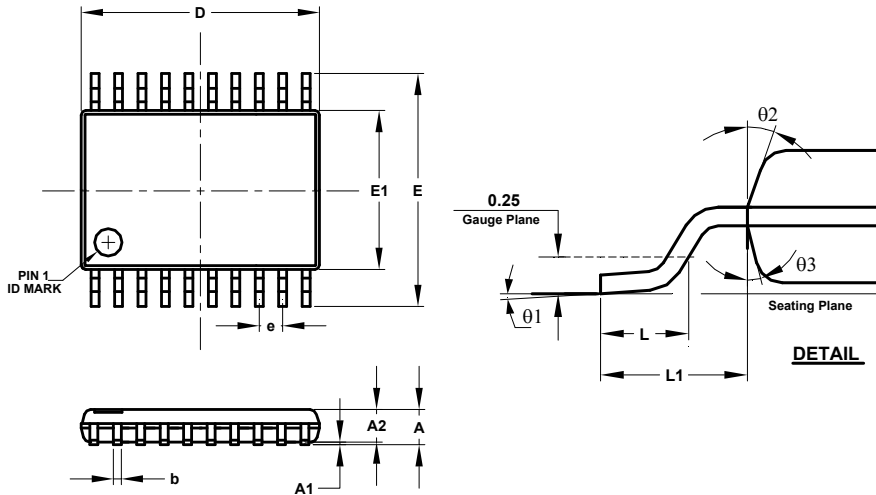


Part Number	Package
74LVC240AQ20	V-QFN4525-20

Package Outline Dimensions (All Dimensions in mm)

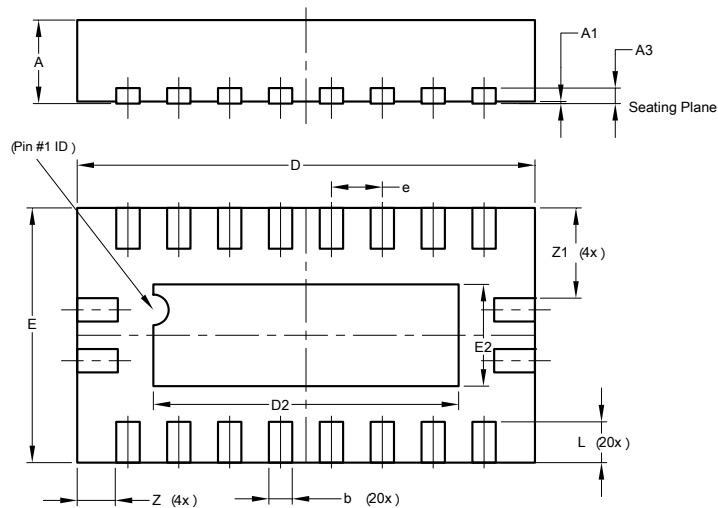
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for the latest version.

(1) TSSOP-20



TSSOP-20			
Dim	Min	Max	Typ
A	-	1.20	-
A1	0.05	0.15	-
A2	0.80	1.05	-
b	0.19	0.30	-
c	0.09	0.20	-
D	6.40	6.60	6.50
E	6.20	6.60	6.40
E1	4.30	4.50	4.40
e	0.65 BSC		
L	0.45	0.75	0.60
L1	1.0 REF		
θ1	0°	8°	-
θ2	10°	14°	12°
θ3	10°	14°	12°
All Dimensions in mm			

(2) QFN-20 (V-QFN4525-20)

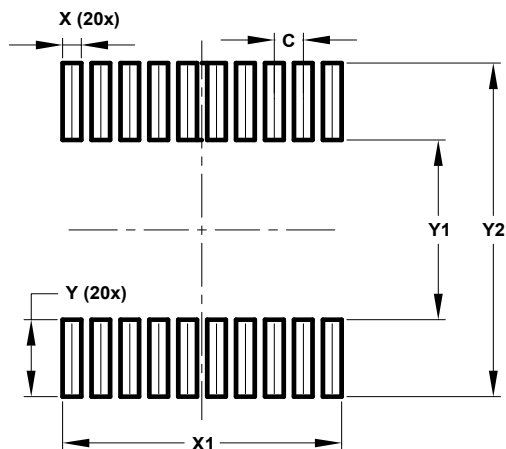


V-QFN4525-20			
Dim	Min	Max	Typ
A	0.75	0.85	0.80
A1	0.00	0.05	0.02
A3	-	-	0.15
b	0.18	0.30	0.23
D	4.45	4.55	4.50
D2	2.85	3.15	3.00
E	2.45	2.55	2.50
E2	0.85	1.15	1.00
e	0.50BSC		
L	0.30	0.50	0.40
Z	-	-	0.385
Z1	-	-	0.885
All Dimensions in mm			

Suggested Pad Layout

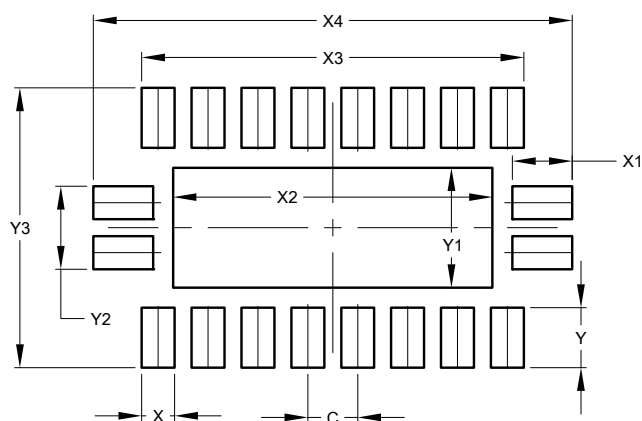
Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.

(1) TSSOP-20



Dimensions	Value (in mm)
C	0.650
X	0.420
X1	6.270
Y	1.789
Y1	4.160
Y2	7.720

(2) QFN-20 (V-QFN4525-20)



Dimensions	Value (in mm)
C	0.500
X	0.330
X1	0.600
X2	3.200
X3	3.830
X4	4.800
Y	0.600
Y1	1.200
Y2	0.830
Y3	2.800

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