

### FEATURES

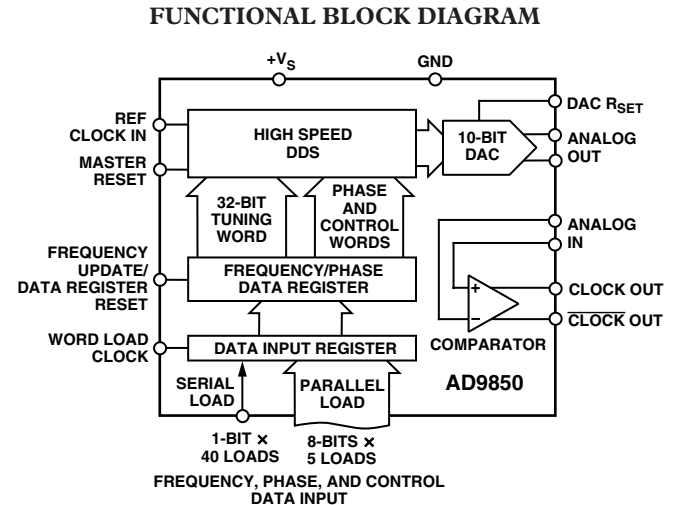
- 125 MHz Clock Rate
- On-Chip High Performance DAC and High Speed Comparator
- DAC SFDR > 50 dB @ 40 MHz A<sub>OUT</sub>
- 32-Bit Frequency Tuning Word
- Simplified Control Interface: Parallel Byte or Serial Loading Format
- Phase Modulation Capability
- 3.3 V or 5 V Single-Supply Operation
- Low Power: 380 mW @ 125 MHz (5 V)  
155 mW @ 110 MHz (3.3 V)
- Power-Down Function
- Ultrasmall 28-Lead SSOP Packaging

### APPLICATIONS

- Frequency/Phase—Agile Sine Wave Synthesis
- Clock Recovery and Locking Circuitry for Digital Communications
- Digitally Controlled ADC Encode Generator
- Agile Local Oscillator Applications

### GENERAL DESCRIPTION

The AD9850 is a highly integrated device that uses advanced DDS technology coupled with an internal high speed, high performance D/A converter and comparator to form a complete, digitally programmable frequency synthesizer and clock generator function. When referenced to an accurate clock source, the AD9850 generates a spectrally pure, frequency/phase programmable, analog output sine wave. This sine wave can be used directly as a frequency source, or it can be converted to a square wave for agile-clock generator applications. The AD9850's innovative high speed DDS core provides a 32-bit frequency tuning word, which results in an output tuning resolution of 0.0291 Hz for a 125 MHz reference clock input. The AD9850's circuit architecture allows the generation of output frequencies of up to one-half the reference clock frequency (or 62.5 MHz), and the output frequency can be digitally changed (asynchronously) at a rate of up to 23 million new frequencies per second. The device also provides five bits of digitally controlled phase modulation, which enables phase shifting of its output in increments of 180°, 90°, 45°, 22.5°,



11.25°, and any combination thereof. The AD9850 also contains a high speed comparator that can be configured to accept the (externally) filtered output of the DAC to generate a low jitter square wave output. This facilitates the device's use as an agile clock generator function.

The frequency tuning, control, and phase modulation words are loaded into the AD9850 via a parallel byte or serial loading format. The parallel load format consists of five iterative loads of an 8-bit control word (byte). The first byte controls phase modulation, power-down enable, and loading format; Bytes 2 to 5 comprise the 32-bit frequency tuning word. Serial loading is accomplished via a 40-bit serial data stream on a single pin. The AD9850 Complete DDS uses advanced CMOS technology to provide this breakthrough level of functionality and performance on just 155 mW of power dissipation (3.3 V supply).

The AD9850 is available in a space-saving 28-lead SSOP, surface-mount package. It is specified to operate over the extended industrial temperature range of -40°C to +85°C.

### REV. H

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# AD9850—SPECIFICATIONS ( $V_S = 5\text{ V} \pm 5\%$ except as noted, $R_{SET} = 3.9\text{ k}\Omega$ )

| Parameter                                    | Temp | Test Level | AD9850BRS |             |          | Unit             |
|--|------|------------|-----------|-------------|----------|------------------|
|  |      |            | Min       | Typ         | Max      |                  |
| <b>CLOCK INPUT CHARACTERISTICS</b>           |      |            |           |             |          |                  |
| Frequency Range                              |      |            |           |             |          |                  |
| 5 V Supply                                   | Full | IV         | 1         |             | 125      | MHz              |
| 3.3 V Supply                                 | Full | IV         | 1         |             | 110      | MHz              |
| Pulse Width High/Low                         |      |            |           |             |          |                  |
| 5 V Supply                                   | 25°C | IV         | 3.2       |             |          | ns               |
| 3.3 V Supply                                 | 25°C | IV         | 4.1       |             |          | ns               |
| <b>DAC OUTPUT CHARACTERISTICS</b>            |      |            |           |             |          |                  |
| Full-Scale Output Current                    |      |            |           |             |          |                  |
| $R_{SET} = 3.9\text{ k}\Omega$               | 25°C | V          |           | 10.24       |          | mA               |
| $R_{SET} = 1.95\text{ k}\Omega$              | 25°C | V          |           | 20.48       |          | mA               |
| Gain Error                                   | 25°C | I          | -10       |             | +10      | % FS             |
| Gain Temperature Coefficient                 | Full | V          |           | 150         |          | ppm/°C           |
| Output Offset                                | 25°C | I          |           |             | 10       | $\mu\text{A}$    |
| Output Offset Temperature Coefficient        | Full | V          |           | 50          |          | nA/°C            |
| Differential Nonlinearity                    | 25°C | I          |           | 0.5         | 0.75     | LSB              |
| Integral Nonlinearity                        | 25°C | I          |           | 0.5         | 1        | LSB              |
| Output Slew Rate (50 $\Omega$ , 2 pF Load)   | 25°C | V          |           | 400         |          | V/ $\mu\text{s}$ |
| Output Impedance                             | 25°C | IV         | 50        | 120         |          | k $\Omega$       |
| Output Capacitance                           | 25°C | IV         |           |             | 8        | pF               |
| Voltage Compliance                           | 25°C | I          |           |             | 1.5      | V                |
| Spurious-Free Dynamic Range (SFDR)           |      |            |           |             |          |                  |
| Wideband (Nyquist Bandwidth)                 |      |            |           |             |          |                  |
| 1 MHz Analog Out                             | 25°C | IV         | 63        | 72          |          | dBc              |
| 20 MHz Analog Out                            | 25°C | IV         | 50        | 58          |          | dBc              |
| 40 MHz Analog Out                            | 25°C | IV         | 46        | 54          |          | dBc              |
| Narrowband                                   |      |            |           |             |          |                  |
| 40.13579 MHz $\pm$ 50 kHz                    | 25°C | IV         |           | 80          |          | dBc              |
| 40.13579 MHz $\pm$ 200 kHz                   | 25°C | IV         |           | 77          |          | dBc              |
| 4.513579 MHz $\pm$ 50 kHz/20.5 MHz CLK       | 25°C | IV         |           | 84          |          | dBc              |
| 4.513579 MHz $\pm$ 200 kHz/20.5 MHz CLK      | 25°C | IV         |           | 84          |          | dBc              |
| <b>COMPARATOR INPUT CHARACTERISTICS</b>      |      |            |           |             |          |                  |
| Input Capacitance                            | 25°C | V          |           | 3           |          | pF               |
| Input Resistance                             | 25°C | IV         | 500       |             |          | k $\Omega$       |
| Input Current                                | 25°C | I          | -12       |             | +12      | $\mu\text{A}$    |
| Input Voltage Range                          | 25°C | IV         | 0         |             | $V_{DD}$ | V                |
| Comparator Offset*                           | Full | VI         | 30        |             | 30       | mV               |
| <b>COMPARATOR OUTPUT CHARACTERISTICS</b>     |      |            |           |             |          |                  |
| Logic 1 Voltage 5 V Supply                   | Full | VI         | 4.8       |             |          | V                |
| Logic 1 Voltage 3.3 V Supply                 | Full | VI         | 3.1       |             |          | V                |
| Logic 0 Voltage                              | Full | VI         |           |             | 0.4      | V                |
| Propagation Delay, 5 V Supply (15 pF Load)   | 25°C | V          |           | 5.5         |          | ns               |
| Propagation Delay, 3.3 V Supply (15 pF Load) | 25°C | V          |           | 7           |          | ns               |
| Rise/Fall Time, 5 V Supply (15 pF Load)      | 25°C | V          |           | 3           |          | ns               |
| Rise/Fall Time, 3.3 V Supply (15 pF Load)    | 25°C | V          |           | 3.5         |          | ns               |
| Output Jitter (p-p)                          | 25°C | V          |           | 80          |          | ps               |
| <b>CLOCK OUTPUT CHARACTERISTICS</b>          |      |            |           |             |          |                  |
| Clock Output Duty Cycle (Clk Gen. Config.)   | 25°C | IV         |           | 50 $\pm$ 10 |          | %                |

| Parameter   | Temp | Test Level | AD9850BRS |     |     | Unit |
|---|------|------------|-----------|-----|-----|------|
|   |      |            | Min       | Typ | Max |      |
| <b>CMOS LOGIC INPUTS (Including CLKIN)</b>        |      |            |           |     |     |      |
| Logic 1 Voltage, 5 V Supply                       | 25°C | I          | 3.5       |     |     | V    |
| Logic 1 Voltage, 3.3 V Supply                     | 25°C | IV         | 2.4       |     |     | V    |
| Logic 0 Voltage                                   | 25°C | IV         |           |     | 0.8 | V    |
| Logic 1 Current                                   | 25°C | I          |           |     | 12  | μA   |
| Logic 0 Current                                   | 25°C | I          |           |     | 12  | μA   |
| Input Capacitance                                 | 25°C | V          |           | 3   |     | pF   |
| <b>POWER SUPPLY (A<sub>OUT</sub> = 1/3 CLKIN)</b> |      |            |           |     |     |      |
| <b>+V<sub>S</sub> Current @</b>                   |      |            |           |     |     |      |
| 62.5 MHz Clock, 3.3 V Supply                      | Full | VI         |           | 30  | 48  | mA   |
| 110 MHz Clock, 3.3 V Supply                       | Full | VI         |           | 47  | 60  | mA   |
| 62.5 MHz Clock, 5 V Supply                        | Full | VI         |           | 44  | 64  | mA   |
| 125 MHz Clock, 5 V Supply                         | Full | VI         |           | 76  | 96  | mA   |
| <b>P<sub>DISS</sub> @</b>                         |      |            |           |     |     |      |
| 62.5 MHz Clock, 3.3 V Supply                      | Full | VI         |           | 100 | 160 | mW   |
| 110 MHz Clock, 3.3 V Supply                       | Full | VI         |           | 155 | 200 | mW   |
| 62.5 MHz Clock, 5 V Supply                        | Full | VI         |           | 220 | 320 | mW   |
| 125 MHz Clock, 5 V Supply                         | Full | VI         |           | 380 | 480 | mW   |
| <b>P<sub>DISS</sub> Power-Down Mode</b>           |      |            |           |     |     |      |
| 5 V Supply  | Full | V          |           | 30  |     | mW   |
| 3.3 V Supply                                      | Full | V          |           | 10  |     | mW   |

\*Tested by measuring output duty cycle variation.

Specifications subject to change without notice.

## TIMING CHARACTERISTICS\* (V<sub>S</sub> = 5 V ± 5% except as noted, R<sub>SET</sub> = 3.9 kΩ)

| Parameter   | Temp | Test Level | AD9850BRS |     |     | Unit         |
|---|------|------------|-----------|-----|-----|--------------|
|   |      |            | Min       | Typ | Max |              |
| t <sub>DS</sub> (Data Setup Time)                     | Full | IV         | 3.5       |     |     | ns           |
| t <sub>DH</sub> (Data Hold Time)                      | Full | IV         | 3.5       |     |     | ns           |
| t <sub>WH</sub> (W_CLK Minimum Pulse Width High)      | Full | IV         | 3.5       |     |     | ns           |
| t <sub>WL</sub> (W_CLK Minimum Pulse Width Low)       | Full | IV         | 3.5       |     |     | ns           |
| t <sub>WD</sub> (W_CLK Delay after FQ_UD)             | Full | IV         | 7.0       |     |     | ns           |
| t <sub>CD</sub> (CLKIN Delay after FQ_UD)             | Full | IV         | 3.5       |     |     | ns           |
| t <sub>FH</sub> (FQ_UD High)                          | Full | IV         | 7.0       |     |     | ns           |
| t <sub>FL</sub> (FQ_UD Low)                           | Full | IV         | 7.0       |     |     | ns           |
| <b>t<sub>CF</sub> (Output Latency from FQ_UD)</b>     |      |            |           |     |     |              |
| Frequency Change                                      | Full | IV         | 18        |     |     | CLKIN Cycles |
| Phase Change  | Full | IV         | 13        |     |     | CLKIN Cycles |
| t <sub>FD</sub> (FQ_UD Minimum Delay after W_CLK)     | Full | IV         | 7.0       |     |     | ns           |
| t <sub>RH</sub> (CLKIN Delay after RESET Rising Edge) | Full | IV         | 3.5       |     |     | ns           |
| t <sub>RL</sub> (RESET Falling Edge after CLKIN)      | Full | IV         | 3.5       |     |     | ns           |
| t <sub>RS</sub> (Minimum RESET Width)                 | Full | IV         | 5         |     |     | CLKIN Cycles |
| t <sub>OL</sub> (RESET Output Latency)                | Full | IV         | 13        |     |     | CLKIN Cycles |
| t <sub>RR</sub> (Recovery from RESET)                 | Full | IV         | 2         |     |     | CLKIN Cycles |
| Wake-Up Time from Power-Down Mode                     | 25°C | V          |           | 5   |     | μs           |

\*Control functions are asynchronous with CLKIN.

Specifications subject to change without notice.

# AD9850

## ABSOLUTE MAXIMUM RATINGS\*

|                                      |                           |
|--------------------------------------|---------------------------|
| Maximum Junction Temperature         | 150°C                     |
| V <sub>DD</sub>                      | 6 V                       |
| Digital Inputs                       | -0.7 V to +V <sub>S</sub> |
| Digital Output Continuous Current    | 5 mA                      |
| DAC Output Current                   | 30 mA                     |
| Storage Temperature                  | -65°C to +150°C           |
| Operating Temperature                | -40°C to +85°C            |
| Lead Temperature (Soldering 10 sec)  | 300°C                     |
| SSOP $\theta_{JA}$ Thermal Impedance | 82°C/W                    |

\*Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure of absolute maximum rating conditions for extended periods of time may affect device reliability.

## EXPLANATION OF TEST LEVELS

### Test Level

- I 100% Production Tested.
- III Sample Tested Only.
- IV Parameter is guaranteed by design and characterization testing.
- V Parameter is a typical value only.
- VI All devices are 100% production tested at 25°C. 100% production tested at temperature extremes for military temperature devices; guaranteed by design and characterization testing for industrial devices.

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9850 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

**Application Note:** Users are cautioned not to apply digital input signals prior to power-up of this device. Doing so may result in a latch-up condition.



## ORDERING GUIDE

| Model            | Temperature Range | Package Description                    | Package Option |
|------------------|-------------------|--|----------------|
| AD9850BRS        | -40°C to +85°C    | Shrink Small Outline Package (SSOP)    | RS-28          |
| AD9850BRS-REEL   | -40°C to +85°C    | Shrink Small Outline Package (SSOP)    | RS-28          |
| AD9850BRSZ*      | -40°C to +85°C    | Shrink Small Outline Package (SSOP)    | RS-28          |
| AD9850BRSZ-REEL* | -40°C to +85°C    | Shrink Small Outline Package (SSOP)    | RS-28          |
| AD9850/CGPCB     |                   | Evaluation Board Clock Generator       |                |
| AD9850/FSPCB     |                   | Evaluation Board Frequency Synthesizer |                |

\*Z = Pb-free part.

## PIN CONFIGURATION

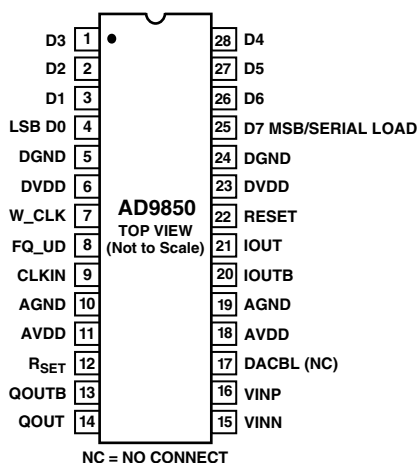
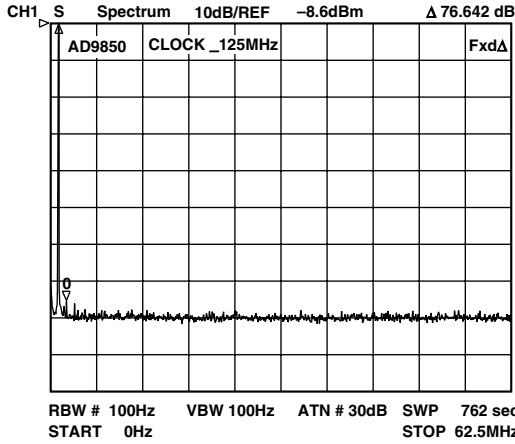


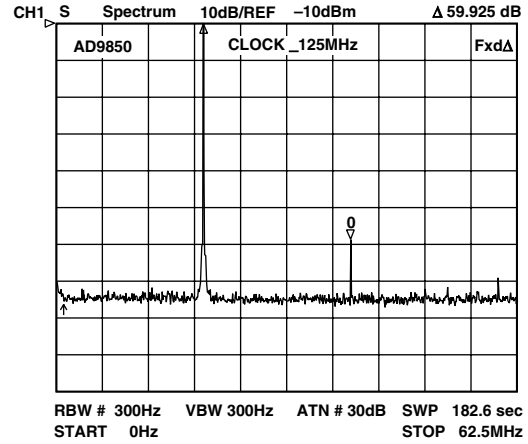
Table I. PIN FUNCTION DESCRIPTIONS

| Pin No.             | Mnemonic         | Function   |
|---------------------|------------------|--|
| 4 to 1,<br>28 to 25 | D0 to D7         | 8-Bit Data Input. This is the 8-bit data port for iteratively loading the 32-bit frequency and the 8-bit phase/control word. D7 = MSB; D0 = LSB. D7 (Pin 25) also serves as the input pin for the 40-bit serial data-word.   |
| 5, 24               | DGND             | Digital Ground. These are the ground return leads for the digital circuitry.   |
| 6, 23               | DVDD             | Supply Voltage Leads for Digital Circuitry.  |
| 7                   | W_CLK            | Word Load Clock. This clock is used to load the parallel or serial frequency/phase/control words.  |
| 8                   | FQ_UD            | Frequency Update. On the rising edge of this clock, the DDS updates to the frequency (or phase) loaded in the data input register; it then resets the pointer to Word 0.   |
| 9                   | CLKIN            | Reference Clock Input. This may be a continuous CMOS-level pulse train or sine input biased at 1/2 V supply. The rising edge of this clock initiates operation.  |
| 10, 19              | AGND             | Analog Ground. These leads are the ground return for the analog circuitry (DAC and comparator).  |
| 11, 18              | AVDD             | Supply Voltage for the Analog Circuitry (DAC and Comparator).  |
| 12                  | R <sub>SET</sub> | DAC's External R <sub>SET</sub> Connection. This resistor value sets the DAC full-scale output current. For normal applications ( $F_s I_{OUT} = 10 \text{ mA}$ ), the value for R <sub>SET</sub> is 3.9 k $\Omega$ connected to ground. The R <sub>SET</sub> /I <sub>OUT</sub> relationship is $I_{OUT} = 32 (1.248 \text{ V}/R_{SET})$ . |
| 13                  | QOUTB            | Output Complement. This is the comparator's complement output.   |
| 14                  | QOUT             | Output True. This is the comparator's true output.   |
| 15                  | VINN             | Inverting Voltage Input. This is the comparator's negative input.  |
| 16                  | VINP             | Noninverting Voltage Input. This is the comparator's positive input.   |
| 17                  | DACBL (NC)       | DAC Baseline. This is the DAC baseline voltage reference; this lead is internally bypassed and should normally be considered a no connect for optimum performance.   |
| 20                  | IOUTB            | Complementary Analog Output of the DAC.  |
| 21                  | IOUT             | Analog Current Output of the DAC.  |
| 22                  | RESET            | Reset. This is the master reset function; when set high, it clears all registers (except the input register), and the DAC output goes to cosine 0 after additional clock cycles—see Figure 7.  |

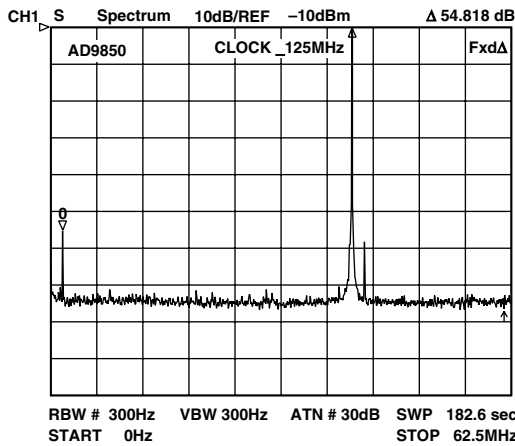
# AD9850—Typical Performance Characteristics



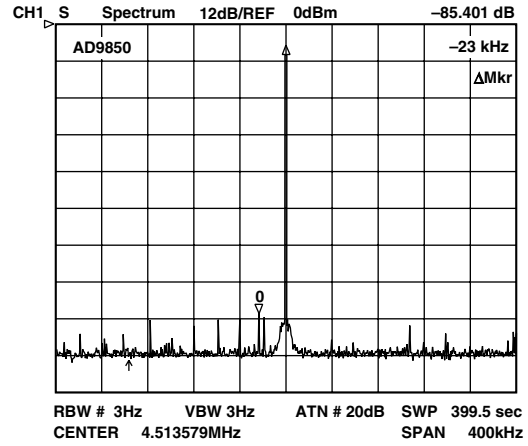
TPC 1. SFDR, CLKIN = 125 MHz/ $f_{OUT}$  = 1 MHz



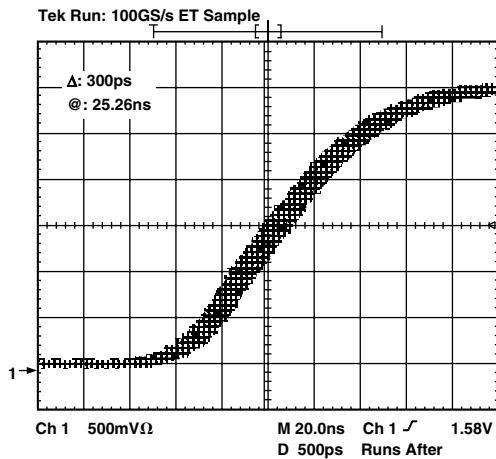
TPC 4. SFDR, CLKIN = 125 MHz/ $f_{OUT}$  = 20 MHz



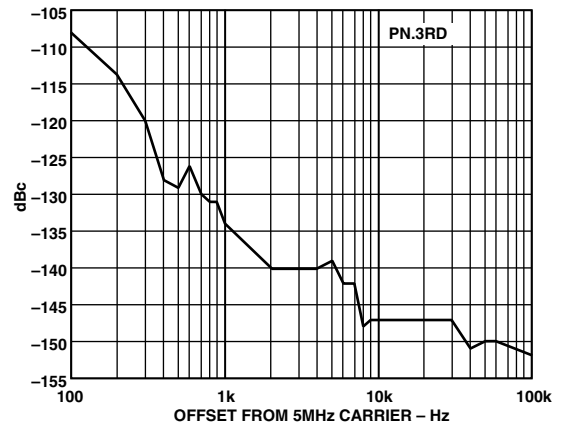
TPC 2. SFDR, CLKIN = 125 MHz/ $f_{OUT}$  = 41 MHz



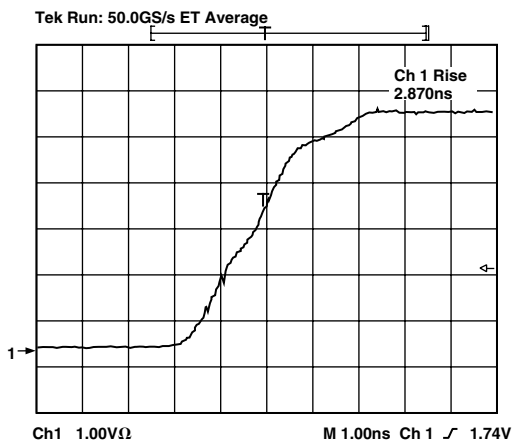
TPC 5. SFDR, CLKIN = 20.5 MHz/ $f_{OUT}$  = 4.5 MHz



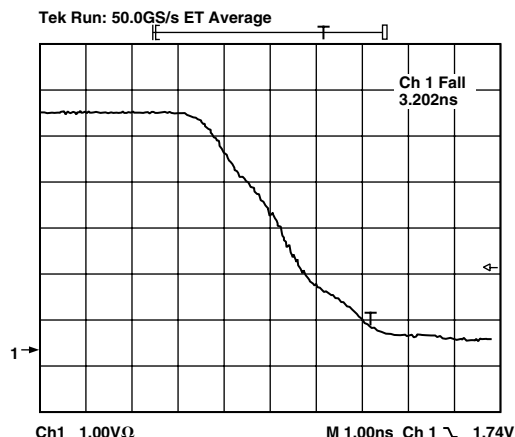
TPC 3. Typical Comparator Output Jitter, AD9850 Configured as Clock Generator with 42 MHz LP Filter (40 MHz  $A_{OUT}$ /125 MHz CLKIN)



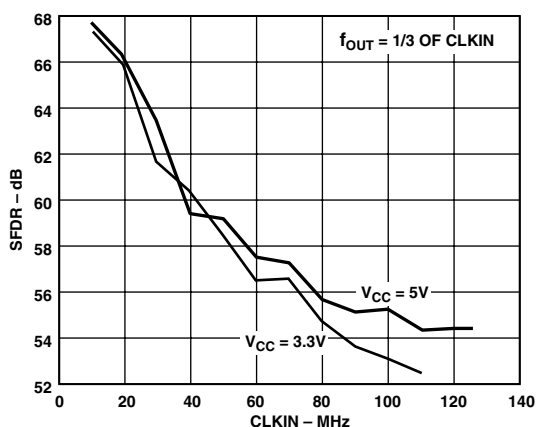
TPC 6. Output Residual Phase Noise (5 MHz  $A_{OUT}$ /125 MHz CLKIN)



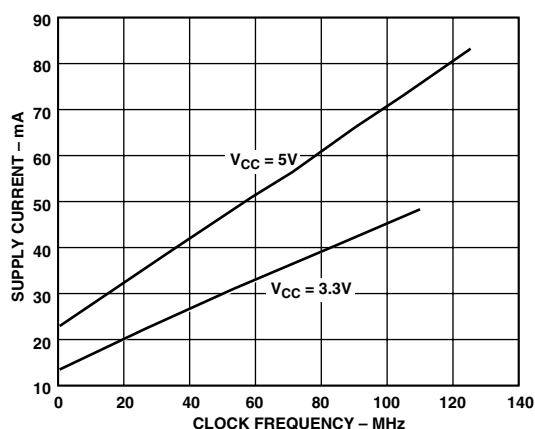
TPC 7. Comparator Output Rise Time  
(5 V Supply/15 pF Load)



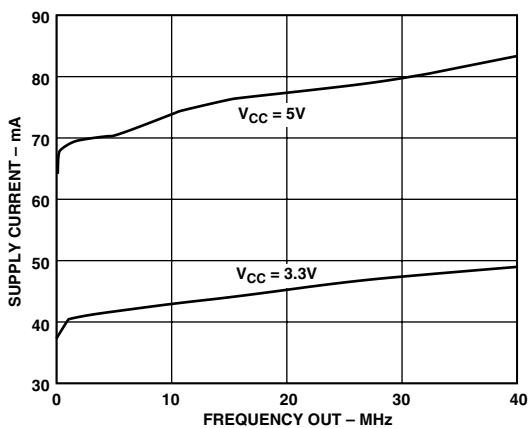
TPC 10. Comparator Output Fall Time  
(5 V Supply/15 pF Load)



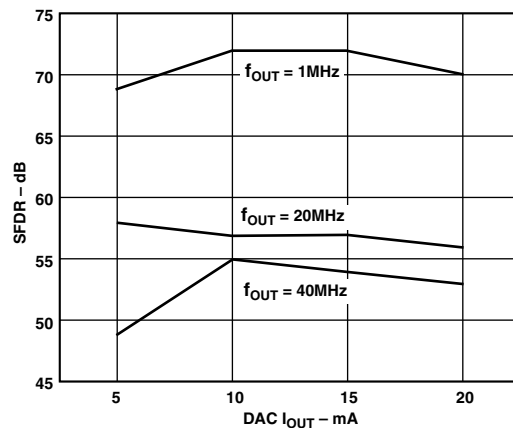
TPC 8. SFDR vs. CLKIN Frequency  
( $A_{OUT} = 1/3$  of CLKIN)



TPC 11. Supply Current vs. CLKIN Frequency  
( $A_{OUT} = 1/3$  of CLKIN)



TPC 9. Supply Current vs.  $A_{OUT}$  Frequency  
(CLKIN = 125/110 MHz for 5 V/3.3 V Plot)



TPC 12. SFDR vs. DAC  $I_{OUT}$  ( $A_{OUT} = 1/3$  of CLKIN)

# AD9850

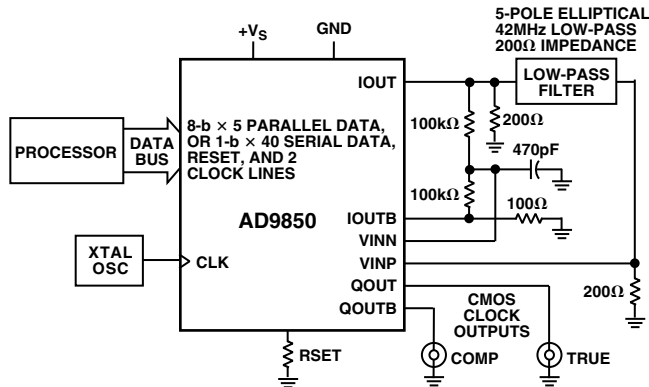


Figure 1. Basic AD9850 Clock Generator Application with Low-Pass Filter

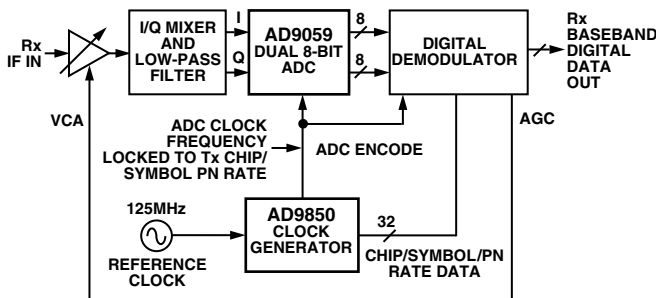


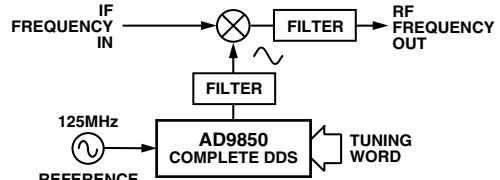
Figure 2. AD9850 Clock Generator Application in a Spread-Spectrum Receiver

## THEORY OF OPERATION AND APPLICATION

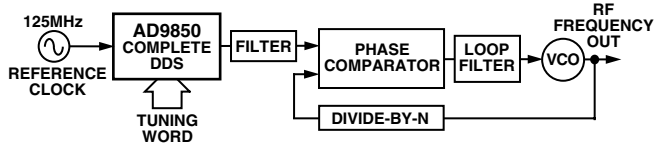
The AD9850 uses direct digital synthesis (DDS) technology, in the form of a numerically controlled oscillator, to generate a frequency/phase-agile sine wave. The digital sine wave is converted to analog form via an internal 10-bit high speed D/A converter, and an on-board high speed comparator is provided to translate the analog sine wave into a low jitter TTL/CMOS compatible output square wave. DDS technology is an innovative circuit architecture that allows fast and precise manipulation of its output frequency under full digital control. DDS also enables very high resolution in the incremental selection of output frequency; the AD9850 allows an output frequency resolution of 0.0291 Hz with a 125 MHz reference clock applied. The AD9850's output waveform is phase continuous when changed.

The basic functional block diagram and signal flow of the AD9850 configured as a clock generator is shown in Figure 4.

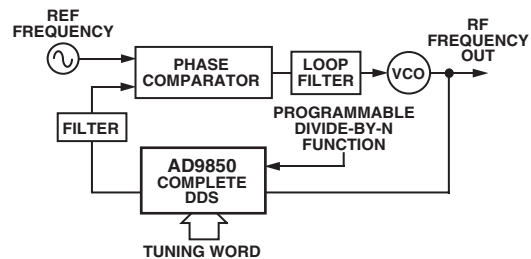
The DDS circuitry is basically a digital frequency divider function whose incremental resolution is determined by the frequency of the reference clock divided by the  $2^N$  number of bits in the tuning word. The phase accumulator is a variable-modulus counter that increments the number stored in it each time it receives a clock pulse. When the counter overflows, it wraps around, making the phase accumulator's output contiguous.



3a. Frequency/Phase-Agile Local Oscillator



3b. Frequency/Phase-Agile Reference for PLL



3c. Digitally-Programmable Divide-by-N Function in PLL

Figure 3. AD9850 Complete DDS Synthesizer in Frequency Up-Conversion Applications

The frequency tuning word sets the modulus of the counter, which effectively determines the size of the increment ( $\Delta$  Phase) that is added to the value in the phase accumulator on the next clock pulse. The larger the added increment, the faster the accumulator overflows, which results in a higher output frequency. The AD9850 uses an innovative and proprietary algorithm that mathematically converts the 14-bit truncated value of the phase accumulator to the appropriate COS value. This unique algorithm uses a much reduced ROM look-up table and DSP techniques to perform this function, which contributes to the small size and low power dissipation of the AD9850. The relationship of the output frequency, reference clock, and tuning word of the AD9850 is determined by the formula

$$f_{OUT} = (\Delta \text{ Phase} \times CLKIN) / 2^{32}$$

where:

$\Delta$  Phase is the value of the 32-bit tuning word.

CLKIN is the input reference clock frequency in MHz.

$f_{OUT}$  is the frequency of the output signal in MHz.

The digital sine wave output of the DDS block drives the internal high speed 10-bit D/A converter that reconstructs the sine wave in analog form. This DAC has been optimized for dynamic performance and low glitch energy as manifested in the low jitter performance of the AD9850. Because the output of the



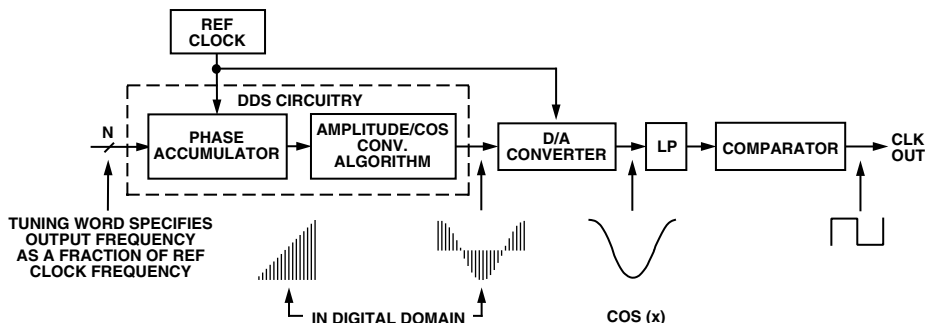


Figure 4. Basic DDS Block Diagram and Signal Flow of AD9850

AD9850 is a sampled signal, its output spectrum follows the Nyquist sampling theorem. Specifically, its output spectrum contains the fundamental plus aliased signals (images) that occur at multiples of the reference clock frequency  $\pm$  the selected output frequency. A graphical representation of the sampled spectrum, with aliased images, is shown in Figure 5.

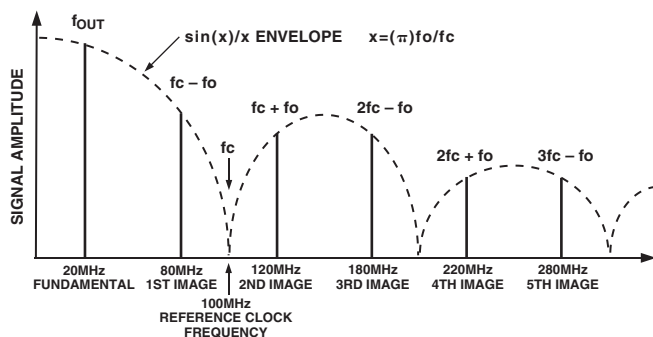


Figure 5. Output Spectrum of a Sampled Signal

In this example, the reference clock is 100 MHz and the output frequency is set to 20 MHz. As can be seen, the aliased images are very prominent and of a relatively high energy level as determined by the  $\sin(x)/x$  roll-off of the quantized D/A converter output. In fact, depending on the  $f_o$ /reference clock relationship, the first aliased image can be on the order of  $-3$  dB below the fundamental. A low-pass filter is generally placed between the output of the D/A converter and the input of the comparator to further suppress the effects of aliased images. Obviously, consideration must be given to the relationship of the selected output frequency and the reference clock frequency to avoid unwanted (and unexpected) output anomalies.

To apply the AD9850 as a clock generator, limit the selected output frequency to  $<33\%$  of reference clock frequency, and thereby avoid generating aliased signals that fall within, or close to, the output band of interest (generally dc-selected output frequency). This practice eases the complexity (and cost) of the external filter requirement for the clock generator application.

The reference clock frequency of the AD9850 has a minimum limitation of 1 MHz. The device has internal circuitry that senses when the minimum clock rate threshold has been exceeded

and automatically places itself in the power-down mode. When in this state, if the clock frequency again exceeds the threshold, the device resumes normal operation. This shutdown mode prevents excessive current leakage in the dynamic registers of the device.

The D/A converter output and comparator inputs are available as differential signals that can be flexibly configured in any manner desired to achieve the objectives of the end system. The typical application of the AD9850 is with single-ended output/input analog signals, a single low-pass filter, and the generation of the comparator reference midpoint from the differential DAC output as shown in Figure 1.

#### Programming the AD9850

The AD9850 contains a 40-bit register that is used to program the 32-bit frequency control word, the 5-bit phase modulation word, and the power-down function. This register can be loaded in a parallel or serial mode.

In the parallel load mode, the register is loaded via an 8-bit bus; the full 40-bit word requires five iterations of the 8-bit word. The  $W\_CLK$  and  $FQ\_UD$  signals are used to address and load the registers. The rising edge of  $FQ\_UD$  loads the (up to) 40-bit control data-word into the device and resets the address pointer to the first register. Subsequent  $W\_CLK$  rising edges load the 8-bit data on words [7:0] and move the pointer to the next register. After *five* loads,  $W\_CLK$  edges are ignored until either a reset or an  $FQ\_UD$  rising edge resets the address pointer to the first register.

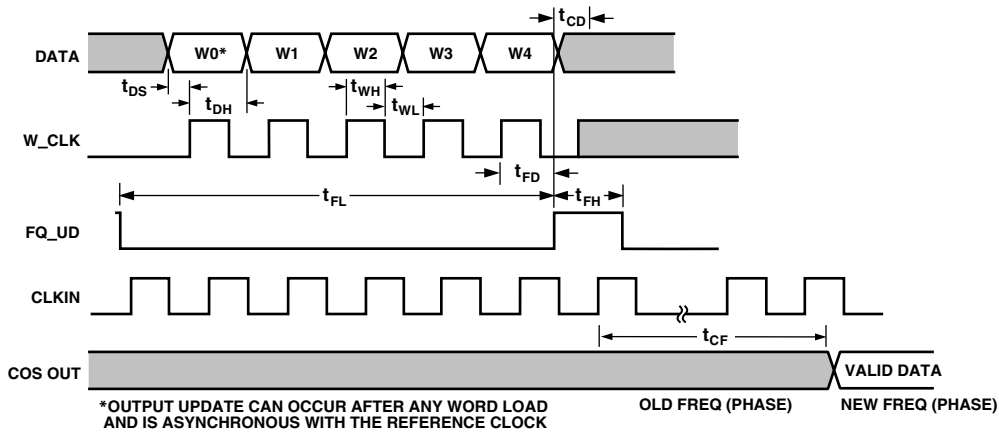
In serial load mode, subsequent rising edges of  $W\_CLK$  shift the 1-bit data on Pin 25 (D7) through the 40 bits of programming information. After 40 bits are shifted through, an  $FQ\_UD$  pulse is required to update the output frequency (or phase).

The function assignments of the data and control words are shown in Table III; the detailed timing sequence for updating the output frequency and/or phase, resetting the device, and powering up/down, are shown in the timing diagrams of Figures 6 through 12.

Note: There are specific control codes, used for factory test purposes, that render the AD9850 temporarily inoperable. The user must take deliberate precaution to avoid inputting the codes listed in Table II.

**Table II. Factory Reserved Internal Test Control Codes**

| Loading Format | Factory Reserved Codes  |
|----------------|---|
| Parallel       | 1) W0 = XXXXXX10<br>2) W0 = XXXXXX01                              |
| Serial         | 1) W32 = 1; W33 = 0<br>2) W32 = 0; W33 = 1<br>3) W32 = 1; W33 = 1 |



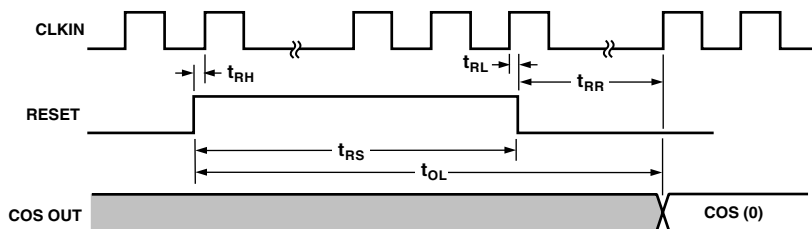
\*OUTPUT UPDATE CAN OCCUR AFTER ANY WORD LOAD AND IS ASYNCHRONOUS WITH THE REFERENCE CLOCK

| SYMBOL   | DEFINITION                | MINIMUM         |
|----------|---------------------------|-----------------|
| $t_{DS}$ | DATA SETUP TIME           | 3.5ns           |
| $t_{DH}$ | DATA HOLD TIME            | 3.5ns           |
| $t_{WH}$ | W_CLK HIGH                | 3.5ns           |
| $t_{WL}$ | W_CLK LOW                 | 3.5ns           |
| $t_{CD}$ | CLK DELAY AFTER FQ_UD     | 3.5ns           |
| $t_{FH}$ | FQ_UD HIGH                | 7.0ns           |
| $t_{FL}$ | FQ_UD LOW                 | 7.0ns           |
| $t_{FD}$ | FQ_UD DELAY AFTER W_CLK   | 7.0ns           |
| $t_{CF}$ | OUTPUT LATENCY FROM FQ_UD |                 |
|          | FREQUENCY CHANGE          | 18 CLOCK CYCLES |
|          | PHASE CHANGE              | 13 CLOCK CYCLES |

Figure 6. Parallel Load Frequency/Phase Update Timing Sequence

**Table III. 8-Bit Parallel Load Data/Control Word Functional Assignment**

| Word | Data[7]        | Data[6]  | Data[5]  | Data[4]  | Data[3]        | Data[2]    | Data[1]  | Data[0]       |
|------|----------------|----------|----------|----------|----------------|------------|----------|---------------|
| W0   | Phase-b4 (MSB) | Phase-b3 | Phase-b2 | Phase-b1 | Phase-b0 (LSB) | Power-Down | Control  | Control       |
| W1   | Freq-b31 (MSB) | Freq-b30 | Freq-b29 | Freq-b28 | Freq-b27       | Freq-b26   | Freq-b25 | Freq-b24      |
| W2   | Freq-b23       | Freq-b22 | Freq-b21 | Freq-b20 | Freq-b19       | Freq-b18   | Freq-b17 | Freq-b16      |
| W3   | Freq-b15       | Freq-b14 | Freq-b13 | Freq-b12 | Freq-b11       | Freq-b10   | Freq-b9  | Freq-b8       |
| W4   | Freq-b7        | Freq-b6  | Freq-b5  | Freq-b4  | Freq-b3        | Freq-b2    | Freq-b1  | Freq-b0 (LSB) |



NOTE: THE TIMING DIAGRAM ABOVE SHOWS THE MINIMAL AMOUNT OF RESET TIME NEEDED BEFORE WRITING TO THE DEVICE. HOWEVER, THE MASTER RESET DOES NOT HAVE TO BE SYNCHRONOUS WITH THE CLKIN IF THE MINIMAL TIME IS NOT REQUIRED.

| SYMBOL   | DEFINITION                        | MINIMUM       |
|----------|-----------------------------------|---------------|
| $t_{RH}$ | CLK DELAY AFTER RESET RISING EDGE | 3.5ns         |
| $t_{RL}$ | RESET FALLING EDGE AFTER CLK      | 3.5ns         |
| $t_{RR}$ | RECOVERY FROM RESET               | 2 CLK CYCLES  |
| $t_{RS}$ | MINIMUM RESET WIDTH               | 5 CLK CYCLES  |
| $t_{OL}$ | RESET OUTPUT LATENCY              | 13 CLK CYCLES |

- RESULTS OF RESET:
- FREQUENCY/PHASE REGISTER SET TO 0
  - ADDRESS POINTER RESET TO W0
  - POWER-DOWN BIT RESET TO 0
  - DATA INPUT REGISTER UNEFFECTED

Figure 7. Master Reset Timing Sequence

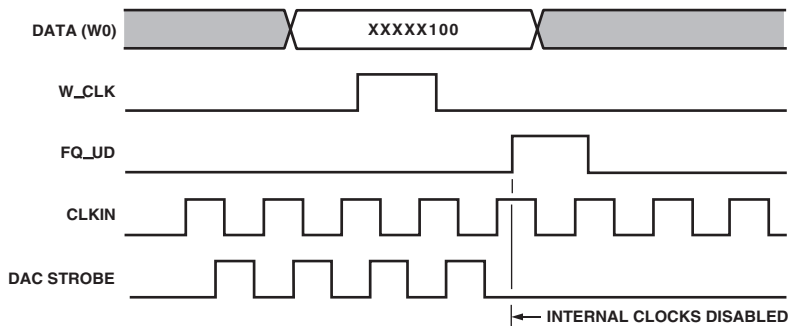


Figure 8. Parallel Load Power-Down Sequence/Internal Operation

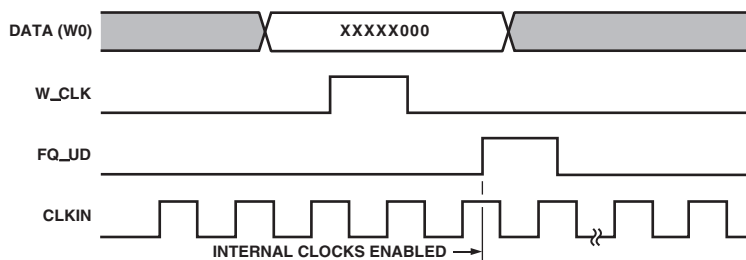


Figure 9. Parallel Load Power-Up Sequence/Internal Operation

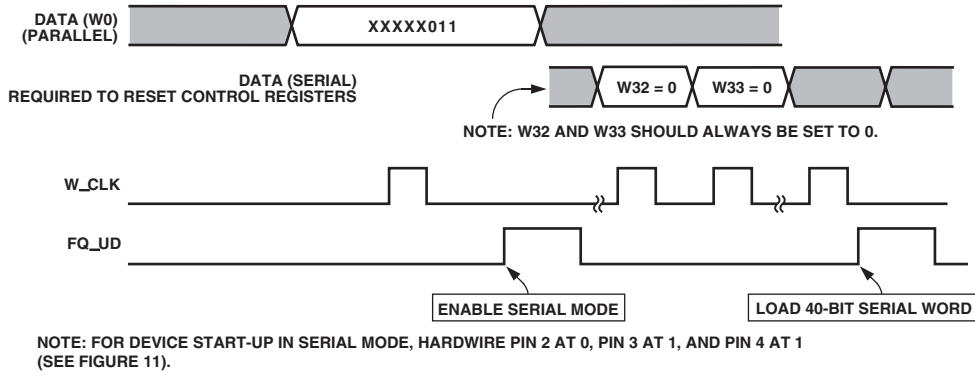


Figure 10. Serial Load Enable Sequence

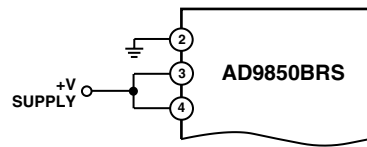


Figure 11. Pins 2 to 4 Connection for Default Serial Mode Operation

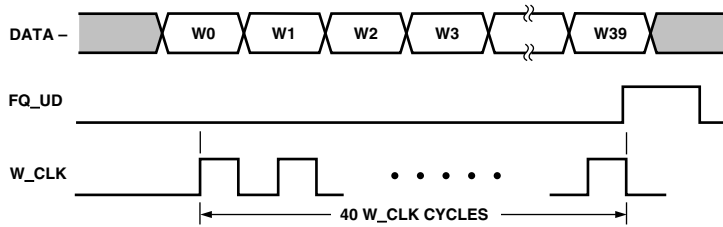


Figure 12. Serial Load Frequency/Phase Update Sequence

Table IV. 40-Bit Serial Load Word Function Assignment

|     |               |     |          |     |                |
|-----|---------------|-----|----------|-----|----------------|
| W0  | Freq-b0 (LSB) | W14 | Freq-b14 | W28 | Freq-b28       |
| W1  | Freq-b1       | W15 | Freq-b15 | W29 | Freq-b29       |
| W2  | Freq-b2       | W16 | Freq-b16 | W30 | Freq-b30       |
| W3  | Freq-b3       | W17 | Freq-b17 | W31 | Freq-b31 (MSB) |
| W4  | Freq-b4       | W18 | Freq-b18 | W32 | Control        |
| W5  | Freq-b5       | W19 | Freq-b19 | W33 | Control        |
| W6  | Freq-b6       | W20 | Freq-b20 | W34 | Power-Down     |
| W7  | Freq-b7       | W21 | Freq-b21 | W35 | Phase-b0 (LSB) |
| W8  | Freq-b8       | W22 | Freq-b22 | W36 | Phase-b1       |
| W9  | Freq-b9       | W23 | Freq-b23 | W37 | Phase-b2       |
| W10 | Freq-b10      | W24 | Freq-b24 | W38 | Phase-b3       |
| W11 | Freq-b11      | W25 | Freq-b25 | W39 | Phase-b4 (MSB) |
| W12 | Freq-b12      | W26 | Freq-b26 |     |                |
| W13 | Freq-b13      | W27 | Freq-b27 |     |                |

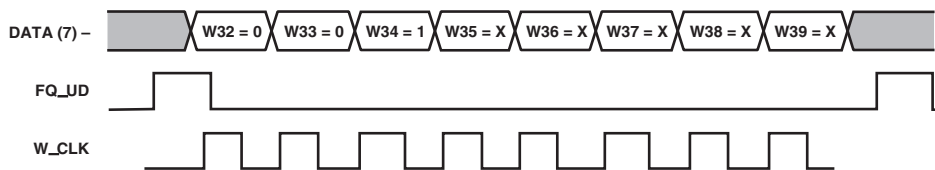


Figure 13. Serial Load Power-Down Sequence

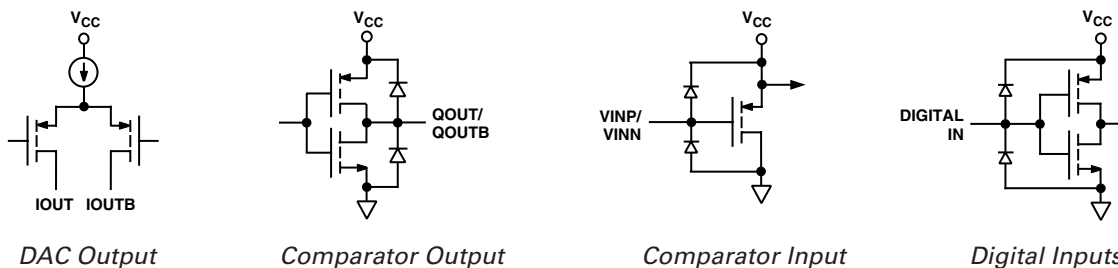


Figure 14. AD9850 I/O Equivalent Circuits

### PCB LAYOUT INFORMATION

The AD9850/CGPCB and AD9850/FSPCB evaluation boards (Figures 15 through 18) represent typical implementations of the AD9850 and exemplify the use of high frequency/high resolution design and layout practices. The printed circuit board that contains the AD9850 should be a multilayer board that allows dedicated power and ground planes. The power and ground planes should be free of etched traces that cause discontinuities in the planes. It is recommended that the top layer of the multilayer board also contain an interspatial ground plane, which makes ground available for surface-mount devices. If separate analog and digital system ground planes exist, they should be connected together at the AD9850 for optimum results.

Avoid running digital lines under the device because these couple noise onto the die. The power supply lines to the AD9850 should use as large a track as possible to provide a low impedance path and reduce the effects of glitches on the power supply line. Fast switching signals like clocks should be shielded with ground to avoid radiating noise to other sections of the board. Avoid crossover of digital and analog signal paths. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the circuit board. Use microstrip techniques where possible.

Good decoupling is also an important consideration. The analog (AVDD) and digital (DVDD) supplies to the AD9850 are independent and separately pinned out to minimize coupling between analog and digital sections of the device. All analog and digital supplies should be decoupled to AGND and DGND, respectively, with high quality ceramic capacitors. To achieve best performance from the decoupling capacitors, they should be placed as close as possible to the device, ideally right up against the device. In systems where a common supply is used to drive both the AVDD and DVDD supplies of the AD9850, it is recommended that the system's AVDD supply be used.

Analog Devices, Inc. applications engineering support is available to answer additional questions on grounding and PCB layout. Call 1-800-ANALOGD or contact us at [www.analog.com/dds](http://www.analog.com/dds).

### Evaluation Boards

Two versions of evaluation boards are available for the AD9850, which facilitate the implementation of the device for bench-top analysis and serve as a reference for PCB layout. The AD9850/FSPCB is used in applications where the device is used primarily as a frequency synthesizer. This version facilitates connection of the AD9850's internal D/A converter output to a 50  $\Omega$  spectrum analyzer input; the internal comparator on the AD9850 DUT is not enabled (see Figure 15 for an electrical schematic of AD9850/FSPCB). The AD9850/CGPCB is used in applications using the device in the clock generator mode. It connects the AD9850's DAC output to the internal comparator input via a single-ended, 42 MHz low-pass, 5-pole elliptical filter. This model facilitates the access of the AD9850's comparator output for evaluation of the device as a frequency- and phase-agile clock source (see Figure 17 for an electrical schematic of AD9850/CGPCB).

Both versions of the AD9850 evaluation board are designed to interface to the parallel printer port of a PC. The operating software runs under Microsoft® Windows® and provides a user-friendly and intuitive format for controlling the functionality and observing the performance of the device. The 3.5 inch floppy provided with the evaluation board contains an executable file that loads and displays the AD9850 function-selection screen. The evaluation board can be operated with 3.3 V or 5 V supplies. The evaluation boards are configured at the factory for an external reference clock input; if the on-board crystal clock source is used, remove R2.

# AD9850

## AD9850 Evaluation Board Instructions

### Required Hardware/Software

- IBM compatible computer operating in a Windows environment.
- Printer port, 3.5 inch floppy drive, and Centronics compatible printer cable.
- XTAL clock or signal generator—if using a signal generator, dc offset the signal to one-half the supply voltage and apply at least 3 V p-p signal across the 50  $\Omega$  (R2) input resistor. Remove R2 for high Z clock input.
- AD9850 evaluation board software disk and AD9850/FSPCB or AD9850/CGPCB evaluation board.
- 5 V voltage supply.

### Setup

1. Copy the contents of the AD9850 disk onto your hard drive (there are three files).
2. Connect the printer cable from your computer to the AD9850 evaluation board.
3. Apply power to AD9850 evaluation board. The AD9850 is powered separately from the connector marked DUT +V. The AD9850 may be powered with 3.3 V to 5 V.
4. Connect external 50  $\Omega$  clock or remove R2 and apply a high Z input clock such as a crystal can oscillator.
5. Locate the file called 9850REV2.EXE and execute that program.
6. Monitor should display a control panel to allow operation of the AD9850 evaluation board.

### Operation

On the control panel, locate the box called COMPUTER I/O. Point to and click the selection marked LPT1 and then point to the TEST box and click. A message will appear telling users if their choice of output ports is correct. Choose other ports as necessary to achieve a correct setting. If they have trouble getting their computer to recognize any printer port, they should try the following: connect three 2 k $\Omega$  pull-up resistors from Pins 9, 8, and 7 of U3 to 5 V. This will assist weak printer port outputs in driving the heavy capacitance load of the printer cable. If troubles persist, try a different printer cable.

Locate the MASTER RESET button with the mouse and click it. This will reset the AD9850 to 0 Hz, 0° phase. The output should be a dc voltage equal to the full-scale output of the AD9850.

Locate the CLOCK box and place the cursor in the frequency box. Type in the clock frequency (in MHz) that the user will be applying to the AD9850. Click the LOAD button or press enter on the keyboard.

Move the cursor to the OUTPUT FREQUENCY box and type in the desired output frequency (in MHz). Click the LOAD button or press the enter key. The BUS MONITOR section of the control panel will show the 32-bit word that was loaded into the AD9850. Upon completion of this step, the AD9850 output should be active and outputting the user's frequency information.

Changing the output phase is accomplished by clicking on the down arrow in the OUTPUT PHASE DELAY box to make a selection and then clicking the LOAD button.

Other operational modes (frequency sweeping, sleep, serial input) are available to the user via keyboard/mouse control.

The AD9850/FSPCB provides access into and out of the on-chip comparator via test point pairs (each pair has an active input and a ground connection). The two active inputs are labeled TP1 and TP2. The unmarked hole next to each labeled test point is a ground connection. The two active outputs are labeled TP5 and TP6. Unmarked ground connections are adjacent to each of these test points.

The AD9850/CGPCB provides BNC inputs and outputs associated with the on-chip comparator and the on-board, fifth-order, 200  $\Omega$  input/output Z, elliptic, 45 MHz, low-pass filter. Jumpering (soldering a wire) E1 to E2, E3 to E4, and E5 to E6 connects the on-board filter and the midpoint switching voltage to the comparator. Users may elect to insert their own filter and comparator threshold voltage by removing the jumpers and inserting a filter between J7 and J6 and then providing a threshold voltage at E1.

If users choose to use the XTAL socket to supply the clock to the AD9850, they must remove R2 (a 50  $\Omega$  chip resistor). The crystal oscillator must be either TTL or CMOS (preferably) compatible.

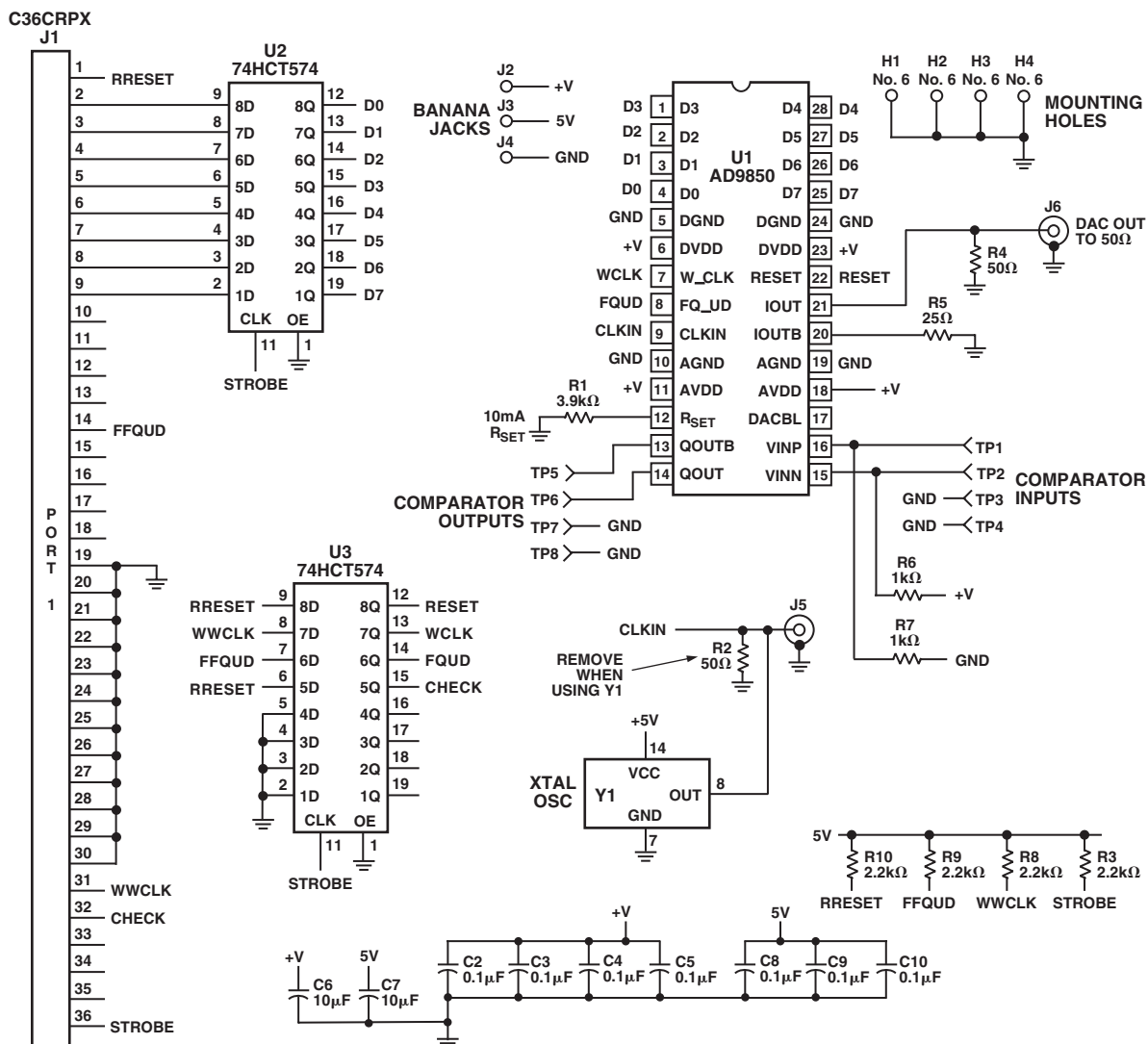


Figure 15. AD9850/FSPCB Electrical Schematic

## COMPONENT LIST

### Integrated Circuits

U1 AD9850BRS (28-Lead SSOP)  
 U2, U3 74HCT574 H-CMOS Octal Flip-Flop

### Capacitors

C2 to C5, C8 to C10 0.1 µF Ceramic Chip Capacitor  
 C6, C7 10 µF Tantalum Chip Capacitor

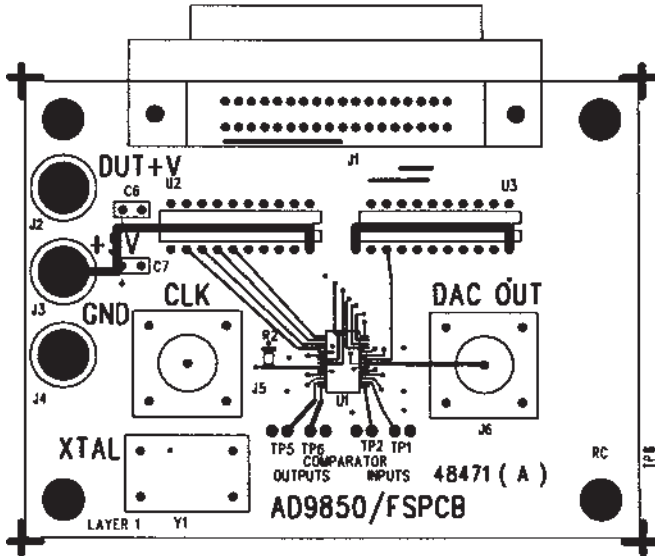
### Resistors

R1 3.9 kΩ Resistor  
 R2, R4 50 Ω Resistor  
 R3, R8, R9, R10 2.2 kΩ Resistor  
 R5 25 Ω Resistor  
 R6, R7 1 kΩ Resistor

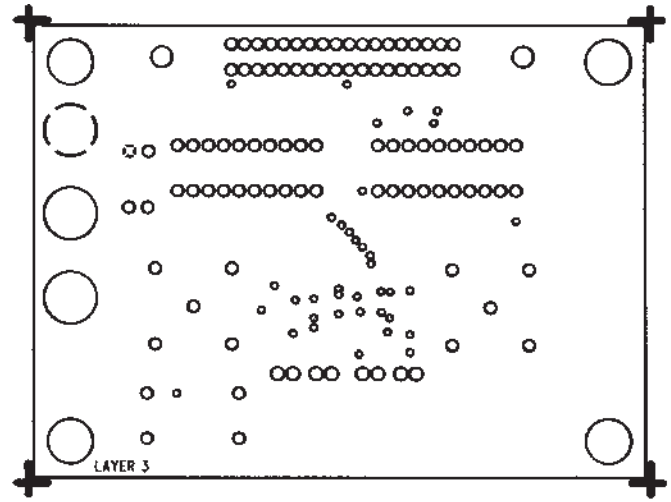
### Connectors

J1 36-Pin D Connector  
 J2, J3, J4 Banana Jack  
 J5, J6 BNC Connector

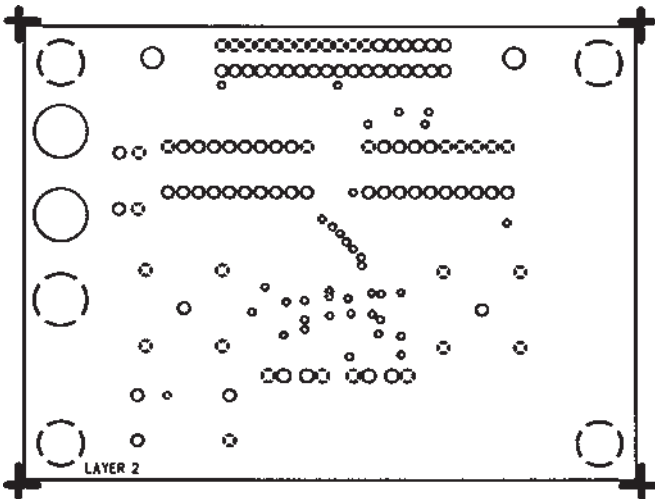
# AD9850



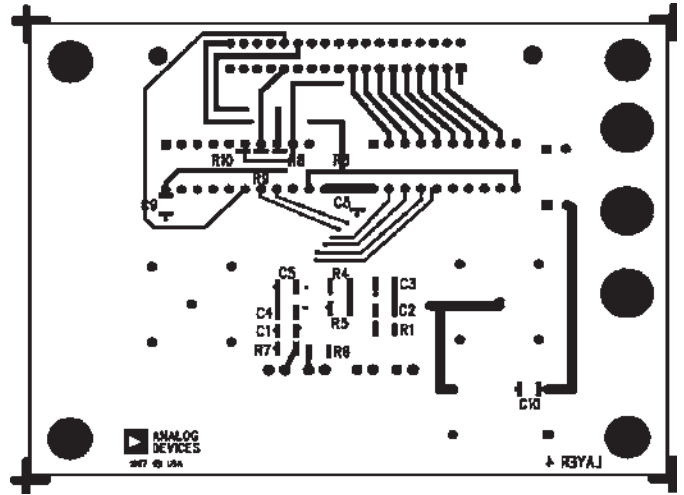
16a. AD9850/FSPCB Top Layer



16c. AD9850/FSPCB Power Plane



16b. AD9850/FSPCB Ground Plane



16d. AD9850/FSPCB Bottom Layer

Figure 16. AD9850/FSPCB Evaluation Board Layout



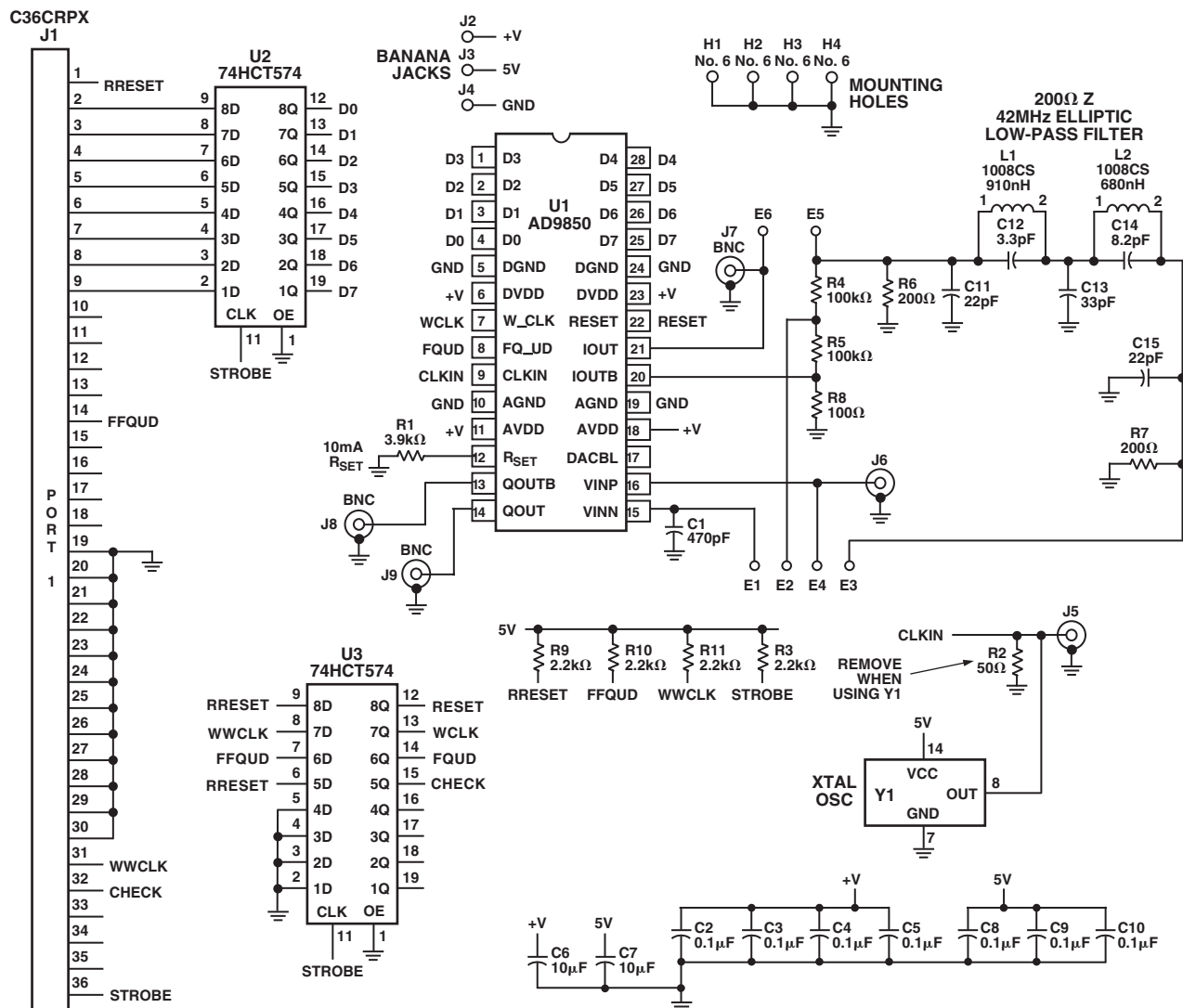


Figure 17. AD9850/CGPCB Electrical Schematic

## COMPONENT LIST

### Integrated Circuits

|        |                                 |
|--------|---------------------------------|
| U1     | AD9850BRS (28-Lead SSOP)        |
| U2, U3 | 74HCT574 H-CMOS Octal Flip-Flop |

### Capacitors

|                     |                                    |
|---------------------|------------------------------------|
| C1                  | 470 pF Ceramic Chip Capacitor      |
| C2 to C5, C8 to C10 | 0.1 $\mu$ F Ceramic Chip Capacitor |
| C6, C7              | 10 $\mu$ F Tantalum Chip Capacitor |
| C11                 | 22 pF Ceramic Chip Capacitor       |
| C12                 | 3.3 pF Ceramic Chip Capacitor      |
| C13                 | 33 pF Ceramic Chip Capacitor       |
| C14                 | 8.2 pF Ceramic Chip Capacitor      |
| C15                 | 22 pF Ceramic Chip Capacitor       |

### Resistors

|                  |                         |
|------------------|-------------------------|
| R1               | 3.9 k $\Omega$ Resistor |
| R2               | 50 $\Omega$ Resistor    |
| R3, R9, R10, R11 | 2.2 k $\Omega$ Resistor |
| R4, R5           | 100 k $\Omega$ Resistor |
| R6, R7           | 200 $\Omega$ Resistor   |
| R8               | 100 $\Omega$ Resistor   |

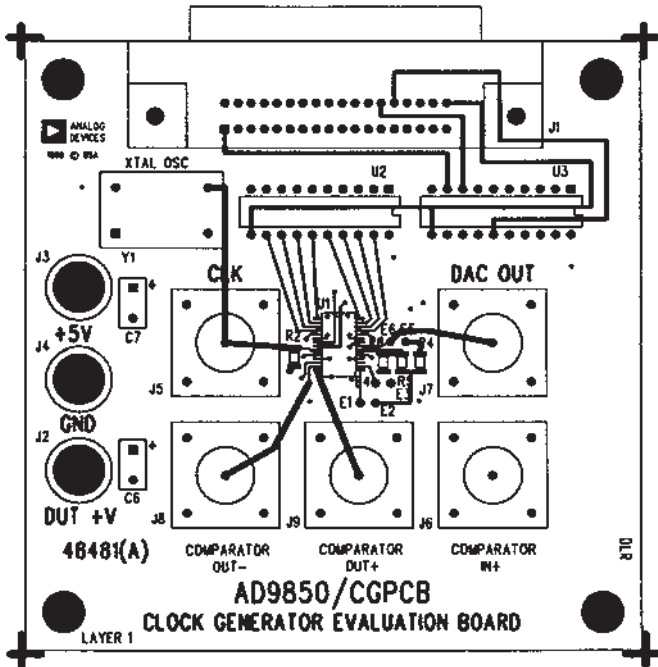
### Connectors

|            |               |
|------------|---------------|
| J2, J3, J4 | Banana Jack   |
| J5 to J9   | BNC Connector |

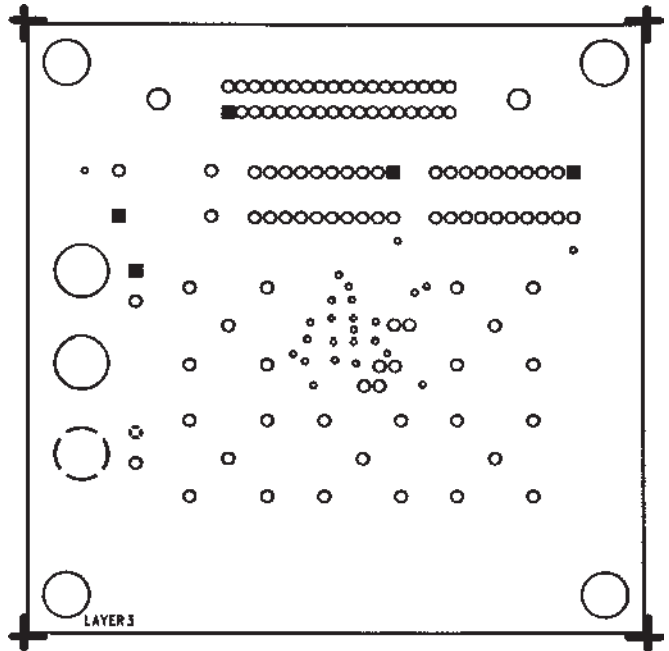
### Inductors

|    |                      |
|----|----------------------|
| L1 | 910 nH Surface Mount |
| L2 | 680 nH Surface Mount |

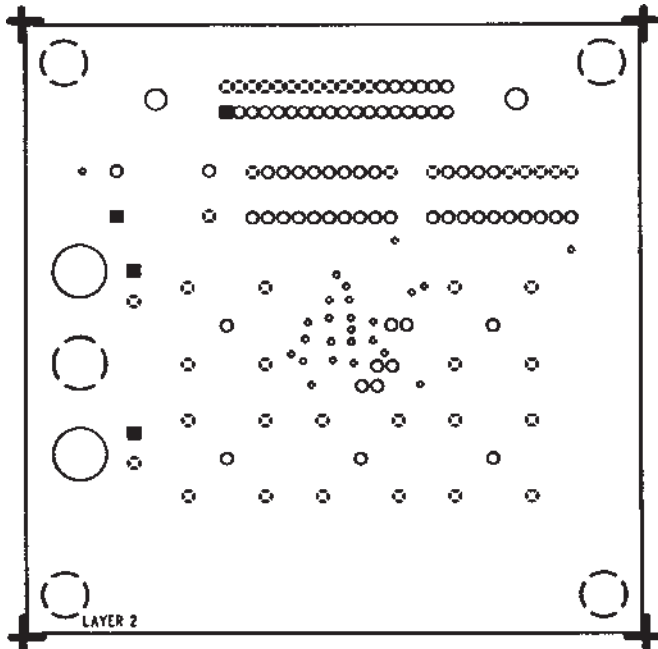
# AD9850



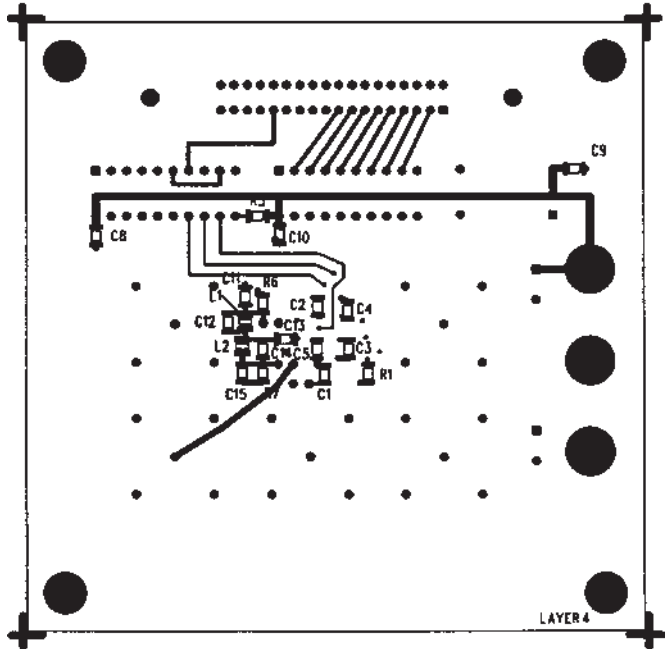
18a. AD9850/CGPCB Top Layer



18c. AD9850/CGPCB Power Plane



18b. AD9850/CGPCB Ground Plane



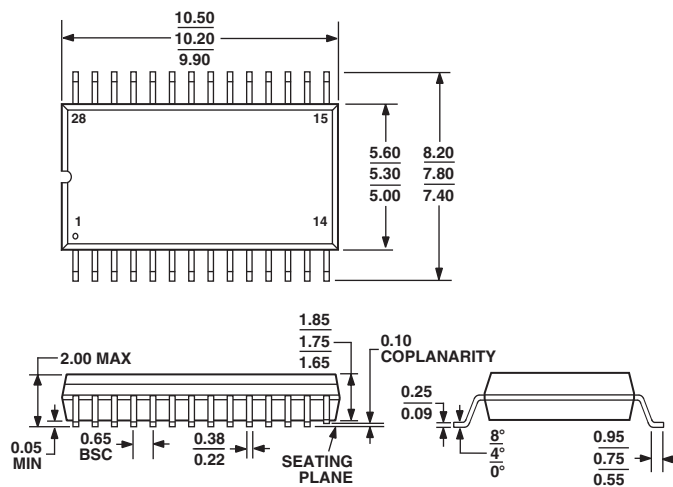
18d. AD9850/CGPCB Bottom Layer

Figure 18. AD9850/CGPCB Evaluation Board Layout

OUTLINE DIMENSIONS

28-Lead Shrink Small Outline Package [SSOP]  
(RS-28)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-150AH

# AD9850

## Revision History

| <b>Location</b>  | <b>Page</b> |
|--|-------------|
| <b>2/04—Data Sheet changed from REV. G to REV. H.</b>  |             |
| Changes to SPECIFICATIONS .....                        | 3           |
| <b>12/03—Data Sheet changed from REV. F to REV. G.</b> |             |
| Changes to SPECIFICATIONS .....                        | 3           |
| Changes to Table I .....                               | 5           |
| <b>11/03—Data Sheet changed from REV. E to REV. F.</b> |             |
| Renumbered figures and TPCs .....                      | Universal   |
| Changes to SPECIFICATIONS .....                        | 2           |
| Changes to ABSOLUTE MAXIMUM RATINGS .....              | 3           |
| Updated ORDERING GUIDE .....                           | 4           |
| Updated OUTLINE DIMENSIONS .....                       | 9           |

C00632-0-2/04(H)

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### Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: [info@moschip.ru](mailto:info@moschip.ru)

Skype отдела продаж:

moschip.ru

moschip.ru\_4

moschip.ru\_6

moschip.ru\_9