Introduction

The LogiCORE™ IP Common Public Radio Interface (CPRI™) core is a high-performance, low-cost flexible solution for implementation of the CPRI interface. It uses state-of-the-art transceivers to implement the Physical Layer. A compact and customizable Data Link Layer is implemented in the FPGA logic.

Additional Documentation

A product guide is available for this core. Access to this material can be requested by going to the CPRI Documentation Lounge.

Features

- UltraScale™ architecture-based device designs operate at line rates of 614.4, 1,228.8, 2,457.6, 3,072, 4,915.2, 6,144, 8,110.08, 9,830.4, 10,137.6, 12,165.12, and 24,330.24 Mb/s using GTHE3, GTYE3, GTHE4 or GTYE4 transceivers. 24,330.24 Mb/s line rate with optional RS-FEC supported using GTYE3 or GTYE4 transceivers, or optional 100G Ethernet RS-FEC using GTYE4 transceivers on selected UltraScale+ parts.

- Zynq®-7000, Virtex®-7, and Kintex®-7 device designs operate at line rates of 614.4, 1,228.8, 2,457.6, 3,072, 4,915.2, 6,144, 9,830.4, 10,137.6, and 12,165.12 Mb/s using GTXE2, GTHE2 transceivers.

- Artix®-7 devices designs operate at line rates of 614.4, 1,228.86 2,457.6, 3,072, 4,915.2, and 6,144 Mb/s using GTPE2 transceivers.

LogiCORE IP Facts	
Core Specifics	
Supported Device Family[1]	UltraScale+™[2] UltraScale™ Zynq®-7000 All Programmable SoC[2] 7 Series[3]
Supported User Interfaces	Generic data, status, configuration and management interfaces, AXI4-Lite management interface
Provided with Core	
Design Files	Encrypted register transfer level (RTL)
Example Design	VHDL
Test Bench	VHDL
Constraints File	Xilinx Design Constraints (XDC)
Simulation Models	VHDL, Verilog
Supported S/W Drivers	N/A
Tested Design Flows[4]	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	Vivado Synthesis
Support	
Provided by Xilinx at the Xilinx Support web page	

Notes:

1. For a complete list of supported devices, see the Vivado IP catalog.
2. Excludes Zynq-7000 007, 010, 014 and 020 devices.
   Excludes Zynq UltraScale+ devices 2cg, 2eg, 3cg and 3eg.
3. Excludes the Artix-7 100T device in CSG324, FTG256 and CS 324 packages.
   Excludes Spartan®-7 devices
4. For the supported version of the tool, see the Xilinx Design Tools: Release Notes Guide.

Features (continued)

- Automatic speed negotiation

- Supports both Fast (Ethernet) and Slow High-Level Data Link Control (HDLC) Control and Management (C&M) channels per the *CPRI Specification* v7.0 [Ref 1].

- Can be configured as a master or slave at generation time. Master core can be switched to operate as a slave through a configuration port.

- Suitable for use in both Radio Equipment Controllers (RECs) and Radio Equipment (RE), including multi-hop systems.

- Easy-to-use interface for in-phase (I) and quadrature-phase (Q) data and synchronization together with optional modules for UMTS terrestrial radio access - frequency division duplexing (UTRA-FDD) and Evolved UMTS Terrestrial Radio Access (E-UTRA) data mappings.

- Supports vendor specific data transport including support for the passing of control AxC information in global system for mobile communications (GSM) systems

- Delay measurement capability meets CPRI Requirement 21 per *CPRI Specification v7.0* [Ref 1]

- Includes the necessary clocking and transceiver logic to enable easy integration into your design

- Synthesizable example design and simple demonstration test bench provided

- Optional Reed-Solomon Forward error correction (RS-FEC) supported at 8,110.08, 10,137.6, 12,165.12 and 24,330.24 Mb/s line rates

- Optional 100G Ethernet RS-FEC supported at a fixed 24,330.24 Mb/s line rate on selected UltraScale+ devices using GTYE4 transceivers

- CPRI core can be converted into a four lane Receiver Hard FEC IP running at a fixed 24,330.24 Mb/s line rate, on UltraScale+ devices with 100G Ethernet RS-FEC support

- UTRA-FDD in-phase and quadrature-phase data (I/Q) module supporting 1 to 48 Antenna-Carriers per core

Overview

The CPRI core implements Layer 1 and Layer 2 of the CPRI specification in UltraScale architecture-based, Zynq-7000, Virtex-7, Kintex-7, and Artix-7 devices. The CPRI core provides these client-side interfaces.

- **I/Q Interface.** Consists of a stream of radio data (I/Q samples) that is synchronized to the Universal Mobile Telecommunications System (UMTS) radio frame pulse.

- **Synchronization Interface.** Provides the means for the client logic to synchronize to the network time by transmitting the UMTS radio frame pulse and clock frequency.

- **High-Level Data Link Control (HDLC) Interface.** Transports management information between master and slave. The HDLC interface is serialized and synchronous.

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- **Ethernet Interface.** When configured to support speeds of up to 3,072 Mb/s, the Ethernet interface is presented as a Media Independent Interface (MII); this allows a 100 Mb Ethernet Media Access Controller (MAC) to be attached to the core to provide a high-speed channel for management information. When speeds over 4,915.2 Mb/s are supported, a Gigabit Media Independent Interface (GMII) option is available. This allows a 1 Gb Ethernet MAC to be attached to the core. The core includes an Ethernet frame buffer in both transmit and receive directions.

- **Vendor-Specific Data Interface.** Provides client logic access to the vendor-specific sub-channels in the CPRI stream.

- **Management Interface.** Provides control and status registers that allow management of the entire design from a supervisory processor. An AXI4-Lite option is available.

The architecture of the core is shown in Figure 1. In addition to the interfaces described previously, the core contains these blocks:

- **Status/Alarm Block.** Reflects the internal state of the core and the state of the link.

- **Start-up Sequencer.** Performs line-rate negotiation and Control and Management (C&M) parameter negotiation at link start-up. This block continuously monitors the state of the link and sends the status to the alarm block.

- **UMTS Terrestrial Radio Access - Frequency Division Duplexing (UTRA FDD) I/Q Module:** A pluggable I/Q module to support multiplexing and demultiplexing of I/Q samples in UTRA FDD systems (shown in Figure 1).

- **Evolved UMTS Terrestrial Radio Access (E-UTRA) I/Q Module**: A pluggable I/Q module to support multiplexing and demultiplexing of I/Q samples in E-UTRA systems (not shown in Figure 1).

- **Legacy raw I/Q Module**: A pluggable I/Q Module for backward compatibility with the raw interfacing timing for v1.x CPRI cores (not shown in Figure 1).

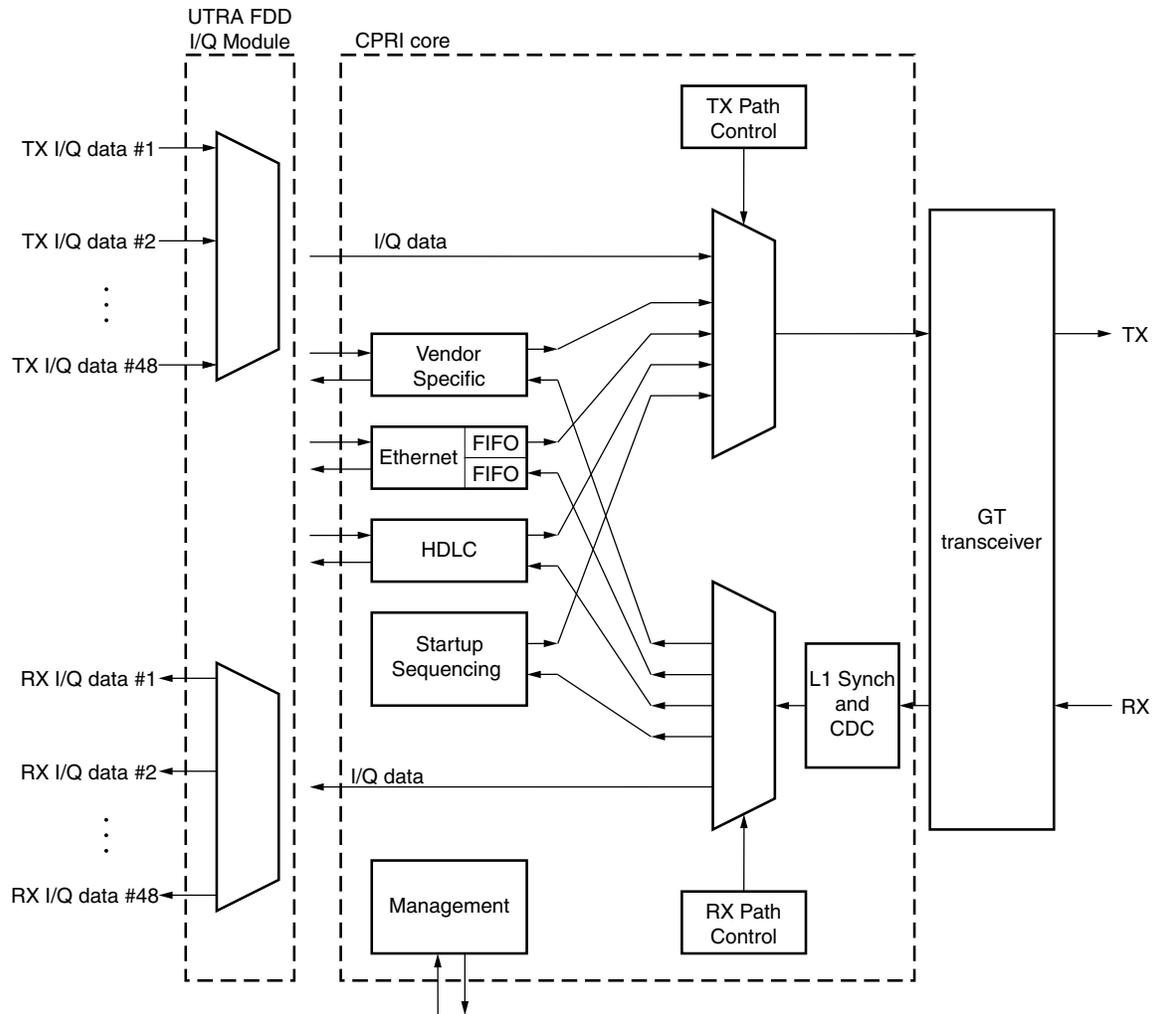Send Feedback

Figure 1: **CPRI Top-Level Block Diagram**

References

To search for Xilinx documentation, go to the Xilinx Support web page.

1. *CPRI Specification v7.0*, October 9, 2015

2. *IEEE Std. 802.3-2005 (*standards.ieee.org/getieee802/)

3. *Vivado AXI Reference Guide (*UG1037)

4. *Vivado Design Suite User Guide: Designing with IP (*UG896)

Technical Support

Xilinx provides technical support at the Xilinx Support web page for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

• Implement the solution in devices that are not defined in the documentation.

• Customize the solution beyond that allowed in the product documentation.

• Change any section of the design labeled DO NOT MODIFY.

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For more information about the CPRI core and about obtaining a license, visit the CPRI product page.

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Related Information

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Revision History

Date	Version	Revision
10/4/2017	8.8	• Added support for 100G Ethernet hard RS-FEC in UltraScale+ parts • Replaced fifo generator instance with xpm_fifo • Added freerun clock rate field to GUI - used by UltraScale GT wizard reset block
05/04/2017	8.7	• Added stat_rx_delay_value port • Added 24,330.24 Mb/s support on UltraScale+ -1 speed grade devices
10/05/2016	8.7	• Added 24,330.24 Mb/s support for GTYE4-based devices • Added Reed-Solomon Forward Error Correction
04/06/2016	8.6	• Added 24,330.24 Mb/s support with a 64-bit datapath option • Added 12,165.12 Mb/s to Kintex-7, Zynq-7000 and Virtex-7 devices • Added debug register and enhanced FIFO transit time registers
11/18/2015	8.5	• Added support for UltraScale+ families. • Added support for GTYE3, GTHE4, and GTYE4 transceivers. • Added 12,165.12 Mb/s support. • Replaced *CPRI Specification v6.0, August 30, 2013* with *CPRI Specification v6.1, July 1, 2014*.
09/30/2015	8.5	• Added UltraScale architecture support for 8,110.08 Mb/s and 12,165.12 Mb/s line rates • Added transceiver location selection for UltraScale devices • Added Ethernet FIFO Fill Level register • Added insertion loss settings for UltraScale device based cores
04/01/2015	8.4	• Changed UltraScale device 10,137.6 Mb/s implementation to use the asynchronous gearbox • Added a software reset feature • Added support for GTYE3 transceivers in Virtex® UltraScale devices
10/01/2014	8.3	• Added speed switching to the 10,137.6 Mb/s capable cores • Added the watchdog timer register • Added the transceiver data monitor interface
06/04/2014	8.2	Associated Product Guide (PG056) updated with parameter table.
04/02/2014	8.2	Added 10137.6 Mb/s line rate
12/18/2013	8.1	• Added UltraScale architecture support • Added transceiver debug interface
10/02/2013	8.0	• Revision number advanced to 8.0 to align with core version number • Added option to bypass the Ethernet frame buffers
03/20/2013	3.0	Updated for Vivado Design Suite and core version 7.0. Removed all ISE design tools and architectures not supported for Vivado.
12/18/2012	2.0	Updated for ISE Design Suite 14.4, Vivado Design Suite 2012.4, and core version 6.1.
07/25/2012	1.0	Initial Xilinx release. Replaces ds611. Data sheet information was incorporated into the new product guide, pg056.

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