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December 2015

FCP650N80Z

N-Channel SuperFET® II MOSFET

800 V, 10 A, 650 mΩ

Features

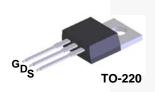
- $R_{DS(on)} = 530 \text{ m}\Omega \text{ (Typ.)}$
- Ultra Low Gate Charge (Typ. Q_q = 27 nC)
- Low E_{oss} (Typ. 2.8 uJ @ 400V)
- Low Effective Output Capacitance (Typ. C_{oss(eff.)} = 124 pF)
- 100% Avalanche Tested
- RoHS Compliant
- · ESD Improved Capability

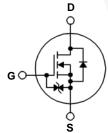
Applications

- AC DC Power Supply
- · LED Lighting

Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. In addition, internal gate-source ESD diode allows to withstand over 2kV HBM surge stress. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as Audio, Laptop adapter, Lighting, ATX power and industrial power applications.





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol		Parameter		FCP650N80Z	Unit
V _{DSS}	Drain to Source Voltage			800	V
V_{GSS}	Cata to Sauraa Valtaga	- DC		±20	V
	Gate to Source Voltage	- AC	(f > 1 Hz)	±30	V
I _D	Drain Current	- Continuous (T _C = 25°C)		10	А
	Drain Current	- Continuous (T _C = 100°C)		6.3	A
I _{DM}	Drain Current	- Pulsed	(Note 1)	24	Α
E _{AS}	Single Pulsed Avalanche Energy	/	(Note 2)	204	mJ
I _{AR}	Avalanche Current		(Note 1)	1.6	Α
E _{AR}	Repetitive Avalanche Energy		(Note 1)	1.62	mJ
al/al#	MOSFET dv/dt			100	1//
dv/dt	Peak Diode Recovery dv/dt (Note 3)		20	V/ns	
D	Davier Dissipation	$(T_C = 25^{\circ}C)$	1 2 2	162	W
P_D	Power Dissipation - Derate Above 25°C			1.30	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range			-55 to +150	°С
TL	Maximum Lead Temperature for	Soldering, 1/8" from Case for 5 S	econds	300	°C

Thermal Characteristics

Symbol	Parameter	FCP650N80Z	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.77	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	10/00

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCP650N80Z	FCP650N80Z	TO-220	Tube	N/A	N/A	50 units

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	teristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}, T_J = 25^{\circ}\text{C}$	800	-	-	V
ΔBV _{DSS} / ΔΤ _J	Breakdown Voltage Temperature Coefficient	I _D = 1 mA, Referenced to 25°C	-	0.8	-	V/°C
1	Zero Gate Voltage Drain Current	V _{DS} = 800 V, V _{GS} = 0 V	-	-	25	μА
IDSS		$V_{DS} = 640 \text{ V}, V_{GS} = 0 \text{ V}, T_{C} = 125^{\circ}\text{C}$	-	-	250	μΑ
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	±10	μΑ

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 0.8 \text{ mA}$	2.5	-	4.5	V
R _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 4 \text{ A}$	-	530	650	mΩ
9 _{FS}	Forward Transconductance	$V_{DS} = 20 \text{ V}, I_{D} = 4 \text{ A}$	-	7.8	-	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 400 V V 0 V	-	1178	1565	pF
C _{oss}	Output Capacitance	$V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1 \text{ MHz}$	- \	36	48	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 101112	- \	0.84	-	pF
C _{oss}	Output Capacitance	$V_{DS} = 480 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	18	-	pF
C _{oss (eff.)}	Effective Output Capacitance	$V_{DS} = 0 \text{ V to } 480 \text{ V}, V_{GS} = 0 \text{ V}$	-	124	-	pF
Q _{g(tot)}	Total Gate Charge at 10V	$V_{DS} = 640 \text{ V}, I_{D} = 8 \text{ A},$	-	27	35	nC
Q_{gs}	Gate to Source Gate Charge	V _{GS} = 10 V	-	6	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	(Note 4)	-	11	-	nC
ESR	Equivalent Series Resistance	f = 1 MHz	-	1.9	-	Ω

Switching Characteristics

t _{d(on)}	Turn-On Delay Time		-	17	44	ns
t _r	Turn-On Rise Time	$V_{DD} = 400 \text{ V}, I_D = 8 \text{ A},$	- /	11	32	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_g = 4.7 \Omega$	-/	40	90	ns
t _f	Turn-Off Fall Time	(Note 4)	-	3.4	17	ns

Drain-Source Diode Characteristics

Is	Maximum Continuous Drain to Source Diode Forward Current		-	-	10	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	24	Α
V_{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 8 A	-	-	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 8 A,	-	365	-	ns
Q _{rr}	Reverse Recovery Charge	$dI_F/dt = 100 A/\mu s$	-	5.9	-	μС

Notes:

- 1. Repetitive rating: pulse width limited by maximum junction temperature.
- 2. I_{AS} = 1.6 A, R_{G} = 25 Ω , Starting T_{J} = 25°C
- 3. $I_{SD} \le 10$ A, di/dt ≤ 200 A/ μs , $V_{DD} \le BV_{DSS}$, Starting T_J = 25°C
- 4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

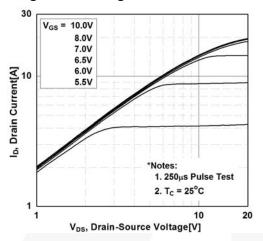


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

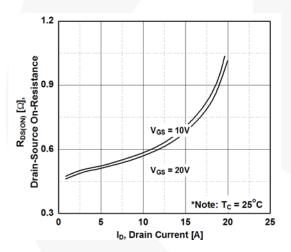


Figure 5. Capacitance Characteristics

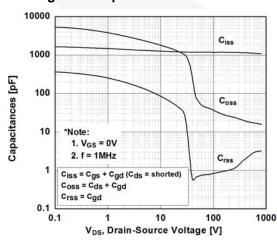


Figure 2. Transfer Characteristics

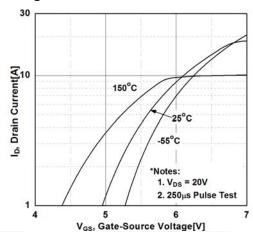


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

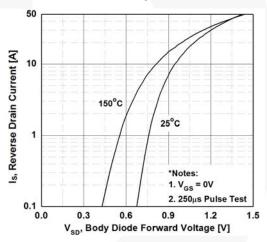
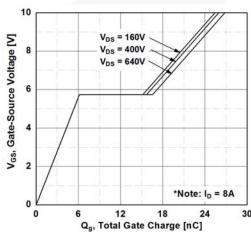


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

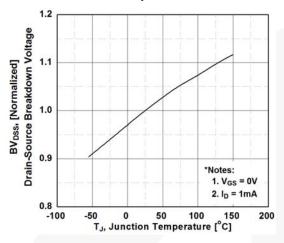


Figure 9. Maximum Safe Operating Area

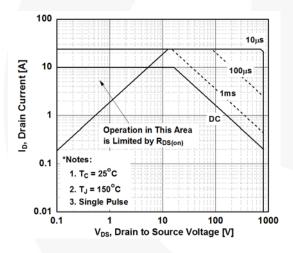


Figure 11. Eoss vs. Drain to Source Voltage

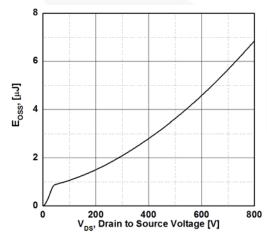


Figure 8. On-Resistance Variation vs. Temperature

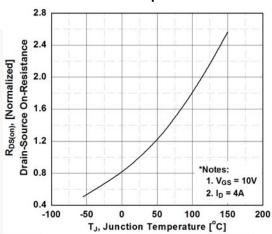
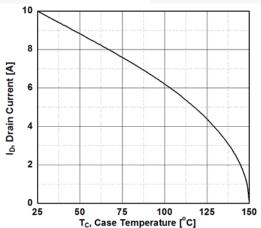
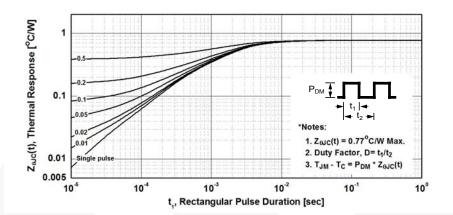


Figure 10. Maximum Drain Current vs. Case Temperature



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



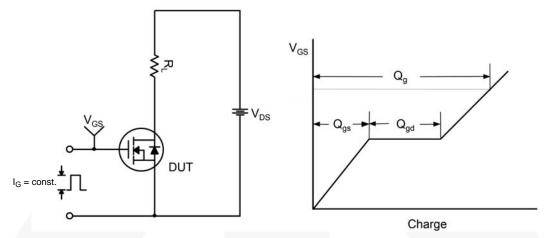


Figure 13. Gate Charge Test Circuit & Waveform

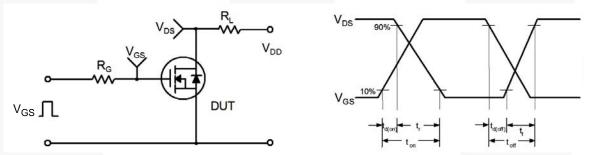


Figure 14. Resistive Switching Test Circuit & Waveforms

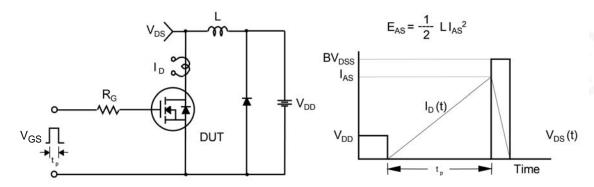


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

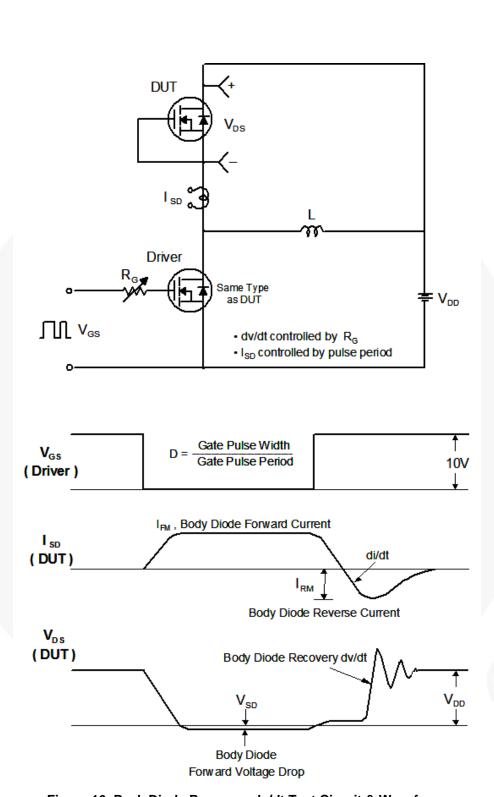
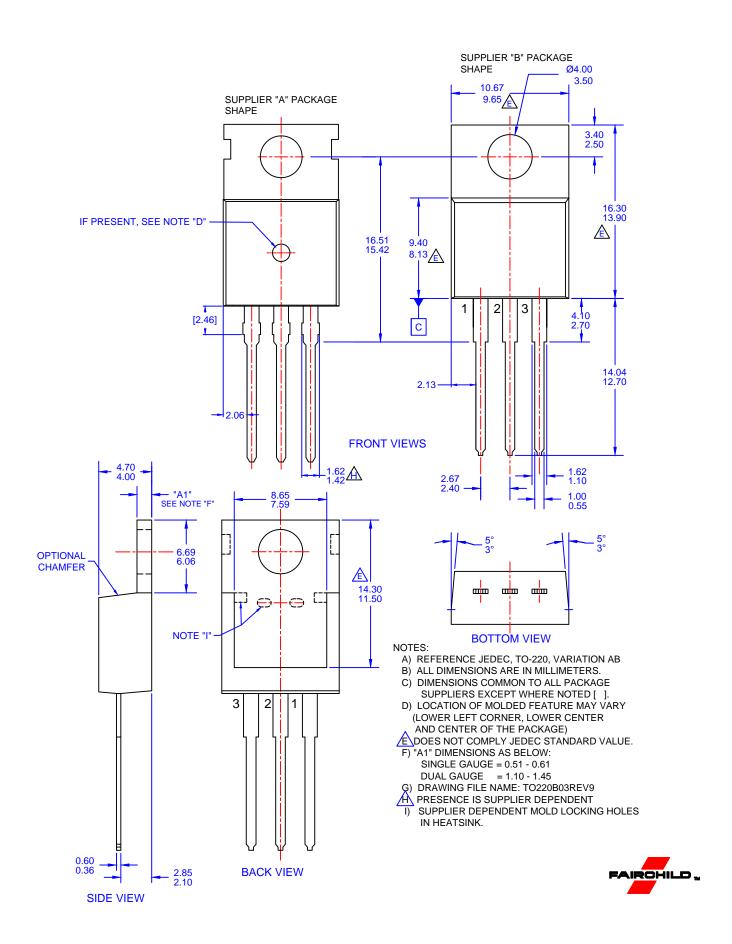


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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