

MC100EP196B

3.3 V ECL Programmable Delay Chip With FTUNE



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Descriptions

The MC100EP196B is a Programmable Delay Chip (PDC) designed primarily for clock deskewing and timing adjustment. It provides variable delay of a differential NECL/PECL input transition. It has similar architecture to the EP195 with the added feature of further tunability in delay using the FTUNE pin. The FTUNE input takes an analog voltage from V_{CC} to V_{EE} to fine tune the output delay from 0 to 60 ps.

The delay section consists of a programmable matrix of gates and multiplexers as shown in the logic diagram, Figure 3. The delay increment of the EP196B has a digitally selectable resolution of about 10 ps and a net range of up to 10.4 ns. The required delay is selected by the 10 data select inputs D[9:0] values and controlled by the LEN (Pin 10). A LOW level on LEN allows a transparent LOAD mode of real time delay values by D[9:0]. A LOW to HIGH transition on LEN will LOCK and HOLD current values present against any subsequent changes in D[10:0]. The approximate delay values for varying tap numbers correlating to D0 (LSB) through D9 (MSB) are shown in Table 6 and Figure 4.

The $\overline{IN}/\overline{IN}$ inputs can accept LVPECL (SE or Diff), or LVDS level signals. Because the MC100EP196B is designed using a chain of multiplexers it has a fixed minimum delay of 2.2 ns. An additional pin D10 is provided for controlling Pins 14 and 15, CASCADE and CASCADE, also latched by LEN, in cascading multiple PDCs for increased programmable range. The cascade logic allows full control of multiple PDCs. Switching devices from all “1” states on D[0:9] with SETMAX LOW to all “0” states on D[0:9] with SETMAX HIGH will increase the delay equivalent to “D0”, the minimum increment.

Select input pins D[10:0] may be threshold controlled by combinations of interconnects between V_{EF} (pin 7) and V_{CF} (pin 8) for receiving LVCMOS, ECL, or LVTTTL level signals. For LVCMOS input levels, leave V_{CF} and V_{EF} open. For ECL operation, short V_{CF} and V_{EF} (Pins 7 and 8). For LVTTTL level operation, connect a 1.5 V supply reference to V_{CF} and leave open V_{EF} pin. The 1.5 V reference voltage at the V_{CF} pin can be accomplished by placing a 2.2 k Ω resistor between V_{CF} and V_{EE} for a 3.3 V power supply.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The 100 Series contains temperature compensation.

Features

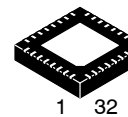
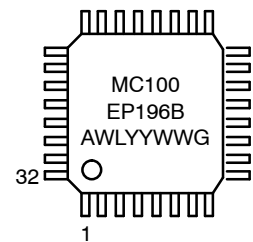
- Maximum Input Clock Frequency >1.2 GHz Typical
- Programmable Range: 0 ns to 10 ns
- Delay Range: 2.2 ns to 12.4 ns
- 10 ps Increments
- Linearity ± 40 ps max
- PECL Mode Operating Range:
 $V_{CC} = 3.0$ V to 3.6 V with $V_{EE} = 0$ V

- NECL Mode Operating Range:
 $V_{CC} = 0$ V with $V_{EE} = -3.0$ V to -3.6 V
- $\overline{IN}/\overline{IN}$ Inputs Accept LVPECL, LVNECL, LVDS Levels
- A Logic High on the \overline{EN} Pin Will Force Q to Logic Low
- D[10:0] Can Select Either LVPECL, LVCMOS, or LVTTTL Input Levels
- V_{BB} Output Reference Voltage
- These are Pb-Free Devices

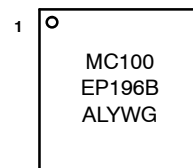
MARKING DIAGRAMS*



LQFP-32
FA SUFFIX
CASE 873A



QFN32
MN SUFFIX
CASE 488AM



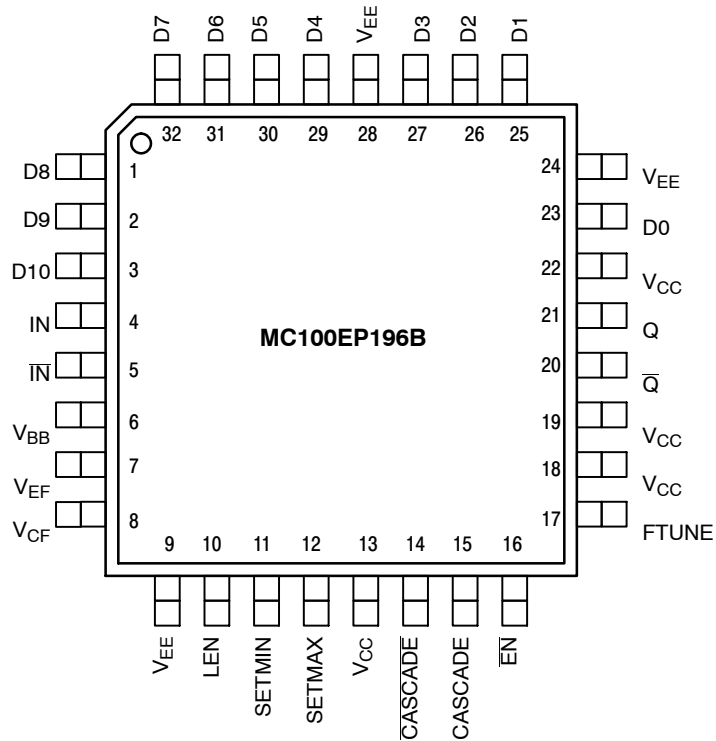
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G = Pb-Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 16 of this data sheet.

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Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 32-Lead LQFP (Top View)

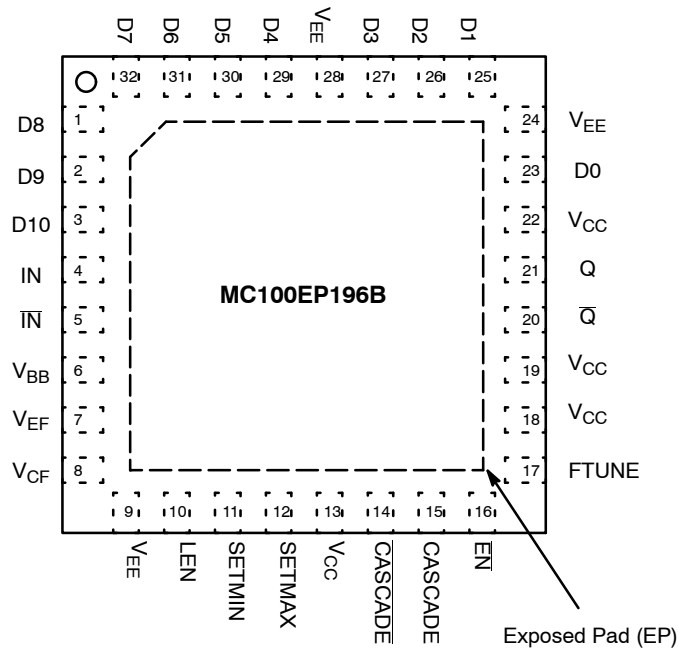


Figure 2. 32-Lead QFN (Top View)

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Table 1. PIN DESCRIPTION

| Pin | Name | I/O | Default State | Description |
|--------------------------------------|-----------------------------|----------------------------|---------------|--|
| 23, 25, 26, 27, 29, 30, 31, 32, 1, 2 | D[0:9] | LVC MOS, LV TTL, ECL Input | Low | Single-Ended Parallel Data Inputs [0:9]. Internal 75 k Ω to V _{EE} . (Note 1) |
| 3 | D[10] | LVC MOS, LV TTL, ECL Input | Low | Single-Ended CASCADE/CASCADE Control Input. Internal 75 k Ω to V _{EE} . (Note 1) |
| 4 | IN | LVPECL, LVDS | Low | Noninverted Differential Input. Internal 75 k Ω to V _{EE} . |
| 5 | $\overline{\text{IN}}$ | LVPECL, LVDS | High | Inverted Differential Input. Internal 75 k Ω to V _{EE} . |
| 6 | V _{BB} | - | - | ECL Reference Voltage Output |
| 7 | V _{EF} | - | - | Reference Voltage for ECL Mode Connection |
| 8 | V _{CF} | - | - | LVC MOS, ECL, OR LV TTL Input Mode Select |
| 9, 24, 28 | V _{EE} | - | - | Negative Supply Voltage. All V _{EE} Pins must be Externally Connected to Power Supply to Guarantee Proper Operation. (Note 2) |
| 13, 18, 19, 22 | V _{CC} | - | - | Positive Supply Voltage. All V _{CC} Pins must be externally Connected to Power Supply to Guarantee Proper Operation. (Note 2) |
| 10 | LEN | ECL Input | Low | Single-ended D pins LOAD / HOLD input. Internal 75 k Ω to V _{EE} . |
| 11 | SETMIN | ECL Input | Low | Single-ended Minimum Delay Set Logic Input. Internal 75 k Ω to V _{EE} . (Note 1) |
| 12 | SETMAX | ECL Input | Low | Single-ended Maximum Delay Set Logic Input. Internal 75 k Ω to V _{EE} . (Note 1) |
| 14 | $\overline{\text{CASCADE}}$ | ECL Output | - | Inverted Differential Cascade Output for D[10]. Typically Terminated with 50 Ω to V _{TT} = V _{CC} - 2 V. |
| 15 | CASCADE | ECL Output | - | Noninverted Differential Cascade Output. for D[10] Typically Terminated with 50 Ω to V _{TT} = V _{CC} - 2 V. |
| 16 | $\overline{\text{EN}}$ | ECL Input | Low | Single-ended Output Enable Pin. Internal 75 k Ω to V _{EE} . |
| 17 | FTUNE | Analog Input | - | Fine Tune Input |
| 21 | Q | ECL Output | - | Noninverted Differential Output. Typically Terminated with 50 Ω to V _{TT} = V _{CC} - 2 V. |
| 20 | $\overline{\text{Q}}$ | ECL Output | - | Inverted Differential Output. Typically Terminated with 50 Ω to V _{TT} = V _{CC} - 2 V. |

1. SETMIN will override SETMAX if both are high. SETMAX and SETMIN will override all D[0:10] inputs.
2. All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

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Table 2. CONTROL PIN

| Pin | State | Function |
|--------|--------------|--|
| EN | LOW (Note 3) | Input Signal is Propagated to the Output |
| | HIGH | Output Holds Logic Low State |
| LEN | LOW (Note 3) | Transparent or LOAD mode for real time delay values present on D[0:10]. |
| | HIGH | LOCK and HOLD mode for delay values on D[0:10]; further changes on D[0:10] are not recognized and do not affect delay. |
| SETMIN | LOW (Note 3) | Output Delay set by D[0:10] |
| | HIGH | Set Minimum Output Delay |
| SETMAX | LOW (Note 3) | Output Delay set by D[0:10] |
| | HIGH | Set Maximum Output Delay |
| D10 | LOW (Note 3) | CASCADE Output LOW, $\overline{\text{CASCADE}}$ Output HIGH |
| | HIGH | $\overline{\text{CASCADE}}$ Output LOW, CASCADE Output HIGH |

3. Internal pulldown resistor will provide a logic LOW if pin is left unconnected.

Table 3. CONTROL D[0:10] INTERFACE

| | | |
|----------|-----------------------|---------------------|
| V_{CF} | V_{EF} Pin (Note 4) | ECL Mode |
| V_{CF} | No Connect | LVC MOS Mode |
| V_{CF} | 1.5 V \pm 100 mV | LVTTL Mode (Note 5) |

4. Short V_{CF} (pin 8) and V_{EF} (pin 7).

5. When Operating in LVTTL Mode, the reference voltage can be provided by connecting an external resistor, R_{CF} (suggested resistor value is 2.2 k Ω \pm 5%), between V_{CF} and V_{EE} pins.

Table 4. DATA INPUT ALLOWED OPERATING VOLTAGE MODE TABLE

| POWER SUPPLY | CONTROL DATA SELECT INPUTS PINS (D [0:10]) | | | |
|---------------------------|--|-------|--------|--------|
| | LVC MOS | LVTTL | LVPECL | LVNECL |
| PECL Mode Operating Range | YES | YES | YES | N/A |
| NECL Mode Operating Range | N/A | N/A | N/A | YES |

Table 5. ATTRIBUTES

| Characteristics | Value |
|---|---|
| Internal Input Pulldown Resistor (R1) | 75 k Ω |
| ESD Protection | Human Body Model Machine Model Charged Device Model |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 6) | Pb-Free Pkg |
| | QFN-32 LQFP-32 |
| Flammability Rating Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in |
| Transistor Count | 1237 Devices |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | |

6. For additional information, see Application Note AND8003/D.

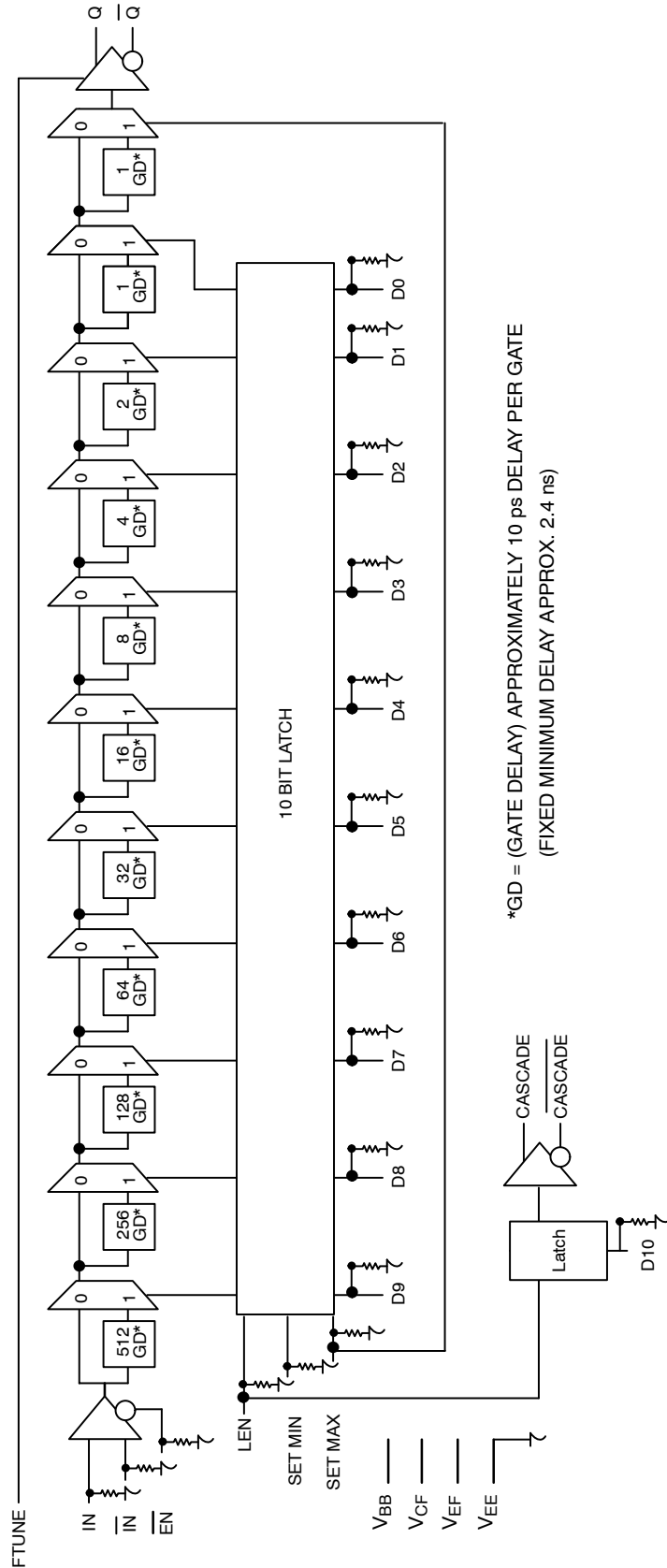


Figure 3. Logic Diagram

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Table 6. THEORETICAL DELAY VALUES

| D(9:0) Value | SETMIN | SETMAX | Programmable Delay* |
|--------------|--------|--------|---------------------|
| XXXXXXXXXX | H | L | 0 ps |
| 000000000 | L | L | 0 ps |
| 000000001 | L | L | 10 ps |
| 000000010 | L | L | 20 ps |
| 000000011 | L | L | 30 ps |
| 000000100 | L | L | 40 ps |
| 000000101 | L | L | 50 ps |
| 000000110 | L | L | 60 ps |
| 000000111 | L | L | 70 ps |
| 000001000 | L | L | 80 ps |
| 000010000 | L | L | 160 ps |
| 000100000 | L | L | 320 ps |
| 001000000 | L | L | 640 ps |
| 001000000 | L | L | 1280 ps |
| 010000000 | L | L | 2560 ps |
| 100000000 | L | L | 5120 ps |
| 111111111 | L | L | 10230 ps |
| XXXXXXXXXX | L | H | 10240 ps |

*Fixed minimum delay not included.

Table 7. TYPICAL FTUNE DELAY PIN

| Input Range | Output Range |
|---------------------|--------------|
| $V_{CC}-V_{EE}$ (V) | 0 – 60 (ps) |

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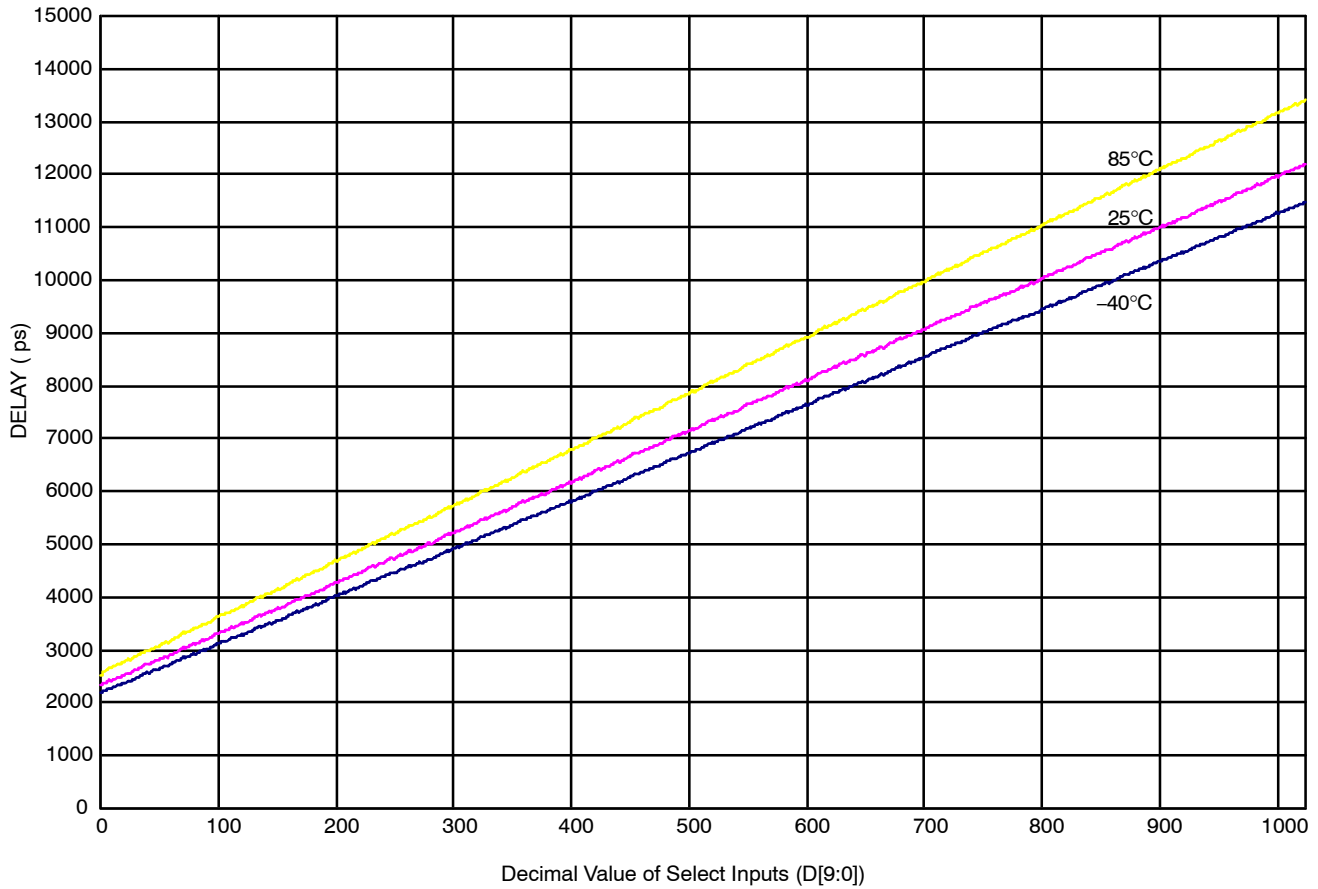


Figure 4. Measured Delay vs. Select Inputs

Table 8. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|------------------|--|--|--|-------------|----------|
| V _{CC} | Positive Mode Power Supply | V _{EE} = 0 V | | 6 | V |
| V _{EE} | Negative Mode Power Supply | V _{CC} = 0 V | | -6 | V |
| V _I | Positive Mode Input Voltage Negative Mode Input Voltage | V _{EE} = 0 V V _{CC} = 0 V | V _I ≤ V _{CC} V _I ≥ V _{EE} | 6 -6 | V V |
| I _{out} | Output Current | Continuous Surge | | 50 100 | mA mA |
| I _{BB} | V _{BB} Sink/Source | | | ±0.5 | mA |
| T _A | Operating Temperature Range | | | -40 to +85 | °C |
| T _{stg} | Storage Temperature Range | | | -65 to +150 | °C |
| θ _{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfm | QFN-32 | 31 | °C/W |
| | | 500 lfm | QFN-32 | 27 | °C/W |
| | | 0 lfm | LQFP-32 | 80 | °C/W |
| | | 500 lfm | LQFP-32 | 55 | °C/W |
| θ _{JC} | Thermal Resistance (Junction-to-Case) | 2S2P standard boards | QFN-32 | 12 | °C/W |
| | | | LQFP-32 | 12 to 17 | °C/W |
| T _{sol} | Wave Solder | Pb-Free | <2 to 3 sec @ 260°C | 265 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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Table 9. 100EP DC CHARACTERISTICS, PECL $V_{CC} = 3.3\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 7)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|-------|------|------|------|------|------|------|------|------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Negative Power Supply Current | 90 | 115 | 170 | 100 | 140 | 170 | 100 | 145 | 175 | mA |
| V_{OH} | Output HIGH Voltage (Note 8) | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | mV |
| V_{OL} | Output LOW Voltage (Note 8) | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | | | | | | | | | | mV |
| | LVPECL | 2075 | | 2420 | 2075 | | 2420 | 2075 | | 2420 | |
| | CMOS | 2000 | | 3300 | 2000 | | 3300 | 2000 | | 3300 | |
| | TTL | 2000 | | 3300 | 2000 | | 3300 | 2000 | | 3300 | |
| V_{IL} | Input LOW Voltage (Single-Ended) | | | | | | | | | | mV |
| | LVPECL | 1355 | | 1675 | 1490 | | 1675 | 1490 | | 1675 | |
| | CMOS | 0 | | 800 | 0 | | 800 | 0 | | 800 | |
| | TTL | 0 | | 800 | 0 | | 800 | 0 | | 800 | |
| V_{BB} | ECL Output Voltage Reference | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | mV |
| V_{CF} | LVTTTL Mode Input Detect Voltage | 1.4 | 1.5 | 1.6 | 1.4 | 1.5 | 1.6 | 1.4 | 1.5 | 1.6 | V |
| V_{EF} | Reference Voltage for ECL Mode Connection | 1900 | 2020 | 2150 | 1900 | 2020 | 2150 | 1900 | 2020 | 2150 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 9) | 1.2 | | 3.3 | 1.2 | | 3.3 | 1.2 | | 3.3 | V |
| I_{IH} | Input HIGH Current (@ V_{IH}) | 0 | | 150 | 0 | | 150 | 0 | | 150 | μA |
| I_{IL} | Input LOW Current (@ V_{IL}) | 0 | | 150 | 0 | | 150 | 0 | | 150 | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

7. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.3 V to -0.3 V.

8. All loading with 50 Ω to $V_{CC} - 2.0\text{ V}$.

9. V_{IHCMR} min varies 1:1 with V_{EE} . V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

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Table 10. 100EP DC CHARACTERISTICS, NECL $V_{CC} = 0\text{ V}$, $V_{EE} = -3.3\text{ V}$ (Note 10)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|---|----------------|-------|-------|----------------|-------|-------|----------------|-------|-------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Negative Power Supply Current (Note 11) | 90 | 115 | 170 | 100 | 140 | 170 | 100 | 145 | 175 | mA |
| V_{OH} | Output HIGH Voltage (Note 12) | -1145 | -1020 | -895 | -1145 | -1020 | -895 | -1145 | -1020 | -895 | mV |
| V_{OL} | Output LOW Voltage (Note 12) | -1945 | -1820 | -1695 | -1945 | -1820 | -1695 | -1945 | -1820 | -1695 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) LVNECL | -1225 | | -880 | -1225 | | -880 | -1225 | | -880 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) LVNECL | -1945 | | -1625 | -1945 | | -1625 | -1945 | | -1625 | mV |
| V_{BB} | ECL Output Voltage Reference | -1525 | -1425 | -1325 | -1525 | -1425 | -1325 | -1525 | -1425 | -1325 | mV |
| V_{EF} | Reference Voltage for ECL Mode Connection | -1400 | -1280 | -1250 | -1400 | -1280 | -1250 | -1400 | -1280 | -1250 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 13) | $V_{EE} + 1.2$ | | 0.0 | $V_{EE} + 1.2$ | | 0.0 | $V_{EE} + 1.2$ | | 0.0 | V |
| I_{IH} | Input HIGH Current (@ V_{IH}) | 0 | | 150 | 0 | | 150 | 0 | | 150 | μA |
| I_{IL} | Input LOW Current (@ V_{IL}) I_N, \bar{I}_N | 0 | | 150 | 0 | | 150 | 0 | | 150 | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

10. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.3 V to -0.3 V.

11. Required 500 lfm air flow when using +5 V power supply. For $(V_{CC} - V_{EE}) > 3.3\text{ V}$, $5\ \Omega$ to $10\ \Omega$ in line with V_{EE} required for maximum thermal protection at elevated temperatures. Recommend $V_{CC} - V_{EE}$ operation at $\leq 3.8\text{ V}$.

12. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.

13. V_{IHCMR} min varies 1:1 with V_{EE} . V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

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Table 11. AC CHARACTERISTICS $V_{CC} = 0\text{ V}$; $V_{EE} = -3.0\text{ V to }-3.6\text{ V}$ or $V_{CC} = 3.0\text{ V to }3.6\text{ V}$; $V_{EE} = 0\text{ V}$ (Note 14)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|------------------------|--|------------------------------|---|------------------------------|------------------------------|---|------------------------------|------------------------------|---|------------------------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| f_{max} | Maximum Frequency | | 1.2 | | | 1.2 | | | 1.2 | | GHz |
| V_{outpp} | Output Voltage Amplitude | 610 | 820 | | 610 | 820 | | 610 | 820 | | mV |
| t_{PLH} t_{PHL} | Propagation Delay IN to Q; D(0-10) = 0, SETMIN IN to Q; D(0-10) = 1023, SETMAX \overline{EN} to Q; D(0-10) = 0 D0 to CASCADE | 2000 10900 1990 375 | 2400 12400 2500 475 | 2800 13900 2990 575 | 2150 11500 2130 400 | 2500 13000 2600 500 | 2950 14500 3130 600 | 2250 12250 2380 425 | 2700 13750 2800 525 | 3050 15250 3380 625 | ps |
| t_{RANGE} | Programmable Range $t_{PD}(\text{max}) - t_{PD}(\text{min})$ | 8950 | 9950 | 10950 | 9450 | 10450 | 11450 | 10110 | 11100 | 12110 | ps |
| Δt | Step Delay (Note 15) D0 High D1 High D2 High D3 High D4 High D5 High D6 High D7 High D8 High D9 High | | 10 16 32 65 155 310 620 1200 2500 4900 | | | 11 18 33 72 166 325 650 1300 2600 5200 | | | 15 26 46 92 195 370 720 1400 2800 5500 | | ps |
| NLIN | Non-Linearity (Notes 16 and 17) 0 to 511 decimal values for D[9:0] range 512 to 1023 dec. values for D[9:0] range 1 to 1023 decimal values for D[9:0] range | | ± 7.0 ± 7.0 ± 11 | | | ± 7.0 ± 7.0 ± 11 | | | ± 7.0 ± 7.0 ± 11 | | ps |
| t_{SKEW} | Duty Cycle Skew (Note 18) $ t_{PHL} - t_{PLH} $ | | 25 | 90 | | 25 | 90 | | 25 | 90 | ps |
| t_s | Setup Time D to LEN D to IN (Note 19) \overline{EN} to IN (Note 20) | 200 500 300 | -40 -550 100 | | 200 500 300 | -40 -590 100 | | 200 500 300 | -40 -650 120 | | ps |
| t_h | Hold Time LEN to D IN to \overline{EN} (Note 21) | 200 400 | 50 -320 | | 200 400 | 40 -350 | | 200 400 | 30 -400 | | ps |
| t_R | Release Time \overline{EN} to IN (Note 22) SET MAX to LEN SET MIN to LEN | 300 400 350 | -150 180 220 | | 300 400 350 | -170 200 250 | | 300 400 350 | -200 210 260 | | ps |
| t_{jitter} | RMS Random Clock Jitter @ 1.2 GHz IN to Q; D(0:10) = 0 or SETMIN IN to Q; D(0:10) = 1023 or SETMAX | | 0.9 1.9 | 2.0 5.0 | | 1.1 2.6 | 2.0 5.0 | | 1.2 3.3 | 2.0 5.0 | ps |
| V_{PP} | Input Voltage Swing (Differential Configuration) | 150 | 800 | 1200 | 150 | 800 | 1200 | 150 | 800 | 1200 | mV |
| t_r t_f | Output Rise/Fall Time @ 50 MHz 20-80% (Q) 20-80% (CASCADE) | 85 110 | 115 160 | 140 210 | 100 120 | 120 175 | 140 230 | 100 120 | 130 190 | 165 250 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

14. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to $V_{CC} - 2.0\text{ V}$.
15. Specification limits represent the amount of delay added with the assertion of each individual delay control pin. The various combinations of asserted delay control inputs will typically realize D0 resolution steps across the specified programmable range.
16. Deviation from a linear delay (actual Min to Max) in the 1024 programmable steps.
17. For NLIN, Max temperature is 70°C.
18. Duty cycle skew guaranteed only for differential operation measured from the cross point of the input to the cross point of the output.
19. This setup time defines the amount of time prior to the input signal the delay tap of the device must be set.
20. This setup time is the minimum time that \overline{EN} must be asserted prior to the next transition of IN/ \overline{IN} to prevent an output response greater than $\pm 75\text{ mV}$ to that IN/ \overline{IN} transition.
21. This hold time is the minimum time that \overline{EN} must remain asserted after a negative going IN or positive going \overline{IN} to prevent an output response greater than $\pm 75\text{ mV}$ to that IN/ \overline{IN} transition.
22. This release time is the minimum time that \overline{EN} must be deasserted prior to the next IN/ \overline{IN} transition to ensure an output response that meets the specified IN to Q propagation delay and transition times.

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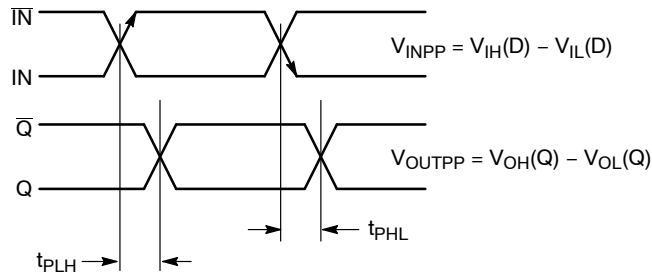


Figure 5. AC Reference Measurement

Using the FTUNE Analog Input

The analog FTUNE pin on the EP196 device is intended to add more delay in a tunable gate to enhance the 10 ps resolution capabilities of the fully digital EP196. The level of resolution obtained is dependent on the voltage applied to the FTUNE pin.

To provide this further level of resolution, the FTUNE pin must be capable of adjusting the additional delay finer than the 10 ps digital resolution (See Logic Diagram). This requirement is easily achieved because a 60 ps additional delay can be obtained over the entire FTUNE voltage range (See Figure 6). This extra analog range ensures that the

FTUNE pin will be capable even under worst case conditions of covering a digital resolution. Typically, the analog input will be driven by an external DAC to provide a digital control with very fine analog output steps. The final resolution of the device will be dependent on the width of the DAC chosen.

To determine the voltage range necessary for the FTUNE input, Figure 6 should be used. There are numerous voltage ranges which can be used to cover a given delay range; users are given the flexibility to determine which one best fits their designs.

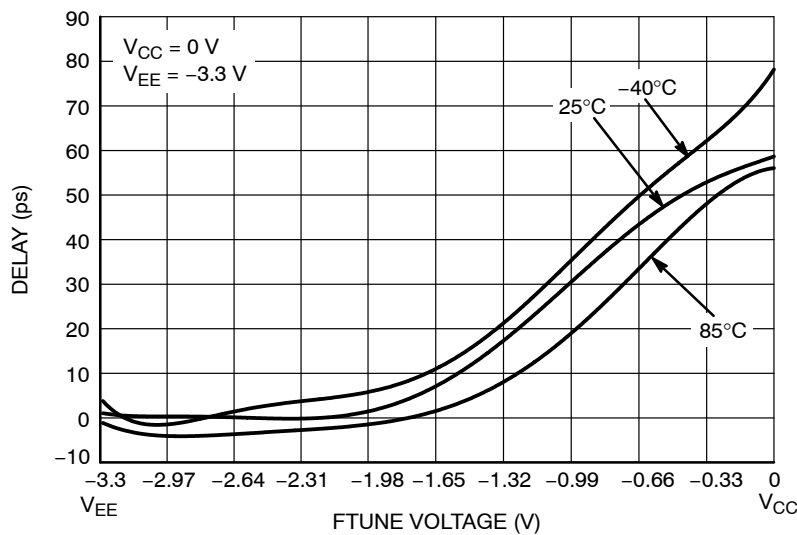


Figure 6. Typical EP196B Delay versus FTUNE Voltage

Cascading Multiple EP196Bs

To increase the programmable range of the EP196B, internal cascade circuitry has been included. This circuitry allows for the cascading of multiple EP196Bs without the need for any external gating. Furthermore, this capability requires only one more address line per added EP196B. Obviously, cascading multiple programmable delay chips will result in a larger programmable range; however, this increase is at the expense of a longer minimum delay.

Figure 7 illustrates the interconnect scheme for cascading two EP196Bs. As can be seen, this scheme can easily be

expanded for larger EP196B chains. The D10 input of the EP196B is the CASCADE control pin. With the interconnect scheme of Figure 7 when D10 is asserted, it signals the need for a larger programmable range than is achievable with a single device and switches output pin CASCADE HIGH and pin $\overline{\text{CASCADE}}$ LOW. The A11 address can be added to generate a cascade output for the next EP196B. For a 2-device configuration, A11 is not required.

MC100EP196B

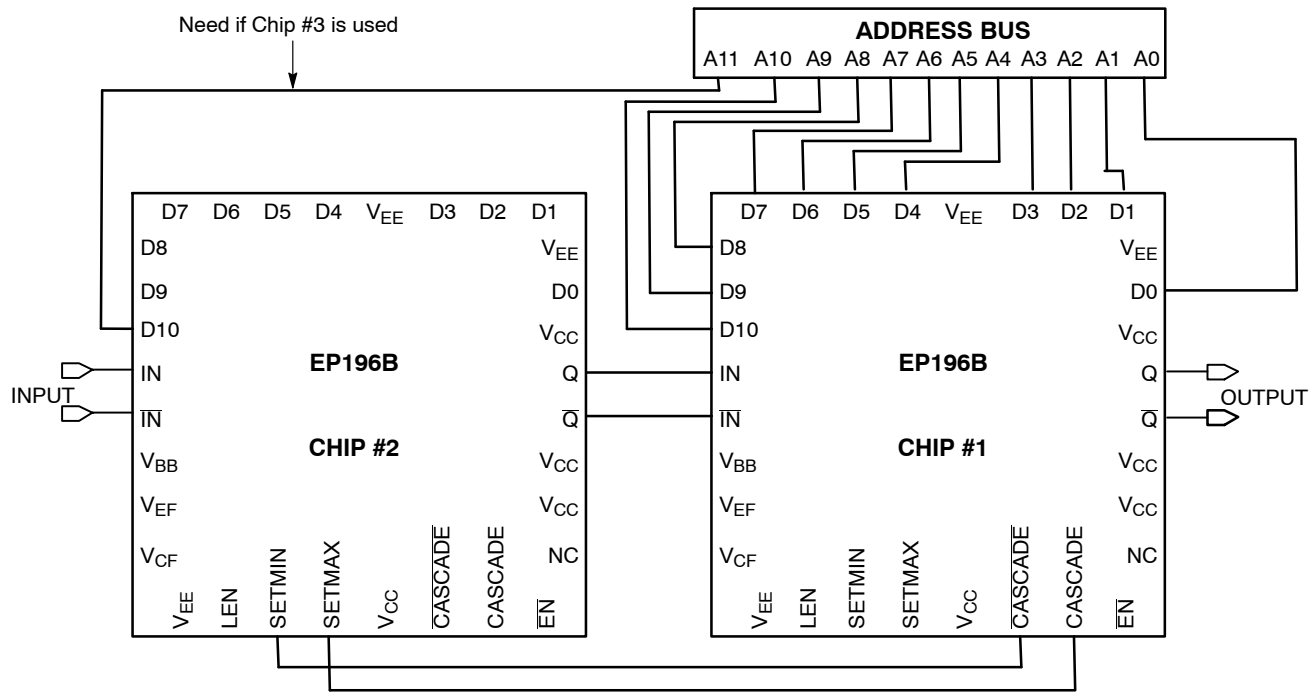


Figure 7. Cascading Interconnect Architecture

MC100EP196B

An expansion of the latch section of the block diagram is pictured in Figure 8. Use of this diagram will simplify the explanation of how the cascade circuitry works. When D10 of chip #1 in Figure 7 is LOW this device's CASCADE output will also be low while the CASCADE output will be high. In this condition the SET MIN pin of chip #2 will be asserted HIGH and thus all of the latches of chip #2 will be reset and the device will be set at its minimum delay.

Chip #1, on the other hand, will have both SET MIN and SET MAX deasserted so that its delay will be controlled entirely by the address bus A0—A9. If the delay needed is greater than can be achieved with 1023 gate delays

(111111111 on the A0—A9 address bus) D10 will be asserted to signal the need to cascade the delay to the next EP196B device. When D10 is asserted, the SET MIN pin of chip #2 will be deasserted and SET MAX pin asserted resulting in the device delay to be the maximum delay. Table 12 shows the delay time of two EP196B chips in cascade.

To expand this cascading scheme to more devices, one simply needs to connect the D10 pin from the next chip to the address bus and CASCADE outputs to the next chip in the same manner as pictured in Figure 7. The only addition to the logic is the increase of one line to the address bus for cascade control of the second programmable delay chip.

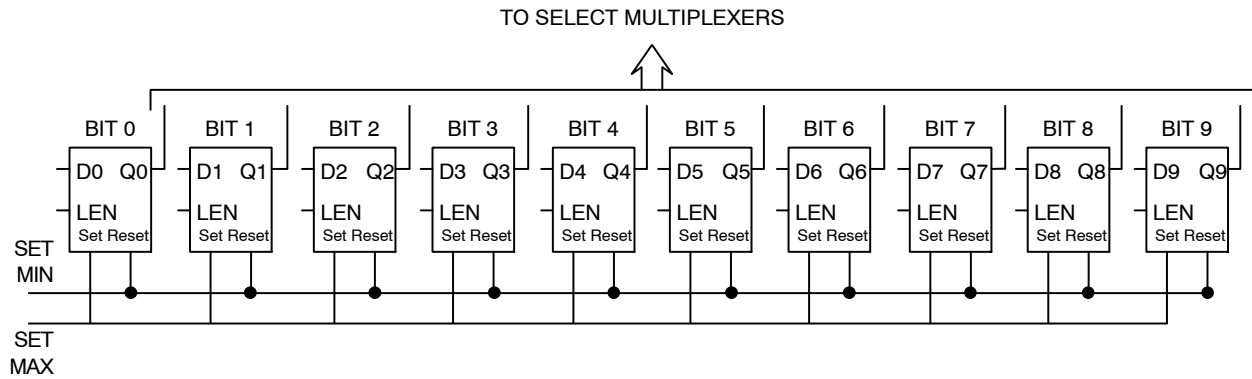


Figure 8. Expansion of the Latch Section of the EP196B Block Diagram

MC100EP196B

Table 12. Delay Value of Two EP196B Cascaded

| VARIABLE INPUT TO CHIP #1 AND SETMIN FOR CHIP #2 | | | | | | | | | | | | |
|--|----|----|----|----|----|----|----|----|----|----|-------------|----------------------|
| INPUT FOR CHIP #1 | | | | | | | | | | | Delay Value | Total Delay Value |
| D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 ps | 4400 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 10 ps | 4410 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 20 ps | 4420 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 30 ps | 4430 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 40 ps | 4440 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 50 ps | 4450 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 60 ps | 4460 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 70 ps | 4470 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 80 ps | 4480 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 160 ps | 4560 ps |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 220 ps | 4720 ps |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 640 ps | 5040 ps |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1280 ps | 5680 ps |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 2560 ps | 6960 ps |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 5120 ps | 9520 ps |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 10230 ps | 14630 ps |

| VARIABLE INPUT TO CHIP #1 AND SETMAX FOR CHIP #2 | | | | | | | | | | | | |
|--|----|----|----|----|----|----|----|----|----|----|-------------|----------------------|
| INPUT FOR CHIP #1 | | | | | | | | | | | Delay Value | Total Delay Value |
| D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 10240 ps | 14640 ps |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 10250 ps | 14650 ps |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 10260 ps | 14660 ps |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 10270 ps | 14670 ps |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 10280 ps | 14680 ps |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 10290 ps | 14690 ps |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 10300 ps | 14700 ps |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 10310 ps | 14710 ps |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 10320 ps | 14720 ps |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10400 ps | 14800 ps |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 10560 ps | 14960 ps |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 10880 ps | 15280 ps |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 11520 ps | 15920 ps |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 12800 ps | 17200 ps |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 15360 ps | 19760 ps |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 20470 ps | 24870 ps |

MC100EP196B

Multi-Channel Deskewing

The most practical application for EP196B is in multiple channel delay matching. Slight differences in impedance and cable length can create large timing skews within a high-speed system. To deskew multiple signal channels, each channel can

be sent through each EP196B as shown in Figure 9. One signal channel can be used as reference and the other EP196Bs can be used to adjust the delay to eliminate the timing skews. Nearly any high-speed system can be fine-tuned (as small as 10 ps) to reduce the skew to extremely tight tolerances.

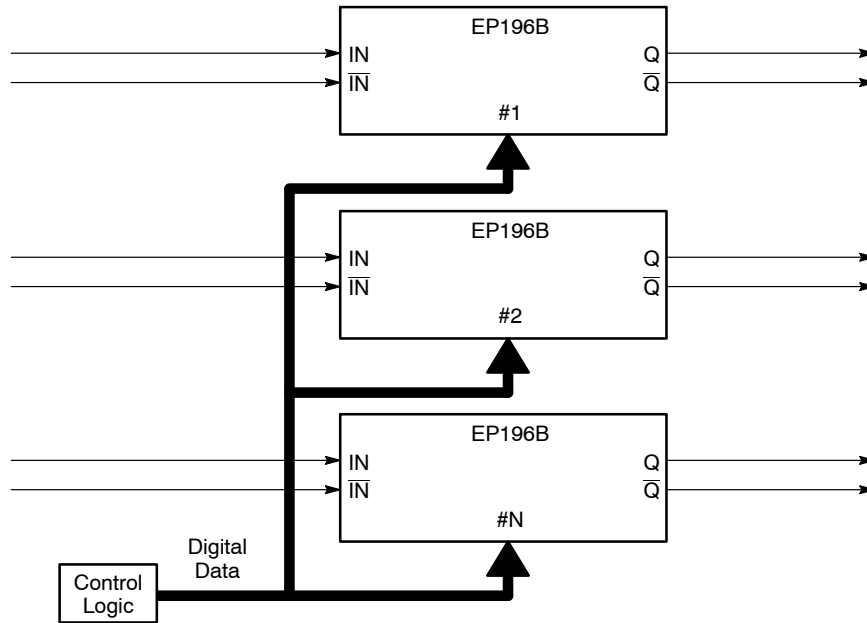


Figure 9. Multiple Channel Deskewing Diagram

Measure Unknown High Speed Device Delays

EP196Bs provide a possible solution to measure the unknown delay of a device with a high degree of precision. By combining two EP196Bs and EP31 as shown in Figure 10, the delay can be measured. The first EP196B can be set to SETMIN and its output is used to drive the unknown delay device, which in turn drives the input of a D flip-flop of EP31. The second EP196B is triggered along with the first EP196B and its output provides a clock signal for EP31. The programmed delay of the second EP196B is varied to detect the output edge from the unknown delay device.

If the programmed delay through the second EP196B is too long, the flip-flop output will be at logic high. On the other hand, if the programmed delay through the second EP196B is too short, the flip-flop output will be at a logic low. If the programmed delay is correctly fine-tuned in the second EP196B, the flip-flop will bounce between logic high and logic low. The digital code in the second EP196B can be directly correlated into an accurate device delay.

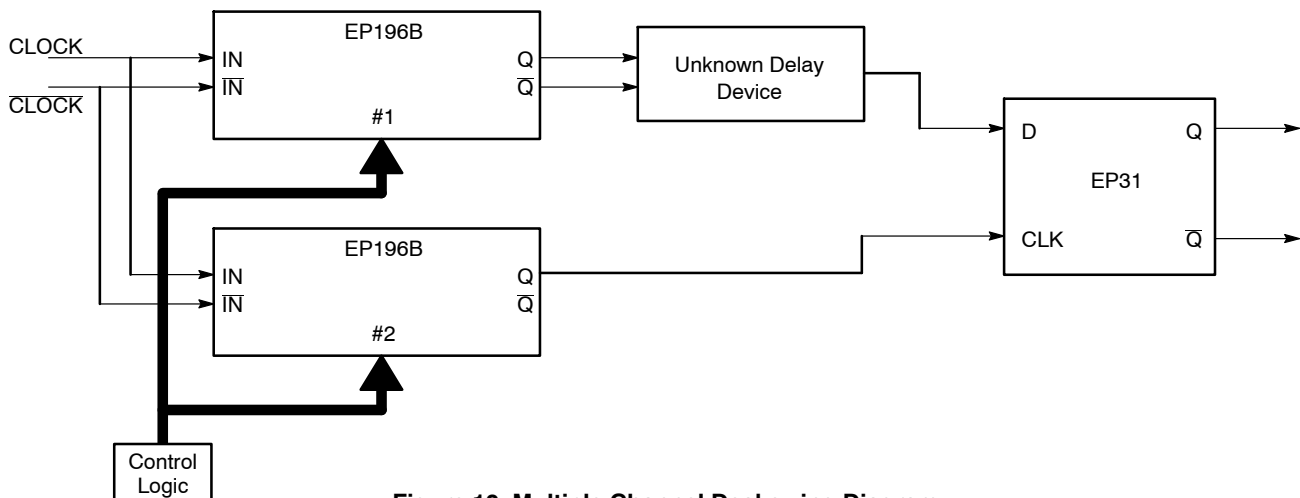
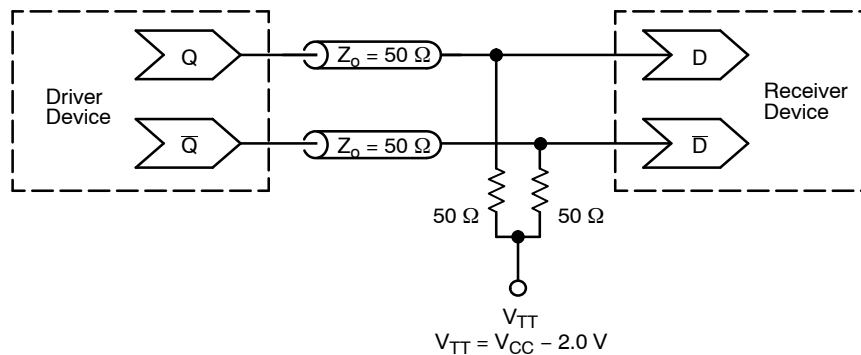


Figure 10. Multiple Channel Deskewing Diagram

MC100EP196B



**Figure 11. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D – Termination of ECL Logic Devices.)**

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|------------------|----------------------|-----------------------|
| MC100EP196BFA | LQFP-32 | 250 Units / Tray |
| MC100EP196BFAG | LQFP-32 (Pb-Free) | 250 Units / Tray |
| MC100EP196BFAR2 | LQFP-32 | 2000 / Tape & Reel |
| MC100EP196BFAR2G | LQFP-32 (Pb-Free) | 2000 / Tape & Reel |
| MC100EP196BMNG | QFN-32 (Pb-Free) | 74 Units / Rail |
| MC100EP196BMNR4G | QFN-32 (Pb-Free) | 1000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

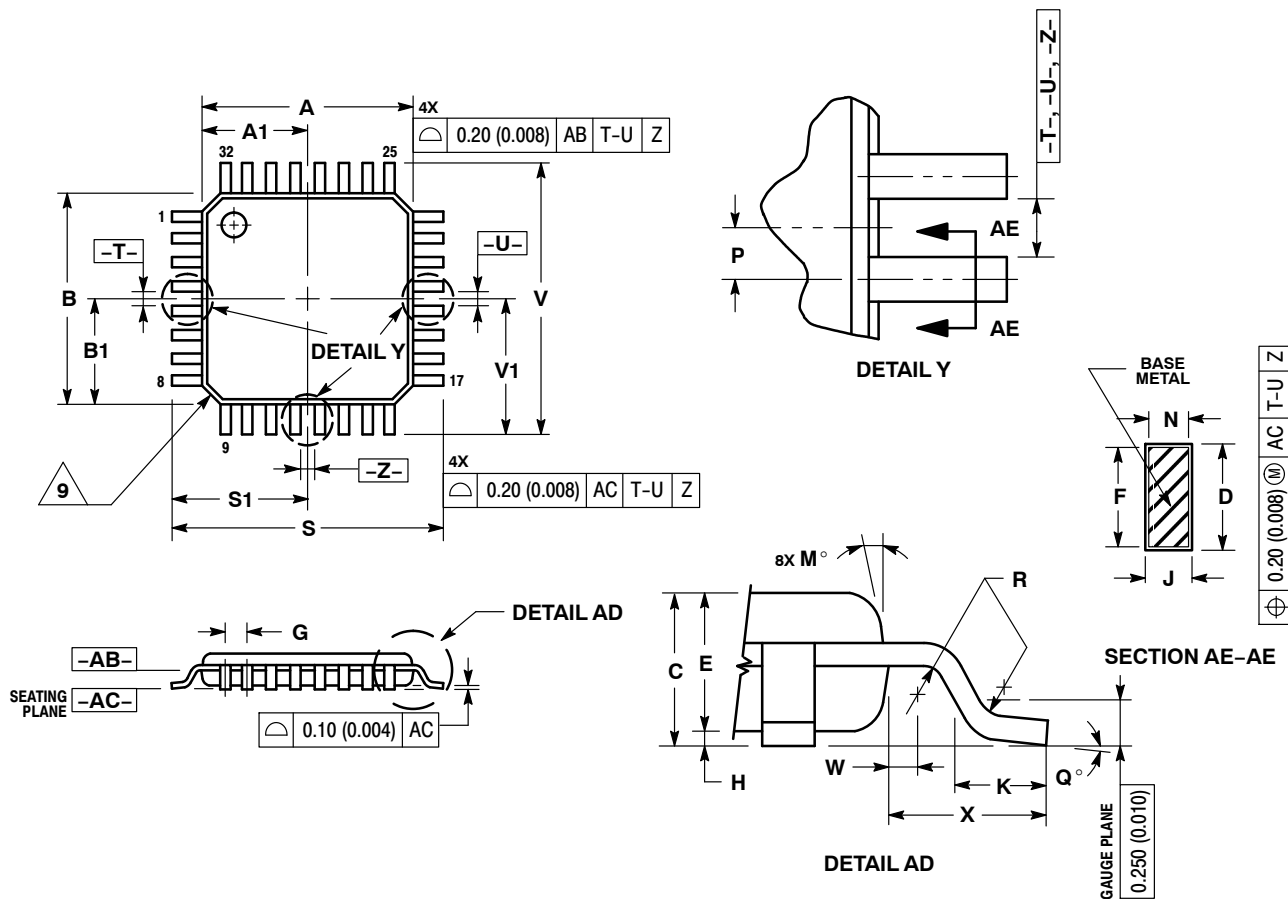
Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

MC100EP196B

PACKAGE DIMENSIONS

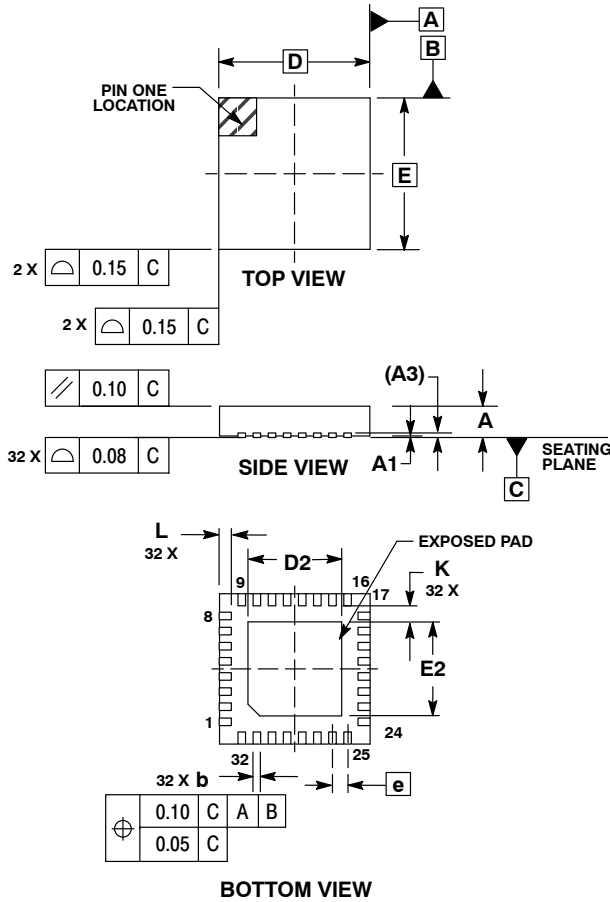
32 LEAD LQFP
CASE 873A-02
ISSUE C



MC100EP196B

PACKAGE DIMENSIONS

QFN32 5*5*1 0.5 P
CASE 488AM-01
ISSUE O

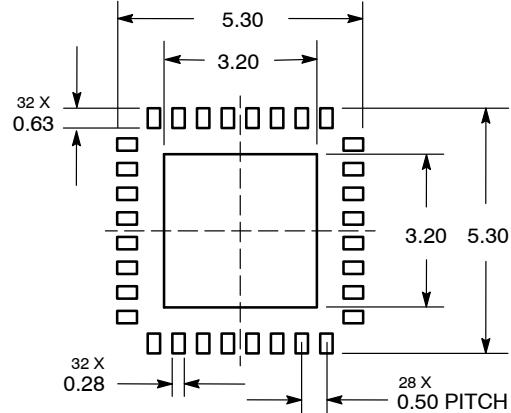


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1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| MILLIMETERS | | | |
|-------------|-----------|-------|-------|
| DIM | MIN | NOM | MAX |
| A | 0.800 | 0.900 | 1.000 |
| A1 | 0.000 | 0.025 | 0.050 |
| A3 | 0.200 REF | | |
| b | 0.180 | 0.250 | 0.300 |
| D | 5.00 BSC | | |
| D2 | 2.950 | 3.100 | 3.250 |
| E | 5.00 BSC | | |
| E2 | 2.950 | 3.100 | 3.250 |
| e | 0.500 BSC | | |
| K | 0.200 | --- | --- |
| L | 0.300 | 0.400 | 0.500 |

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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