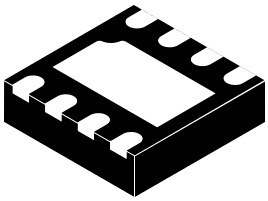
TS488

Datasheet

Pop-free 120 mW stereo headphone amplifier



Product status link
TS488

Product summary	
Order code	TS488IQT
Temperature range	-40 to +85 °C
Package	DFN8 2x2 mm
Packing	Tape and reel
Marking	K88

Features

- Pop and click noise protection circuitry
- Operating range from VCC = 2.2 V to 5.5 V
- Standby mode active low
- Output power:
  - 120 mW at 5 V, into 16 Ω with 0.1% THD+N max. (1 kHz)
  - 55 mW at 3.3 V, into 16 Ω with 0.1% THD+N max. (1 kHz)
- Low current consumption: 2.7 mA max. at 5 V
- Ultra-low standby current consumption: 10 nA typical
- High signal-to-noise ratio
- High crosstalk immunity: 102 dB (F = 1 kHz)
- PSRR: 70 dB typ. (F = 1 kHz), inputs grounded at 5 V
- Unity-gain stable
- Short-circuit protection circuitry
- Available in DFN8 2x2 mm

Applications

- Headphone amplifiers
- Mobile phones, PDAs, computer motherboards
- High-end TVs, portable audio players

Description

The TS488 is a dual audio power amplifier capable of driving, in single-ended mode, either a 16 Ω or a 32 Ω stereo headset.

The TS488 eliminates pop and click noise and reduces the number of required external passive components.

Capable of descending to low voltages, it delivers up to 31 mW per channel (into 16 Ω loads) of continuous average power with 0.1% THD+N in the audio bandwidth from a 2.5 V power supply.

An externally-controlled standby mode reduces the supply current to 10 nA (typ.). The unity gain stable is configured by external gain-setting resistors.

1 Typical application schematic

Figure 1. Typical application for the TS488

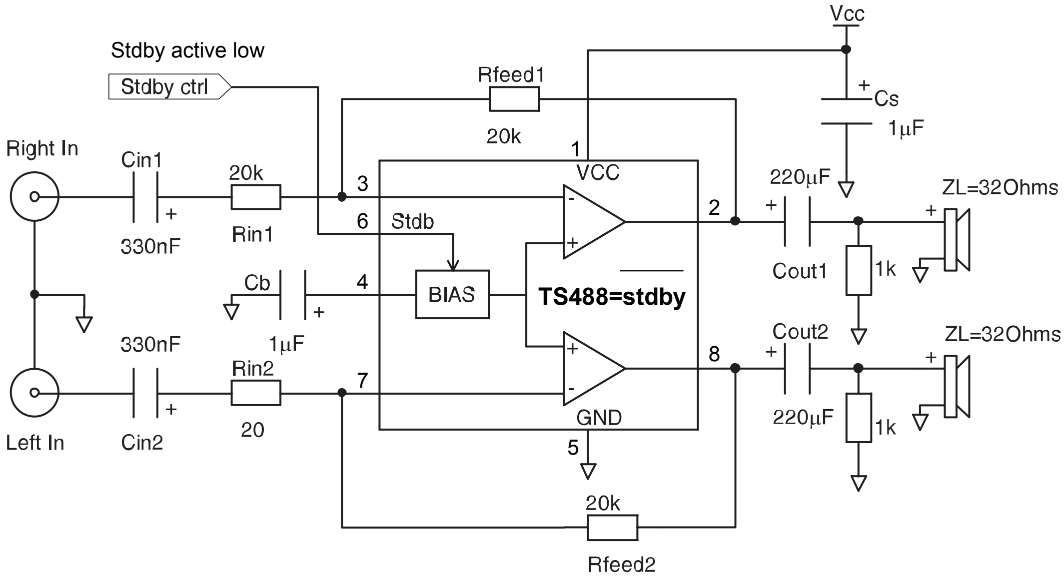


Table 1. Application component information

Component	Functional description
$R_{in1,2}$	Inverting input resistor that sets the closed loop gain in conjunction with R_{feed}. This resistor also forms a high pass filter with C_{in} [F_c = 1 / (2 x Pi x R_{in} x C_{in})]
$C_{in1,2}$	Input coupling capacitor that blocks the DC voltage at the amplifier input terminal
$R_{feed1,2}$	Feedback resistor that sets the closed loop gain in conjunction with R_{in}. A_V= closed loop gain= -R_{feed}/R_{in}
C_s	Supply output capacitor that provides power supply filtering
C_b	Bypass capacitor that provides half supply filtering
$C_{out1,2}$	Output coupling capacitor that blocks the DC voltage at the load input terminal. This capacitor also forms a high pass with RL [F_c = 1 / (2 x Pi x RL x C_{out})]

2 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage [(1)]	6	V
V_i	Input voltage	-0.3 V to V_{CC} +0.3 V	V
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction-to-ambient	70	°C/W
P_{diss}	Power dissipation[(2)]	1.79	W
ESD	Human body model (pin to pin)	2	kV
	Machine mode l220 pF - 240 pF (pin-to-pin)	200	V
	200	V	
Latch-up	Latch-up immunity (all pins)	200	mA
	Lead temperature (soldering, 10 s)	250	°C
	Output short-circuit to VCC or GND	continuous [(3)]	

1. *All voltage values are measured with respect to the ground pin.*
2. *P_{diss} is calculated with T_{amb} = 25 °C, T_j = 150 °C.*
3. *Attention must be paid to continuous power dissipation (VDD x 250 mA). Short-circuits can cause excessive heating and destructive dissipation. Exposing the IC to a short-circuit for an extended period of time dramatically reduceS the product's life expectancy.*

Table 3. Operational data

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.2 to 5.5	V
R_L	Load resistor	≥ 16	Ω
T_{oper}	Operating free air temperature range	-40 to + 85	°C
C_L	Load capacitor: RL = 16 to 100 Ω	400	pF
	RL>100 Ω	100	
V_{STBY}	TS488 active	1.5 ≤ V ≤ VCC	V
	TS488 in standby	GND ≤ V_{STBY} ≤ 0.4[(1)]	
R_{thja}	Thermal resistance junction-to-ambient: DFN8[(2)]	40	°C/W

1. *The minimum current consumption (I_{STBY}) is guaranteed at GND for the whole temperature range.*
2. *When mounted on a 4-layer PCB.*

3 Electrical characteristics

Table 4. Electrical characteristics at V_{CC}=+5 V with GND =0 V, T_{amb}= 25 °C (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current	No input signal, no load		2	2.7	mA
I_{STBY}	Standby current	No input signal, V_{STBY} = GND RL = 32 Ω		10	1000	nA
P_{out}	Output power	THD+N = 0.1% max., F = 1 kHz, RL = 32 Ω		75		mW
		THD+N = 1% max. F = 1 kHz, RL = 32 Ω	70	80		
		THD+N = 0.1% max., F = 1 kHz, RL = 16 Ω		120		
		THD+N = 1% max., F = 1 kHz, RL = 16 Ω	100	130		
THD+N	Total harmonic distortion + noise	A_V=-1, RL = 32 Ω, Pout = 60 mW, 20 Hz ≤ F ≤ 20 kHz		0.3		%
		AV=-1, RL = 16 Ω, Pout = 90 mW, 20 Hz ≤ F ≤ 20 kHz		0.3		
PSRR	Power supply rejection ratio, inputs grounded[(1)]	A_V=-1, RL ≥ 16 Ω, C_b=1 µF, F = 1 kHz, V_{ripple} = 200 mVpp	64	70		dB
		A_V=-1, RL ≥ 16 Ω, C_b=1 µF, F = 217 kHz, V_{ripple} = 200 mVpp	62	68		
V_O	Output swing	V_{OL}: RL = 32 Ω		0.23	0.31	V
		V_{OH}: RL = 32 Ω	4.53	4.72		
		V_{OL}: RL = 16 Ω		0.44	0.57	
		V_{OH}: RL = 16 Ω	4.18	4.48		
SNR	Signal-to-noise ratio	A-weighted, A_V=-1, RL = 32 Ω, THD+N < 0.4%, 20 Hz ≤ F ≤ 20 kHz		105		dB
Crosstalk	Channel separation	RL = 32 Ω, AV = -1, F = 1 kHz, F = 20 Hz to 20 kHz		-102		dB
		RL = 32 Ω, AV = -1, F = 1 kHz, F = 20 Hz to 20 kHz		-84		
C_i	Input capacitance			1		pF
GBP	Gain bandwidth product	RL = 32 Ω		1.1		MHz
SR	Slew rate, unity gain inverting	RL = 16 Ω		0.65		V/µs
V_{IO}	Input offset voltage	V_{icm}=V_{CC}/2		1	20	mV
t_{wu}	Wake-up time			100		ms

1. *Guaranteed by design and evaluation.*

Table 5. **Electrical characteristics at V_{CC}=+3.3 V with GND =0 V, T_{amb}= 25 °C (unless otherwise specified)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current	No input signal, no load		1.8	2.5	mA
I_{STBY}	Standby current	No input signal, V_{STBY} = GND RL = 32 Ω		10	1000	nA
P_{out}	Output power	THD+N = 0.1% max., F = 1 kHz, RL = 32 Ω		34		mW
		THD+N = 1% max. F = 1 kHz, RL = 32 Ω	30	35		
		THD+N = 0.1% max., F = 1 kHz, RL = 16 Ω		55		
		THD+N = 1% max, F = 1 kHz, RL = 16 Ω	47	57		
THD+N	Total harmonic distortion + noise	A_V=-1, RL = 32 Ω, Pout = 16 mW, 20 Hz ≤ F ≤ 20 kHz		0.3		%
		AV=-1, RL = 16 Ω, Pout = 35 mW, 20 Hz ≤ F ≤ 20 kHz		0.3		
PSRR	Power supply rejection ratio, inputs grounded[1]	A_V=-1, RL ≥ 16 Ω, C_b=1 µF, F = 1 kHz, V_{ripple} = 200 mVpp	63	69		dB
		A_V=-1, RL ≥ 16 Ω, C_b=1 µF, F = 217 kHz, V_{ripple} = 200 mVpp	61	67		
V_O	Output swing	V_{OL}: RL = 32 Ω		0.15	0.2	V
		V_{OH}: RL = 32 Ω	3.03	3.12		
		V_{OL}: RL = 16 Ω		0.28	0.36	
		V_{OH}: RL = 16 Ω	2.82	2.97		
SNR	Signal-to-noise ratio	A-weighted, A_V=-1, RL = 32 Ω, THD+N < 0.4%, 20 Hz ≤ F ≤ 20 kHz		102		dB
Crosstalk	Channel separation	RL = 32 Ω, AV = -1, F = 1 kHz, F = 20 Hz to 20 kHz		-102		dB
		RL = 32 Ω, AV = -1, F = 1 kHz, F = 20 Hz to 20 kHz		-84		dB
C_i	Input capacitance			1		pF
GBP	Gain bandwidth product	RL = 32 Ω		1.1		MHz
SR	Slew rate, unity gain inverting	RL = 16 Ω		0.6		V/µs
V_{IO}	Input offset voltage	V_{icm}=V_{CC}/2		1	20	mV
t_{wu}	Wake-up time			100		ms

1. *Guaranteed by design and evaluation.*

Note: *All electrical values are guaranteed with correlation measurements at 2.5 V and 5 V.*

Table 6. **Electrical characteristics at V_{CC}=+2.5 V with GND =0 V, T_{amb}= 25 °C (unless otherwise specified)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current	No input signal, no load		1.8	2.5	mA
I_{STBY}	Standby current	No input signal, V_{STBY} = GND RL = 32 Ω		10	1000	nA
P_{out}	Output power	THD+N = 0.1% max., F = 1 kHz, RL = 32 Ω		19		mW
		THD+N = 1% max. F = 1 kHz, RL = 32 Ω	18	20		
		THD+N = 0.1% max., F = 1 kHz, RL = 16 Ω		31		
		THD+N = 1% max, F = 1 kHz, RL = 16 Ω	27	32		
THD+N	Total harmonic distortion + noise	A_V=-1, RL = 32 Ω, Pout = 10 mW, 20 Hz ≤ F ≤ 20 kHz		0.3		%
		AV=-1, RL = 16 Ω, Pout = 16 mW, 20 Hz ≤ F ≤ 20 kHz		0.3		
PSRR	Power supply rejection ratio, inputs grounded[(1)]	A_V=-1, RL ≥ 16 Ω, C_b=1 µF, F = 1 kHz, V_{ripple} = 200 mVpp		68		dB
		A_V=-1, RL ≥ 16 Ω, C_b=1 µF, F = 217 kHz, V_{ripple} = 200 mVpp	61	66		
V_O	Output swing	V_{OL}: RL = 32 Ω		0.12	0.16	V
		V_{OH}: RL = 32 Ω	2.03	2.36		
		V_{OL}: RL = 16 Ω		0.22	0.28	
		V_{OH}: RL = 16 Ω	2.15	2.25		
SNR	Signal-to-noise ratio	A-weighted, A_V=-1, RL = 32 Ω, THD+N < 0.4%, 20 Hz ≤ F ≤ 20 kHz		100		dB
Crosstalk	Channel separation	RL = 32 Ω, AV = -1, F = 1 kHz, F = 20 Hz to 20 kHz		-102		dB
		RL = 32 Ω, AV = -1, F = 1 kHz, F = 20 Hz to 20 kHz		-84		dB
C_i	Input capacitance			1		pF
GBP	Gain bandwidth product	RL = 32 Ω		1.1		MHz
SR	Slew rate, unity gain inverting	RL = 16 Ω		0.6		V/µs
V_{IO}	Input offset voltage	V_{icm}=V_{CC}/2		1	20	mV
t_{wu}	Wake-up time			100		ms

1. *Guaranteed by design and evaluation.*

4 Electrical characteristics curves

Figure 2. Open-loop frequency response V_{CC} = 2.5 V RL=16 Ω

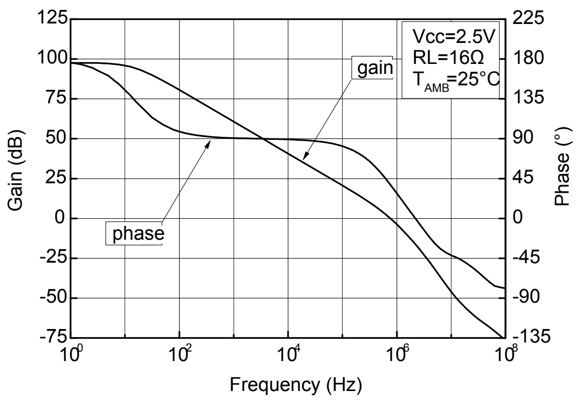


Figure 3. Open-loop frequency response V_{CC} = 5 V RL=16 Ω

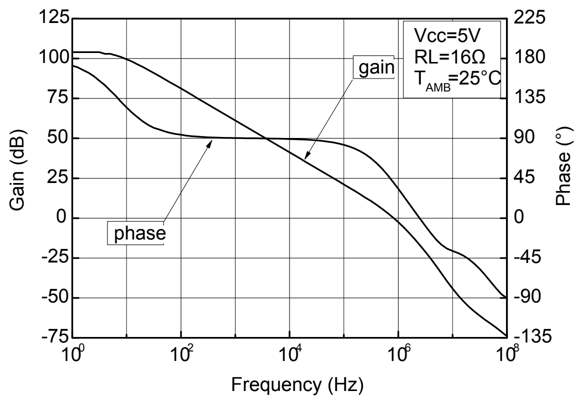


Figure 4. Open-loop frequency response V_{CC}=2.5 V RL=16 Ω, CL=400 pF

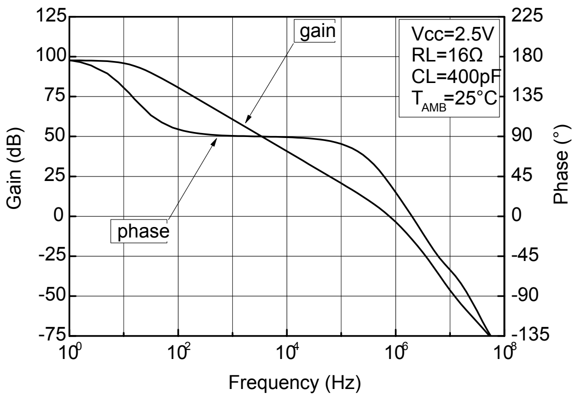


Figure 5. Open-loop frequency response V_{CC}=5 V RL=16 Ω, CL=400 pF

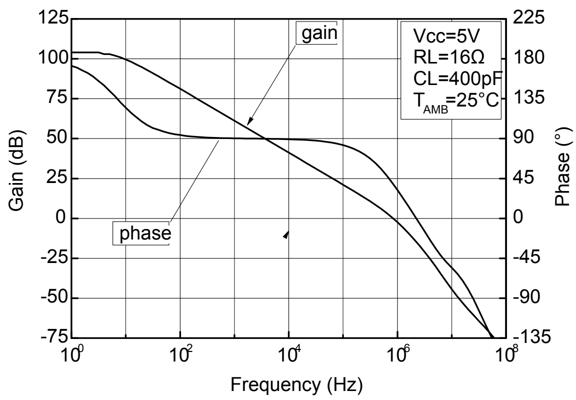


Figure 6. Open-loop frequency response V_{CC} = 2.5 V RL=32 Ω

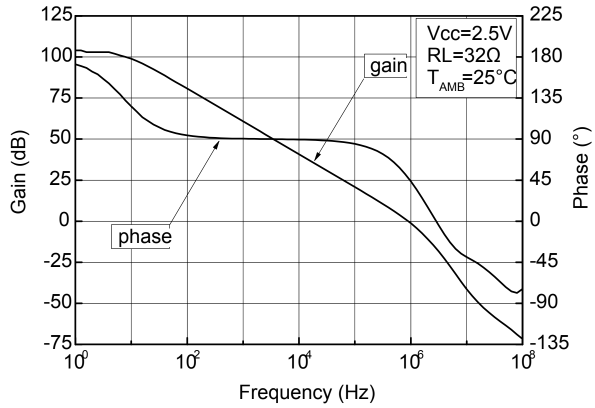


Figure 7. Open-loop frequency response V_{CC} = 5 V RL=32 Ω

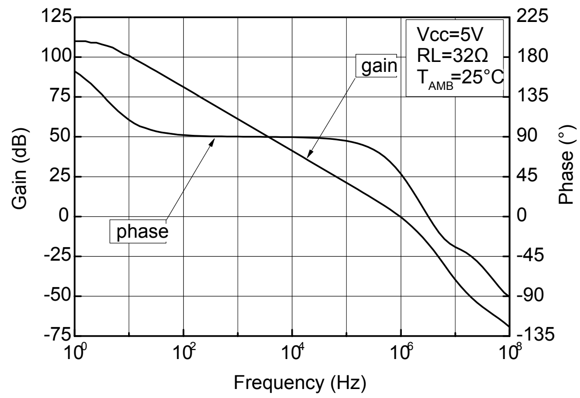


Figure 8. Open-loop frequency response V_{CC}=2.5 V RL=32 Ω, CL=400 pF

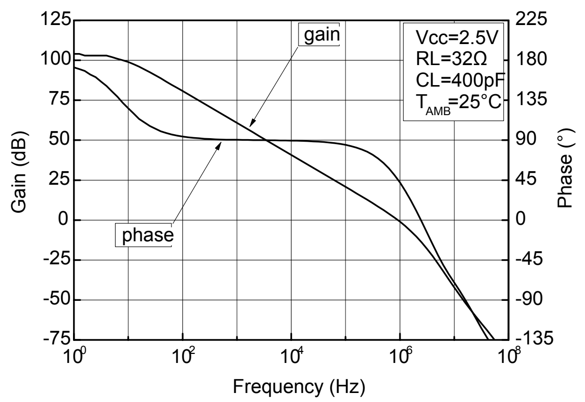


Figure 9. Open-loop frequency response V_{CC} = 5 V RL=32 Ω, CL=400 pF

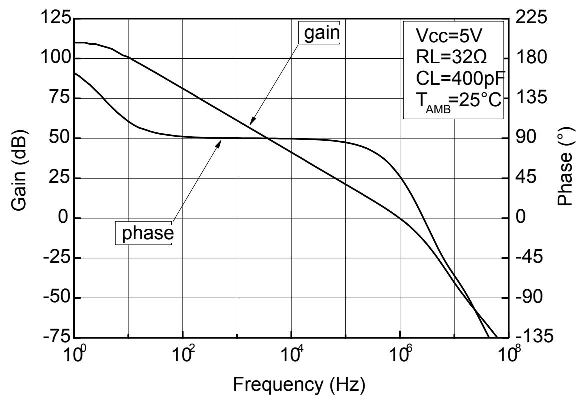


Figure 10. Open-loop frequency response V_{CC}=2.5 V RL=600 Ω

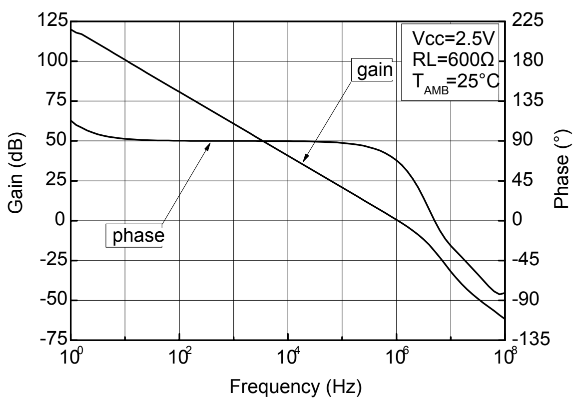


Figure 11. Open-loop frequency response V_{CC}=5 V RL=600 Ω

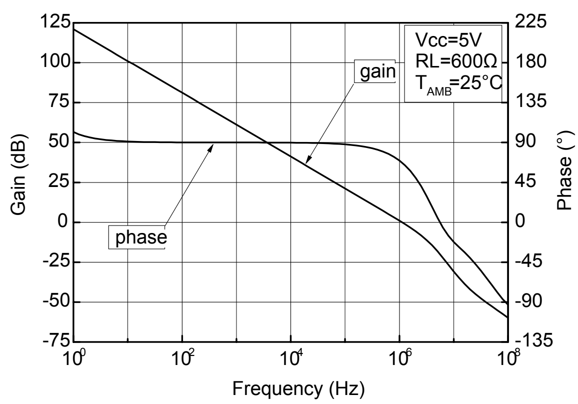


Figure 12. **Power derating curves**

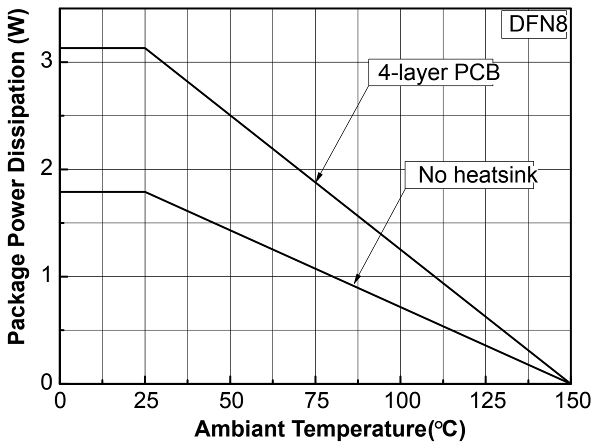


Figure 13. **Signal-to-noise ratio vs. power supply voltage A weighted A_V=-1**

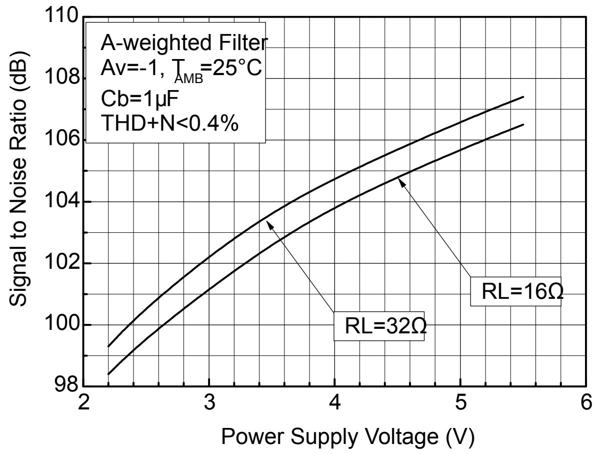


Figure 14. **Signal-to-noise ratio vs. power supply voltage A unweighted A_V=-1**

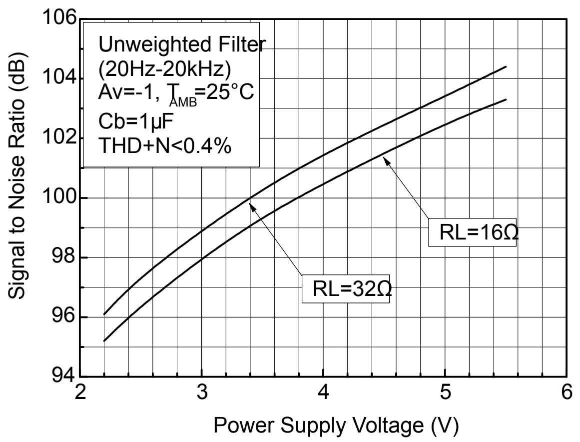


Figure 15. **Signal-to-noise ratio vs. power supply voltage A weighted A_V=-2**

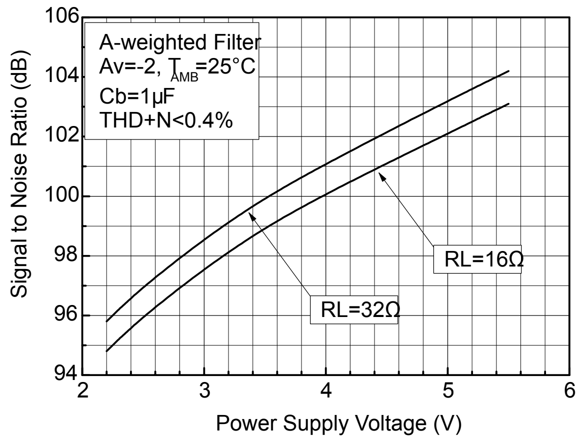


Figure 16. Signal-to-noise ratio vs. power supply voltage A unweighted A_V=-2

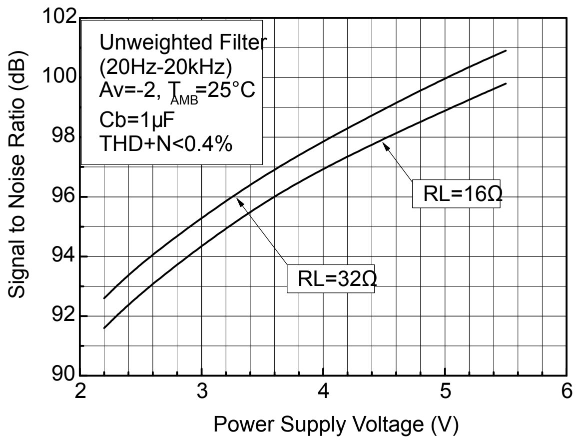


Figure 17. Signal-to-noise ratio vs. power supply voltage A weighted A_V=-4

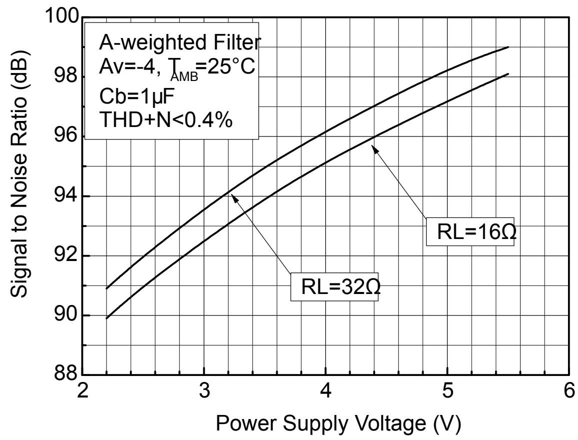


Figure 18. Signal-to-noise ratio vs. power supply voltage A unweighted A_V=-4

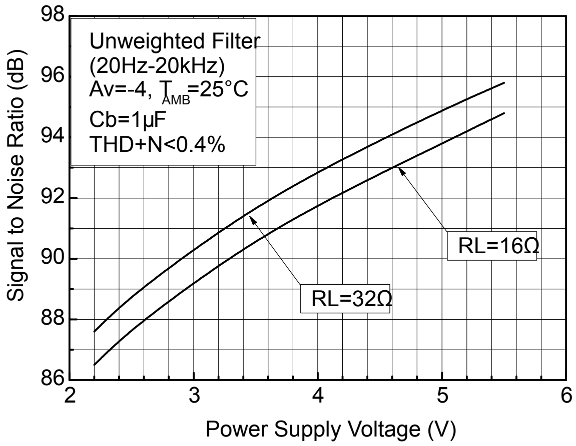


Figure 19. Power dissipation vs. output power per channel V_{CC}= 2.5 V

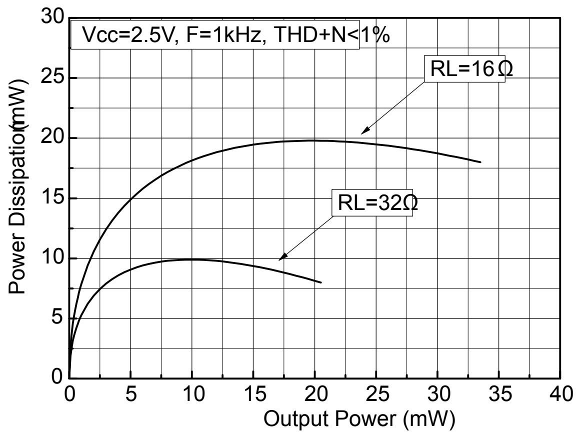


Figure 20. Power dissipation vs. output power per channel V_{CC}= 3.3 V

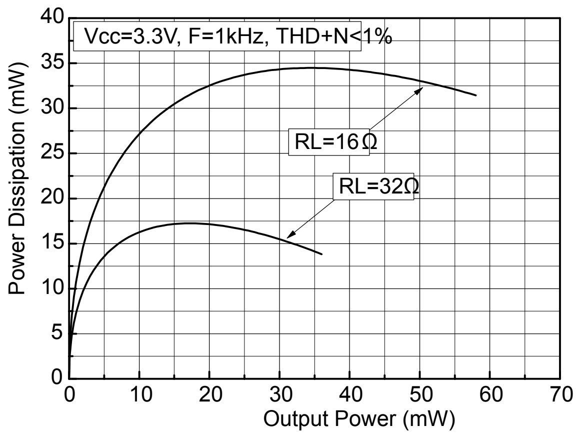


Figure 21. Power dissipation vs. output power per channel V_{CC}= 5 V

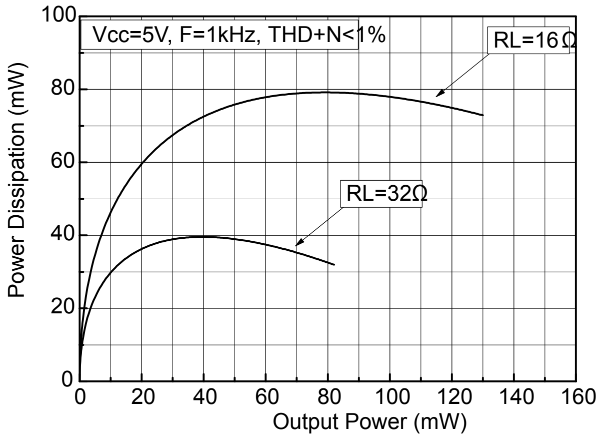


Figure 22. Power supply rejection ratio vs. frequency

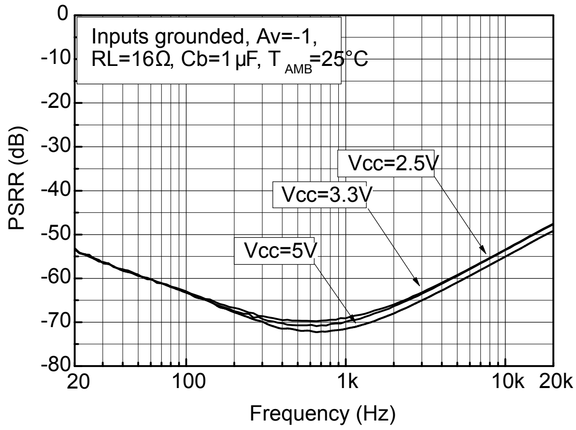


Figure 23. Power supply rejection ratio vs. frequency V_{CC}= 3.3 V

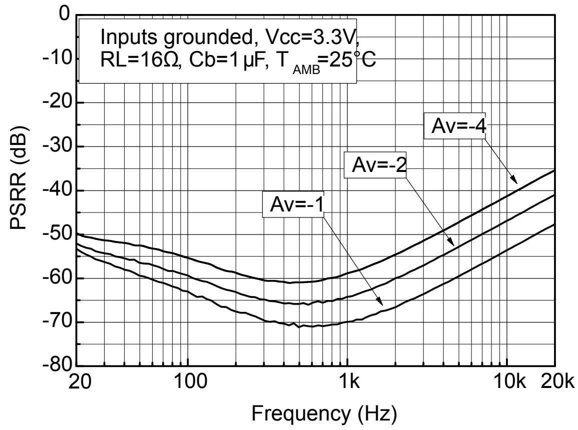


Figure 24. Power supply rejection ratio vs. frequency V_{CC}= 3.3 V, A_V= -1

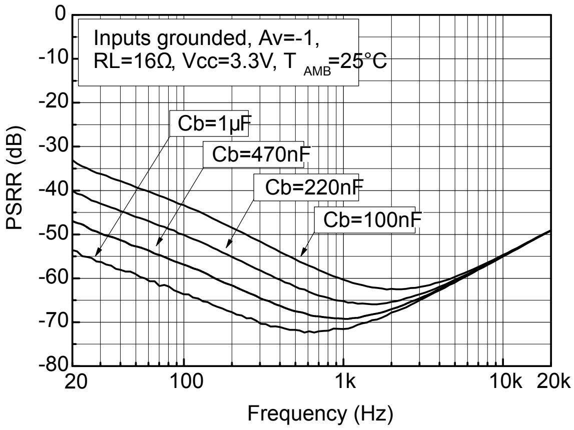


Figure 25. Total harmonic distortion plus noise vs. output power RL=16 Ω

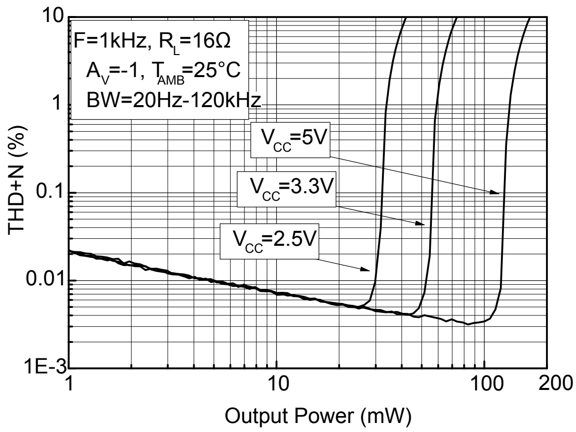


Figure 26. Total harmonic distortion plus noise vs. output power RL=16 Ω, F=20 kHz

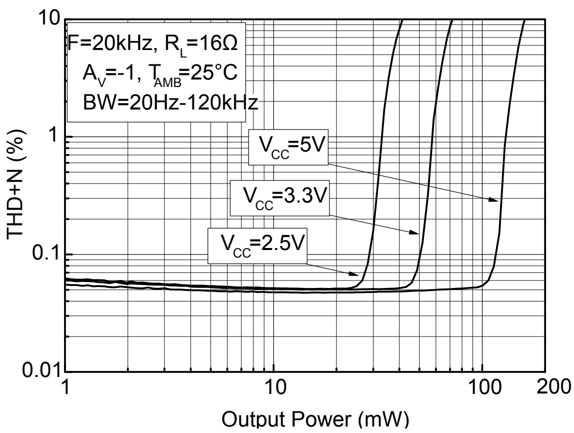


Figure 27. Total harmonic distortion plus noise vs. output power RL=32 Ω, F=1 kHz

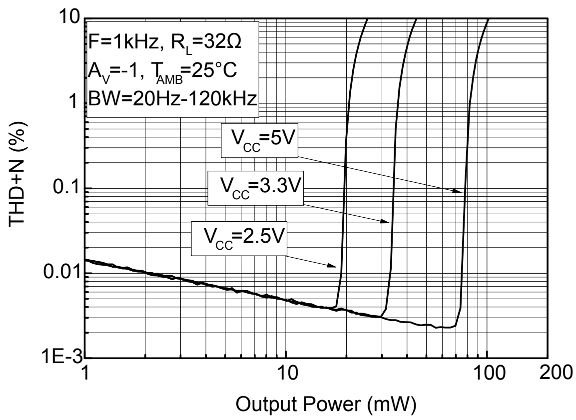


Figure 28. Total harmonic distortion plus noise vs. output power RL=32 Ω, F=20 kHz

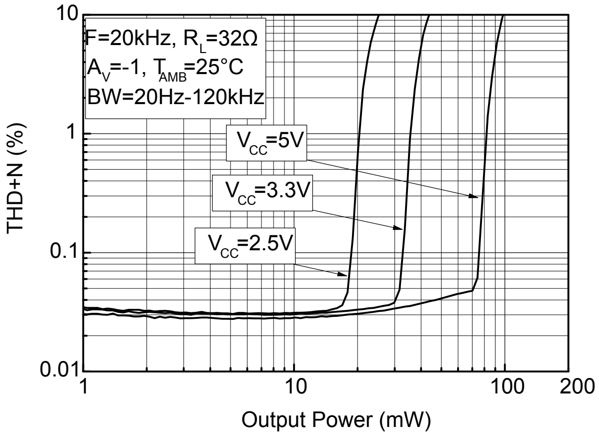


Figure 29. Total harmonic distortion plus noise vs. output power RL=600 Ω, F=1 kHz

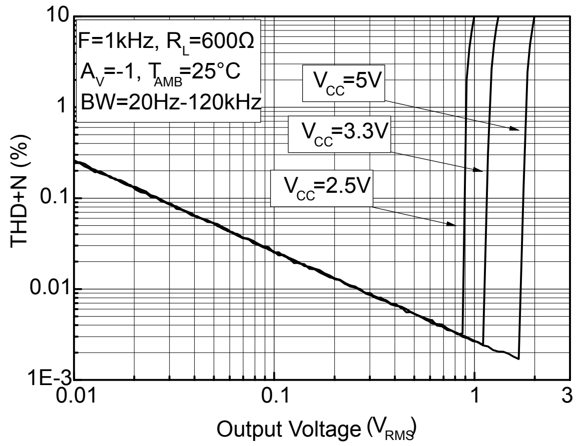


Figure 30. Total harmonic distortion plus noise vs. output power RL=600 Ω, F=20 kHz

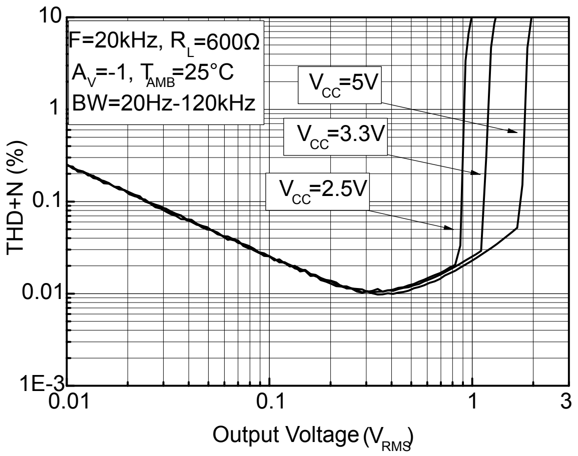


Figure 31. Total harmonic distortion plus noise vs. output power RL=16 Ω, F=1 kHz, A_V=-2

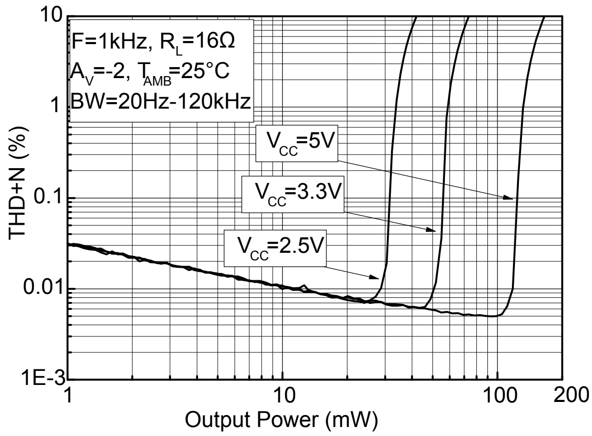


Figure 32. Total harmonic distortion plus noise vs. output power RL=16 Ω, F=20 kHz, A_V=-2

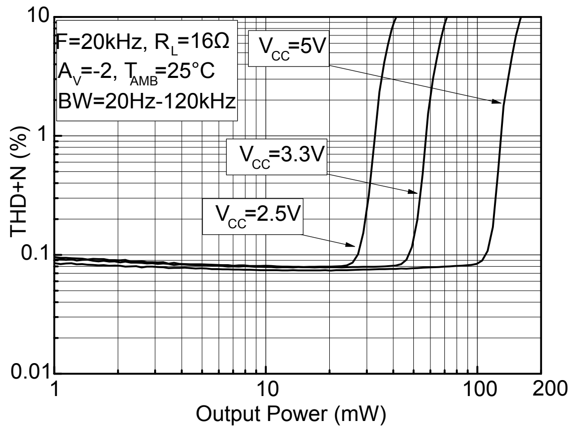


Figure 33. Total harmonic distortion plus noise vs. output power RL=32 Ω, F=1 kHz, A_V=-2

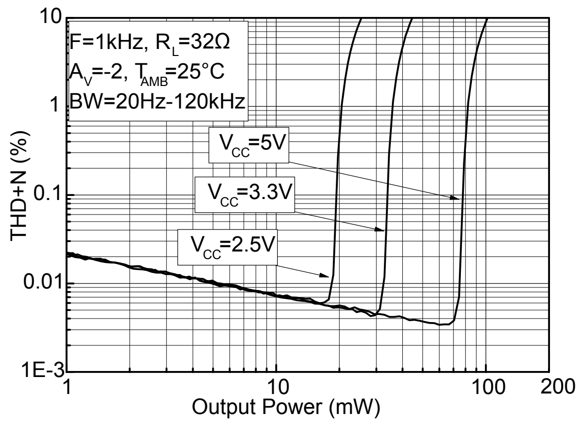


Figure 34. Total harmonic distortion plus noise vs. output power RL=32 Ω, F=20 kHz, A_V=-2

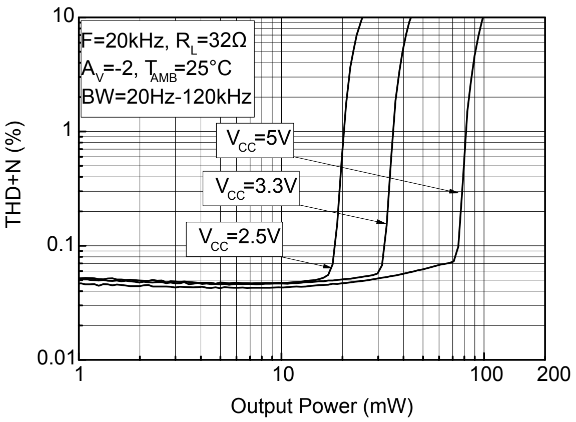


Figure 35. Total harmonic distortion plus noise vs. output power RL=600 Ω, F=1 kHz, A_V=-2

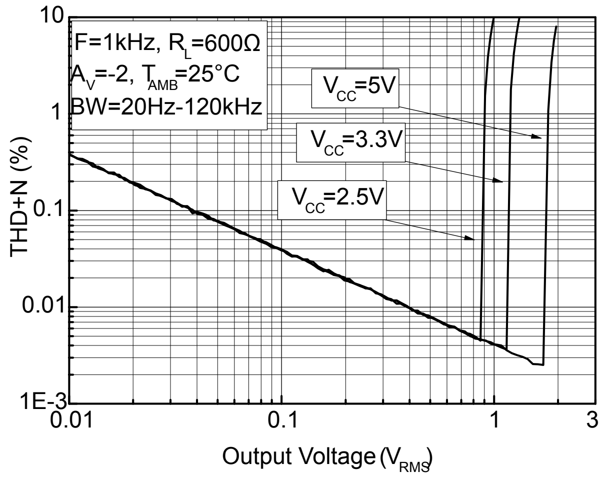


Figure 36. Total harmonic distortion plus noise vs. output power RL=600 Ω, F=20 kHz, A_V=-2

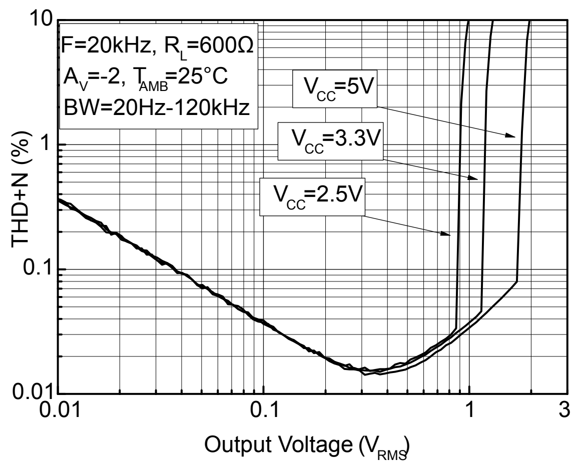


Figure 37. Total harmonic distortion plus noise vs. output power RL=16 Ω, F=1 kHz, A_V=-4

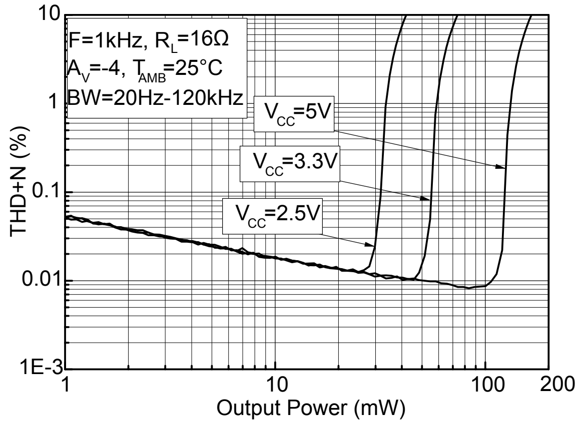


Figure 38. Total harmonic distortion plus noise vs. output power RL=16 Ω, F=20 kHz, A_V=-4

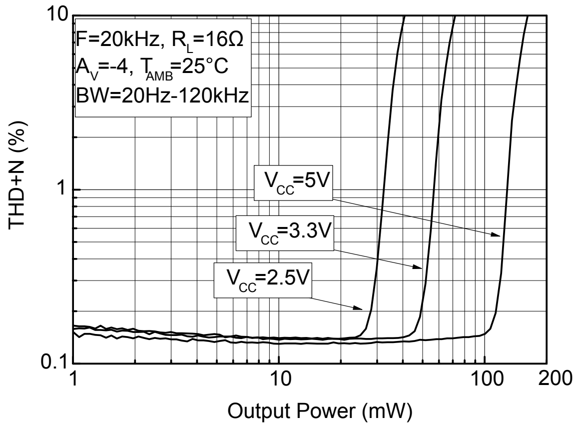


Figure 39. Total harmonic distortion plus noise vs. output power RL=32 Ω, F=1 kHz, A_V=-4

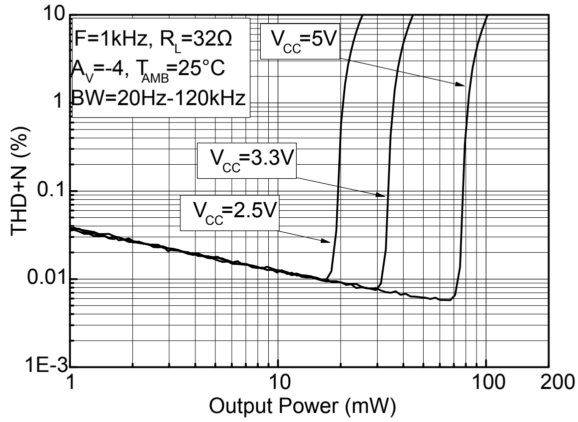


Figure 40. Total harmonic distortion plus noise vs. output power RL=32 Ω, F=20 kHz, A_V=-4

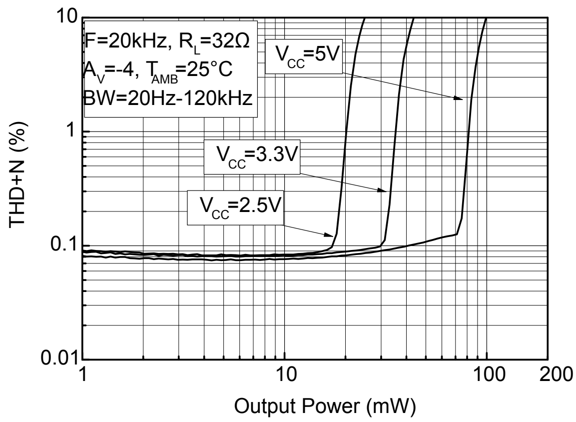


Figure 41. Total harmonic distortion plus noise vs. output power RL=600 Ω, F=1 kHz, A_V=-4

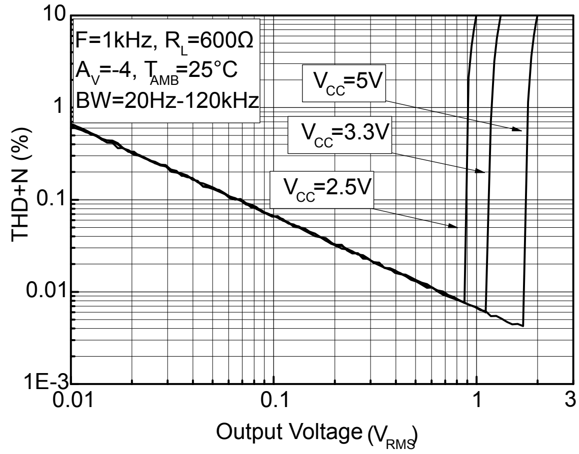


Figure 42. Total harmonic distortion plus noise vs. output power RL=600 Ω, F=20 kHz, A_V=-4

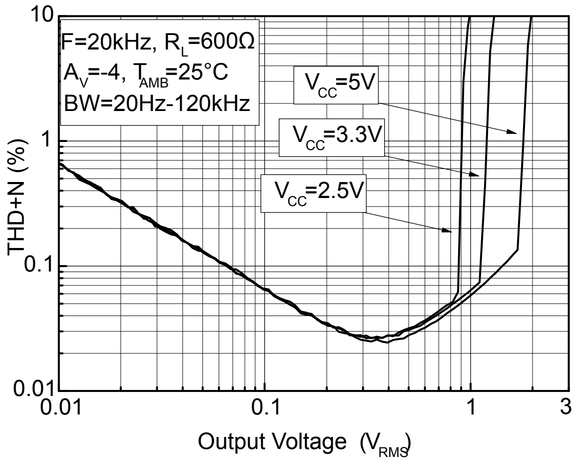


Figure 43. Total harmonic distortion plus noise vs. frequency RL=16 Ω

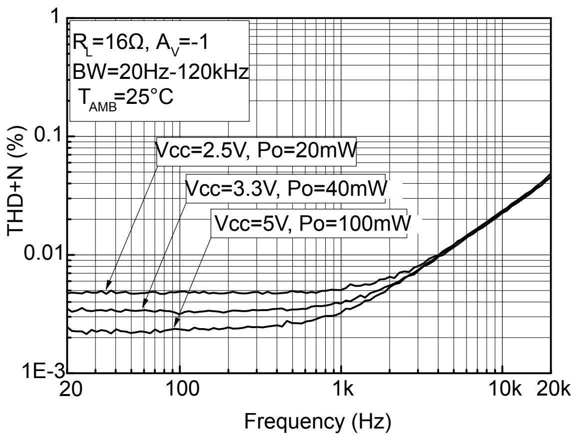


Figure 44. Total harmonic distortion plus noise vs. frequency RL=32 Ω

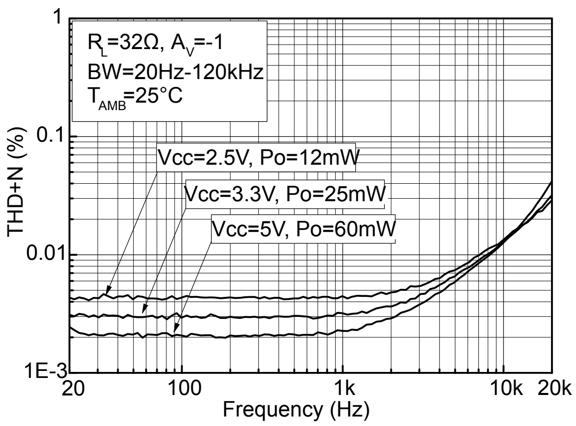


Figure 45. Total harmonic distortion plus noise vs. frequency RL=600 Ω

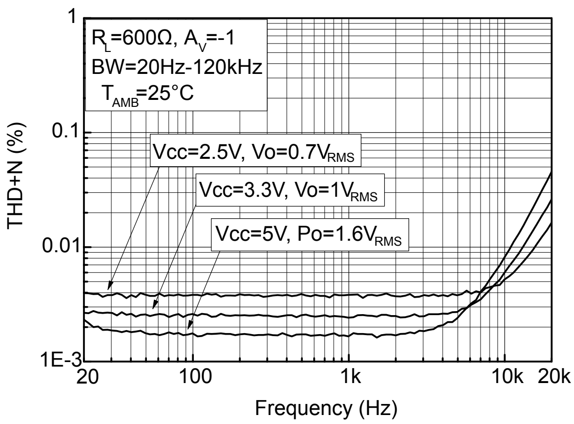


Figure 46. Total harmonic distortion plus noise vs. frequency RL=16 Ω, A_V=-2

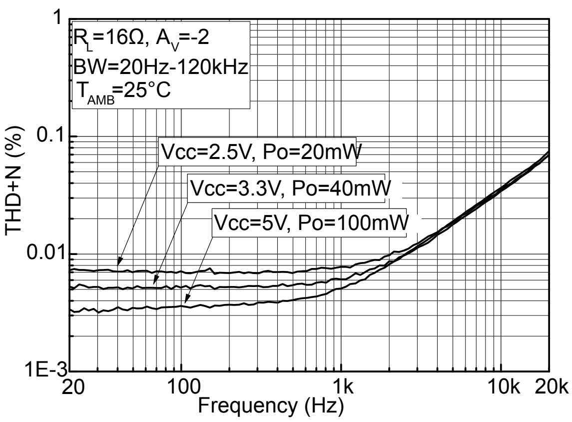


Figure 47. Total harmonic distortion plus noise vs. frequency RL=32 Ω, A_V=-2

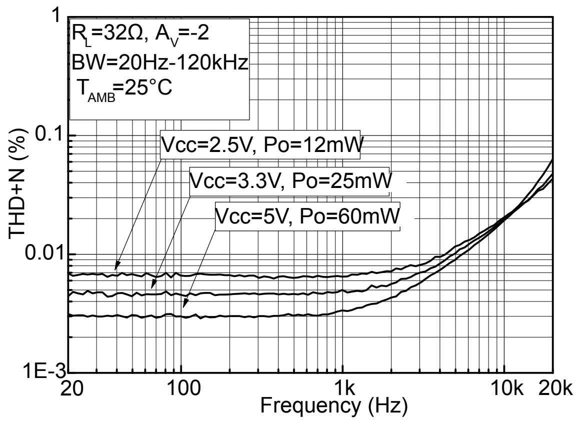


Figure 48. Total harmonic distortion plus noise vs. frequency RL=600 Ω, A_V=-2

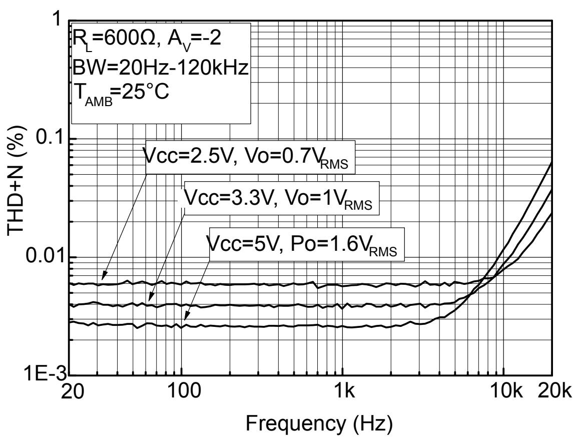


Figure 49. Total harmonic distortion plus noise vs. frequency RL=16 Ω, A_V=-4

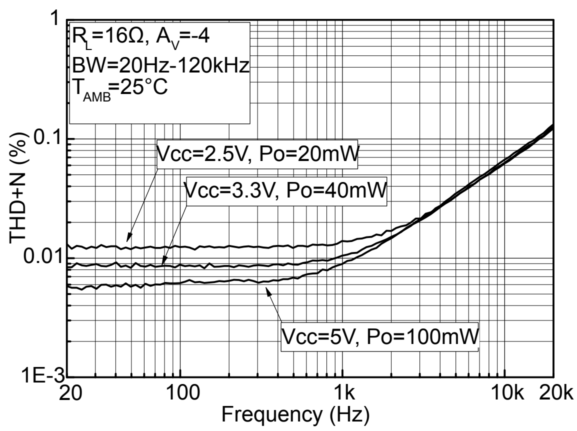


Figure 50. Total harmonic distortion plus noise vs. frequency RL=32 Ω, A_V=-4

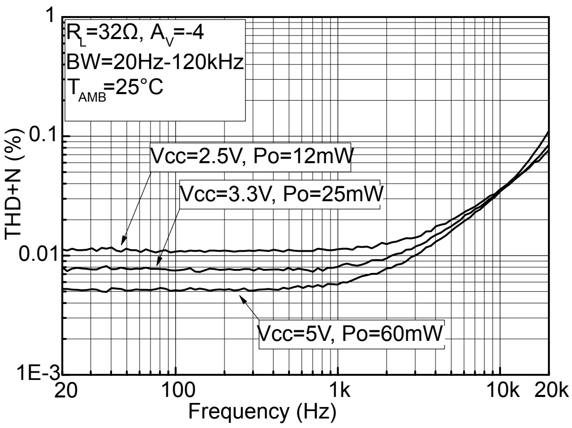


Figure 51. Total harmonic distortion plus noise vs. frequency RL=600 Ω, A_V=-4

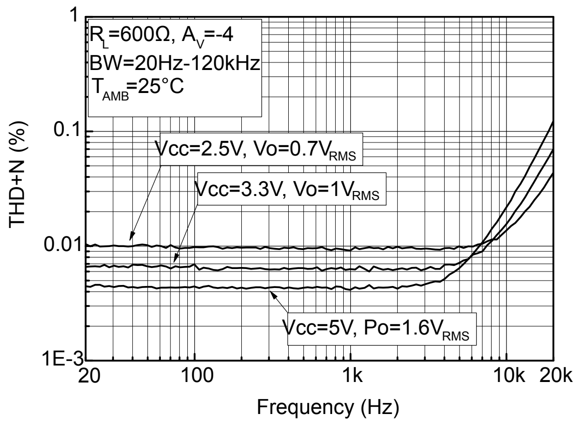


Figure 52. Output power vs. load resistance V_{CC}=2.5 V

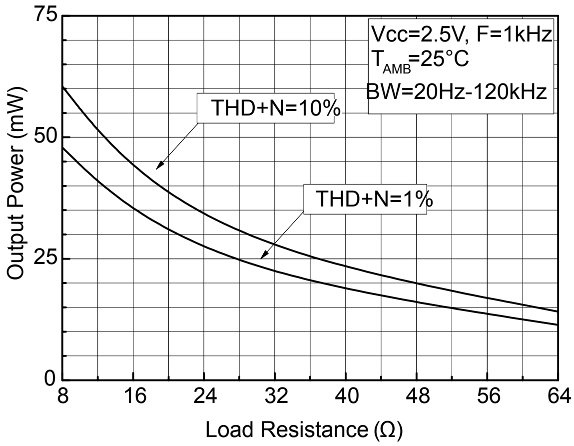


Figure 53. Output power vs. load resistance V_{CC}=3.3 V

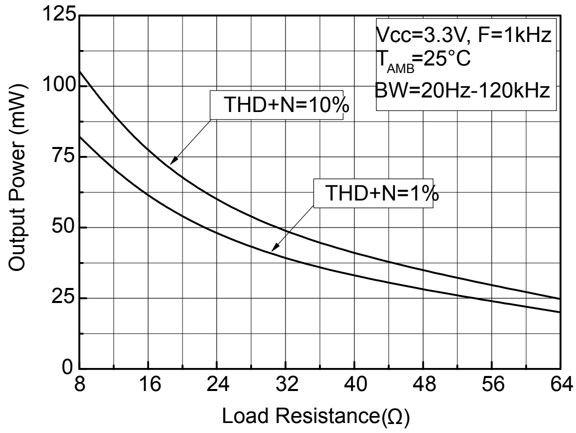


Figure 54. Output power vs. load resistance V_{CC}=5 V

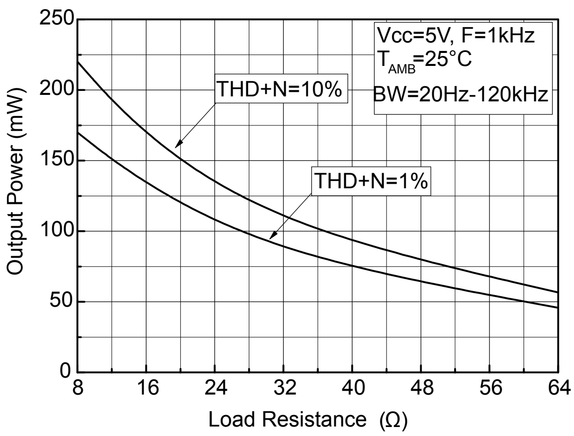


Figure 55. Output power vs. power supply voltage

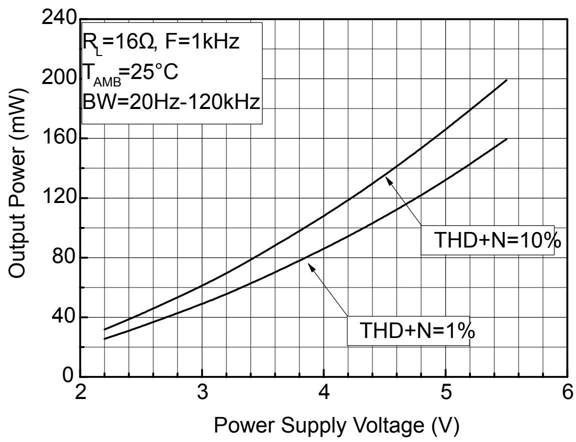


Figure 56. Output power vs. power supply voltage RL=32 Ω

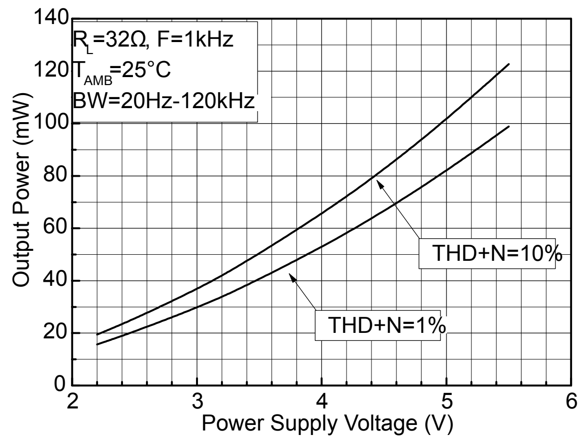


Figure 57. Output power swing vs. power supply voltage

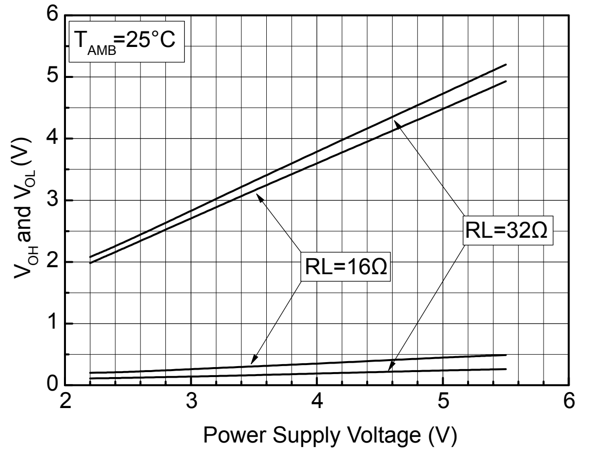


Figure 58. Current consumption vs. power supply voltage

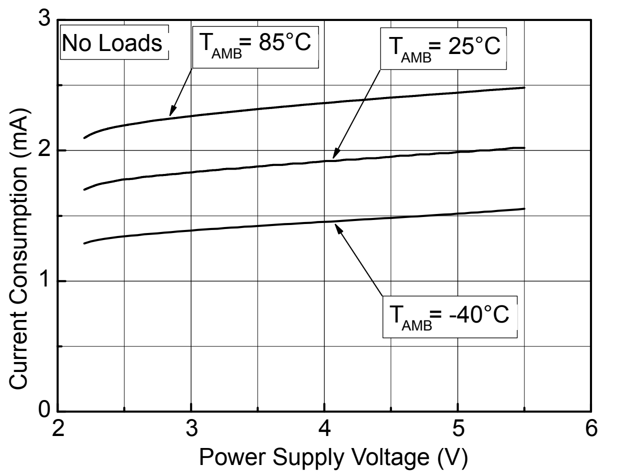


Figure 59. Current consumption vs. standby voltage

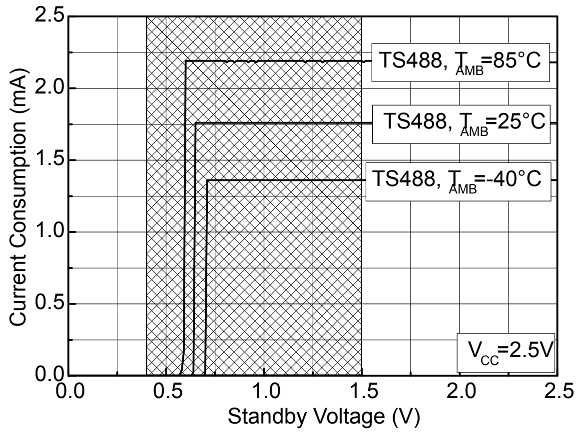


Figure 60. Current consumption vs. standby voltage V_{CC}=3.3 V

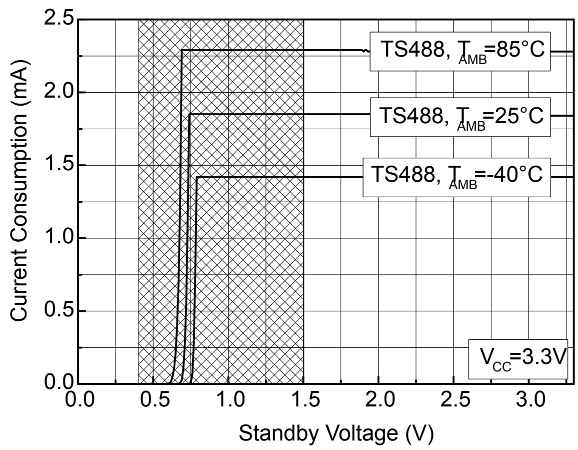


Figure 61. Current consumption vs. standby voltage V_{CC}=5 V

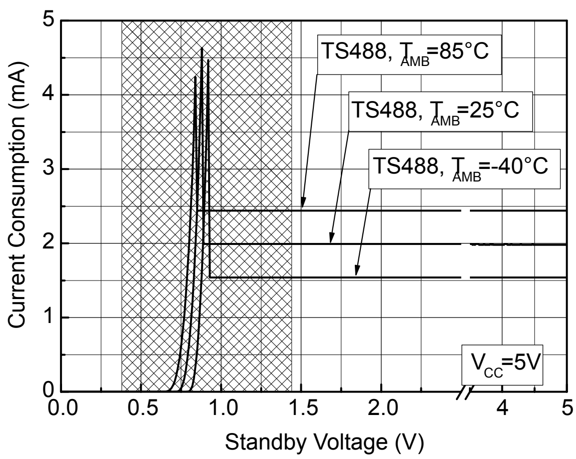


Figure 62. **Crosstalk vs. frequency**

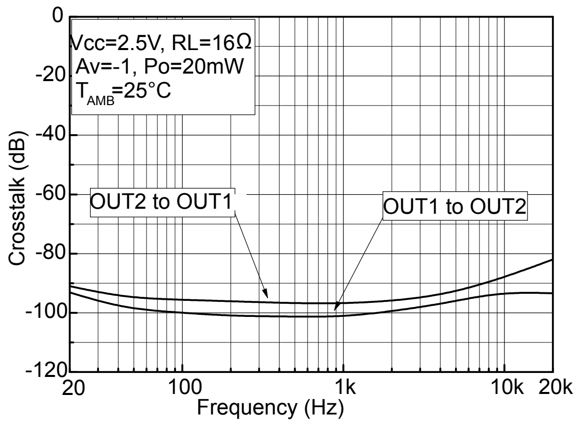


Figure 63. **Crosstalk vs. frequency RL=32 Ω**

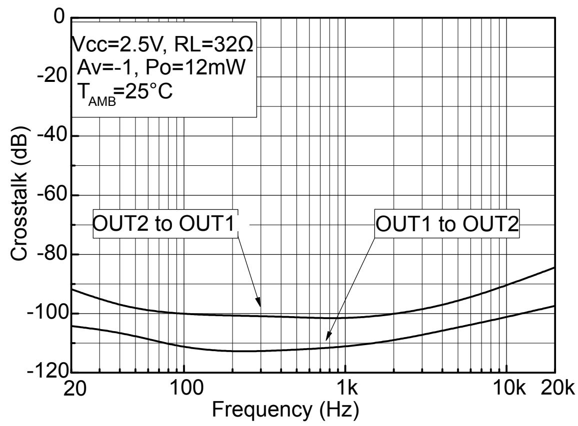


Figure 64. **Crosstalk vs. frequency RL=16 Ω, V_{CC}=3.3 V**

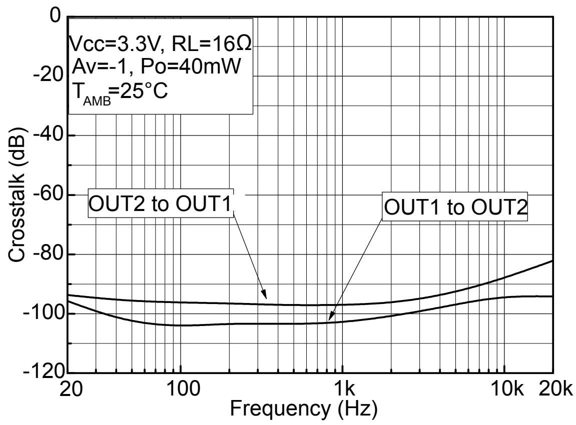


Figure 65. **Crosstalk vs. frequency RL=32 Ω, V_{CC}=3.3 V, P_O=25 mW**

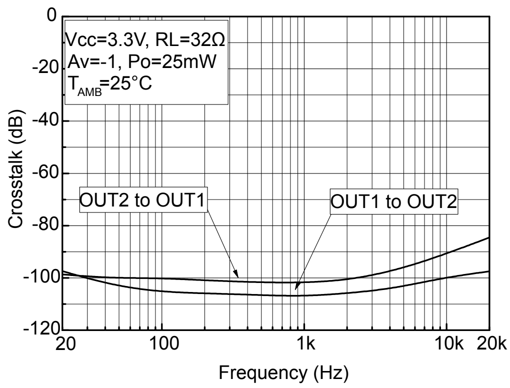


Figure 66. **Crosstalk vs. frequency RL=16 Ω, V_{CC}=5 V**

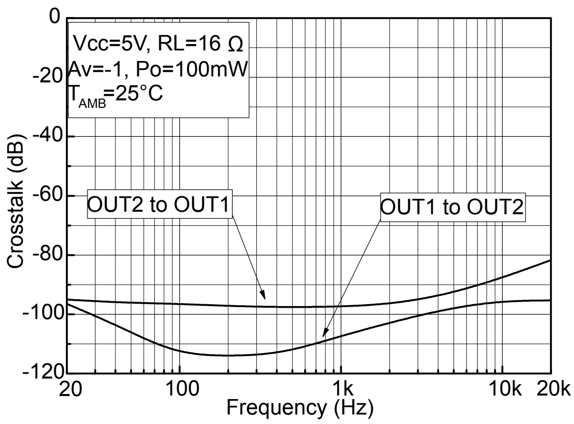


Figure 67. **Crosstalk vs. frequency RL=32 Ω, V_{CC}=5 V, P_O=60 mW**

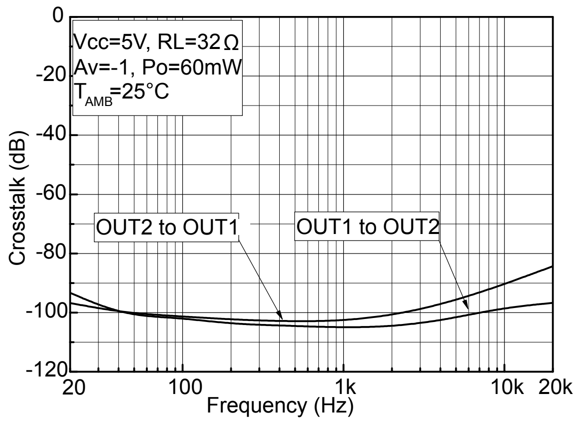


Figure 68. **Crosstalk vs. frequency RL=16 Ω, V_{CC}=2.5 V, P_O=20 mW A_V=-4**

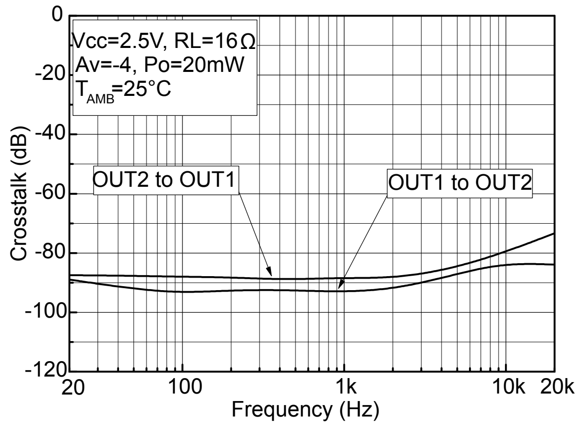


Figure 69. **Crosstalk vs. frequency RL=32 Ω, V_{CC}=2.5 V, P_O=12 mW, A_V=-4**

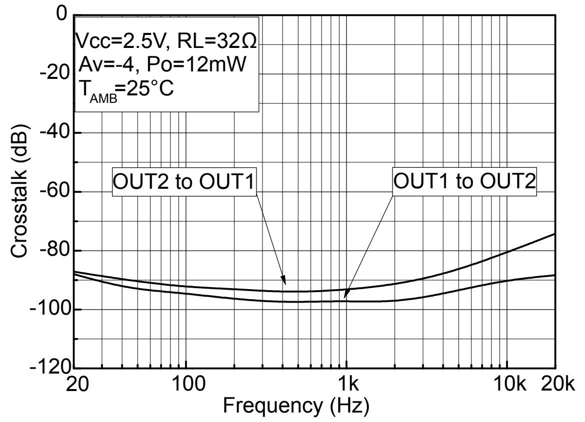


Figure 70. **Crosstalk vs. frequency RL=16 Ω, V_{CC}=3.3 V, P_O=40 mW, A_V=-4**

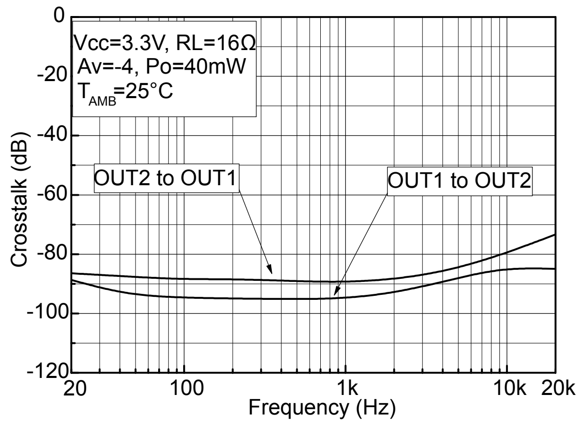


Figure 71. **Crosstalk vs. frequency RL=32 Ω, V_{CC}=3.3 V, P_O=25 mW, A_V=-4**

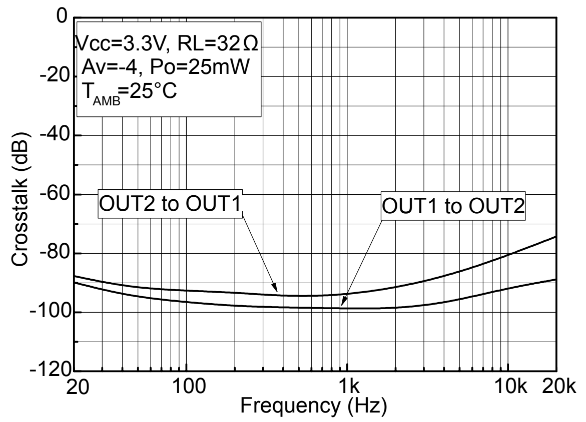


Figure 72. **Crosstalk vs. frequency RL=16 Ω, V_{CC}=5 V, P_O=100 mW, A_V=-4**

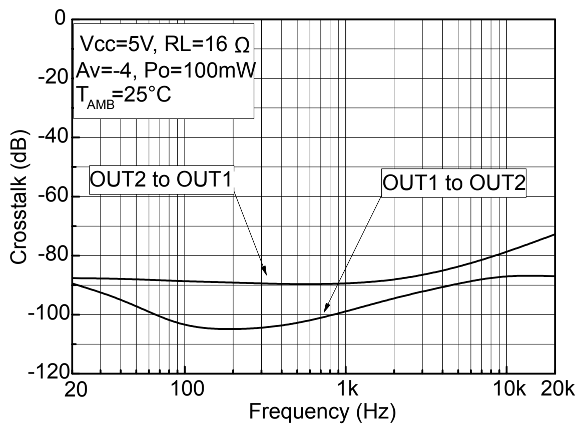
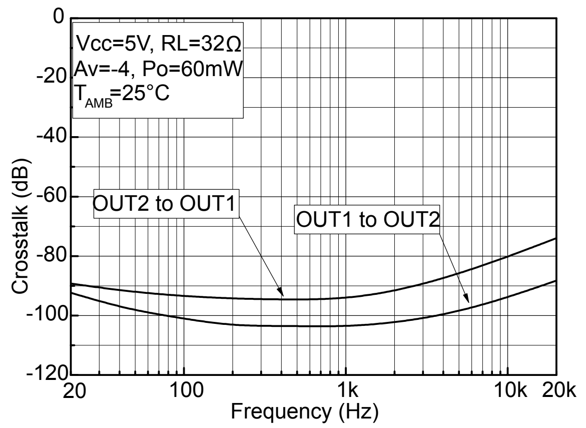


Figure 73. **Crosstalk vs. frequency RL=32 Ω, V_{CC}=5 V, P_O=60 mW**



5 Application information

5.1 Power dissipation and efficiency

Hypotheses:

- Voltage and current in the load are sinusoidal (V_{out} and I_{out})
- Supply voltage is a pure DC source (V_{CC})

Regarding the load, we have:

$$V_{OUT} = V_{PEAK} \sin \omega t (V) \quad (1)$$

and

$$I_{OUT} = \frac{V_{OUT}}{R_L} (A) \quad (2)$$

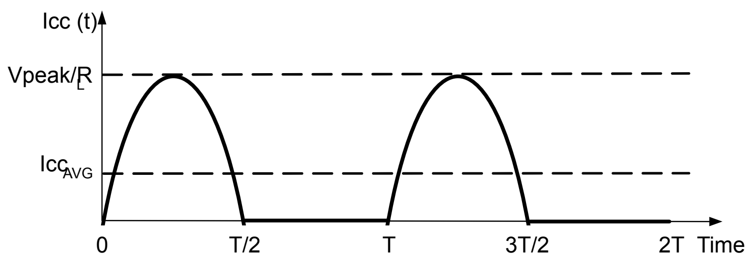
and

$$P_{OUT} = \frac{V^2{}_{PEAK}}{2R_L} (A) \quad (3)$$

The average current delivered by the power supply voltage is:

$$I_{CC_{AVG}} = \frac{1}{2\pi} \int_0^{\pi} \frac{V_{PEAK}}{R_L} \sin(t) dt = \frac{V_{PEAK}}{\pi R_L} (A) \quad (4)$$

Figure 74. Current delivered by power supply voltage in single-ended configuration



The power delivered by power supply voltage is:

$$P_{\text{supply}} = V_{CC} I_{CC_{AVG}} (W) \quad (5)$$

So, the power dissipation by each power amplifier is:

$$P_{diss} = P_{\text{supply}} - P_{OUT} (W) \quad (6)$$

$$P_{diss} = \frac{\sqrt{2} V_{CC}}{\pi \sqrt{R_L}} \sqrt{P_{OUT}} - P_{OUT} (W) \quad (7)$$

and the maximum value is obtained when:

$$\frac{\partial P_{diss}}{\partial P_{OUT}} = 0 \quad (8)$$

and its value is:

$$P_{dissMAX} = \frac{V^2{}_{CC}}{\pi^2 R_L}(W) \quad (9)$$

Note: This maximum value depends only on power supply voltage and load values.

The efficiency is the ratio between the output power and the power supply:

$$\eta = \frac{P_{OUT}}{P_{supply}} = \frac{\pi V_{peak}}{2V_{CC}} \quad (10)$$

The maximum theoretical value is reached when $V_{peak} = V_{CC}/2$, so

$$\eta = \frac{\pi}{4} = 78.5\,\% \quad (11)$$

5.2 Total power dissipation

The TS488 is stereo (dual channel) amplifier. It has two independent power amplifiers. Each amplifier produces heat due to its power dissipation. Therefore the maximum die temperature is the sum of each amplifier's maximum power dissipation. It is calculated as follows:

- $P_{diss\ R}$ = power dissipation due to the right channel power amplifier
- $P_{diss\ L}$ = power dissipation due to the left channel power amplifier
- Total $P_{diss} = P_{diss\ R} + P_{diss\ L}$ (W)

Typically, $P_{diss\ R}$ is equal to $P_{diss\ L}$, giving:

$$TotalP_{diss} = 2P_{dissR} = 2P_{dissL}$$
$$TotalP_{diss} = \frac{2\sqrt{2V_{CC}}}{\pi\sqrt{R_L}}\sqrt{P_{OUT}} - 2P_{OUT} \quad (12)$$

5.3 Lower cut-off frequency

The lower cut-off frequency F_{CL} of the amplifier depends on input capacitors C_{in} and output capacitors C_{out}.

The input capacitor C_{in} (output capacitor C_{out}) in serial with the input resistor R_{in} (load resistor R_L) of the amplifier is equivalent to a first order high pass filter. Assuming that F_{CL} is the lowest frequency to be amplified (with a 3 dB attenuation), the minimum value of the C_{in} (Cout) is:

$$C_{in} = \frac{1}{2\pi \cdot F_{CL} \cdot R_{in}}$$
$$C_{out} = \frac{1}{2\pi \cdot F_{CL} \cdot R_L} \quad (13)$$

Figure 75. Lower cut-off frequency vs. input capacitor

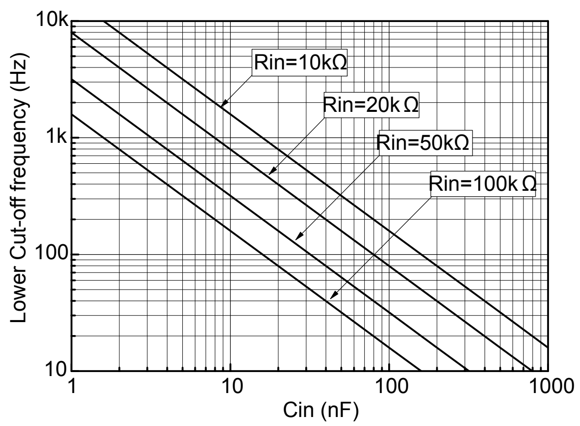
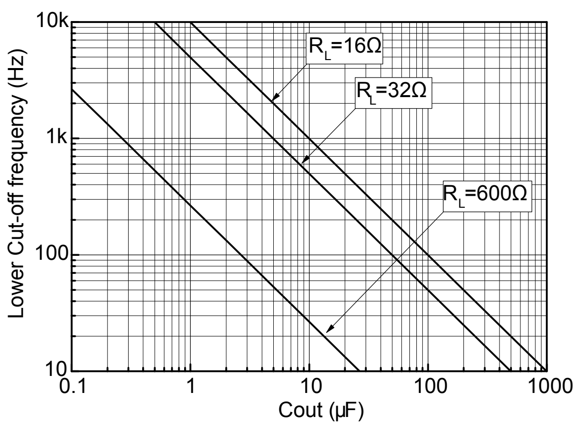


Figure 76. Lower cut-off frequency vs. output capacitor



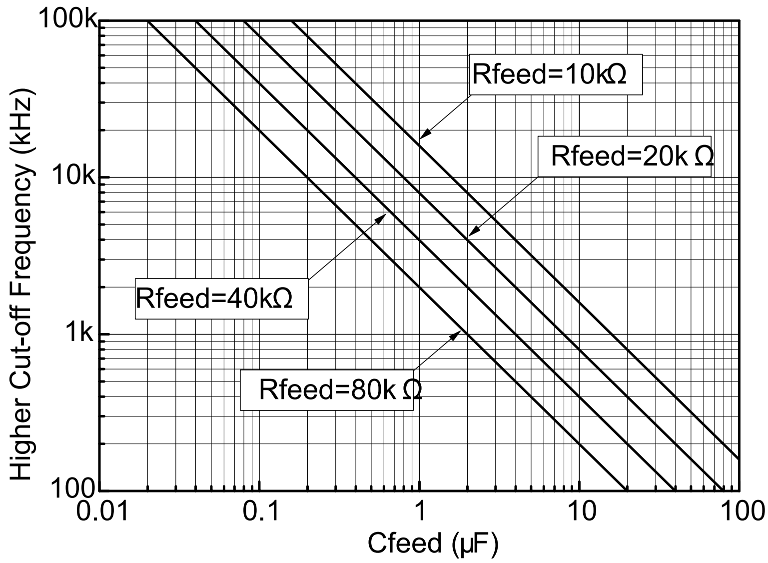
Note: In case F_{CL} is kept the same for calculation, It must be taken in account that the 1st order high-pass filter on the input and the 1st order high-pass filter on the output create a 2nd order high-pass filter in the audio signal path with an attenuation 6 dB on F_{CL} and a roll-off 40 db⁄decade.

5.4 Higher cut-off frequency

In the high-frequency region, you can limit the bandwidth by adding a capacitor C_{feed} in parallel with R_{feed}. It forms a low-pass filter with a -3 dB cut-off frequency F_{CH}. Assuming that F_{CH} is the highest frequency to be amplified (with a 3 dB attenuation), the maximum value of C_{feed} is:

$$F_{CH} = \frac{1}{2\pi \cdot R_{feed} \cdot C_{feed}} \quad (14)$$

Figure 77. Higher cut-off frequency vs. feedback capacitor



5.5 Gain settings

In the flat frequency response region (with no effect from C_{in}, C_{out}, C_{feed}), the output voltage is:

$$V_{OUT} = V_{IN} \cdot \left(-\frac{R_{feed}}{R_{in}}\right) = V_{IN} \cdot A_V \quad (15)$$

The gain A_V is:

$$A_V = -\frac{R_{feed}}{R_{in}} \quad (16)$$

5.6 Decoupling of the circuit

Two capacitors are needed to properly bypass the TS488, a power supply capacitor C_s and a bias voltage bypass capacitor C_b.

C_s has a strong influence on the THD+N in the high frequency range (above 7 kHz) and indirectly on the power supply disturbances. With 1 µF, you can expect THD+N performance to be similar to the one shown in the datasheet. If C_s is lower than 1 µF, the THD+N increases in the higher frequencies and disturbances on the power supply rail are less filtered. On the contrary, if C_s is higher than 1 µF, the disturbances on the power supply rail are more filtered.

C_b has an influence on the THD+N in the low frequency range. Its value is critical on the PSRR with grounded inputs in the lower frequencies:

- If C_b is lower than 1 µF, the THD+N improves and the PSRR worsens
- If C_b is higher than 1 µF, the benefit on the THD+N and PSRR is small

Note: The input capacitor C_{in} also has a significant effect on the PSRR at lower frequencies. The lower the value of C_{in}, the higher the PSRR.

5.7 Decoupling of the circuit

Two capacitors are needed to properly bypass the TS488, a power supply capacitor C_s and a bias voltage bypass capacitor C_b.

C_s has a strong influence on the THD+N in the high frequency range (above 7 kHz) and indirectly on the power supply disturbances. With 1 µF, you can expect THD+N performance to be similar to the one shown in the datasheet. If C_s is lower than 1 µF, the THD+N increases in the higher frequencies and disturbances on the power supply rail are less filtered. On the contrary, if C_s is higher than 1 µF, the disturbances on the power supply rail are more filtered.

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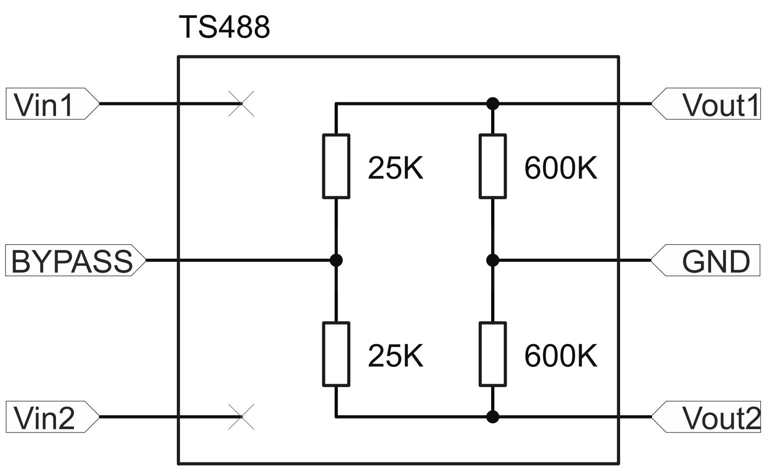
- If C_b is lower than 1 µF, the THD+N improves and the PSRR worsens
- If C_b is higher than 1 µF, the benefit on the THD+N and PSRR is small

Note: The input capacitor C_{in} also has a significant effect on the PSRR at lower frequencies. The lower the value of C_{in}, the higher the PSRR.

5.8 Standby mode

When the standby mode is activated an internal circuit of the TS488 is charged (see Figure 78. Internal equivalent schematic of the TS488 in standby mode). A time required to change the internal circuit is a few microseconds

Figure 78. Internal equivalent schematic of the TS488 in standby mode



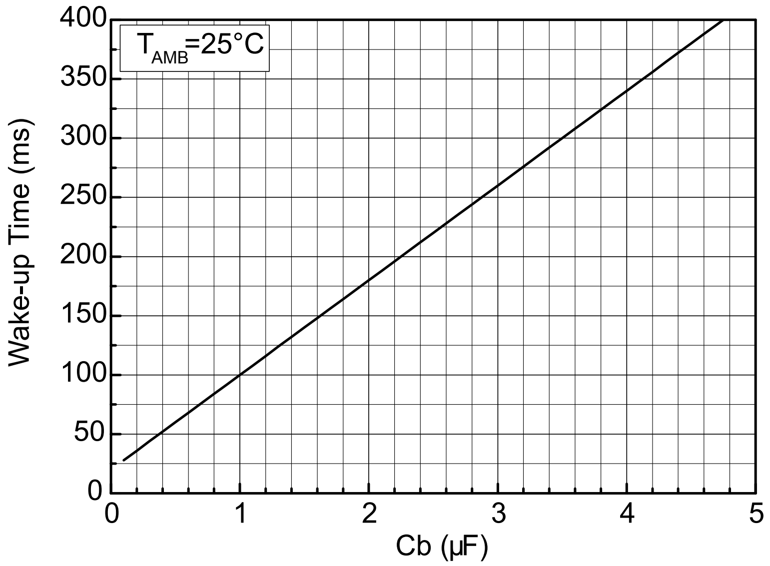
5.9 Wake-up time

When the standby is released to put the device ON, the bypass capacitor C_b is charged immediately. As C_b is directly linked to the bias of the amplifier, the bias does not work properly until the C_b voltage is correct. The time to reach this voltage plus a time delay of 20 ms (pop precaution) is called the wake-up time or t_{WU}; it is specified in the electrical characteristics table with C_b = 1 µF.

If C_b has a value other than 1 µF, t_{WU} can be calculated by applying the following formulas or can be read directly from Figure 79. Typical wake-up time vs. bypass capacitance

$$t_{WU} = \frac{C_b \cdot 2.5}{0.03125} + 20[ms; \mu F] \quad (17)$$

Figure 79. Typical wake-up time vs. bypass capacitance



Note: It is assumed that the C_b voltage is equal to 0 V. If the C_b voltage is not equal to 0 V, the wake-up time is shorter.

5.10 POP performance

Pop performance is closely related to the size of the input capacitor C_{in}. The size of C_{in} is dependent on the lower cut-off frequency and PSRR values requested.

In order to reach low pop, C_{in} must be charged to VCC/2 in less than 20 ms. To follow this rule, the equivalent input constant time ($R_{in}C_{in}$) should be less then 6.7 ms:

tin = R_{in} x C_{in} < 0.0067 (s)

Example calculation:

In the typical application schematic R_{in} is 20 kΩ and C_{in} is 330 nF. The lower cut-off frequency (-3 db attenuation) is given by the following formula

$$F_{CL} = \frac{1}{2\pi \cdot R_{in} \cdot C_{in}} \quad (18)$$

With the values above, the result is F_{CL} = 25 Hz.

In this case, tin = R_{in} x C_{in}=6.6 ms.

This value is sufficient with regard to the previous formula, thus we can state that the pop is imperceptible.

Connecting the headphones

Generally headphones are connected using jack connectors. To prevent a pop in the headphones when plugging in the jack, a pull-down resistor should be connected in parallel with each headphone output. This allows the capacitors C_{out} to be charged even when the headphones are not plugged in.

Pull-down resistors with a value of 1 kΩ are high enough to be a negligible load, and low enough to charge the capacitors C_{out} in less than one second.

Note: The pop&click reduction circuitry works properly only when both channels have the same value for the external components C_{in}, C_{out}, R_{load} and $R_{pulldown}$.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 DFN8 2x2 package information

Figure 80. DFN8 2x2 package outline

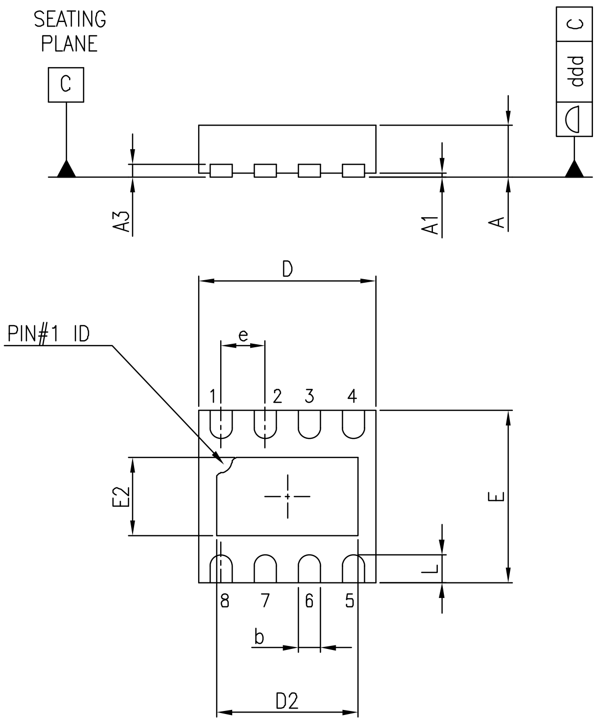


Table 7. DFN8 2x2 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.51	0.55	0.60	0.020	0.022	0.024
A1			0.05			0.002

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A3		0.15			0.006	
b	0.18	0.25	0.30	0.007	0.010	0.012
D	1.85	2.00	2.15	0.073	0.079	0.085
D2	1.45	1.60	1.70	0.057	0.063	0.067
E	1.85	2.00	2.15	0.073	0.079	0.085
E2	0.75	0.90	1.00	0.030	0.035	0.039
e		0.50			0.020	
L	0.225	0.325	0.425	0.009	0.013	0.017
ddd			0.08			0.003

Revision history

Table 8. Document revision history

Date	Version	Changes
02-Jan-2006	1	Initial release.
01-Feb-2006	2	Removal of typical application schematic on first page (it appears in Figure 1 on page 3). Minor grammatical and formatting corrections throughout
04-Aug-2006	3	Update of marking. Update of DFN8 package height. Editorial update.
15-Sep-2006	4	Revision corresponding to the release to production of the TS488 - TS489
14-May-2012	5	Removed obsolete part numbers TS489IQT and TS489IST from the cover page and Table 8: Order codes. Updated ECOPACK® text in Section 5: Package mechanical data. Updated package in Section 5.2: DFN8 package.
13-Apr-2017	6	Updated Section 5.2: DFN8 package information: "L" dimension changed from 0.5 mm to 0.425 mm. Minor changes throughout the document.
17-Apr-2019	7	Removed the part number TS489 and all its references.
06-May-2020	8	UpdatedFigure 1. Typical application for the TS488.

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