

CMLDM8002A
CMLDM8002AG*
CMLDM8002AJ

SURFACE MOUNT SILICON
DUAL P-CHANNEL
ENHANCEMENT-MODE
MOSFETS



SOT-563 CASE

* Device is **Halogen Free** by design



www.centrasemi.com

DESCRIPTION:

These CENTRAL SEMICONDUCTOR devices are dual chip P-Channel enhancement-mode MOSFETs, manufactured by the P-Channel DMOS Process, designed for high speed pulsed amplifier and driver applications. The CMLDM8002A utilizes the USA pinout configuration, while the CMLDM8002AJ, utilizing the Japanese pinout configuration, is available as a special order. These special dual transistor devices offer low $r_{DS(on)}$ and low $V_{DS(on)}$.

MARKING CODES: CMLDM8002A: C08
CMLDM8002AG*: CG8
CMLDM8002AJ: CJ8

APPLICATIONS:

- Load/Power Switches
- Power Supply Converter Circuits
- Battery Powered Portable Equipment

FEATURES:

- Dual Chip Device
- Low $r_{DS(on)}$
- Low $V_{DS(on)}$
- Low Threshold Voltage
- Fast Switching
- Logic Level Compatible
- Small SOT-563 package

MAXIMUM RATINGS: ($T_A=25^\circ\text{C}$)

Drain-Source Voltage
Drain-Gate Voltage
Gate-Source Voltage
Continuous Drain Current
Continuous Source Current (Body Diode)
Maximum Pulsed Drain Current
Maximum Pulsed Source Current
Power Dissipation (Note 1)
Power Dissipation (Note 2)
Power Dissipation (Note 3)
Operating and Storage Junction Temperature
Thermal Resistance

SYMBOL

V_{DS} 50
 V_{DG} 50
 V_{GS} 20
 I_D 280
 I_S 280
 I_{DM} 1.5
 I_{SM} 1.5
 P_D 350
 P_D 300
 P_D 150
 T_J, T_{stg} -65 to +150
 Θ_{JA} 357

UNITS

V
V
V
mA
mA
A
A
mW
mW
mW
 $^\circ\text{C}$
 $^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS PER TRANSISTOR: ($T_A=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
I_{GSSF}, I_{GSSR}	$V_{GS}=20\text{V}, V_{DS}=0$		100	nA
I_{DSS}	$V_{DS}=50\text{V}, V_{GS}=0$		1.0	μA
I_{DSS}	$V_{DS}=50\text{V}, V_{GS}=0, T_J=125^\circ\text{C}$		500	μA
$I_{D(ON)}$	$V_{GS}=10\text{V}, V_{DS}=10\text{V}$	500		mA
BV_{DSS}	$V_{GS}=0, I_D=10\mu\text{A}$	50		V
$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.0	2.5	V
$V_{DS(ON)}$	$V_{GS}=10\text{V}, I_D=500\text{mA}$		1.5	V
$V_{DS(ON)}$	$V_{GS}=5.0\text{V}, I_D=50\text{mA}$		0.15	V
V_{SD}	$V_{GS}=0, I_S=115\text{mA}$		1.3	V

Notes: (1) Ceramic or aluminum core PC Board with copper mounting pad area of 4.0mm²
(2) FR-4 Epoxy PC Board with copper mounting pad area of 4.0mm²
(3) FR-4 Epoxy PC Board with copper mounting pad area of 1.4mm²

R7 (8-June 2015)

CMLDM8002A
CMLDM8002AG*
CMLDM8002AJ

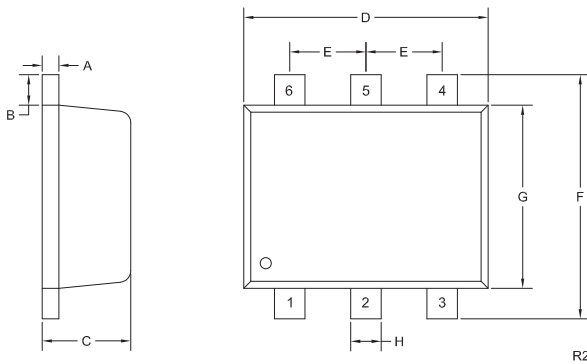
**SURFACE MOUNT SILICON
DUAL P-CHANNEL
ENHANCEMENT-MODE
MOSFETS**



ELECTRICAL CHARACTERISTICS PER TRANSISTOR - Continued: ($T_A=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$r_{DS(ON)}$	$V_{GS}=10\text{V}, I_D=500\text{mA}$			2.5	Ω
$r_{DS(ON)}$	$V_{GS}=10\text{V}, I_D=500\text{mA}, T_J=125^\circ\text{C}$			4.0	Ω
$r_{DS(ON)}$	$V_{GS}=5.0\text{V}, I_D=50\text{mA}$			3.0	Ω
$r_{DS(ON)}$	$V_{GS}=5.0\text{V}, I_D=50\text{mA}, T_J=125^\circ\text{C}$			5.0	Ω
gFS	$V_{DS}=10\text{V}, I_D=200\text{mA}$	200			mS
C_{rss}	$V_{DS}=25\text{V}, V_{GS}=0, f=1.0\text{MHz}$			7.0	pF
C_{iss}	$V_{DS}=25\text{V}, V_{GS}=0, f=1.0\text{MHz}$			70	pF
C_{oss}	$V_{DS}=25\text{V}, V_{GS}=0, f=1.0\text{MHz}$			15	pF
$Q_{g(tot)}$	$V_{DS}=25\text{V}, V_{GS}=4.5\text{V}, I_D=100\text{mA}$		0.72		nC
Q_{gs}	$V_{DS}=25\text{V}, V_{GS}=4.5\text{V}, I_D=100\text{mA}$		0.25		nC
Q_{gd}	$V_{DS}=25\text{V}, V_{GS}=4.5\text{V}, I_D=100\text{mA}$		0.16		nC
t_{on}, t_{off}	$V_{DD}=30\text{V}, V_{GS}=10\text{V}, I_D=200\text{mA}$ $R_G=25\Omega, R_L=150\Omega$			20	ns

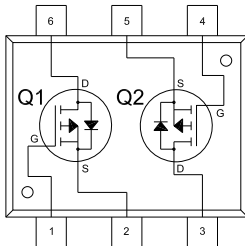
SOT-563 CASE - MECHANICAL OUTLINE



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.0027	0.007	0.07	0.18
B		0.008		0.20
C	0.017	0.024	0.45	0.60
D	0.059	0.067	1.50	1.70
E		0.020		0.50
F	0.059	0.067	1.50	1.70
G	0.043	0.051	1.10	1.30
H	0.006	0.012	0.15	0.30

SOT-563 (REV: R2)

**CMLDM8002A (USA Pinout)
CMLDM8002AG***



LEAD CODE:

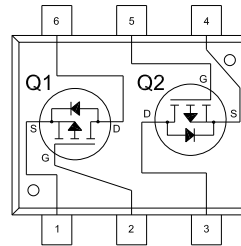
- 1) Gate Q1
- 2) Source Q1
- 3) Drain Q2
- 4) Gate Q2
- 5) Source Q2
- 6) Drain Q1

MARKING CODES:

CMLDM8002A: C08
CMLDM8002AG*: CG8

* Device is *Halogen Free* by design

CMLDM8002AJ (Japanese Pinout)



LEAD CODE:

- 1) Source Q1
- 2) Gate Q1
- 3) Drain Q2
- 4) Source Q2
- 5) Gate Q2
- 6) Drain Q1

MARKING CODE: CJ8

R7 (8-June 2015)

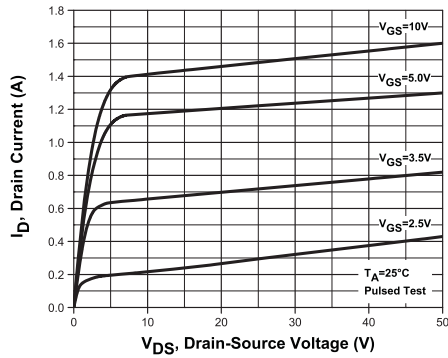
CMLDM8002A
CMLDM8002AG*
CMLDM8002AJ

SURFACE MOUNT SILICON
DUAL P-CHANNEL
ENHANCEMENT-MODE
MOSFETS

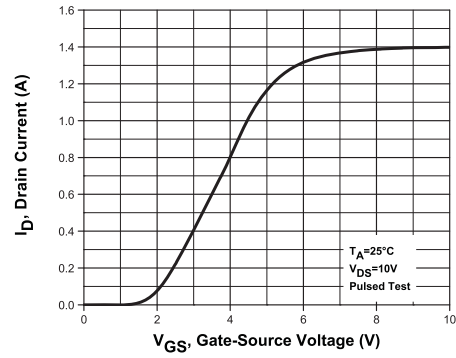


TYPICAL ELECTRICAL CHARACTERISTICS

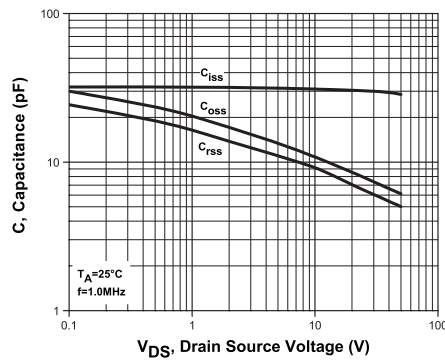
Output Characteristics



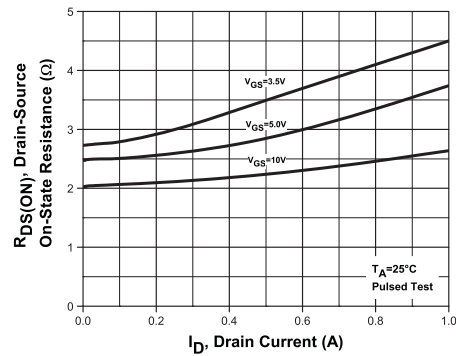
Transfer Characteristics



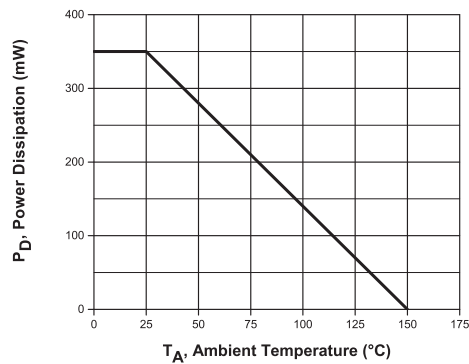
Capacitance



Drain Source On Resistance



Power Derating



R7 (8-June 2015)

CMLDM8002A
CMLDM8002AG*
CMLDM8002AJ

**SURFACE MOUNT SILICON
DUAL P-CHANNEL
ENHANCEMENT-MODE
MOSFETS**



SERVICES

- Bonded Inventory
- Custom Electrical Screening
- Custom Electrical Characteristic Curves
- SPICE Models
- Custom Packaging
- Package Base Options
- Custom Device Development/ Multi Discrete Modules (MDM™)
- Bare Die Available for Hybrid Applications

LIMITATIONS AND DAMAGES DISCLAIMER: In no event shall Central be liable for any collateral, indirect, punitive, incidental, consequential, or exemplary damages in connection with or arising out of a purchase order or contract or the use of products provided hereunder, regardless of whether Central has been advised of the possibility of such damages. Excluded damages shall include, but not be restricted to: cost of removal or reinstallation, rework, ancillary costs to the procurement of substitute products, loss of profits, loss of savings, loss of use, loss of data, or business interruption. No claim, suit, or action shall be brought against Central more than two (2) years after the related cause of action has occurred.

In no event shall Central's aggregate liability from any warranty, indemnity, or other obligation arising out of or in connection with a purchase order or contract, or any use of any Central product provided hereunder, exceed the total amount paid to Central for the specific products sold under a purchase order or contract with respect to which losses or damages are claimed. The existence of more than one (1) claim against the specific products sold to Buyer under a purchase order or contract shall not enlarge or extend this limit.

Buyer understands and agrees that the foregoing liability limitations are essential elements of a purchase order or contract and that in the absence of such limitations, the material and economic terms of the purchase order or contract would be substantially different.

R7 (8-June 2015)

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru

moschip.ru_4

moschip.ru_6

moschip.ru_9