

P-Channel Power MOSFET

-60V, -18A, 68mΩ

FEATURES

- Improved dV/dt capability
- Fast switching
- 100% Eas Guaranteed
- Pb-free plating
- RoHS compliant
- Halogen-free mold compound

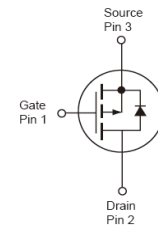
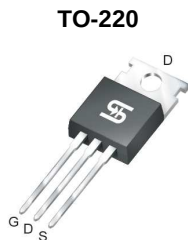
KEY PERFORMANCE PARAMETERS

PARAMETER		VALUE	UNIT
V_{DS}		-60	V
$R_{DS(on)}$ (max)	$V_{GS} = -10V$	68	mΩ
	$V_{GS} = -4.5V$	110	
Q_g		16.4	nC

APPLICATION

- Motor Drive
- Power Tools
- LED Lighting


RoHS
COMPLIANT

HALOGEN
FREE

Notes: Moisture sensitivity level: level 3. Per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	IPAK/DPAK		ITO-220	TO-220	UNIT
Drain-Source Voltage		V _{DS}	-60				V
Gate-Source Voltage		V _{GS}	±20				V
Continuous Drain Current ^(Note 1)	T _C = 25°C	I _D	-18				A
	T _C = 100°C		-11				
Pulsed Drain Current ^(Note 2)		I _{DM}	-72				A
Total Power Dissipation @ T _C = 25°C		P _{DTOT}	20	17	42	W	
Single Pulsed Avalanche Energy ^(Note 3)		E _{AS}	12.8				mJ
Single Pulsed Avalanche Current ^(Note 3)		I _{AS}	-16				A
Operating Junction and Storage Temperature Range		T _J , T _{STG}	- 55 to +150				°C

THERMAL PERFORMANCE

PARAMETER	SYMBOL	IPAK/DPAK	ITO-220	TO-220	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	6.1	7.5	3	$^\circ\text{C/W}$
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	62			$^\circ\text{C/W}$

Notes: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB in still air.

ELECTRICAL SPECIFICATIONS (T _C = 25°C unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static (Note 4)						
Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = -250μA	BV _{DSS}	-60	--	--	V
Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250μA	V _{GS(TH)}	-1.2	-1.6	-2.2	V
Gate Body Leakage	V _{GS} = ±20V, V _{DS} = 0V	I _{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V _{DS} = -60V, V _{GS} = 0V	I _{DSS}	--	--	-1	μA
	V _{DS} = -48V, T _C = 125°C		--	--	-10	
Drain-Source On-State Resistance	V _{GS} = -10V, I _D = -6A	R _{DS(on)}	--	54	68	mΩ
	V _{GS} = -4.5V, I _D = -3A		--	72	110	
Forward Transconductance	V _{DS} = -10V, I _D = -6A	g _{fs}	--	8.5	--	S
Dynamic (Note 5)						
Total Gate Charge	V _{DS} = -30V, I _D = -6A, V _{GS} = -10V	Q _g	--	16.4	--	nC
Gate-Source Charge		Q _{gs}	--	2.8	--	
Gate-Drain Charge		Q _{gd}	--	3.6	--	
Input Capacitance	V _{DS} = -30V, V _{GS} = 0V, f = 1.0MHz	C _{iss}	--	870	--	pF
Output Capacitance		C _{oss}	--	70	--	
Reverse Transfer Capacitance		C _{rss}	--	42	--	
Gate Resistance	F = 1MHz, open drain	R _g	--	16	--	Ω
Switching (Note 6)						
Turn-On Delay Time	V _{DD} = -30V, R _{GEN} = 6Ω, I _D = -1A	t _{d(on)}	--	8.3	--	ns
Turn-On Rise Time		t _r	--	29.6	--	
Turn-Off Delay Time		t _{d(off)}	--	51.7	--	
Turn-Off Fall Time		t _f	--	15.6	--	
Source-Drain Diode (Note 3)						
Forward On Voltage	I _S = -1A, V _{GS} = 0V	V _{SD}	--	--	-1	V
Reverse Recovery Time	I _S = 1A di _F /dt = 100A/μs	t _{rr}	--	20	--	ns
Reverse Recovery Charge		Q _{rr}	--	10	--	nC
Maximum Continuous Forward Current	Integral reverse diode in the MOSFET	I _S	--	--	-13	A
Maximum Pulse Forward Current		I _{SM}	--	--	-52	A

Notes:

- Current limited by package
- Pulse width limited by the maximum junction temperature
- $L = 0.1\text{mH}, I_{AS} = -16A, V_{DD} = -25V, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
- Pulse test: $PW \leq 300\mu s$, duty cycle $\leq 2\%$
- For DESIGN AID ONLY, not subject to production testing.
- Switching time is essentially independent of operating temperature.

ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM680P06CZ C0G	TO-220	50pcs / Tube
TSM680P06CI C0G	ITO-220	50pcs / Tube
TSM680P06CH C5G	TO-251S (IPAK SL)	75pcs / Tube
TSM680P06CP ROG	TO-252 (DPAK)	2,500pcs / 13" Reel

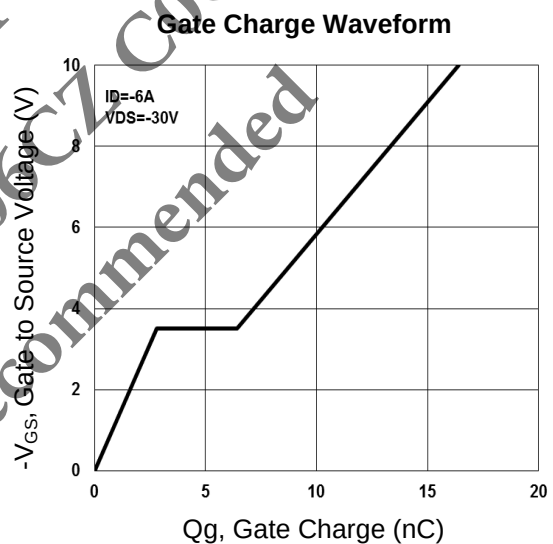
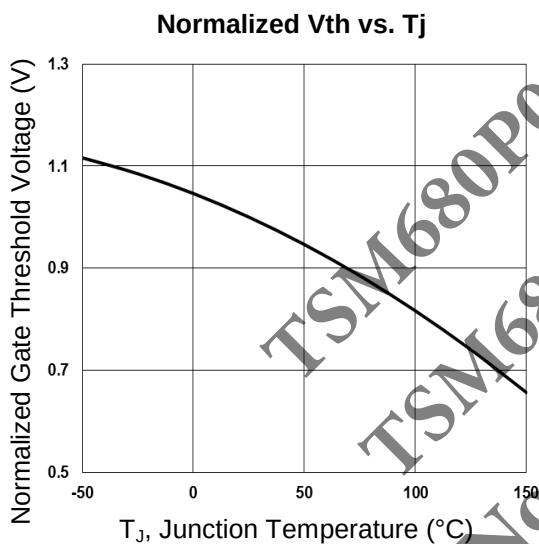
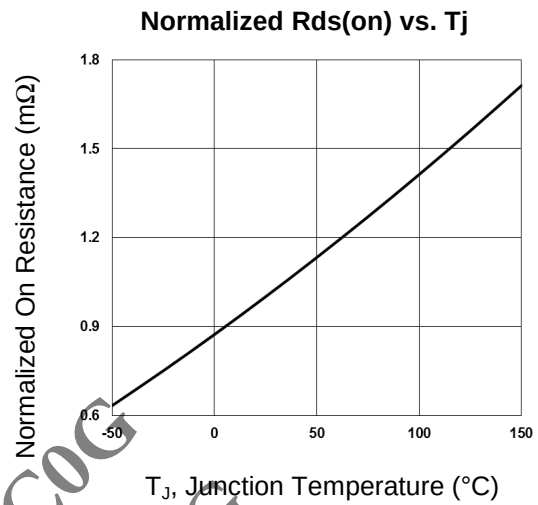
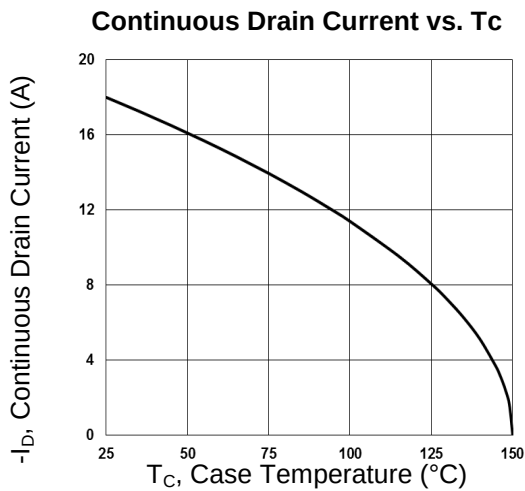
Note:

1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
2. Halogen-free according to IEC 61249-2-21 definition

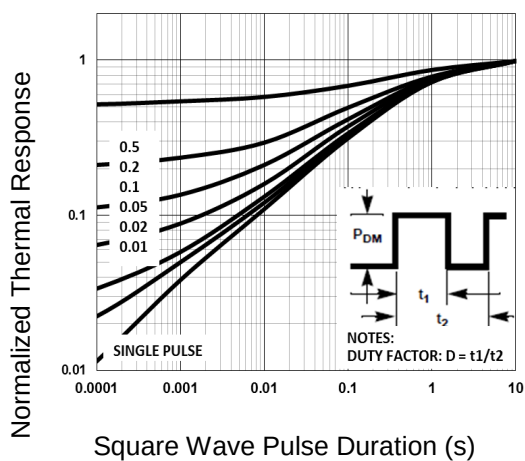
TSM680P06CI C0G
TSM680P06CZ C0G
Not Recommended

CHARACTERISTICS CURVES

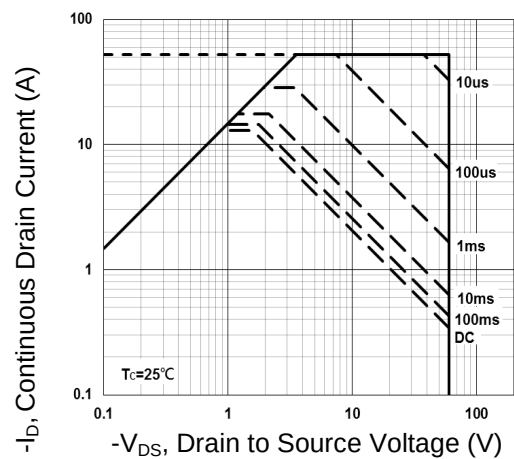
($T_C = 25^\circ\text{C}$ unless otherwise noted)



Normalized Transient Impedance (TO-251S)



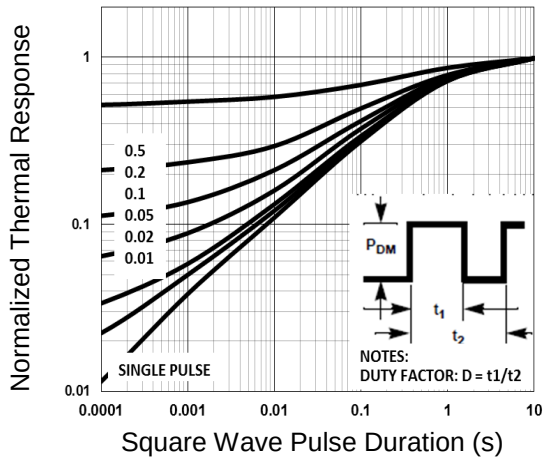
Maximum Safe Operation Area (TO-251S)



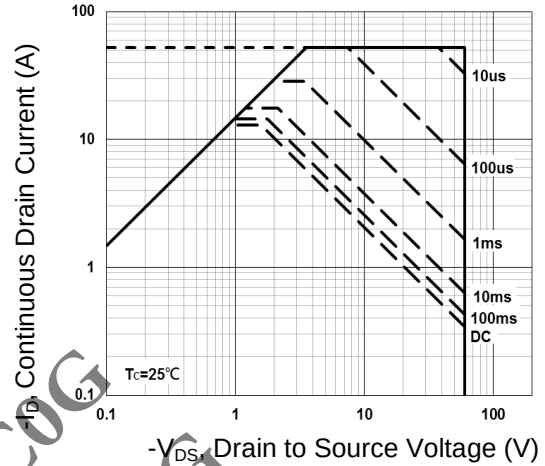
CHARACTERISTICS CURVES

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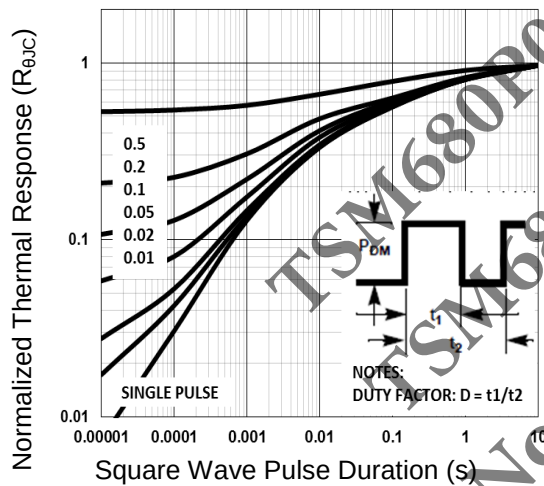
Normalized Transient Impedance (TO-252)



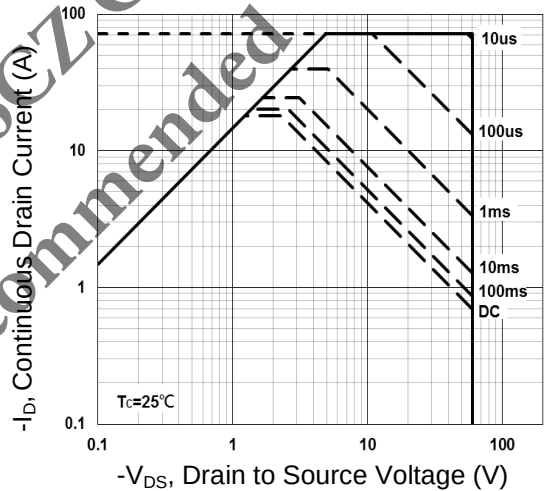
Maximum Safe Operation Area (TO-252)



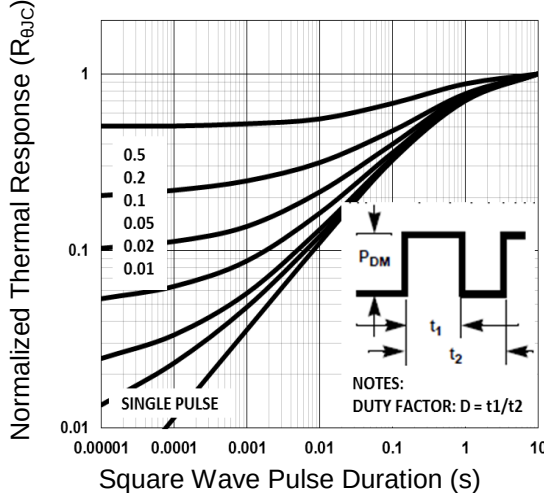
Normalized Transient Impedance (TO-220)



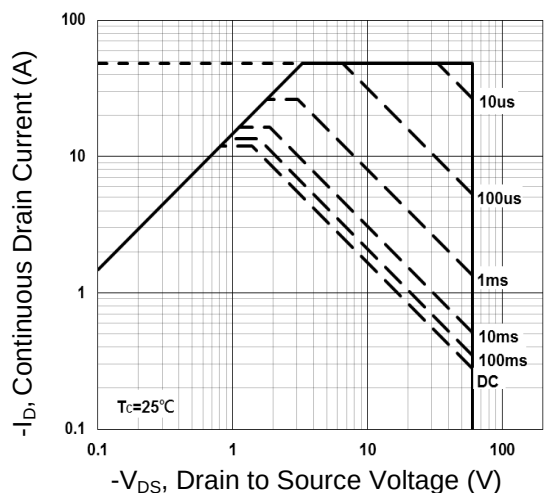
Maximum Safe Operation Area (TO-220)



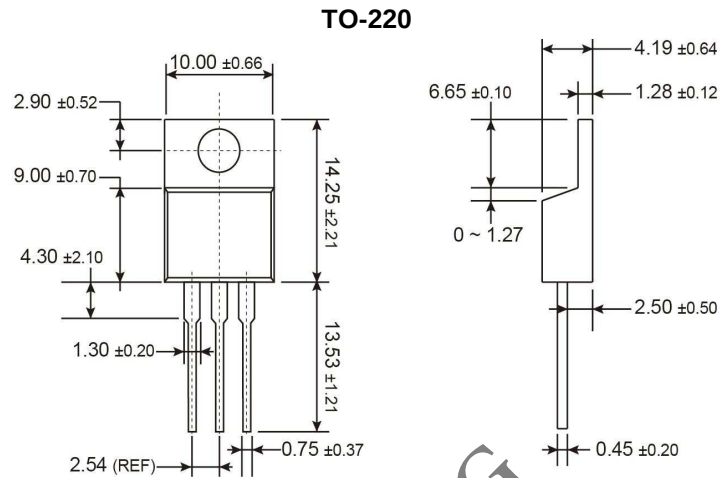
Normalized Transient Impedance (ITO-220)



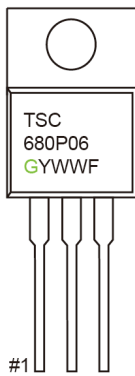
Maximum Safe Operation Area (ITO-220)



PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



MARKING DIAGRAM



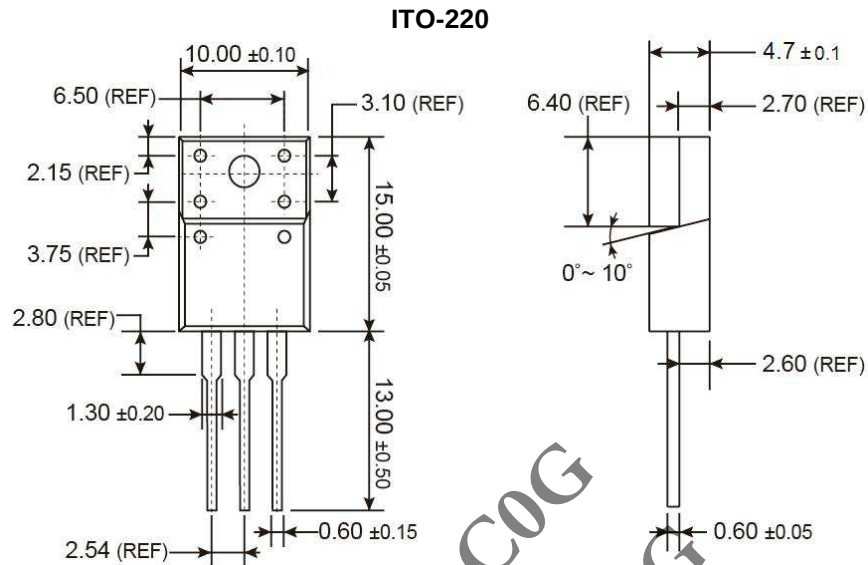
- G** = Halogen Free
- Y** = Year Code
- WW** = Week Code (01~52)
- F** = Factory Code

TSM680P06C1 C0G

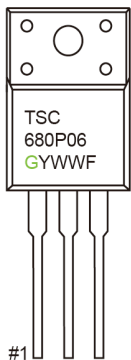
TSM680P06CZ C0G

Not Recommended

PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

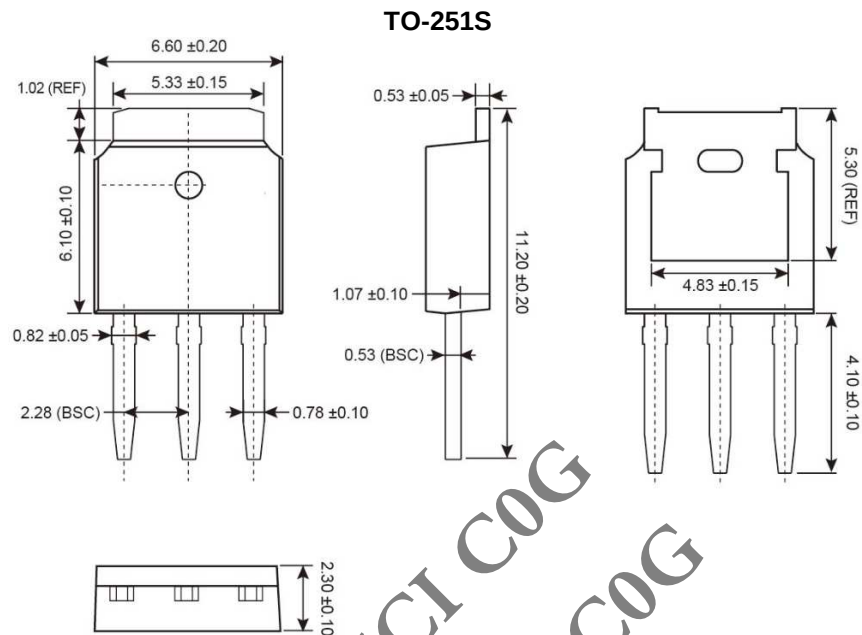


MARKING DIAGRAM

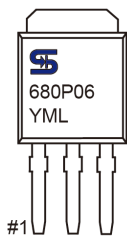


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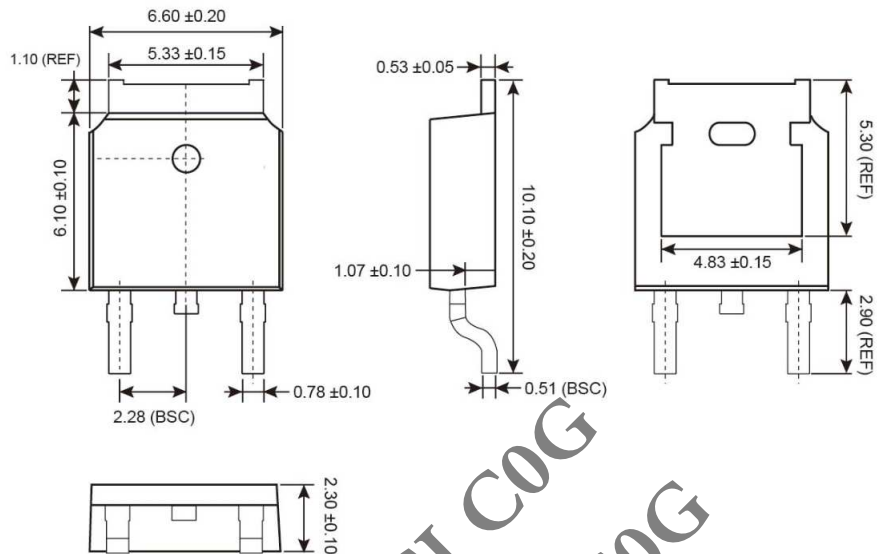
MARKING DIAGRAM



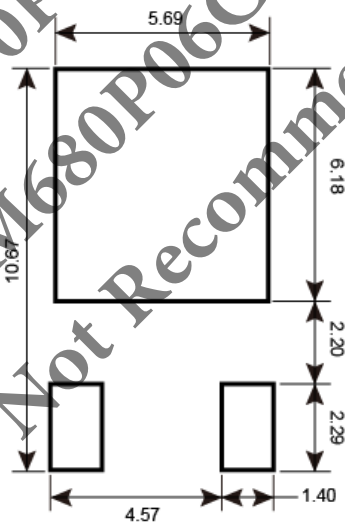
Y = Year Code
M = Month Code for Halogen Free Product
O =Jan **P** =Feb **Q** =Mar **R** =Apr
S =May **T** =Jun **U** =Jul **V** =Aug
W =Sep **X** =Oct **Y** =Nov **Z** =Dec
L = Lot Code (1~9, A~Z)

PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

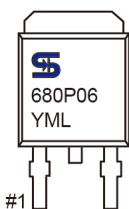
TO-252



SUGGESTED PAD LAYOUT



MARKING DIAGRAM



Y = Year Code
M = Month Code for Halogen Free Product

O =Jan	P =Feb	Q =Mar	R =Apr
S =May	T =Jun	U =Jul	V =Aug
W =Sep	X =Oct	Y =Nov	Z =Dec

L = Lot Code (1~9, A~Z)

TSM680P06CI C0G
TSM680P06CZ C0G
Not Recommended

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