Is Now Part of

ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD SEMICONDUCTOR®

June 2013

FAN3180
Single 2-A Low-Side Driver with 3.3-V LDO

Features

LDO

- 3.3-V, 15-mA Output
- ±1% at 25°C, ±2.5% Total Variation

Gate Driver

- Peak 2.8-A Sink / 2.5-A Source at V_{DD} = 12 V
- Controlled Output Pulses at Startup and Shutdown
- Non-Inverting Logic Configuration
- TTL-Compatible Input Thresholds
- 23-ns Typical Delay Time
- 19-ns / 13-ns Rise and Fall Times with 1-nF Load

General

- -40°C to +125°C Operation Temperature
- 5-V to 18-V Operating Range
- V_{ON} / V_{OFF} UVLO of 4.75 V / 4.55 V
- 200-µA Maximum Standby Supply Current
- Lead (Pb)-Free Green 5-Pin SOT23 Package

Applications

- Gate Drive with Power for the MCU
- Switched-Mode Power Supplies, Consumer Electronics, Portable Hand Tools

Description

The FAN3180 combines a high-speed low-side gate driver with a 3.3-V output Low Drop Out (LDO) regulator. The gate driver is rated to 2.8-A peak current at V_{DD} of 12 V and is designed to drive an N-channel enhancement-mode MOSFET in low-side switching applications. The FAN3180 also integrates a 3.3-V, 15-mA LDO with tight voltage tolerance of ±1% at 25°C and ±2.5% of total variation for powering external microcontrollers.

Internal circuitry provides an Under-Voltage Lockout (UVLO) function by holding the output low until the supply voltage is within the operating range and the first full input pulse is detected. The FAN3180 has UVLO thresholds of 4.75-V V_{ON} and 4.55-V V_{OFF} and a maximum standby supply current of 200 µA.

The driver delivers fast MOSFET switching performance to maximize efficiency in high-frequency power converter designs. It incorporates the MillerDrive™ architecture for the final output driver stage. This bipolar-MOSFET combination provides high peak current during the Miller plateau stage of the MOSFET turn-on / turn-off process to minimize switching loss, while providing rail-to-rail voltage swing and reverse-current capability. Thermal shutdown function is included as an additional safety feature.

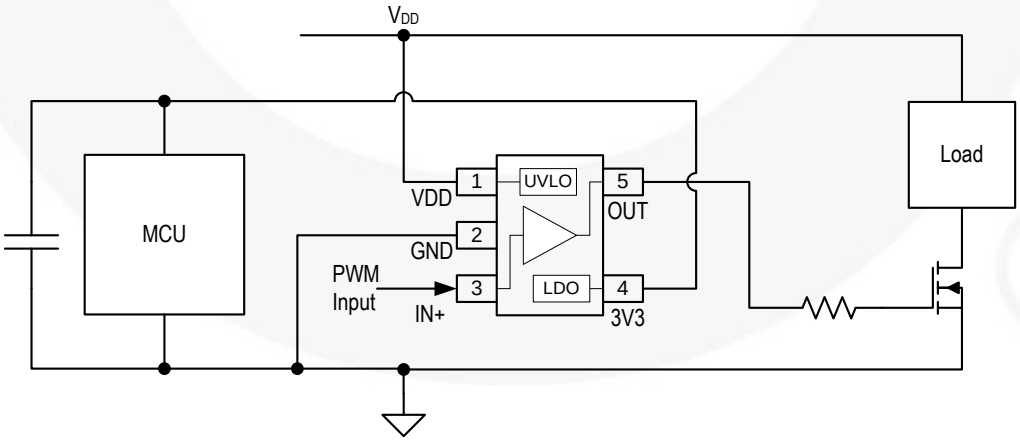

Figure 1. Typical Application

Ordering Information

Part Number	Input Threshold	UVLO (V_{ON} / V_{OFF})	Package	Packing Method	Reel Quantity
FAN3180TSX	TTL	4.75 V / 4.55 V	5-Pin SOT23	Tape & Reel	3000

Functional Pin Configuration

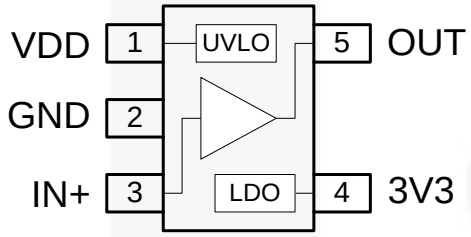

Figure 2. Top View

Thermal Characteristics[1]

Package	Θ_{JL}[2]	Θ_{JT}[3]	Θ_{JA}[4]	Ψ_{JB}[5]	Ψ_{JT}[6]	Units
5-Pin SOT23	58	102	161	53	6	°C/W

Notes:

1. Estimates derived from thermal simulation; actual values depend on the application.
2. Theta_JL (Θ_{JL}): Thermal resistance between the semiconductor junction and the bottom surface of all the leads (including any thermal pad) that are typically soldered to a PCB.
3. Theta_JT (Θ_{JT}): Thermal resistance between the semiconductor junction and the top surface of the package, assuming it is held at a uniform temperature by a top-side heat sink.
4. Theta_JA (Θ_{JA}): Thermal resistance between junction and ambient, dependent on the PCB design, heat sinking, and airflow. The value given is for natural convection with no heat sink using a 2S2P board, as specified in JEDEC standards JESD51-2, JESD51-5, and JESD51-7, as appropriate.
5. Psi_JB (Ψ_{JB}): Thermal characterization parameter providing correlation between semiconductor junction temperature and an application circuit board reference point for the thermal environment defined in Note 4. For the SOT23-5 package, the board reference is defined as the PCB copper adjacent to pin 2.
6. Psi_JT (Ψ_{JT}): Thermal characterization parameter providing correlation between the semiconductor junction temperature and the center of the top of the package for the thermal environment defined in Note 4.

Pin Definitions

Pin #	Name	Description
1	VDD	**Supply Voltage**. Provides power to the IC.
2	GND	**Ground**. Common ground reference for input and output circuits.
3	IN+	**Non-Inverting Input**. Connect to VDD to enable output.
4	3V3	**3.3-V LDO Output** with 15 mA output capability.
5	OUT	**Gate Drive Output**. Held LOW unless required input is present and V_{DD} is above UVLO threshold.

Output Logic

IN+	OUT
0[7]	0
1	1

Note:
7. Default input signal if no external connection is made.

Block Diagram

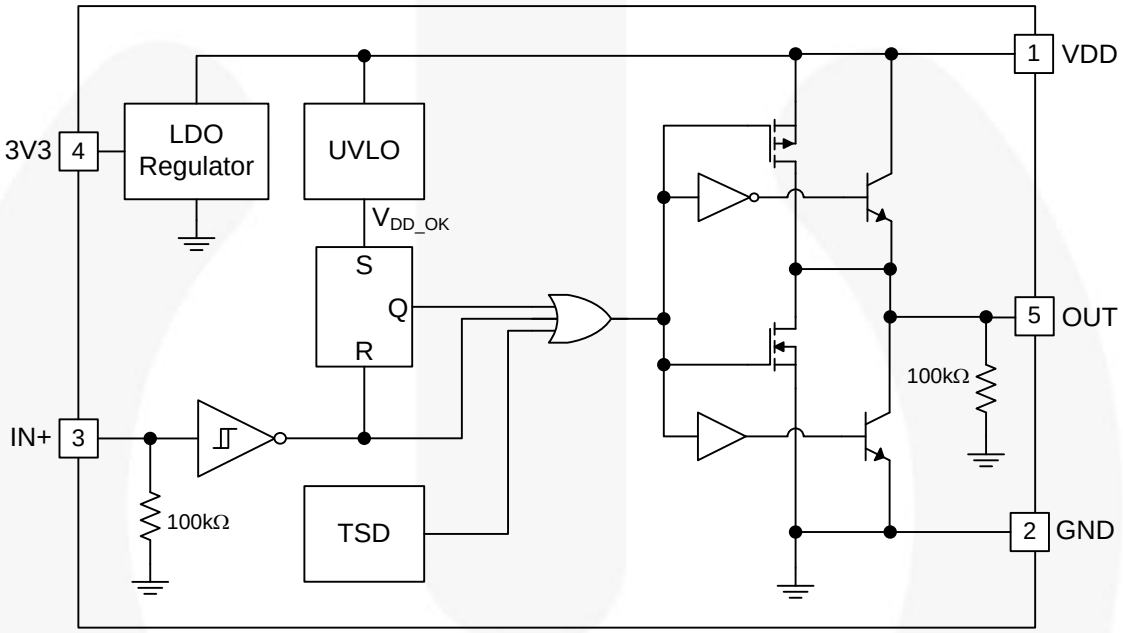

Figure 3. Simplified Block Diagram

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	VDD to GND	-0.3	20.0	V
V_{IN}	Voltage on IN+ to GND	-0.3	V_{DD} + 0.3	V
V_{OUT}	Voltage on OUT to GND	-0.3	V_{DD} + 0.3	V
V_{3V3}	3.3-V Output Voltage Pin to GND		6.0	V
T_L	Lead Soldering Temperature (10 Seconds)		+260	ºC
T_J	Junction Temperature		+125	ºC
T_{STG}	Storage Temperature	-65	+150	ºC

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply Voltage Range	4.5	18.0	V
V_{IN}	Input Voltage IN+	0	V_{DD}	V
C_{BYP}	Supply Bypass Capacitor	1.0		µF
T_A	Operating Ambient Temperature	-40	+125	ºC

Electrical Characteristics

Unless otherwise noted, V_{DD} = 12 V, T_J = -40°C to +125°C. Currents are defined as positive into the device and negative out of the device.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply						
V_{DD}	Operating Range		5		18	V
I_{DD_STATIC}	Static Supply Current	Inputs Not Connected; 3V3 Not Loaded			200	µA
I_{DD_OPER}	Operating Supply Current[8]	f_{SW}=100 kHz, No Load		0.6		mA
		f_{SW}=1 MHz, No Load		3.8		
		f_{SW}=100 kHz, 1 nF Load		1.5		
		f_{SW}=1 MHz, 1 nF Load		12.5		
V_{ON}	Turn-On Voltage	V_{DD} Increasing	4.50	4.75	5.00	V
V_{OFF}	Turn-Off Voltage	V_{DD} Decreasing	4.30	4.55	4.80	V
V_{HYS_VDD}	Supply Voltage Hysteresis		150	200	250	mV
Input						
V_{IL_T}	IN+, Low-Voltage Threshold, Maximum				0.8	V
V_{IH_T}	IN+, High-Voltage Threshold, Minimum		2			V
V_{HYS_IN}	Input Hysteresis Voltage		0.2	0.5	0.8	V
I_{INL}	IN+ Current, LOW	IN from 0 to V_{DD}	-1.00	0.05	1.00	µA
I_{INH}	IN+ Current, HIGH	IN from 0 to V_{DD}	-50	-30	1	µA
3V3 LDO						
V_{LDO}	LDO Output Voltage	T_A=25°C	3.267	3.300	3.333	V
		Total Variation	3.217		3.382	
$V_{LDO\_LineReg}$	LDO Line Regulation	V_{DD}=5 to 13 V, I_{OUT}=10 mA		1	10	mV
$V_{LDO\_LoadReg}$	LDO Load Regulation	V_{DD}=5 to 13 V, I_{OUT}=0.1 mA to 10 mA		5	20	mV
I_{LDO_MAX}	Maximum LDO Current			15		mA
$I_{LDO\_I\text{-}LIM}$	LDO Current Limit		10	35		mA
Thermal Shutdown						
TSD_{ON}	Thermal Shutdown Activation[8]			150		°C
TSD_{OFF}	Thermal Shutdown Deactivation[8]			125		°C

Continued on the following page…

Electrical Characteristics

Unless otherwise noted, V_{DD} = 12 V, T_J = -40°C to +125°C. Currents are defined as positive into the device and negative out of the device.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Output						
I_{SINK}	OUT Current, Mid-Voltage, Sinking[8]	OUT at V_{DD}/2, C_{LOAD}=0.1 µF, f=1 kHz		2.5		A
I_{SOURCE}	OUT Current, Mid-Voltage, Sourcing[8]	OUT at V_{DD}/2, C_{LOAD} =0.1 µF, f=1 kHz		-1.8		A
I_{PK_SINK}	OUT Current, Peak, Sinking[8]	C_{LOAD}=0.1 µF, f=1 kHz		2.8		A
I_{PK_SOURCE}	OUT Current, Peak, Sourcing[8]	C_{LOAD}=0.1 µF, f=1 kHz		-2.5		A
t_{RISE}	Output Rise Time[9]	C_{LOAD}=1000 pF		19	30	ns
t_{FALL}	Output Fall Time[9]	C_{LOAD}=1000 pF		13	25	ns
t_{D1}	Output Prop. Delay, Input Rising[9]	0 - 3.3 V_{IN}, 1 V/ns Slew Rate	12	23	36	ns
t_{D2}	Output Prop. Delay, Input Falling[9]	0 - 3.3 V_{IN}, 1 V/ns Slew Rate	13	24	35	ns
I_{RVS}	Output Reverse Current Withstand[8]			250		mA

Notes:
8. Not tested in production.
9. *See Figure 4.*

Timing Diagrams

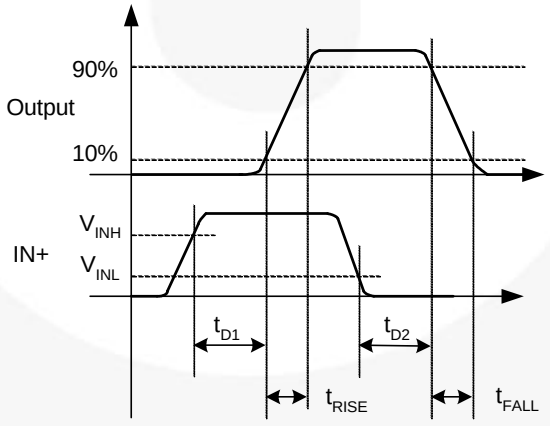

Figure 4. Non-Inverting Waveforms

Typical Performance Characteristics

Typical characteristics are provided at 25°C and V_{DD}=12 V unless otherwise noted.

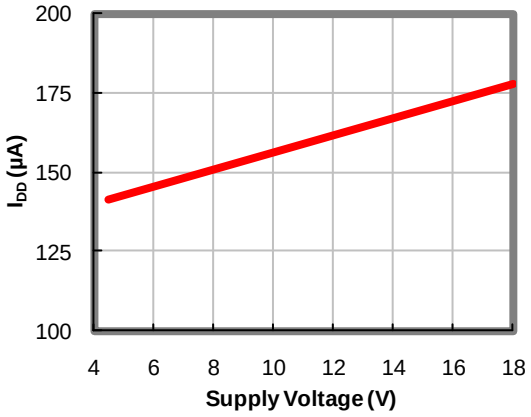

Figure 5. I_{DD} (Static) vs. Supply Voltage

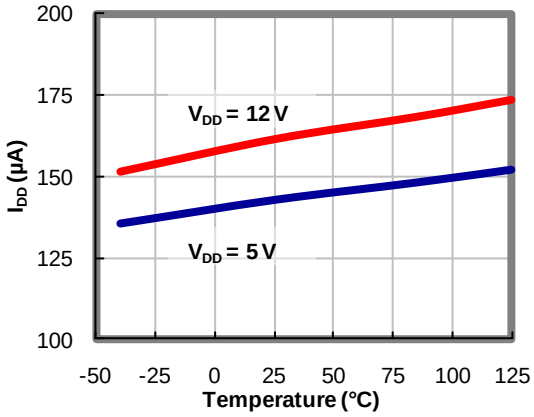

Figure 6. I_{DD} (Static) vs. Temperature

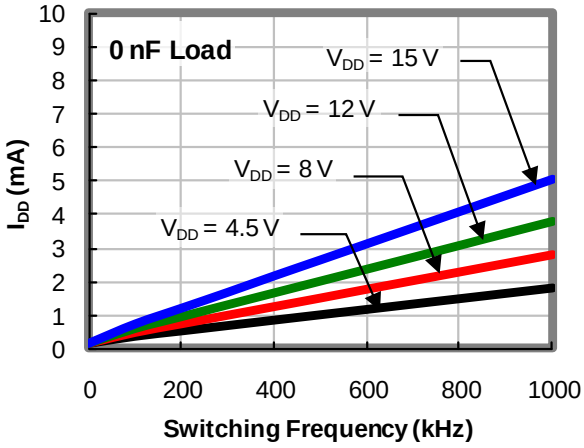

Figure 7. I_{DD} (No-Load) vs. Frequency

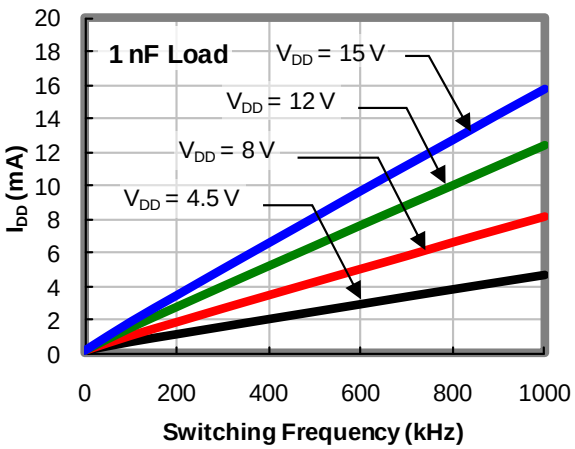

Figure 8. I_{DD} (1 nF Load) vs. Frequency

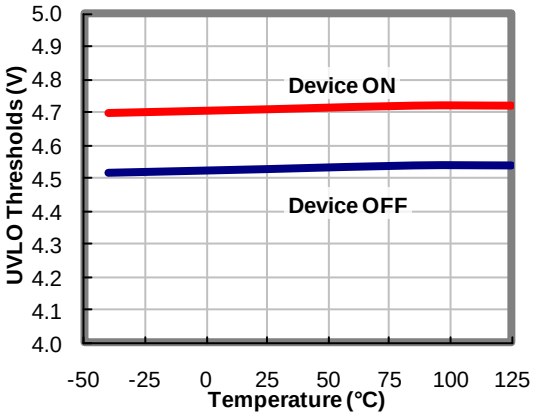

Figure 9. UVLO Thresholds vs. Temperature

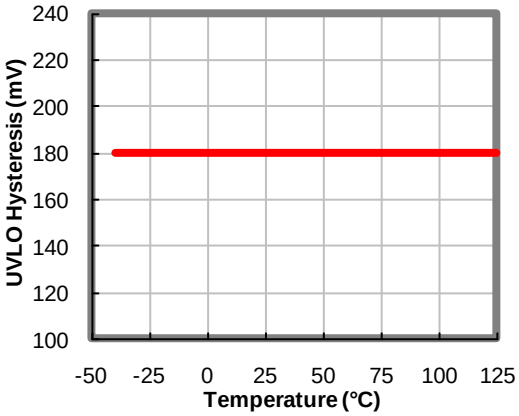

Figure 10. UVLO Hysteresis vs. Temperature

Typical Performance Characteristics

Typical characteristics are provided at 25°C and V_{DD}=12 V unless otherwise noted.

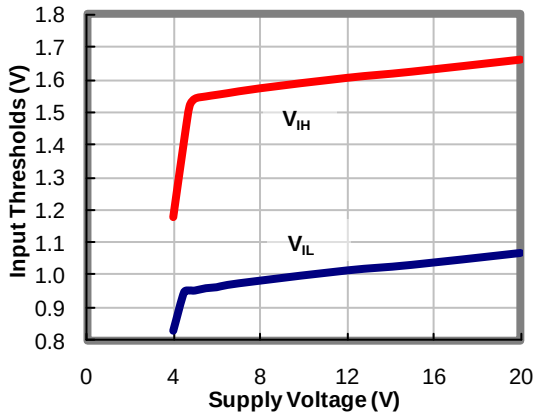

Figure 11. Input Thresholds vs. Supply Voltage

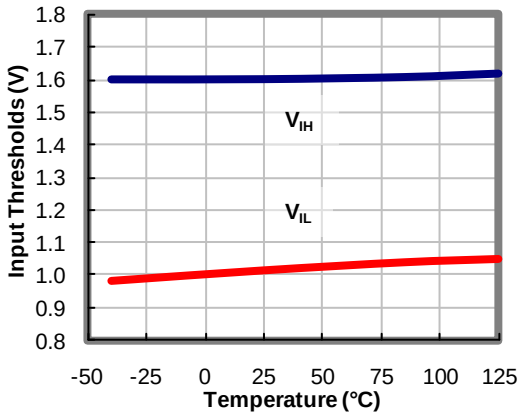

Figure 12. TTL Input Thresholds vs. Temperature

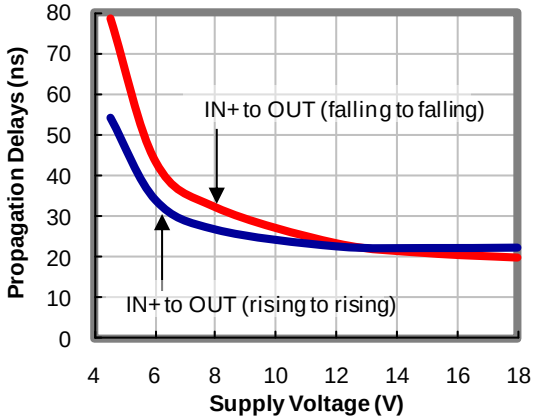

Figure 13. Propagation Delay vs. Supply Voltage

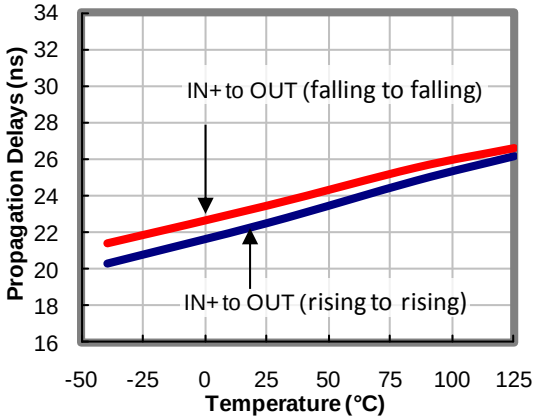

Figure 14. Propagation Delay vs. Temperature

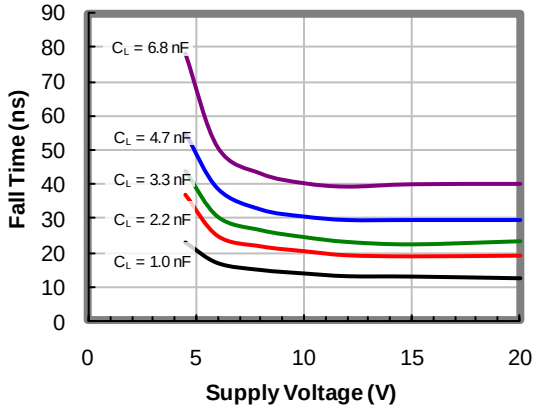

Figure 15. Fall Time vs. Supply Voltage

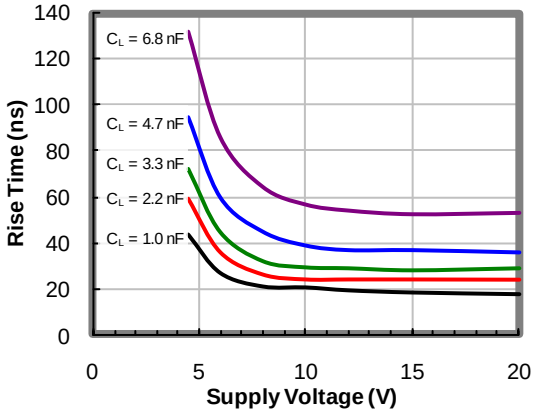

Figure 16. Rise Time vs. Supply Voltage

Typical Performance Characteristics

Typical characteristics are provided at 25°C and V_{DD}=12 V unless otherwise noted.

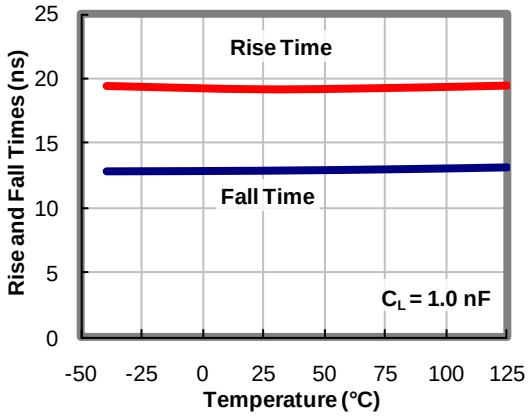

Figure 17. Rise and Fall Time vs. Temperature

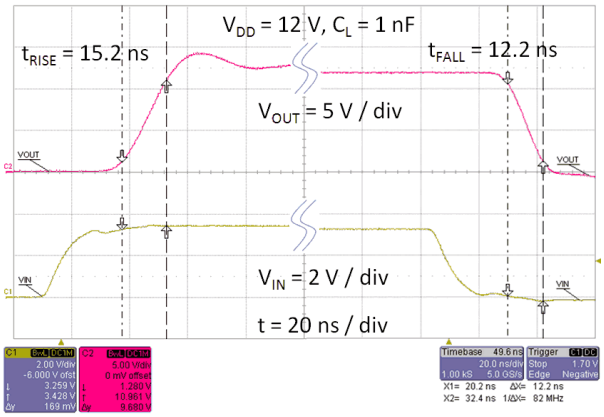

Figure 18. Rise / Fall Waveforms with 1 nF Load

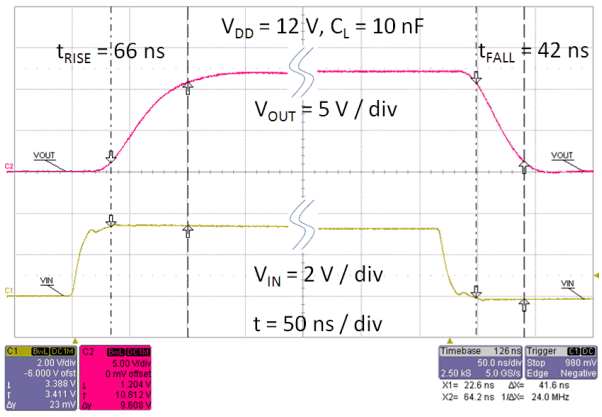

Figure 19. Rise / Fall Waveforms with 10 nF Load

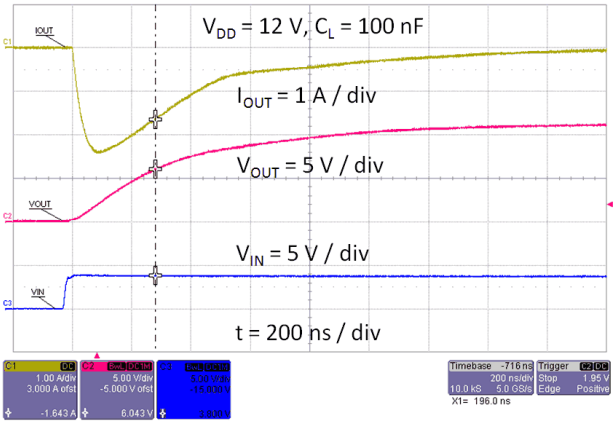

Figure 20. Quasi-Static Source Current with V_{DD}=12 V

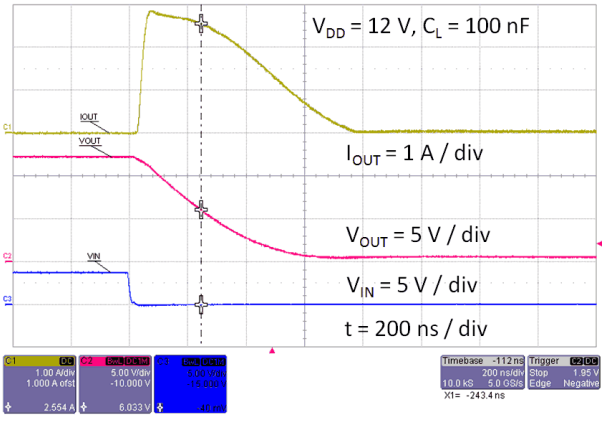

Figure 21. Quasi-Static Sink Current with V_{DD}=12 V

Typical Performance Characteristics

Typical characteristics are provided at 25°C and V_{DD}=12 V unless otherwise noted.

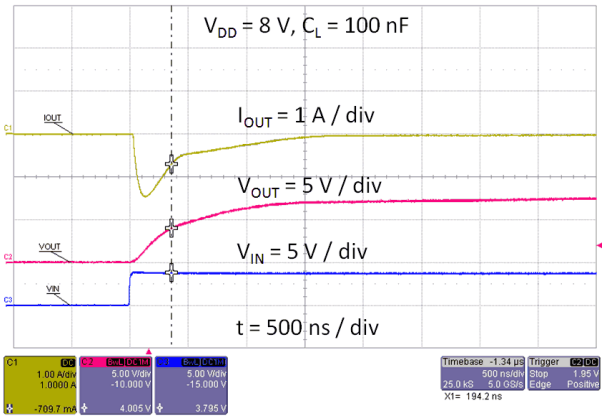

Figure 22. Quasi-Static Source Current with V_{DD}=8 V

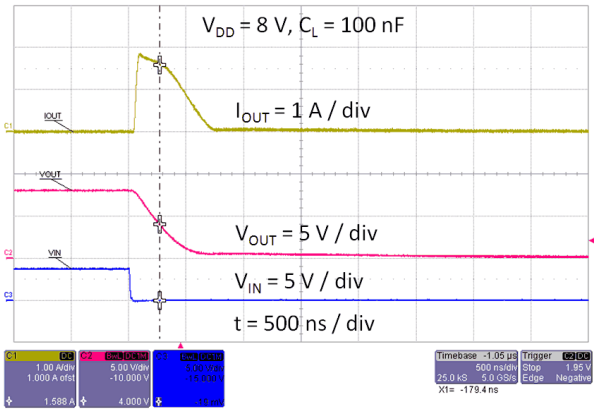

Figure 23. Quasi-Static Sink Current with V_{DD}=8 V

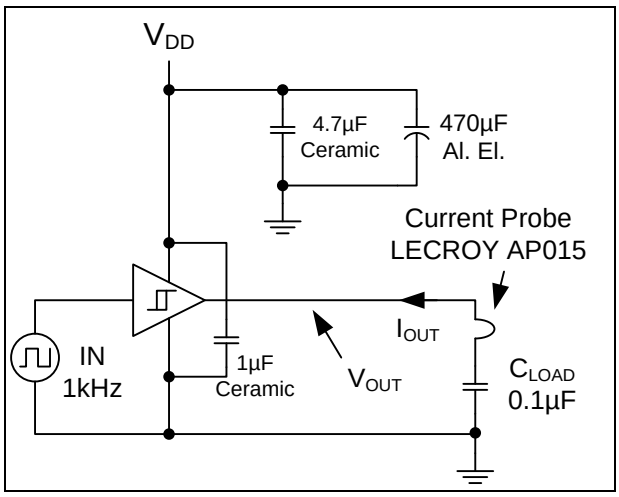

Figure 24. Quasi-Static I_{OUT} / V_{OUT} Test Circuit

Application Information

Input Stage

The FAN3180 input thresholds between 2 V and 5 V meet industry-standard TTL-logic thresholds, independent of the V_{DD} voltage. The input rising-edge threshold is approximately 50% of 3.3 V and the input falling-edge threshold is approximately 30% of 3.3 V. The TTL-like input configuration offers a hysteresis voltage of approximately 0.7 V. These levels permit the inputs to be driven from a range of input logic signal levels for which a voltage over 2 V is considered logic HIGH. The driving signal for the TTL inputs should have fast rising and falling edges with a slew rate of 6 V/µs or faster, so the rise time from 0 to 3.3 V should be 550 ns or less. With reduced slew rate, circuit noise could cause the driver input voltage to exceed the hysteresis voltage and retrigger the driver input, causing erratic operation.

MillerDrive™ Gate Drive Technology

The FAN3180 incorporates the MillerDrive™ architecture shown in Figure 25 for the output stage, a combination of bipolar and MOSFET devices capable of providing large currents over a wide range of supply-voltage and temperature variations. The bipolar devices carry the bulk of the current as OUT swings between 1/3 to 2/3 V_{DD} and the MOSFET devices pull the output to the high or low rail.

The purpose of the MillerDrive™ architecture is to speed up switching by providing the highest current during the Miller plateau region when the gate-drain capacitance of the MOSFET is being charged or discharged as part of the turn-on / turn-off process. For applications with Zero-Voltage Switching (ZVS) during the MOSFET turn-on or turn-off interval, the driver supplies high peak current for fast switching even though the Miller plateau is not present. This situation often occurs in synchronous rectifier applications because the body diode is generally conducting before the MOSFET is switched on.

The output-pin slew rate is determined by V_{DD} voltage and the load on the output. It is not adjustable, but if a slower rise or fall time at the MOSFET gate is needed, a series resistor can be added.

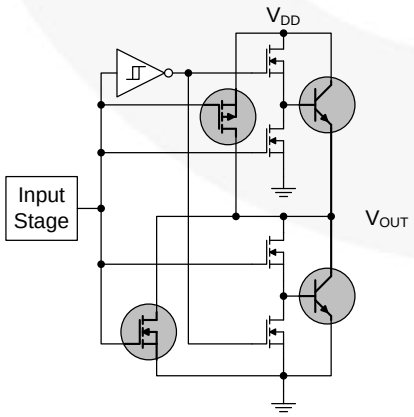

Figure 25. MillerDrive™ Output Architecture

Under-Voltage Lockout

The FAN3180 startup logic is optimized to drive ground referenced N-channel MOSFETs with an under-voltage lockout (UVLO) function to ensure the IC starts up in an orderly fashion. When V_{DD} is rising, yet below the 4.5 V operational level, this circuit holds the output LOW, regardless of the status of the input pins. After the part is active, the supply voltage must drop 0.2 V before the part shuts down. This hysteresis helps prevent chatter when low V_{DD} supply voltages have noise from the power switching. This configuration is not suitable for driving high-side P-channel MOSFETs because the low output voltage of the driver would turn the P-channel MOSFET on with V_{DD} below 4.5 V.

V_{DD} Bypass Capacitor Guidelines

To enable this IC to turn a power device on quickly, a local, high-frequency, bypass capacitor, C_{BYP}, with low ESR and ESL should be connected between the VDD and GND pins with minimal trace length. This capacitor is in addition to bulk electrolytic capacitance of 10µF to 47 µF often found on driver and controller bias circuits.

A typical criterion for choosing the value of C_{BYP} is to keep the ripple voltage on the V_{DD} supply ≤5%. Often this is achieved with a value ≥ 20 times the equivalent load capacitance C_{EQV}, defined here as Q_{gate}/V_{DD}. Ceramic capacitors of 0.1 µF to 1 µF or larger are common choices, as are dielectrics such as X5R and X7R, which have good temperature characteristics and high pulse current capability.

If circuit noise affects normal operation, the value of C_{BYP} may be increased to 50-100 times C_{EQV} or C_{BYP} may be split into two capacitors. One should be a larger value, based on equivalent load capacitance, and the other a smaller value, such as 1-10 nF, mounted closest to the VDD and GND pins to carry the higher-frequency components of the current pulses.

3V3 Internal Regulator

For microcontroller or ASIC applications requiring a low-power 3.3-V bias, FAN3180 includes an internal 3.3-V regulator. The regulator is rated to source up to 15 mA with a typical current limit of 35 mA, shown in Figure 26.

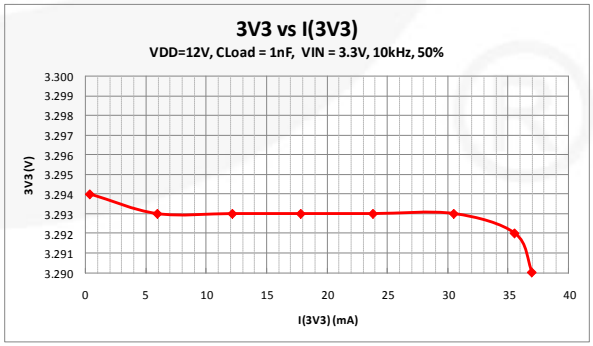

Figure 26. 3V3 Regulation vs. $I_{(3V3)}$

During normal operation, a 0.1 µF ceramic capacitor should be connected between 3V3 and GND.

During startup, 3V3 is internally monitored by a signal that prevents the output from switching until 80 µs after 3V3 is within regulation. Therefore, if V_{DD} is applied quickly and there is a valid V_{IN} signal, there are no output pulses until 80 µs after 3V3 is in full regulation, even though V_{DD}>$UVLO_{ON}$.

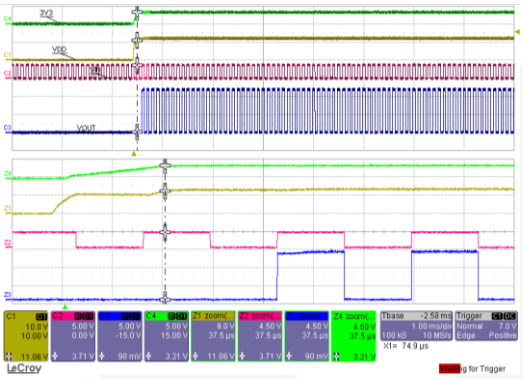

Figure 27. V_{DD}>$UVLO_{ON}$ Before 3V3

Conversely, if V_{DD} is applied slowly ($UVLO_{ON}$ occurs after 80 µs 3V3 startup) and there is a valid V_{IN} signal, there are no output pulses until V_{DD} reaches $UVLO_{ON}$, even though 3V3 is in full regulation.

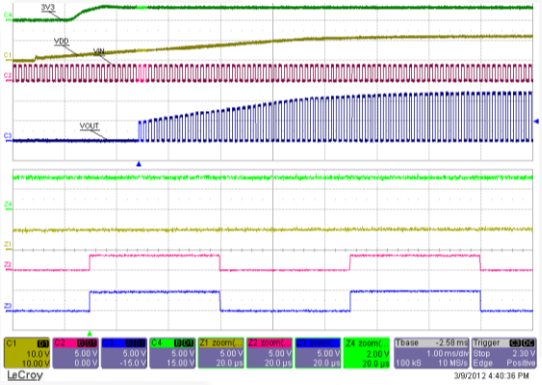

Figure 28. 3V3 Before V_{DD}>$UVLO_{ON}$

Two conditions are required for valid output switching:

1. V_{DD}>$UVLO_{ON}$,
2. 3V3 in regulation.

Startup Logic

When V_{DD}>$UVLO_{ON}$ and 3V3 is in regulation, output switching begins following the first valid rising edge of the V_{IN} signal.

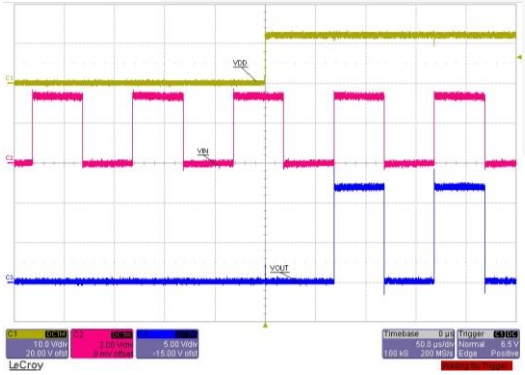

Figure 29. V_{DD} Applied when V_{IN} HIGH

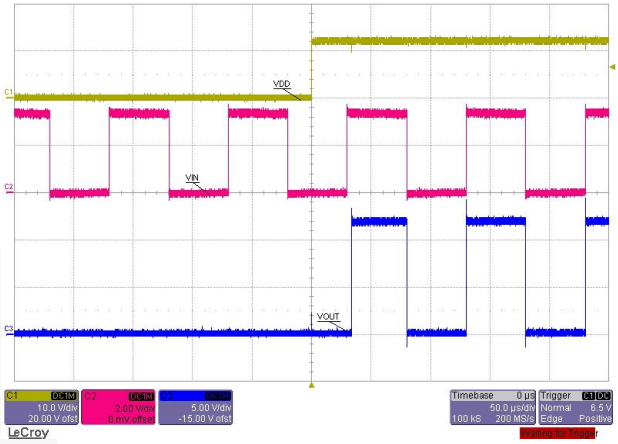

Figure 30. V_{DD} Applied when V_{IN} LOW

Holding off the output until the first valid rising edge prevents an incomplete pulse from appearing on the output, as shown in Figure 29.

Shutdown

When V_{DD} is removed and falls below $UVLO_{OFF}$, the output immediately terminates switching regardless of the V_{IN} signals.

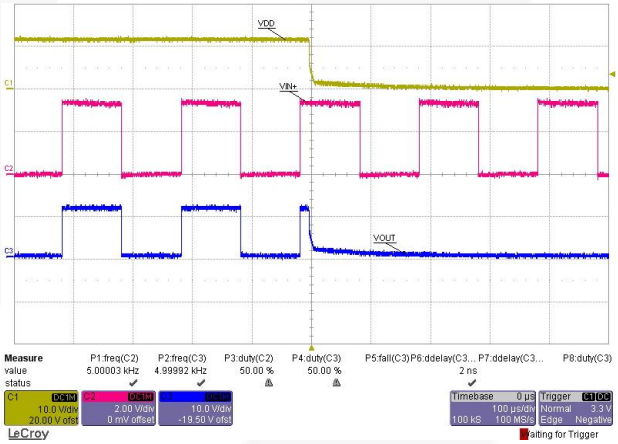

Figure 31. Turn-Off During V_{IN} HIGH

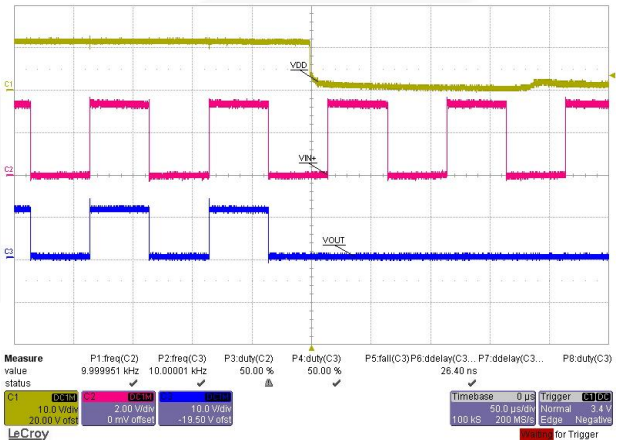

Figure 32. Turn-Off During V_{IN} LOW

Layout and Connection Guidelines

The FAN3180 incorporates fast reacting input circuits, short propagation delays, and output stages capable of delivering current peaks over 1 A to facilitate voltage transition times from under 10 ns to over 100 ns. The following guidelines are strongly recommended:

- Keep high-current output and power ground paths separate from logic input signals and signal ground paths. This is especially critical when dealing with TTL-level logic thresholds.
- Keep the driver as close to the load as possible to minimize the length of high-current traces. This reduces the series inductance to improve high-speed switching, while reducing the loop area that can radiate EMI to the driver inputs and other surrounding circuitry.
- Many high-speed power circuits can be susceptible to noise injected from their own output or other external sources, possibly causing output re-triggering. These effects can be especially obvious if the circuit is tested in breadboard or non-optimal circuit layouts with long input, enable, or output leads. For best results, make connections to all pins as short and direct as possible.
- The turn-on and turn-off current paths should be minimized as discussed in the following sections.

Figure 33 shows the pulsed gate-drive current path when the gate driver is supplying gate charge to turn the MOSFET on. The current is supplied from the local bypass capacitor, C_{BYP}, and flows through the driver to the MOSFET gate and to ground. To reach the high peak currents possible, the resistance and inductance in the path should be minimized. The localized C_{BYP} acts to contain the high peak-current pulses within this driver-MOSFET circuit, preventing them from disturbing the sensitive analog circuitry in the PWM controller.

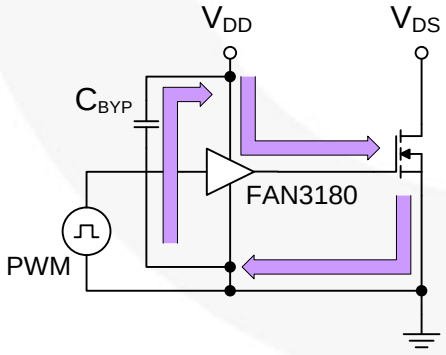

Figure 33. Current Path for MOSFET Turn-On

Figure 34 shows the current path when the gate driver turns the MOSFET off. Ideally, the driver shunts the current directly to the source of the MOSFET in a small circuit loop. For fast turn-off times, the resistance and inductance in this path should be minimized.

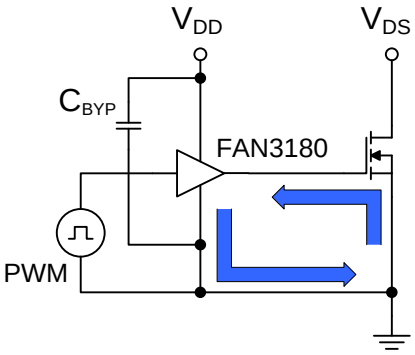

Figure 34. Current Path for MOSFET Turn-Off

Thermal Guidelines

Gate drivers used to switch MOSFETs and IGBTs at high frequencies can dissipate significant amounts of power. It is important to determine the driver power dissipation and the resulting junction temperature in the application to ensure that the part is operating within acceptable temperature limits.

The total power dissipation in a gate driver is the sum of three components; P_{GATE}, $P_{QUIESCENT}$, and $P_{DYNAMIC}$:

$$P_{total} = P_{gate} + P_{Dynamic} \quad (1)$$

Gate Driving Loss: The most significant power loss results from supplying gate current (charge per unit time) to switch the load MOSFET on and off at the switching frequency. The power dissipation that results from driving a MOSFET at a specified gate-source voltage, V_{GS}, with gate charge, Q_G, at switching frequency, f_{SW}, is determined by:

$$P_{GATE} = Q_G \bullet V_{GS} \bullet f_{sw} \quad (2)$$

Dynamic Pre-drive / Shoot-through Current: A power loss resulting from internal current consumption under dynamic operating conditions, including pin pull-up / pull-down resistors, can be obtained using the *I_{DD} (No-Load) vs. Frequency* graphs in Typical Performance Characteristics to determine the current $I_{DYNAMIC}$ drawn from V_{DD} under actual operating conditions:

$$P_{DYNAMIC} = I_{DYNAMIC} \bullet V_{DD} \quad (3)$$

Once the power dissipated in the driver is determined, the driver junction temperature rise with respect to the device lead can be evaluated using thermal equation:

$$T_J = P_{TOTAL}\,\Theta_{JL} + T_C \quad (4)$$

where:

T_J = driver junction temperature;

θ_{JL} = thermal resistance from junction to lead; and

T_L = lead temperature of device in application.

The power dissipated in a gate-drive circuit is independent of the drive-circuit resistance and is split proportionately among the resistances present in the driver, any discrete series resistor present, and the gate resistance internal to the power switching MOSFET. Power dissipated in the driver may be estimated using the following equation:

$$P_{PKG} = P_{TOTAL}\left(\frac{R_{OUT,Driver}}{R_{OUT,DRIVER} + R_{EXT} + R_{GATE,FET}}\right) \quad (5)$$

where:

P_{PKG} = power dissipated in the driver package;

$R_{OUT,DRIVER}$ = estimated driver impedance derived from I_{OUT} vs. V_{OUT} waveforms;

R_{EXT} = external series resistance connected between the driver output and the gate of the MOSFET; and

$R_{GATE,FET}$ = resistance internal to the load MOSFET gate and source connections.

Transitioning from FAN3100

Many applications use a combination of a microcontroller (MCU) and a gate driver, such as the FAN3100. In these configurations, an external low-dropout regulator (LDO) is needed to power the MCU. The FAN3180 integrates a 3.3-V output voltage regulator to power the microcontroller or ASICs. Therefore, systems using the FAN3100 and similar configurations can transition to the FAN3180 to save component count, board space, and cost.

The FAN3180 pinout is also such that minimal effort is needed to transition from designs already using the FAN3100TSX (the SOT23-5 package option). Four of the five pins are the same on both devices. The IN- input (pin 4 on the FAN3100) has been replaced with 3V3 LDO output on the FAN3180.

The following two diagrams show typical application examples of both the FAN3100 and FAN3180 designs powering a microcontroller.

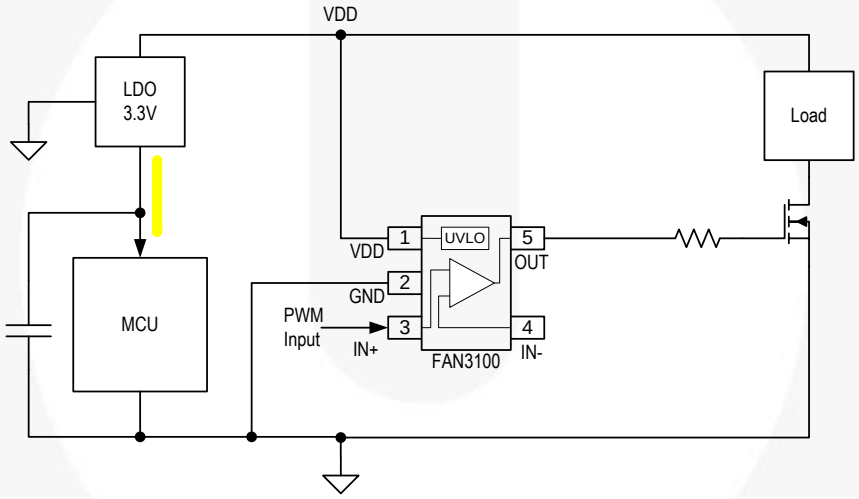

Figure 35. FAN3100TSX with an External LDO to Power a MCU

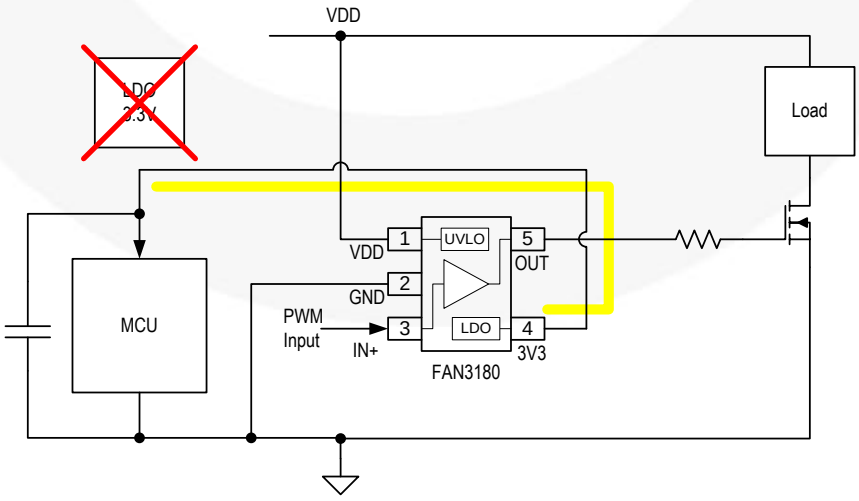

Figure 36. FAN3180TSX (with Integrated LDO) to Power a MCU

Table 1. Related Products

Part Number	Type	Gate Drive[10] (Sink/Src)	Input Threshold	Logic	Package
FAN3111C	Single 1 A	+1.1 A / -0.9 A	CMOS	Single Channel of Dual-Input/Single-Output	SOT23-5, MLP6
FAN3111E	Single 1 A	+1.1 A / -0.9 A	External[11]	Single Non-Inverting Channel with External Reference	SOT23-5, MLP6
FAN3100C	Single 2 A	+2.5 A / -1.8 A	CMOS	Single Channel of Two-Input/One-Output	SOT23-5, MLP6
FAN3100T	Single 2 A	+2.5 A / -1.8 A	TTL	Single Channel of Two-Input/One-Output	SOT23-5, MLP6
FAN3180	**Single 2 A**	**+2.4 A / -1.6 A**	**TTL**	Single Non-Inverting Channel + 3.3-V LDO	**SOT23-5**
FAN3216T	Dual 2 A	+2.4 A / -1.6 A	TTL	Dual Inverting Channels	SOIC8
FAN3217T	Dual 2 A	+2.4 A / -1.6 A	TTL	Dual Non-Inverting Channels	SOIC8
FAN3226C	Dual 2 A	+2.4 A / -1.6 A	CMOS	Dual Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3226T	Dual 2 A	+2.4 A / -1.6 A	TTL	Dual Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3227C	Dual 2 A	+2.4 A / -1.6 A	CMOS	Dual Non-Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3227T	Dual 2 A	+2.4 A / -1.6 A	TTL	Dual Non-Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3229C	Dual 2 A	+2.4 A / -1.6 A	CMOS	Dual Channels of Two-Input/One-Output	SOIC8, MLP8
FAN3229T	Dual 2 A	+2.4 A / -1.6 A	TTL	Dual Channels of Two-Input/One-Output	SOIC8, MLP8
FAN3268T	Dual 2 A	+2.4 A / -1.6 A	TTL	20 V Non-Inverting Channel (NMOS) and Inverting Channel (PMOS) + Dual Enables	SOIC8
FAN3278T	Dual 2 A	+2.4 A / -1.6 A	TTL	30 V Non-Inverting Channel (NMOS) and Inverting Channel (PMOS) + Dual Enables	SOIC8
FAN3213T	Dual 4 A	+4.3 A / -2.8 A	TTL	Dual Inverting Channels	SOIC8
FAN3214T	Dual 4 A	+4.3 A / -2.8 A	TTL	Dual Non-Inverting Channels	SOIC8
FAN3223C	Dual 4 A	+4.3 A / -2.8 A	CMOS	Dual Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3223T	Dual 4 A	+4.3 A / -2.8 A	TTL	Dual Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3224C	Dual 4 A	+4.3 A / -2.8 A	CMOS	Dual Non-Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3224T	Dual 4 A	+4.3 A / -2.8 A	TTL	Dual Non-Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3225C	Dual 4 A	+4.3 A / -2.8 A	CMOS	Dual Channels of Two-Input/One-Output	SOIC8, MLP8
FAN3225T	Dual 4 A	+4.3 A / -2.8 A	TTL	Dual Channels of Two-Input/One-Output	SOIC8, MLP8
FAN3121C	Single 9 A	+9.7 A / -7.1 A	CMOS	Single Inverting Channel + Enable	SOIC8, MLP8
FAN3121T	Single 9 A	+9.7 A / -7.1 A	TTL	Single Inverting Channel + Enable	SOIC8, MLP8
FAN3122T	Single 9 A	+9.7 A / -7.1 A	CMOS	Single Non-Inverting Channel + Enable	SOIC8, MLP8
FAN3122C	Single 9 A	+9.7 A / -7.1 A	TTL	Single Non-Inverting Channel + Enable	SOIC8, MLP8
FAN3240	Dual 12 A	+12.0 A	TTL	Dual-Coil Relay Driver, Timing Config. 0	SOIC8
FAN3241	Dual 12 A	+12.0 A	TTL	Dual-Coil Relay Driver, Timing Config. 1	SOIC8

Notes:

10. Typical currents with OUT at 6 V and V_{DD}=12 V.
11. Thresholds proportional to an externally supplied reference voltage.

Physical Dimensions

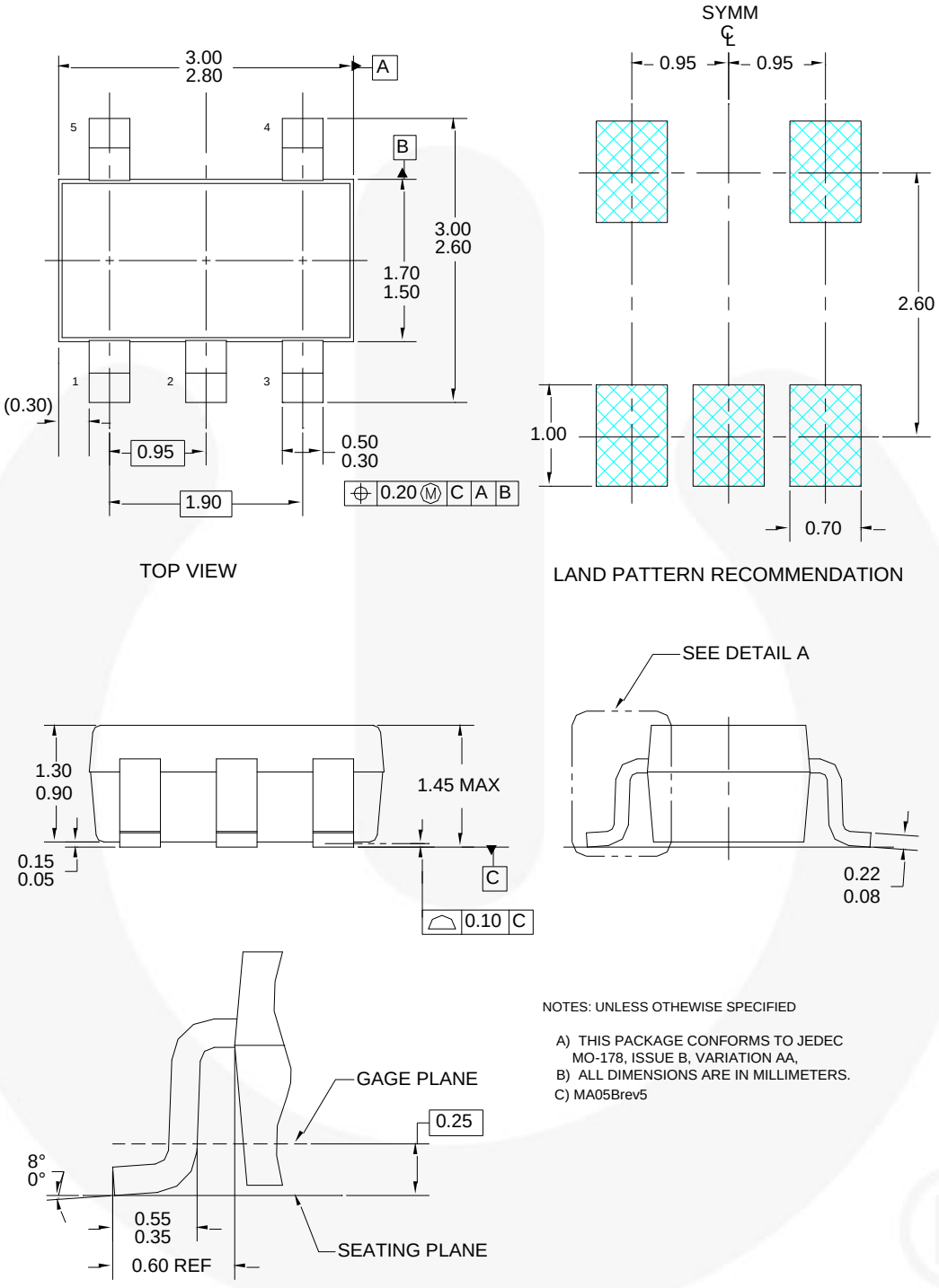

Figure 37.5-Lead SOT-23

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
http://www.fairchildsemi.com/packaging/.

FAIRCHILD SEMICONDUCTOR®

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

2Cool™
AccuPower™
AX-CAP®*
BitSiC™
Build it Now™
CorePLUS™
CorePOWER™
CROSSVOLT™
CTL™
Current Transfer Logic™
DEUXPEED®
Dual Cool™
EcoSPARK®
EfficientMax™
ESBC™
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FETBench™
FPS™
F-PFS™
FRFET®
Global Power Resource℠
GreenBridge™
Green FPS™
Green FPS™ e-Series™
Gmax™
GTO™
IntelliMAX™
ISOPLANAR™
Making Small Speakers Sound Louder and Better™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MicroPak2™
MillerDrive™
MotionMax™
mWSaver™
OptoHiT™
OPTOLOGIC®
OPTOPLANAR®
PowerTrench®
PowerXS™
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
Saving our world, 1mW/W/kW at a time™
SignalWise™
SmartMax™
SMART START™
Solutions for Your Success™
SPM®
STEALTH™
SuperFET®
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS®
SyncFET™
Sync-Lock™
SYSTEM GENERAL®*
TinyBoost™
TinyBuck™
TinyCalc™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
TranSiC™
TriFault Detect™
TRUECURRENT®*
μSerDes™
SerDes™
UHC®
Ultra FRFET™
UniFET™
VCX™
VisualMax™
VoltagePlus™
XS™

* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I64

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

ON Semiconductor:

FAN3180TSX

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9