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June 2013

# **FJD5555**

# **NPN Silicon Transistor**

#### **Features**

- Fast Speed Switching
- Wide Safe Operating Area
- High Voltage Capability

## **Application**

- Electronic Ballast
- · Switch Mode Power Supplies



# **Ordering Information**

Part Number	Marking	Package	Packing Method
FJD5555TM	J5555	D-PAK	Tape & Reel

## **Absolute Maximum Ratings**

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at  $T_A = 25^{\circ}\text{C}$  unless otherwise noted.

Symbol	Parameter	Value	Units
BV <sub>CBO</sub>	Collector-Base Voltage	1050	V
BV <sub>CEO</sub>	Collector-Emitter Voltage	400	V
BV <sub>EBO</sub>	Emitter-Base Voltage	14	V
I <sub>C</sub>	Collector Current (DC)	5	Α
I <sub>CP</sub>	Collector Current (Pulse)	10	Α
I <sub>B</sub>	Base Current (DC)	2	Α
I <sub>BP</sub>	Base Current (Pulse)	4	Α
$T_J$	Junction Temperature	150	°C
T <sub>STG</sub>	Storage Junction Temperature Range	- 55 to +150	°C

#### **Thermal Characteristics**

Values are at  $T_{\Lambda} = 25^{\circ}$ C unless otherwise noted.

Symbol	Parameter		Value	Units
P <sub>D</sub>	Total Device Dissipation	T <sub>A</sub> = 25°C	1.34	W
		$T_C = 25^{\circ}C$	100	W
$R_{\theta ja}^{(1)}$	Thermal Resistance, Junction to Ambient		95	°C/W
R <sub>θjc</sub> <sup>(2)</sup>	Thermal Resistance, Junction to Case		1.25	°C/W

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#### **Notes**

- 1.  $R_{\theta ia}$  test board and fixture under natural convection; JESD51-3 recommended thermal test board.
- 2.  $R_{\theta ic}$  test fixture under infinite cooling condition.

# Electrical Characteristics(3)

Values are at  $T_A = 25$ °C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Units
BV <sub>CBO</sub>	Collector-Base Breakdown Voltage	$I_C = 500  \mu A, I_E = 0$	1050			V
BV <sub>CEO</sub>	Collector-Emitter Breakdown Voltage	$I_C = 5 \text{ mA}, I_B = 0$	400			V
BV <sub>EBO</sub>	Emitter-Base Breakdown Voltage	$I_E = 500  \mu A,  I_C = 0$	14			V
h <sub>FE</sub>	DC Current Gain	$V_{CE} = 5 \text{ V}, I_{C} = 10 \text{ mA}$	10			
		$V_{CE} = 3 \text{ V}, I_{C} = 0.8 \text{ A}$	20		40	
V <sub>CE</sub> (sat)	Collector-Emitter Saturation Voltage	$I_C = 1 \text{ A}, I_B = 0.2 \text{ A}$		0.17	0.50	V
		$I_C = 3.5 \text{ A}, I_B = 1.0 \text{ A}$			1.5	V
V <sub>BE</sub> (sat)	Base-Emitter Saturation Voltage	$I_C = 3.5 \text{ A}, I_B = 1.0 \text{ A}$			1.2	V
C <sub>ob</sub>	Output Capacitance	V <sub>CB</sub> = 10 V, f = 1 MHz		45		pF
t <sub>ON</sub>	Turn-On Time	$V_{CC} = 125 \text{ V}, I_{C} = 0.5 \text{ A},$			1.0	μs
t <sub>STG</sub>	Storage Time	$I_{B1} = 45 \text{ mA}, I_{B2} = -0.5 \text{ A},$			1.2	μs
t <sub>F</sub>	Fall Time	$R_L = 250 \Omega$		0.3		μs
t <sub>ON</sub>	Turn-On Time	$V_{CC} = 250 \text{ V}, I_{C} = 2.5 \text{ A},$			2.0	μs
t <sub>STG</sub>	Storage Time	$I_{B1} = 0.5 \text{ A}, I_{B2} = -1.0 \text{ A},$ $R_L = 100 \Omega$			2.5	μs
t <sub>F</sub>	Fall Time				0.3	μs
EAS	Avalanche Energy	L = 2 mH	6			mJ

#### Note:

3. Pulse test: pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2\%.$ 

# **Typical Performance Characteristics**

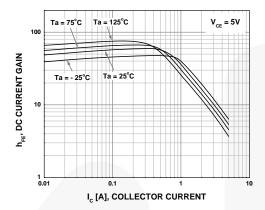


Figure 1. DC Current Gain

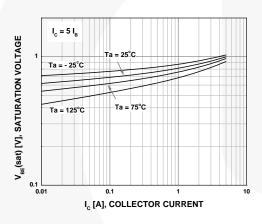


Figure 3. Saturation Voltage

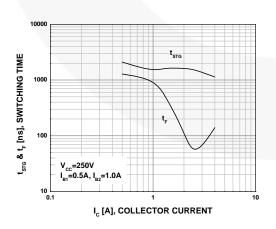


Figure 5. Resistive Load Switching

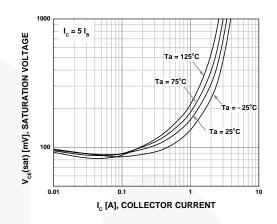


Figure 2. Saturation Voltage

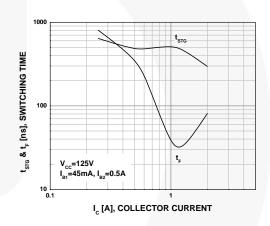


Figure 4. Resistive Load Switching

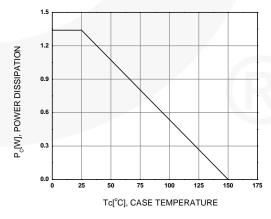


Figure 6. Power Derating

# **Typical Performance Characteristics** (Continued)

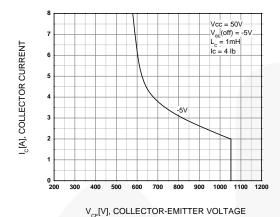


Figure 7. Reverse Bias Safe Operating

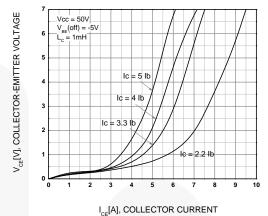
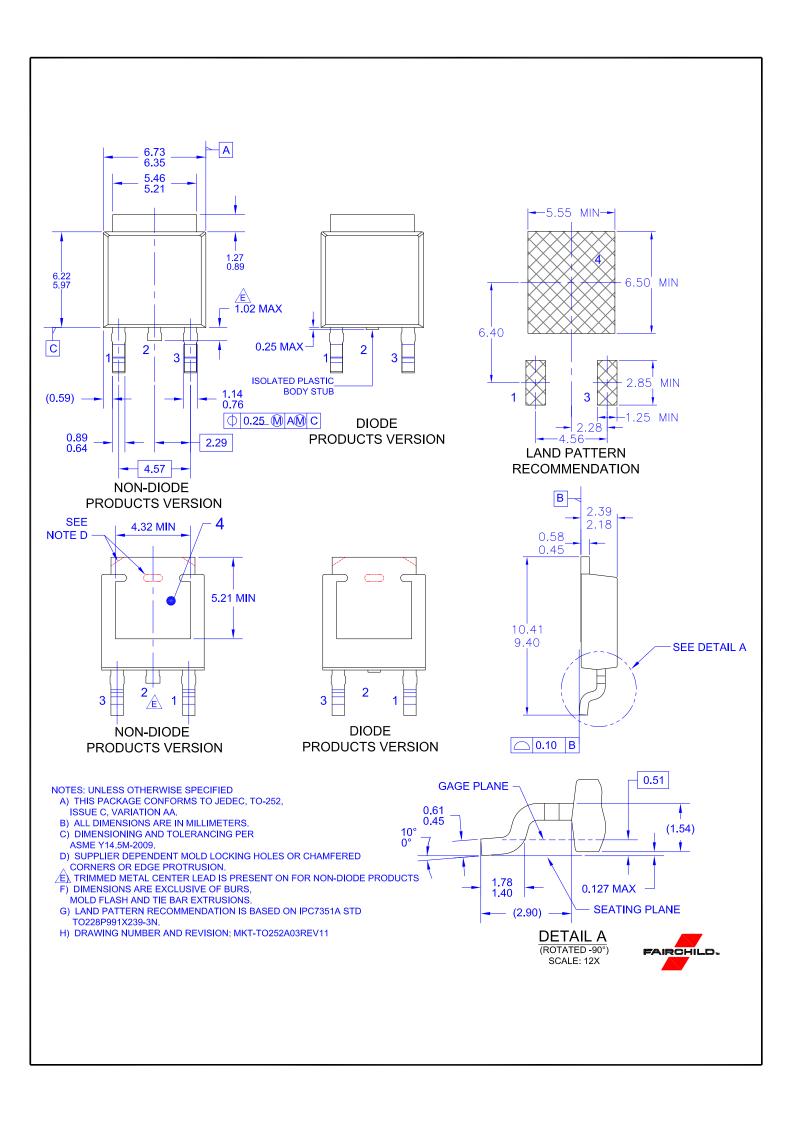


Figure 8. V<sub>CE</sub> Saturation vs. h<sub>FE</sub>



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