

Data sheet acquired from Harris Semiconductor SCHS048C – Revised October 2003

### CMOS Liquid-Crystal Display Drivers

High-Voltage Types (20-Volt Rating)

CD4054B - 4-Segment Display Driver

CD4055B — BCD to 7-Segment Decoder/Driver with "Display-Frequency" Output

CD4056B — BCD to 7-Segment Decoder/Driver with Strobed-Latch Function

single-digit BCD-to-7-segment decoder/driver circuits that provide level-shifting functions on the chip. This feature permits the BCD input-signal swings (VDD to VSS) to be the same as or different from the 7-segment output-signal swings (VDD to VEE). For example, the BCD input-signal swings (VDD to VSS) may be as small as 0 to -3 V, whereas the output-display drive-signal swing (VDD to VEE) may be as large as from 0 to -15V. If VDD to VEE exceeds 15 V, VDD to VSS should be at least 4V (0 to -4V).

The 7-segment outputs are controlled by the DISPLAY-FREQUENCY (DF) input which causes the selected segment outputs to be low, high, or a square-wave output (for liquid-crystal displays). When the DF input is low the output segments will be high when selected by the BCD inputs. When the DF input is high, the output segments will be low when selected by the BCD inputs. When a square-wave is present at the DF input, the selected segments will have a square-wave output that is 180° out of phase with the DF input. Those segments which are not selected will have a squarewave output that is in phase with the input. DF square-wave repetition rates for liquidcrystal displays usually range from 30 Hz (well above flicker rate) to 200 Hz (well below the upper limit of the liquid-crystal frequency response). The CD4055B provides a level-shifted high-amplitude DF output which is required for driving the common electrode in liquid-crystal displays. The CD4056B provides a strobed-latch function at the BCD inputs. Decoding of all input combinations on the CD4055B and CD4056B provides displays of 0 to 9 as well as L. P. H, A, -, and a blank position.

The CD4054B provides level shifting similar to the CD4055B and CD4056B independently strobed latches, and common DF control on 4 signal lines. The CD4054B is intended to provide drive-signal compatibility with the CD4055B and CD4056B 7-segment decoder types for the decimal point, colon, polarity, and similar display lines. A level-shifted high-amplitude DF output can be obtained from any CD4054B output line by connect-

#### CD4054B, CD4055B, CD4056B Types

#### Features:

- Operation of liquid crystals with CMOS circuits provides ultra-low-power displays
- Equivalent ac output drive for liquidcrystal displays — no external capacitor required
- Voltage doubling across display, e.g.
   VDD VEE = 18 V results in effective
   36 V p-p drive across selected display segments
- Low- or high-output level dc drive for other types of displays
- On-chip logic-level conversion for different input- and output-level swings
- Full decoding of all input combinations:
   0-9, L, H, P, A,-, and blank positions
- Strobed-latch function—CD4054B Series and CD4056B Series
- DISPLAY-FREQUENCY (DF) output for liquid-crystal common-line drive signal— CD4055B Series (CD4054B Series also: see introductory text)
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):

1 V at V<sub>DD</sub> = 5 V 2 V at V<sub>DD</sub> = 10 V 2.5 V at V<sub>DD</sub> = 15 V

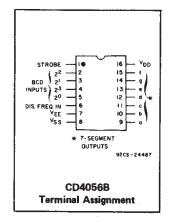
■ 5-V, 10-V, and 15-V parametric ratings

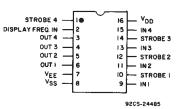
#### **Applications**

- General-purpose displays
- Calculators and meters
- Wall and table clocks
- Industrial control panels
- Portable lab instruments
- Panel meters
- Auto dashboard displays
- Appliance control panels

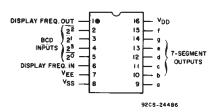
ing the corresponding input and strobe lines to a low and high level, respectively and applying a square wave to DFIN. The CD4054B may also be utilized for logic-level "up conversion" or "down conversion". For example, input-signal swings (VDD to VSS) from +5 to 0 V can be converted to outputsignal swings (VDD to VEE) of +5 to -5 V. The level-shifted function on all three types permits the use of different input- and output-signal swings. The input swings from a low level of VSS to a high level of VDD while the output swings from a low level of VEE to the same high level of VDD. Thus, the input and output swings can be selected independently of each other over a 3-to-18 V range. VSS may be connected to VEE when no level-shift function is required.

For the CD4054B and CD4056B, data are





CD4054B Terminal Assignment

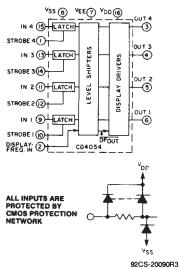


CD40558 Terminal Assignment

transferred from input to output by placing a high voltage level at the strobe input. A low voltage level at the strobe input latches the data input and the corresponding output segments remain selected (or non-selected) while the strobe is low.

Whenever the level-shifting function is required, the CD4055B can be used by itself to drive a liquid-crystal display (Fig.16 and Fig.20). The CD4056B, however, must be used together with a CD4054B to provide the common DF output (Fig.19). The capability of extending the voltage swing on the negative end (this voltage cannot be extended on the positive end) can be used to advantage in the setup of Fig.18. Fig.17 is common to all three types.

The CD4054B-, CD4055B-, and CD4056B-series types are supplied in 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes). The CD4054B- and CD4056B-series types also are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix).



**9**0 (O) -(12) d -(15) VDD ALL INPUTS ARE PROTECTED BY CMOS PROTECTION NETWORK 92CS-20092R2

Fig.1 - CD4054B functional diagram.

Fig.2 - CD4055B functional diagram.

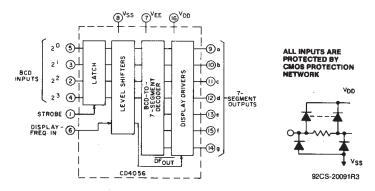


Fig.3 - CD4056B functional diagram.

#### **CD4054B TRUTH TABLE**

DF	IN	ST	OUT
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	0
Х	Х	0	•

X = Don't Care.

\*Depends upon the input mode previously applied when ST = 1.

#### TRUTH TABLE FOR CD4055B and CD4056B

- 11	NPU	r co	DE			OUTF	UT S	TAT	E	- 1		DISPLAY CHARAC-
23	22	21	20	а	ь	C	d	е	f	g	Н	TER
0	0	0	0	1	1	1	1	1	1	0	П	1_1
0	0	0	1	0	1	1	0	0	0	0	$\ $	
0	0	1	0	1	1	0	1	1	0	1		
0	0	1	1	1	1	1	1	0	0	1		=
0	1	0	0	0	1	1	0	0	1	1		1—
0	1	0	1	1	0	1	1	0	1	1	П	<u>'</u>
0	1	1	0	1	0	1	1	1	1	1		ΙΞ,
0	1	1	1	1	1	1	0	0	0	0		
1	0	0	0	1	1	1	1	1	1	1	$\ $	
1	0	0	1	1	1	1	1	0	1	1		'골'
1	0	1	0	0	0	0	1	1	1	0	П	1_
1	0	1	1	0	1	1	0	1	1	1		
1	1	0	0	1	1	0	0	1	1	1		
1	1	0	1	1	1	1	0	1	1	1		; <del>=</del> ;
1	1	1	0	0	0	0	0	0	0	1	$\ $	_
1	1	1	1	0	0	0	0	0	0	0		BLANK

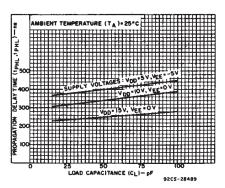


Fig.4 - Typical propagation delay time vs. load capacitance for CD4054B.

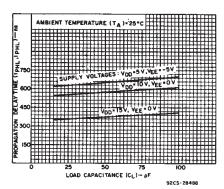


Fig.5 — Typical propagation delay time vs. load capacitance for CD4055 and CD4056B.

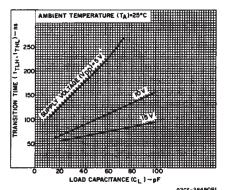


Fig.6 - Typical transition time vs. load capacitance.

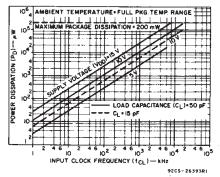


Fig.7 - Typical input clock frequency vs. power dissipation.

MAXIMUM RATINGS, Absolute-Maximum Values:	
DC SUPPLY-VOLTAGE RANGE, (V <sub>DD</sub> )	
Voltages referenced to VSS Terminal)	0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS	
DC INPUT CURRENT, ANY ONE INPUT	±10mA
POWER DISSIPATION PER PACKAGE (PD):	
For $T_A = -55^{\circ}C$ to $+100^{\circ}C$	500mW
For T <sub>A</sub> = +100°C to +125°C	12mW/OC to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR TA = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100mW
OPERATING-TEMPERATURE RANGE (TA)	55°C to +125°C
STORAGE TEMPERATURE RANGE (T <sub>stg</sub> )	65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 $\pm$ 1/32 inch (1.59 $\pm$ 0.79mm) from case for 10s max	+265°C

## MBIENT TEMPERATURE (TA )=25°C 5 IO I5 DRAIN-TO-SOURCE VOLTAGE (V<sub>DS</sub>)-V 92C9-35963

Fig.8 - Typical n-channel output low (sink) current characteristics.

## NT TEMPERATURE (TA) - 25°C DRAIN-TO-SOUR E VOLTAGE (VDS)-V

Fig.9 - Minimum n-channel output low (sink) current characteristics.

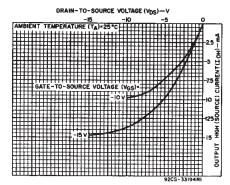


Fig. 10 - Typical p-channel output high (source) current characteristics.

# DRAIN-TO-SOURCE VOLTAGE (VDS)-V

Fig. 13 — Minimum p-channel output high (source) current characteristics.

#### STATIC ELECTRICAL CHARACTERISTICS

		_	NDIT	ONS		LIMIT	S AT II	NDICA.	TED TE	MPER	ATURE	s (°C)	
Characteristic	V <sub>EE</sub>	V <sub>SS</sub>	4	V <sub>IN</sub>	V <sub>DD</sub>	<u> </u>	<u> </u>		Ī —	T	+25°C	<del></del>	Units
				L		-55°	-40°	+850	+1250	Min.	Тур.	Max.	1
Quiescent Device	- 5	0			5		5	150	150	-	0.04	5	μА
Current, IDD	0	0			10		10	300	300		0.04	10	1 "
MAX.	0	0	ļ		15		20	600	600	_	0.04	20	1
	0	0	<u> </u>	L	20	1	00	3000	3000	. –	0.08	100	1
Output Voltage:													
	0	0	L	0,5	5		0	.05			0	0.05	
Low Level, VOL	0	0	L	0,10	10		0	.05			0	0.05	1
MAX.	0	0		0,15	15		0	.05			0	0.05	1
	0	0		0,5	5		4	.95		4.95	5	-	V
High Level, VOH	0	0		0,10	10		9.95			9.95	10		1 1
MIN.	MIN. 0 0 0,15 15 14.95		1.95		14.95	15		1 1					
Input Low Voltage,	0	0	0.5, 4.5		5		1	.5		_	_	1.5	
VIL MAX.	0	0	1,9		10			3				3	
	0	0 1	.5,13.	5	15			4			1 -	4	
Input High	<b>-</b> 5	0	0.5,4.5		5		3	.5	-	3.5			V
Voltage,	0	0	1,9		10			7		7	-		
VIH MIN.	0	0 1	.5,13.5		15		1	11		11	-	-	
Output Low (Sink)	-5	0	-4.5		5	0.98	0.92	0.67	0.55	0.8	1.6		
Current, IOL	0	0	0.5		10	0.98	0.92	0.67	0.55	0.8	1.6	_	
	0	0	1.5		15	3.6	3.4	2.4	2	2.9	5.8		ŀ
Output High	-5	0	4.5		5	-0.6	0.55	0.35	0.3	-0.45	-0.9		mA
(Source)	0	0	9.5		10	-0.6	0.55	0.35	-0.3	-0.45	-0.9		
		13.5		15	-1.9			-1.1	- 1.5	-3		- 1	
Input Current,	0	0	-	0,18	18	±0.1	±0.1	±1	±1	-	±10-5	±0.1	μΑ

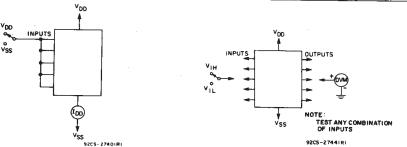


Fig. 11 - Quiescent-device-current test circuit.

Fig. 12 - Input-voltage test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS at TA = 25°C, CL = 50 pF, Input tr, tr = 20 ns, RL = 200 k $\Omega$ 

	COI	NDITI				LIMITS	VDEC		
CHARACTERISTIC	VEE (V)	Vss (V)	V <sub>DD</sub>		1054	CKAGE T	UNITS		
	(4)	(٧)	(V)	Тур.	Max.	Тур.	Max.		
Propagation Delay Time,	<b>–</b> 5	0	5	400	800	650	1300		
tPHL,tPLH	0	0	10	340	680	575	1150	ns	
(Any Input to Any Output)	0 -	0	15	250	500	375	750		
Transition Time, t <sub>THL</sub> ,t <sub>TLH</sub>	-5	0	5	100	200	100	200		
	0	0	10	100	200	100	200	ns	
(Any Output)	0	0	15	75	150	75	150		
Minimum Data Setup	-5	0	5	110	220	110	220		
Time, to*	0	0	10	50	100	50	100	ns	
Time, ts			15	35	70	35	70		
Minimum Strobe Pulse	-5	0	5	110	220	110	220		
	0	0	10	50	100	50	100	ns	
Width, t <sub>W</sub> *	0	0	15	35	70	35	70		
Input Capacitance, CIN (Any Input)	_	-	-	5	7.5	5	7.5	pF	

<sup>\*</sup> CD4054 and CD4056 only.

#### RECOMMENDED OPERATING CONDITIONS at T<sub>A</sub> = 25°C (Unless otherwise specified)

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	VEE	VSS	V <sub>DD</sub>	LIM	ITS	UNITS
CHARACTERISTIC	(V)	(V)	(V)	Min.	Max.	DIVITS
Supply Voltage Range: (At TA = Full Package Temperature Range)				3	18	>
	5	0	5	220	_	
Setup Time (t <sub>c</sub> )●	0	0	10	100	T	ns
	0	0	15	70	_	
	-5	-0	5	220		
Strobe Pulse Width (tw)	0	0	10	100		ns
·	0	0	15	70	_	<u> </u>

For CD4054 and CD4056 only.

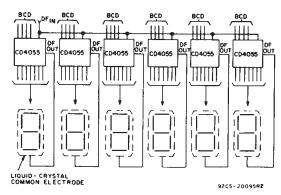


Fig. 16 - Clock display:  $V_{DD}$  = 0 V,  $V_{SS}$  =-5 V,  $V_{EE}$  = -15 V,  $DF_{IN}$  = 30 Hz square wave.

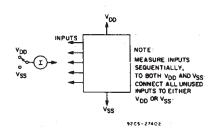


Fig. 14 - Input-current test circuit.

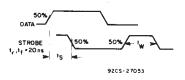
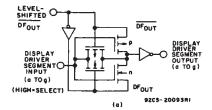


Fig. 15 — Data setup time and strobe pulse duration.



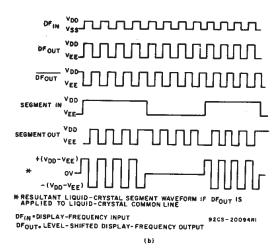


Fig. 17 — Display-driver circuit for one segment line and waveforms,

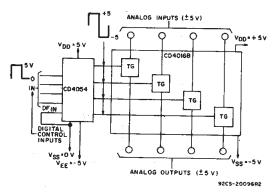


Fig. 18 - Digital (0 to +5 V) to bidirectional analog control (+5 to -5 V) level shifter.

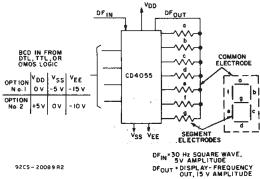


Fig.20 - Single-digit liquid-crystal display.

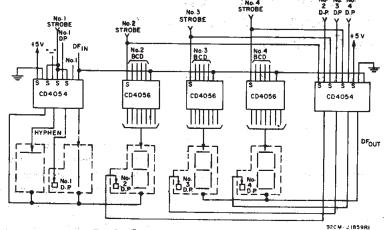


Fig. 19 — Typical 3½-digit liquid-crystal display: V<sub>DD</sub> = +5 V, V<sub>SS</sub> = 0 V, V<sub>EE</sub> = -10 V, DF<sub>IN</sub> = 30 Hz square wave.

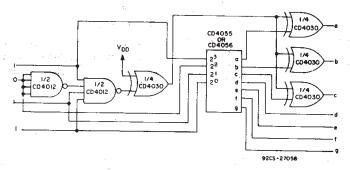


Fig.21 - Conversion of "H" display to "F" display.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.

Grid graduations are in mils (10<sup>-3</sup> inch),

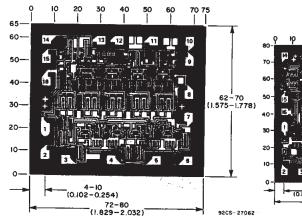
examp display

One of VEE=N

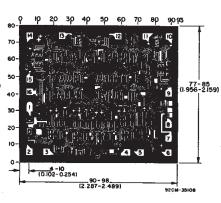
In addition to the letters L, H, P, and A (See the truth table), five other letters can be displayed through the use of simple logic circuits preceding and following the CD4055B or CD4056B devices. Fig.21 is an example of a circuit that converts an "H" display (code 1011) to an "F" display. One condition that must be met is that VEE=VSS. If VEE=VSS, the CD4054B must be used to level shift in the appropriate places.

In a similar manner the letters C, E, J, and U can be displayed. These circuits can also be used to drive LED displays provided the exclusive-OR gates have sufficient output-current drive.

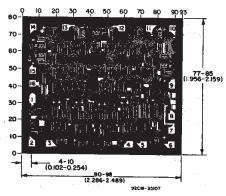
The letters B, D, G, I, O, and S may be represented by the codes for numbers 8, 0, 6, 1, 0, and 5, respectively, when there is preknowledge that only letters are to be displayed.



Dimensions and pad layout for CD4054BH.



Dimensions and pad layout for CD4055BH



Dimensions and pad layout for CD4056BH





24-Aug-2014

#### **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	_	Pins	_		Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
CD4054BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4054BE	Samples
CD4054BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4054BF3A	Samples
CD4054BM	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4054BM	Samples
CD4054BM96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4054BM	Samples
CD4054BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM054B	Samples
CD4055BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4055BE	Samples
CD4055BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4055BE	Samples
CD4055BM	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4055BM	Samples
CD4055BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM055B	Samples
CD4056BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4056BE	Samples
CD4056BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4056BE	Samples
CD4056BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4056BF3A	Samples
CD4056BM	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4056BM	Samples
CD4056BM96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4056BM	Samples
CD4056BM96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4056BM	Samples
CD4056BM96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4056BM	Samples
CD4056BME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4056BM	Samples



#### PACKAGE OPTION ADDENDUM

24-Aug-2014

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
CD4056BMG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4056BM	Samples
CD4056BMT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4056BM	Samples
CD4056BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM056B	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between

the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.



#### **PACKAGE OPTION ADDENDUM**

24-Aug-2014

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF CD4054B, CD4054B-MIL, CD4056B, CD4056B-MIL:

• Catalog: CD4054B, CD4056B

www.ti.com

• Military: CD4054B-MIL, CD4056B-MIL

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

#### PACKAGE MATERIALS INFORMATION

www.ti.com 18-Aug-2014

#### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4054BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4056BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

www.ti.com 18-Aug-2014



#### \*All dimensions are nominal

Device	Package Type	kage Type Package Drawing		SPQ	Length (mm)	Width (mm)	Height (mm)
CD4054BM96	SOIC	D	16	2500	333.2	345.9	28.6
CD4056BM96	SOIC	D	16	2500	333.2	345.9	28.6

#### 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

#### N (R-PDIP-T\*\*)

#### PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



#### D (R-PDS0-G16)

#### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



#### D (R-PDSO-G16)

#### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

#### PLASTIC SMALL OUTLINE

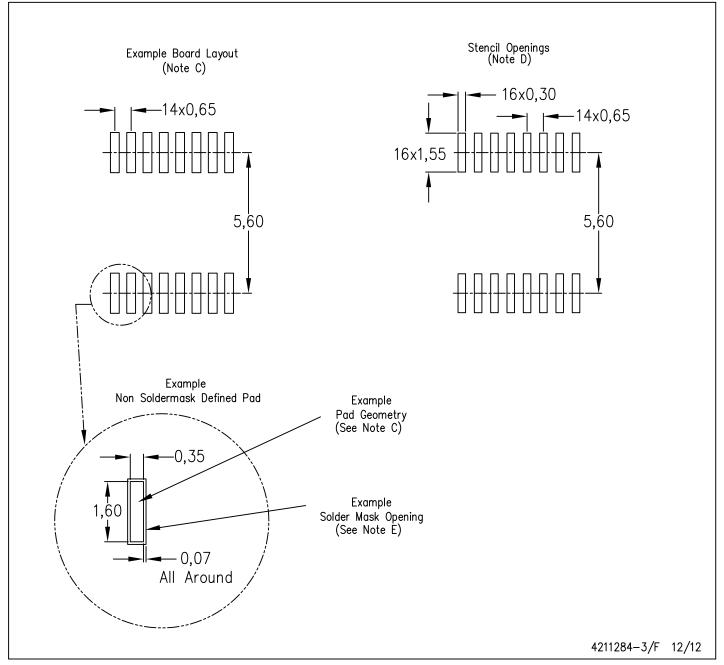


- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



#### PW (R-PDSO-G16)

#### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



#### IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have *not* been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products Applications

Audio www.ti.com/audio Automotive and Transportation www.ti.com/automotive Communications and Telecom Amplifiers amplifier.ti.com www.ti.com/communications **Data Converters** dataconverter.ti.com Computers and Peripherals www.ti.com/computers **DLP® Products** www.dlp.com Consumer Electronics www.ti.com/consumer-apps

DSP **Energy and Lighting** dsp.ti.com www.ti.com/energy Clocks and Timers www.ti.com/clocks Industrial www.ti.com/industrial Interface interface.ti.com Medical www.ti.com/medical logic.ti.com Logic Security www.ti.com/security

Power Mgmt power.ti.com Space, Avionics and Defense www.ti.com/space-avionics-defense

Microcontrollers <u>microcontroller.ti.com</u> Video and Imaging <u>www.ti.com/video</u>

RFID <u>www.ti-rfid.com</u>

OMAP Applications Processors <a href="https://www.ti.com/omap">www.ti.com/omap</a> TI E2E Community <a href="https://example.com/omap">e2e.ti.com/omap</a>

Wireless Connectivity <u>www.ti.com/wirelessconnectivity</u>

#### **ПОСТАВКА** ЭЛЕКТРОННЫХ КОМПОНЕНТОВ

многоканальный

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001 Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

#### Данный компонент на территории Российской Федерации Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

#### http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

#### Офис по работе с юридическими лицами:

105318, г. Москва, ул. Щербаковская д. 3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru moschip.ru\_6 moschip.ru\_4 moschip.ru\_9