FAIRCHILD SEMICONDUCTOR®

December 2004

FDSS2407
N-Channel Dual MOSFET
62V, 3.3A, 132mΩ

Features

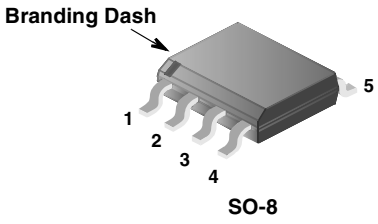
- 62V, 132mΩ, 5V Logic Level Gate Dual MOSFET in SO-8
- 5V Logic Level feedback signal of the drain to source voltage. Multiple devices can be wired “OR’d” to a single monitoring circuit input.
- Gate Drive Disable Input. Multiple devices controllable by a single disable transistor.
- Qualified to AEC Q101

Applications

- Automotive Injector Driver
- Solenoid Driver

General Description

This dual N-Channel MOSFET provides added functions as compared to a conventional Power MOSFET. These are: 1. A drain to source voltage feedback signal and 2. A gate drive disable control function that previously required external discrete circuitry. Including these functions within the MOSFET saves printed circuit board space. The drain to source voltage feedback function provides a 5V level output whenever the drain to source voltage is above 62V. This can monitor the time an inductive load takes to dissipate its stored energy. Multiple feedback signals can be wired “OR’d” together to a single input of the monitoring circuit. The gate disable function allows the device to be turned off independent of the drive signal on the gate. This function permits a second control circuit the ability to deactivate the load if necessary. It can also be wired “OR’d” allowing multiple devices to be controlled by a single open collector / drain control transistor.

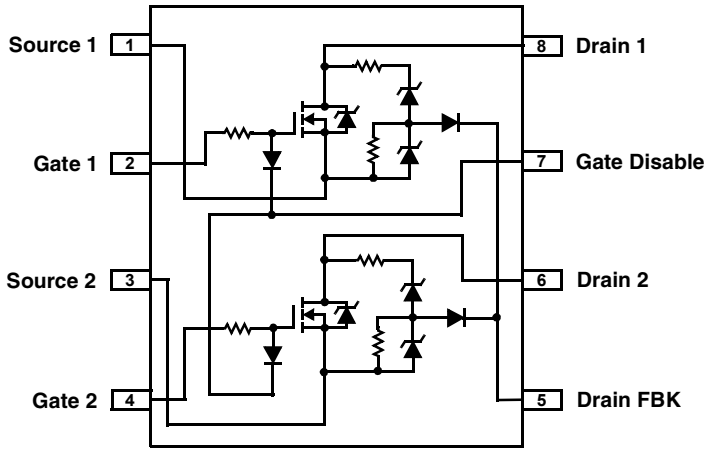


SO-8

Pin 5 - Drain Feedback Output

Pin 7 - Gate Drive Disable Input

Internal Diagram



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MOSFET Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	62	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current Continuous (T_A = 25°C, V_{GS} = 10V, $R_{\theta JA}$ = 55°C/W)	3.3	A
	Continuous (T_A = 25°C, V_{GS} = 5V, $R_{\theta JA}$ = 55°C/W)	3.0	A
	Pulsed	Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	140	mJ
P_D	Power dissipation	2.27	W
	Derate above 25°C	18	mW/°C
T_J, T_{STG}	Operating and Storage Temperature	-55 to 150	°C

Thermal Characteristics

$R_{\theta JA}$	Pad Area = 0.50 in^2 (323 mm^2) (Note 2)	55	°C/W
$R_{\theta JA}$	Pad Area = 0.027 in^2 (17.4 mm^2) (Note 3)	180	°C/W
$R_{\theta JA}$	Pad Area = 0.006 in^2 (3.87 mm^2) (Note 4)	200	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
2407	FDSS2407	SO-8	330 mm	12 mm	2500

Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
Off Characteristics							
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 5mA, V_{GS} = 0V		62	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 15V, V_{GS}=0V		-	-	1	µA
		V_{DS} = 15V, V_{GS}=0V, T_A=150°C		-	-	250	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V		-	-	±100	nA
On Characteristics							
$V_{GS(TH)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250µA		1	-	3	V
$r_{DS(ON)}$	Drain to Source On Resistance	I_D = 3.3A, V_{GS} = 10V		-	0.099	0.110	Ω
		I_D = 3.0A, V_{GS} = 5V		-	0.115	0.132	
Dynamic Characteristics							
C_{ISS}	Input Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 75kHz		-	300	-	pF
C_{OSS}	Output Capacitance			-	140	-	pF
C_{RSS}	Reverse Transfer Capacitance			-	16	-	pF
R_G	Gate Resistance			-	8500	-	Ω
$Q_{g(TOT)}$	Total Gate Charge at 5V	V_{GS} = 0V to 5V	V_{DD} = 30V I_D = 3.3A I_g = 1.0mA	-	3.3	4.3	nC
$Q_{g(TH)}$	Threshold Gate Charge	V_{GS} = 0V to 1V		-	0.4	0.5	nC
Q_{gs}	Gate to Source Gate Charge			-	1.2	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau			-	0.8	-	nC
Q_{gd}	Gate to Drain “Miller” Charge			-	2.0	-	nC

Switching Characteristics (V_{GS} = 10V)

t_{ON}	Turn-On Time	V_{DD} = 30V, I_D = 3.3A V_{GS} = 10V, R_{GS} = 47Ω	-	-	2700	ns
$t_{d(ON)}$	Turn-On Delay Time		-	630	-	ns
t_r	Rise Time		-	1200	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	8700	-	ns
t_f	Fall Time		-	3500	-	ns
t_{OFF}	Turn-Off Time		-	-	18500	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	I_{SD} = 3.3A	-	-	1.25	V
		I_{SD} = 1.7A	-	-	1.0	V
t_{rr}	Reverse Recovery Time	I_{SD} = 3.3A, dI_{SD}/dt = 100A/μs	-	-	45	ns
Q_{RR}	Reverse Recovered Charge	I_{SD} = 3.3A, dISD/dt = 100A/μs	-	-	60	nC

Drain Feedback Characteristics

$V_{FBK(Low)}$	Feedback to Source Voltage	V_{DS} = 35V, $R_{FBK-SOURCE}$ =51KΩ	-	1	1.5	V
$V_{FBK(High)}$	Feedback to Source Voltage	V_{DS} = 62V, $R_{FBK-SOURCE}$ =51KΩ	3.5	4.4	-	V

Gate Drive Disable Characteristics

$V_{DIS(High)}$	Gate Drive Disable Input Voltage, Gate Enabled	V_{GS} = 5V, I_D = 3.0A, T_J=25°C	3	-	-	V
$V_{DIS(Low)}$	Gate Drive Disable Input Voltage, Gate Disabled	V_{GS} = V_{DS} = 10V, $I_D \leq$ 250μA, T_J=150°C	-	-	0.4	V

Notes:

1. Starting T_J = 25°C, L = 42mH, I_{AS} = 2.6A, V_{DD} = 62V, V_{GS} = 10V.

2. 55°C/W measured using FR-4 board with 0.50 in^2 (323 mm^2) copper pad at 1 second.

3. 180°C/W measured using FR-4 board with 0.027 in^2 (17.4 mm^2) copper pad at 1000 seconds.

4. 200°C/W measured using FR-4 board with 0.006 in^2 (3.87 mm^2) copper pad at 1000 seconds.

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: http://www.aecouncil.com/
All Fairchild Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

Typical Characteristics T_A = 25°C unless otherwise noted

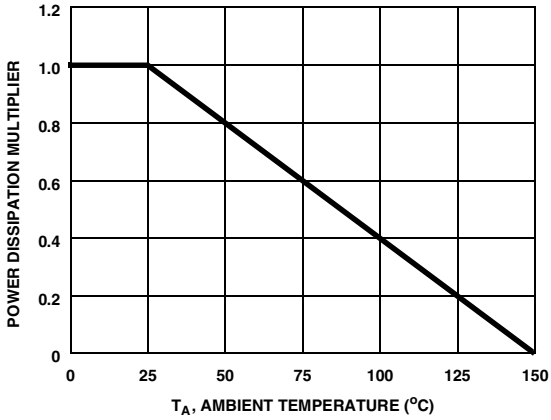


Figure 1. Normalized Power Dissipation vs Ambient Temperature

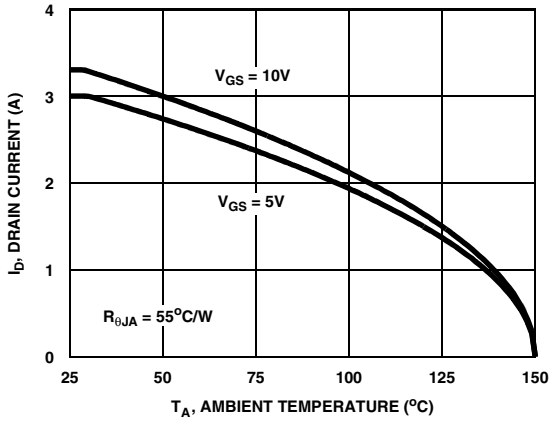


Figure 2. Maximum Continuous Drain Current vs Ambient Temperature

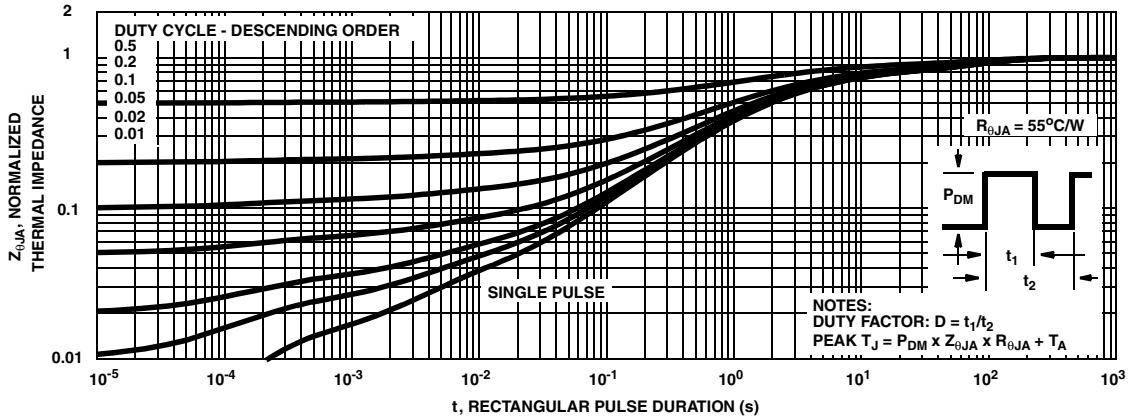


Figure 3. Normalized Maximum Transient Thermal Impedance

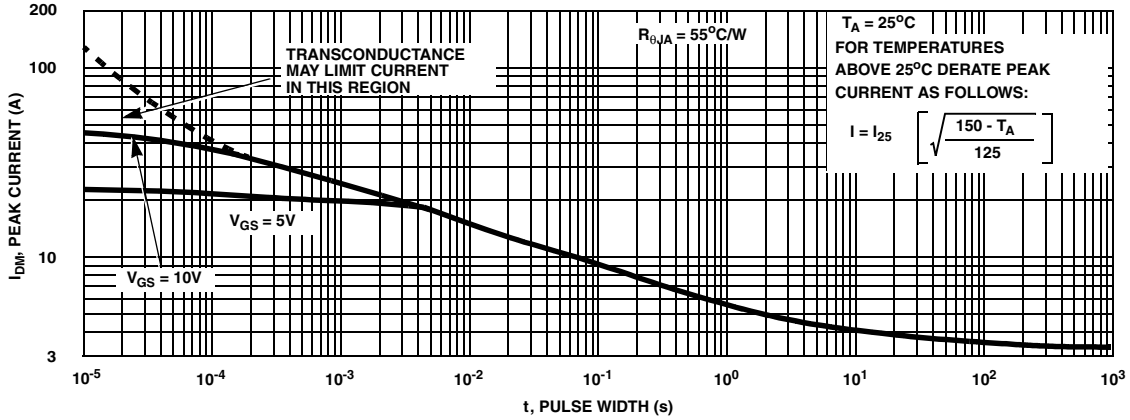


Figure 4. Peak Current Capability

Typical Characteristics (Continued) T_A = 25°C unless otherwise noted

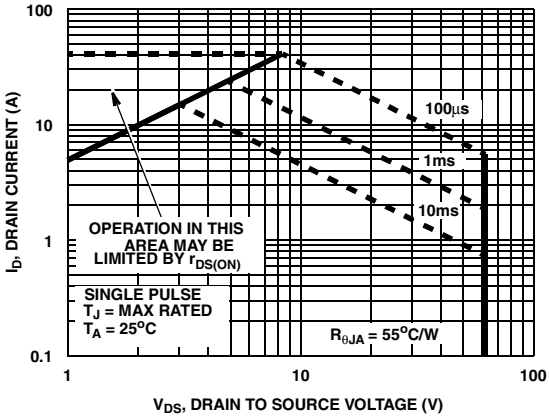
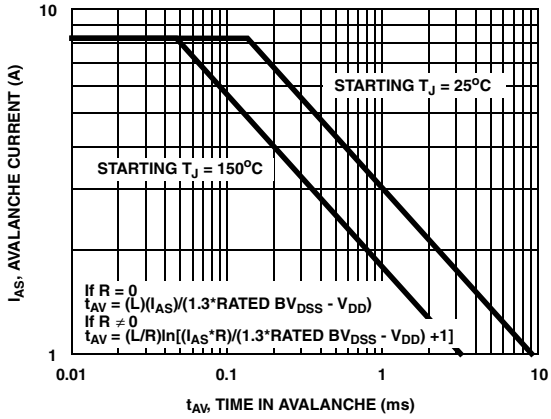


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

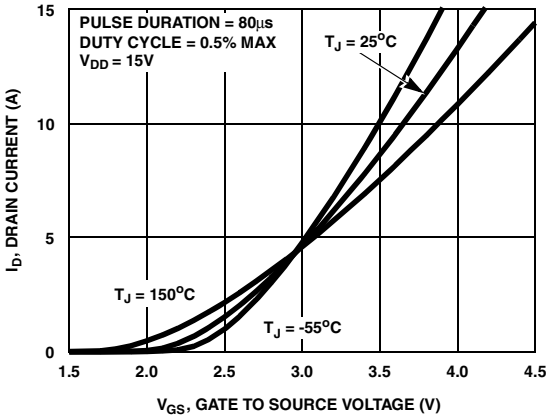


Figure 7. Transfer Characteristics

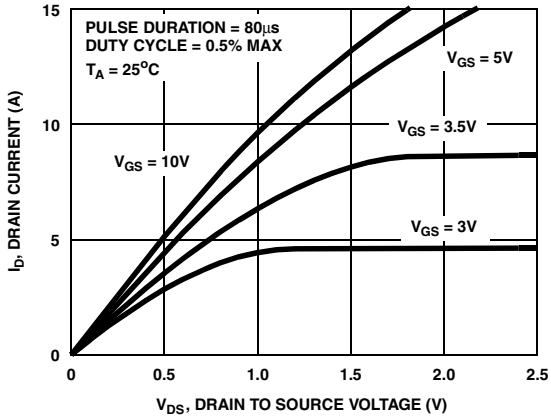


Figure 8. Saturation Characteristics

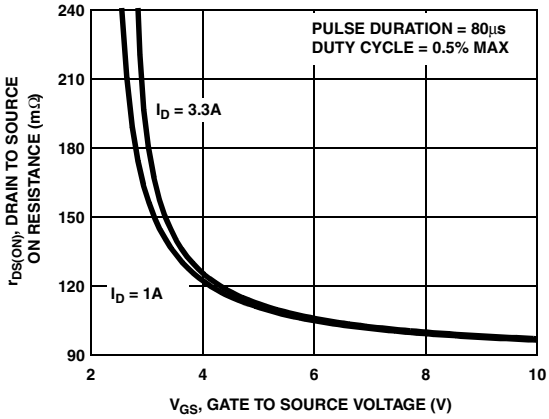


Figure 9. Drain to Source On Resistance vs Gate Voltage and Drain Current

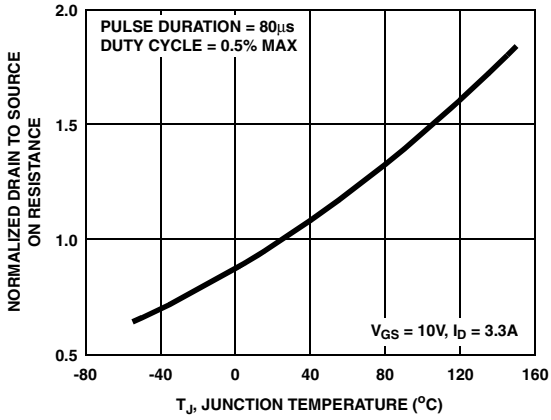


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics (Continued) T_A = 25°C unless otherwise noted

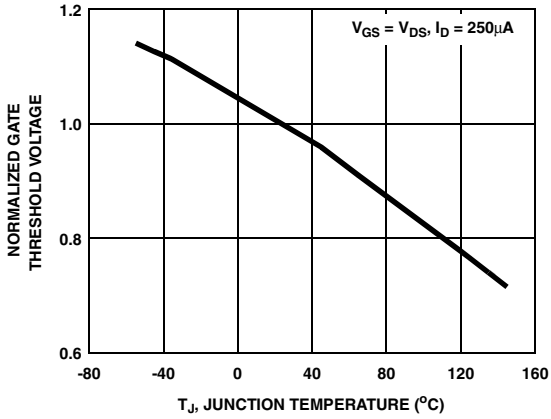


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

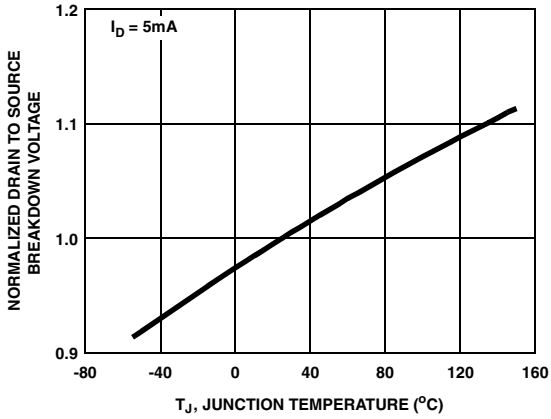


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

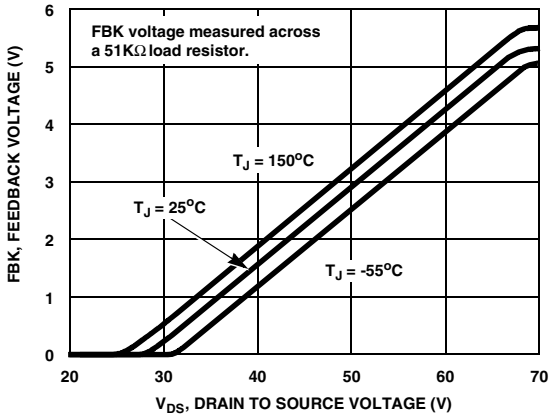


Figure 13. Feedback Voltage vs Drain to Source Voltage

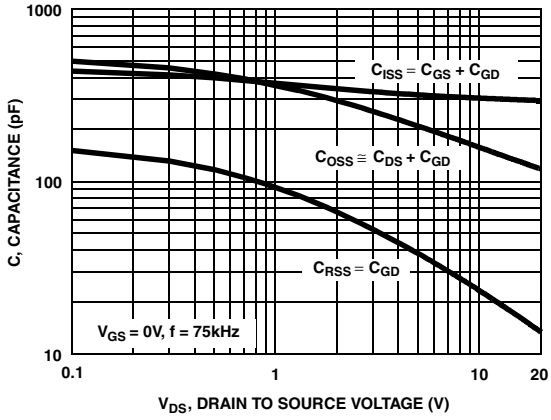


Figure 14. Capacitance vs Drain to Source Voltage

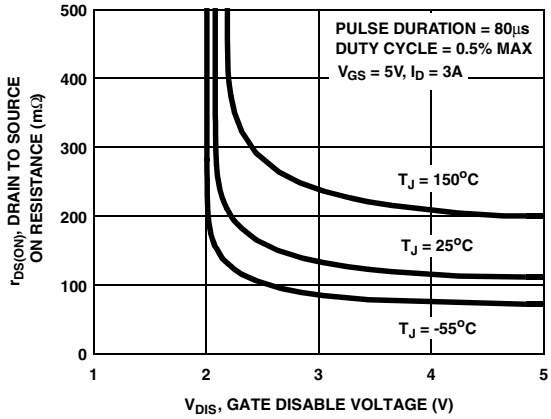


Figure 15. Drain to Source On Resistance vs Gate Disable Voltage

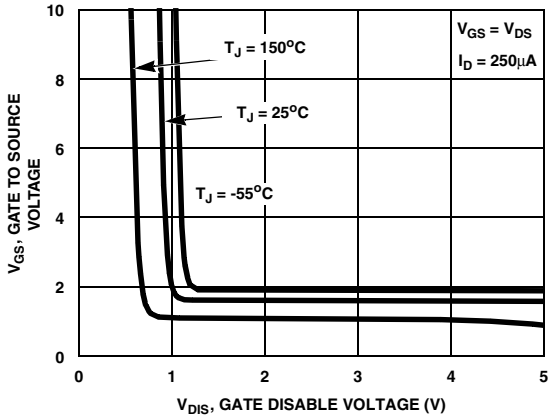


Figure 16. Gate to Source Voltage vs Gate Disable Voltage

Typical Characteristics (Continued) T_A = 25°C unless otherwise noted

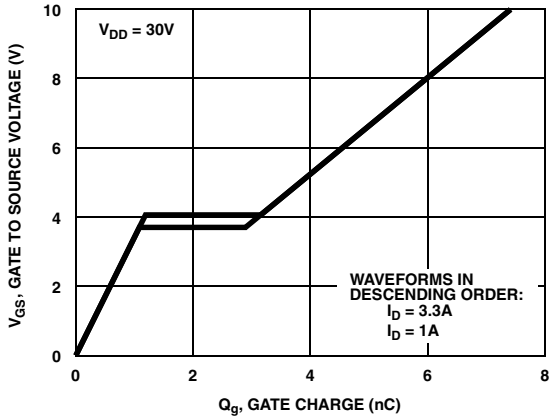


Figure 17. Gate Charge Waveforms for Constant Gate Currents

Test Circuits and Waveforms

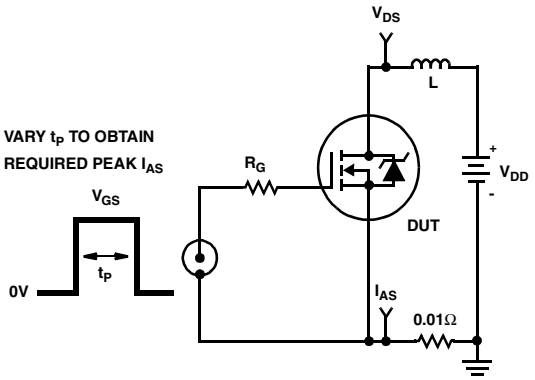


Figure 18. Unclamped Energy Test Circuit

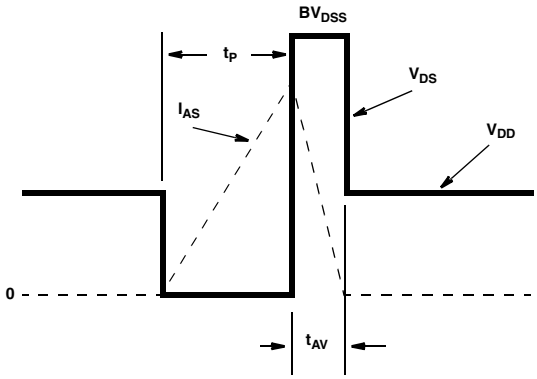


Figure 19. Unclamped Energy Waveforms

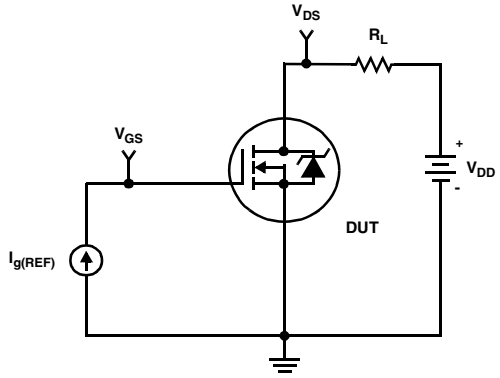


Figure 20. Gate Charge Test Circuit

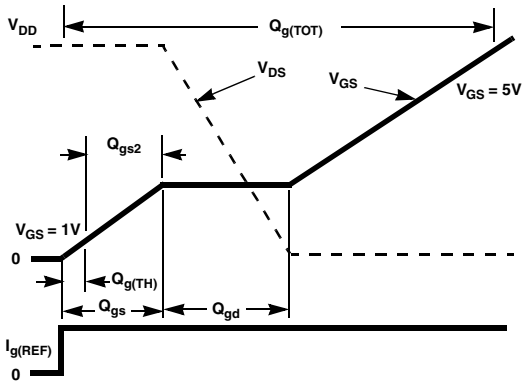


Figure 21. Gate Charge Waveforms

Test Circuits and Waveforms (Continued)

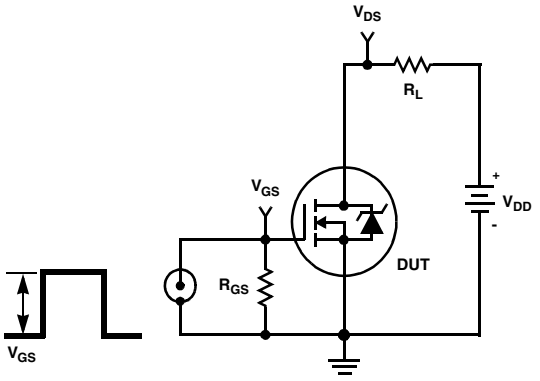


Figure 22. Switching Time Test Circuit

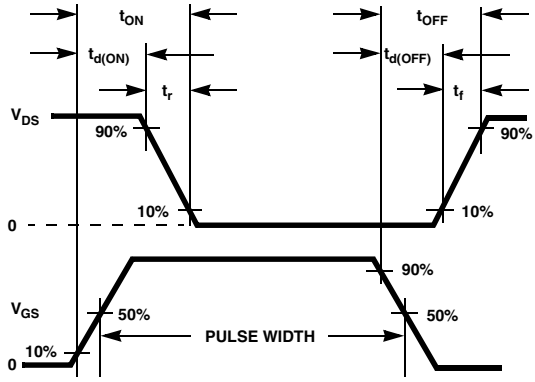


Figure 23. Switching Time Waveforms

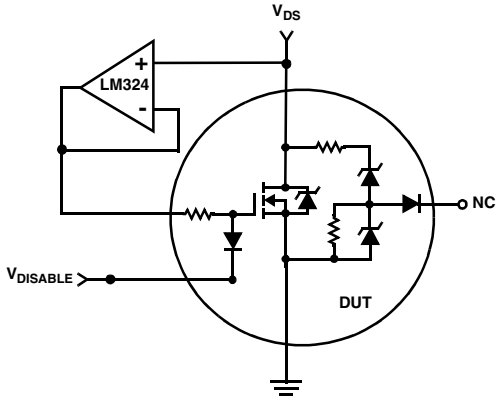


Figure 24. Gate to Source Voltage vs Gate Disable Voltage

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM}, and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM}, in an application. Therefore the application's ambient temperature, T_A (^oC), and thermal resistance $R_{\theta JA}$ ($^oC/W$) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \quad \text{(EQ. 1)}$$

In using surface mount devices such as the SO8 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 25 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 25 or by calculation using Equation 2. The area, in square inches is the top copper area including the gate and source pads.

$$R_{\theta JA} = 79.9 + \frac{15}{0.14 + Area} \quad \text{(EQ. 2)}$$

The transient thermal impedance ($Z_{\theta JA}$) is also effected by varied top copper board area. Figure 26 shows the effect of copper pad area on single pulse transient thermal impedance. Each trace represents a copper pad area in square inches corresponding to the descending list in the graph. Spice and SABER thermal models are provided for each of the listed pad areas.

Copper pad area has no perceivable effect on transient thermal impedance for pulse widths less than 100ms. For pulse widths less than 100ms the transient thermal impedance is determined by the die and package. Therefore, CTHERM1 through CTHERM5 and RTHERM1 through RTHERM5 remain constant for each of the thermal models. A listing of the model component values is available in Table 1.

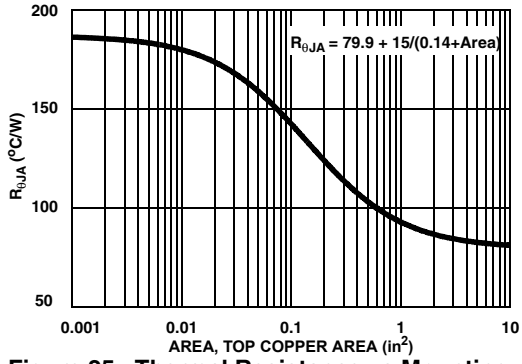


Figure 25. Thermal Resistance vs Mounting Pad Area

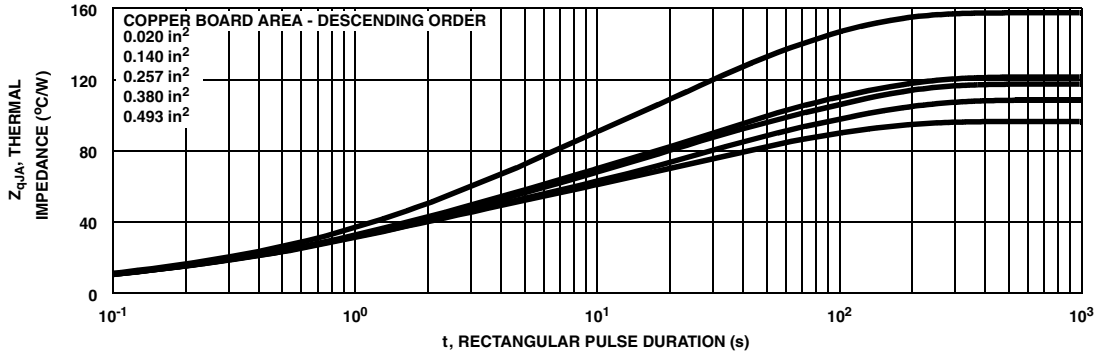
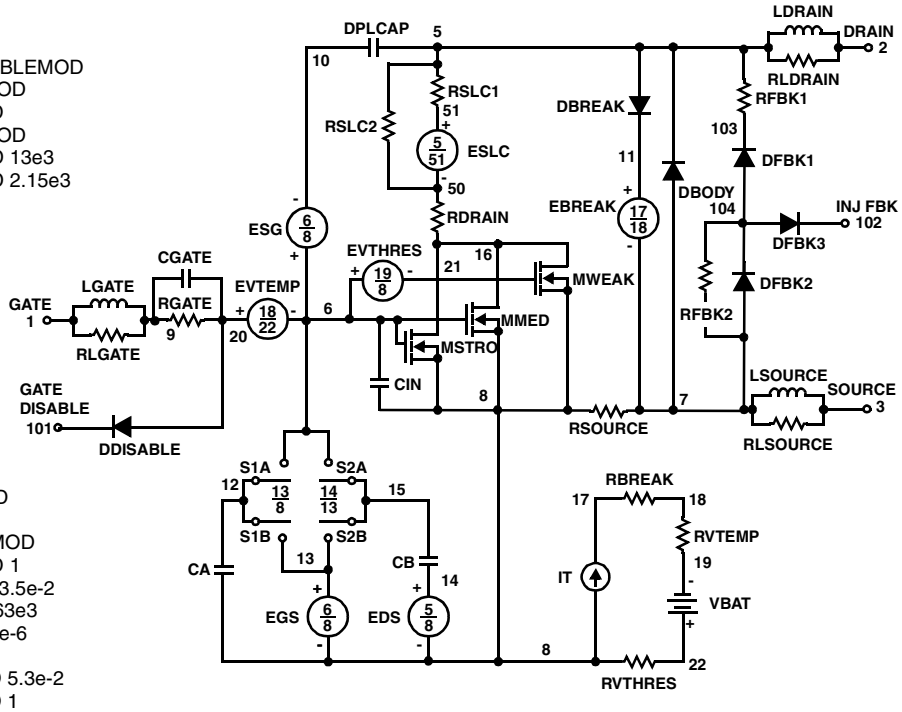


Figure 26. Thermal Impedance vs Mounting Pad Area

PSPICE Electrical Model

```
.SUBCKT FDSS2407  2 1 3 101 102      ;      rev July 2004
Ca 12 8 1e-10
Cb 15 14 4e-10
Cin 6 8 2.8e-10
Dbody 7 5 DbodyMOD
Dbreak 5 11 DbreakMOD
Dplcap 10 5 DplcapMOD
CGATE 9 20 5e-9
DDISABLE 20 101 DDISABLEMOD
DFBK1 104 103 DFBK1MOD
DFBK2 7 104 DFBK2MOD
DFBK3 104 102 DFBK3MOD
RFBK1 5 103 RFBK1MOD 13e3
RFBK2 104 7 RFBK2MOD 2.15e3
Ebreak 11 7 17 18 67.4
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Evthres 6 21 19 8 1
Evtemp 20 6 18 22 1
It 8 17 1
Lgate 1 9 1.8e-9
Ldrain 2 5 1.0e-9
Lsource 3 7 0.6e-9
RLgate 1 9 18
RLdrain 2 5 10
RLsource 3 7 6
Mmed 16 6 8 8 MmedMOD
Mstro 16 6 8 8 MstroMOD
Mweak 16 21 8 8 MweakMOD
Rbreak 17 18 RbreakMOD 1
Rdrain 50 16 RdrainMOD 3.5e-2
Rgate 9 20 RgateMOD 8.63e3
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
Rsource 8 7 RsourceMOD 5.3e-2
Rvthres 22 8 RvthresMOD 1
Rvtemp 18 19 RvtempMOD 1
S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD
Vbat 22 19 DC 1
ESLC 51 50  VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*20),3.5))}
.MODEL DbodyMOD D (IS=1.1E-12 N=1.05 IKF=4e-1 RS=4.2e-2 TRS1=3e-4 TRS2=1.3e-6
+ CJO=3.3e-10 TT=3e-8 M=0.38, XTI=3.5)
.MODEL DbreakMOD D (RS=1 TRS1=1e-3 TRS2=-9e-6)
.MODEL DplcapMOD D (CJO=1.97e-10 IS=1e-30 N=10 M=0.84)
.MODEL DDISABLEMOD D (RS=30 IS=1e-15 BV=4.7 TBV1=-3e-4 TBV2=-3e-6 XTI=0)
.MODEL DFBK1MOD D (IS=1e-15 BV=23.8 IKF=2 TBV1=-6e-4 TBV2=6e-6)
.MODEL DFBK2MOD D (RS=1 IS=1e-30 BV=5.6 N=3.3 NBV=1)
.MODEL DFBK3MOD D (RS=1 IS=1e-15 BV=4.2 NBV=2.5)
.MODEL MmedMOD NMOS (VTO=1.7 KP=1.08 IS=1e-30 N=10 TOX=1 L=1u W=1u RG= 8.56e3)
.MODEL MstroMOD NMOS (VTO=2 KP=14 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL MweakMOD NMOS (VTO=1.5 kp=0.04 IS=1e-30 N=10 TOX=1 L=1u W=1u RG= 8.56e4 RS=0.1)
.MODEL RbreakMOD RES (TC1=1.05e-3 TC2=-9e-7)
.MODEL RdrainMOD RES (TC1=9e-3 TC2=2.7e-5)
.MODEL RSLCMOD RES (TC1=2e-3 TC2=6e-6)
.MODEL RsourceMOD RES (TC1=3e-3 TC2=1e-6)
.MODEL RvthresMOD RES (TC1=-1.1e-3 TC2=-3.3e-6)
.MODEL RvtempMOD RES (TC1=-1.6e-3 TC2=1e-7)
.MODEL RFBK1MOD RES (TC1=-1.4e-3 TC2=1e-6)
.MODEL RFBK2MOD RES (TC1=-1.4e-3 TC2=1e-6)
.MODEL RgateMOD RES (TC1=-1.4e-3 TC2=1e-5)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4.0 VOFF=-3.0)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3.0 VOFF=-4.0)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1.0 VOFF=-0.5)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.5 VOFF=-1.0)
.ENDS
```



Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SABER Electrical Model

```
REV July 2004
template FDSS2407 n2,n1,n3,n101,n102
electrical n2,n1,n3,n101,n102
{
var i iscl
dp..model dbodymod = (isl=1.1e-12,nl=1.05,ikf=4e-1,rs=4.2e-2,trs1=3e-4,trs2=1.3e-6,cjo=3.3e-10,tt=3e-8,m=0.38,xti=3.5)
dp..model dbreakmod = (rs=1,trs1=1e-3,trs2=-9e-6)
dp..model ddisablemod = (rs=30, isl=1e-15,bv=4.7,tbv1=-3e-4,tbv2=-3e-6,xti=0)
dp..model dfbk1mod = (isl=1e-15,bv=23.8,ikf=2,tbv1=-6e-4,tbv2=6e-6)
dp..model dfbk2mod = (rs=1,isl=1e-30,bv=5.6,nl=3.3,nbv=1)
dp..model dfbk3mod = (rs=1,isl=1e-15,bv=4.2,nbv=2.5)
dp..model dplcapmod = (cjo=1.97e-10,isl=10e-30,nl=10,m=0.84)

m..model mmedmod = (type=_n,vto=1.7,kp=1.08,is=1e-30,tox=1)
m..model mstrongmod = (type=_n,vto=2,kp=14,is=1e-30,tox=1)
m..model mweakmod = (type=_n,vto=1.5,kp=0.04,is=1e-30, tox=1,rs=0.1)
m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

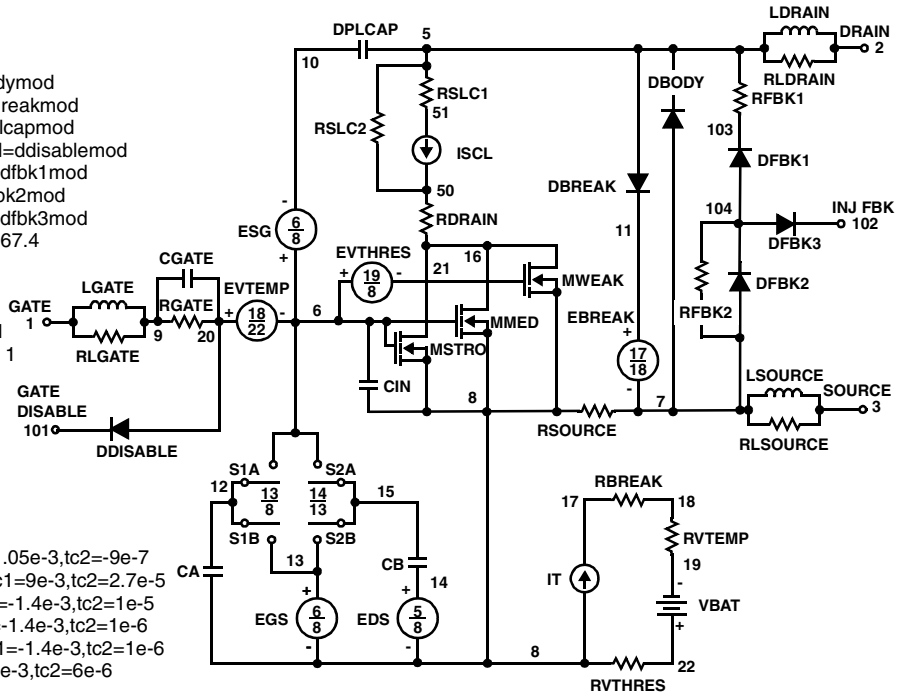
sw_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-4.0,voff=-3.0)
sw_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-3.0,voff=-4.0)
sw_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-1.0,voff=-0.5)
sw_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=-0.5,voff=-1.0)

c.ca n12 n8 = 1e-10
c.cb n15 n14 = 4e-10
c.cin n6 n8 = 2.8e-10
c.cgate n9 n20 = 5e-9

dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod
dp.ddisable n20 n101 = model=ddisablemod
dp.dfbk1 n104 n103 = model=dfbk1mod
dp.dfbk2 n7 n104 = model=dfbk2mod
dp.dfbk3 n104 n102 = model=dfbk3mod
spe.ebreak n11 n7 n17 n18 = 67.4
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evthres n6 n21 n19 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1

i.it n8 n17 = 1
l.lgate n1 n9 = 1.8e-9
l.ldrain n2 n5 = 1.0e-9
l.lsource n3 n7 = 0.6e-9
res.rlgate n1 n9 = 18
res.rldrain n2 n5 = 10
res.rlsource n3 n7 = 6
res.rbreak n17 n18 = 1, tc1=1.05e-3,tc2=-9e-7
res.rdrain n50 n16 = 3.5e-2,tc1=9e-3,tc2=2.7e-5
res.rgate n9 n20 = 8.63e3,tc1=-1.4e-3,tc2=1e-5
res.rfbk1 n5 n103 = 13e3,tc1=-1.4e-3,tc2=1e-6
res.rfbk2 n104 n7 = 2.15e3,tc1=-1.4e-3,tc2=1e-6
res.rslc1 n5 n51 = 1e-6,tc1=2e-3,tc2=6e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 5.3e-2,tc1=3e-3,tc2=1e-6
res.rvthres n22 n8 = 1,tc1=-1.1e-3,tc2=-3.3e-6
res.rvtemp n18 n19 = 1,tc1=-1.6e-3,tc2=1e-7

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod
v.vbat n22 n19 = dc=1
equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/20))** 3.5))
}
}
```



SPICE Thermal Model

REV July 2004
FDSS2407T
Copper Area =0.5 in^2

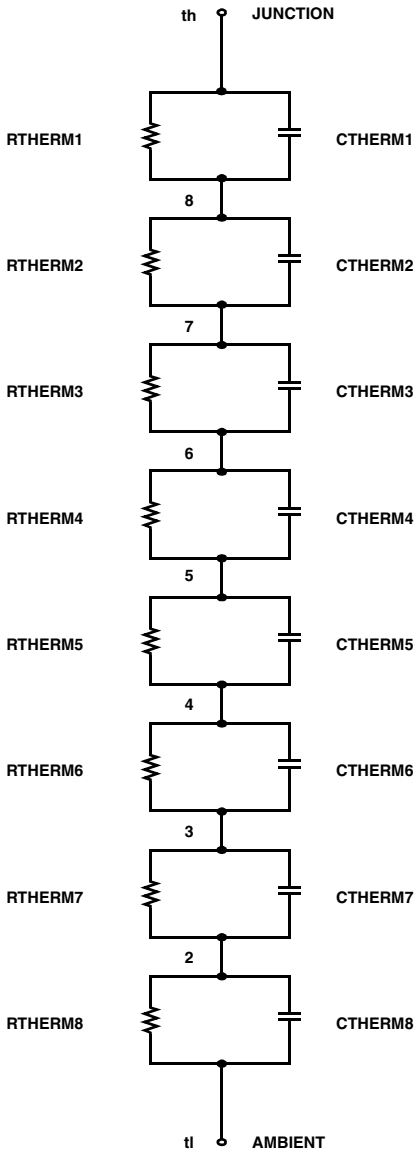
CTHERM1 Junction c2 1.2e-4
CTHERM2 c2 c3 2e-3
CTHERM3 c3 c4 2e-2
CTHERM4 c4 c5 3.0e-2
CTHERM5 c5 c6 4e-2
CTHERM6 c6 c7 7e-2
CTHERM7 c7 c8 2e-1
CTHERM8 c8 Ambient 2.8

RTHERM1 Junction c2 1.4
RTHERM2 c2 c3 2.0
RTHERM3 c3 c4 2.8
RTHERM4 c4 c5 9.0
RTHERM5 c5 c6 18.0
RTHERM6 c6 c7 26.0
RTHERM7 c7 c8 28.0
RTHERM8 c8 Ambient 29.0

SABER Thermal Model

Copper Area = 0.5 in^2
template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th c2 =1.2e-4
ctherm.ctherm2 c2 c3 =2e-3
ctherm.ctherm3 c3 c4 =2e-2
ctherm.ctherm4 c4 c5 =3.0e-2
ctherm.ctherm5 c5 c6 =4e-2
ctherm.ctherm6 c6 c7 =7e-2
ctherm.ctherm7 c7 c8 =2e-1
ctherm.ctherm8 c8 tl =2.8

rtherm.rtherm1 th c2 =1.4
rtherm.rtherm2 c2 c3 =2.0
rtherm.rtherm3 c3 c4 =2.8
rtherm.rtherm4 c4 c5 =9.0
rtherm.rtherm5 c5 c6 =18.0
rtherm.rtherm6 c6 c7 =26.0
rtherm.rtherm7 c7 c8 =28.0
rtherm.rtherm8 c8 tl =29.0
}



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EnSigna™	I^2C™	MSX™	Quiet Series™	TruTranslation™
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		OCX™	RapidConnect™	UltraFET®
Across the board. Around the world.™		OCXPro™	µSerDes™	UniFET™
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Rev. I15

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