NXP Semiconductors
Data Sheet: Technical Data

Document Number: MPC5777C
Rev. 14, 01/2020

MPC5777C

MPC5777C Microcontroller Data Sheet

Features

- This document provides electrical specifications, pin assignments, and package diagram information for the MPC5777C series of microcontroller units (MCUs).
- For functional characteristics and the programming model, see the MPC5777C Reference Manual.

Table of Contents

1 Introduction

1.1 Features summary

On-chip modules available within the family include the following features:

- Three dual issue, 32-bit CPU core complexes (e200z7), two of which run in lockstep
  - Power Architecture embedded specification compliance
  - Instruction set enhancement allowing variable length encoding (VLE), optional encoding of mixed 16-bit and 32-bit instructions, for code size footprint reduction
  - On the two computational cores: Signal processing extension (SPE1.1) instruction support for digital signal processing (DSP)
  - Single-precision floating point operations
  - On the two computational cores: 16 KB I-Cache and 16 KB D-Cache
  - Hardware cache coherency between cores
- 16 hardware semaphores
- 3-channel CRC module
- 8 MB on-chip flash memory
  - Supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
- 512 KB on-chip general-purpose SRAM including 64 KB standby RAM
- Two multichannel direct memory access controllers (eDMA)
  - 64 channels per eDMA
- Dual core Interrupt Controller (INTC)
- Dual phase-locked loops (PLLs) with stable clock domain for peripherals and frequency modulation (FM) domain for computational shell
- Crossbar Switch architecture for concurrent access to peripherals, flash memory, or RAM from multiple bus masters with End-To-End ECC
- External Bus Interface (EBI) for calibration and application use
- System Integration Unit (SIU)
- Error Injection Module (EIM) and Error Reporting Module (ERM)
- Four protected port output (PPO) pins
- Boot Assist Module (BAM) supports serial bootload via CAN or SCI
- Three second-generation Enhanced Time Processor Units (eTPUs)
  - 32 channels per eTPU
  - Total of 36 KB code RAM
  - Total of 9 KB parameter RAM

- Enhanced Modular Input/Output System (eMIOS) supporting 32 unified channels with each channel capable of single action, double action, pulse width modulation (PWM) and modulus counter operation
- Two Enhanced Queued Analog-to-Digital Converter (eQADC) modules with:
  - Two separate analog converters per eQADC module
  - Support for a total of 70 analog input pins, expandable to 182 inputs with off-chip multiplexers
  - Interface to twelve hardware Decimation Filters
  - Enhanced "Tap" command to route any conversion to two separate Decimation Filters
- Four independent 16-bit Sigma-Delta ADCs (SDADCs)
- 10-channel Reaction Module
- Ethernet (FEC)
- Two PSI5 modules
- Two SENT Receiver (SRX) modules supporting 12 channels
- Zipwire: SIPI and LFAST modules
- Five Deserial Serial Peripheral Interface (DSPI) modules
- Five Enhanced Serial Communication Interface (eSCI) modules
- Four Controller Area Network (FlexCAN) modules
- Two M_CAN modules that support FD
- Fault Collection and Control Unit (FCCU)
- Clock Monitor Units (CMUs)
- Tamper Detection Module (TDM)
- Cryptographic Services Engine (CSE)
  - Complies with *Secure Hardware Extension (SHE) Functional Specification Version 1.1* security functions
  - Includes software selectable enhancement to key usage flag for MAC verification and increase in number of memory slots for security keys
- PASS module to support security features
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard, with some support for 2010 standard
- Device and board test support per Joint Test Action Group (JTAG) IEEE 1149.1 and 1149.7
- On-chip voltage regulator controller (VRC) that derives the core logic supply voltage from the high-voltage supply
- On-chip voltage regulator for flash memory
- Self Test capability

1.2 Block diagram

The following figure shows a top-level block diagram of the MPC5777C. The purpose of the block diagram is to show the general interconnection of functional modules through the crossbar switch.

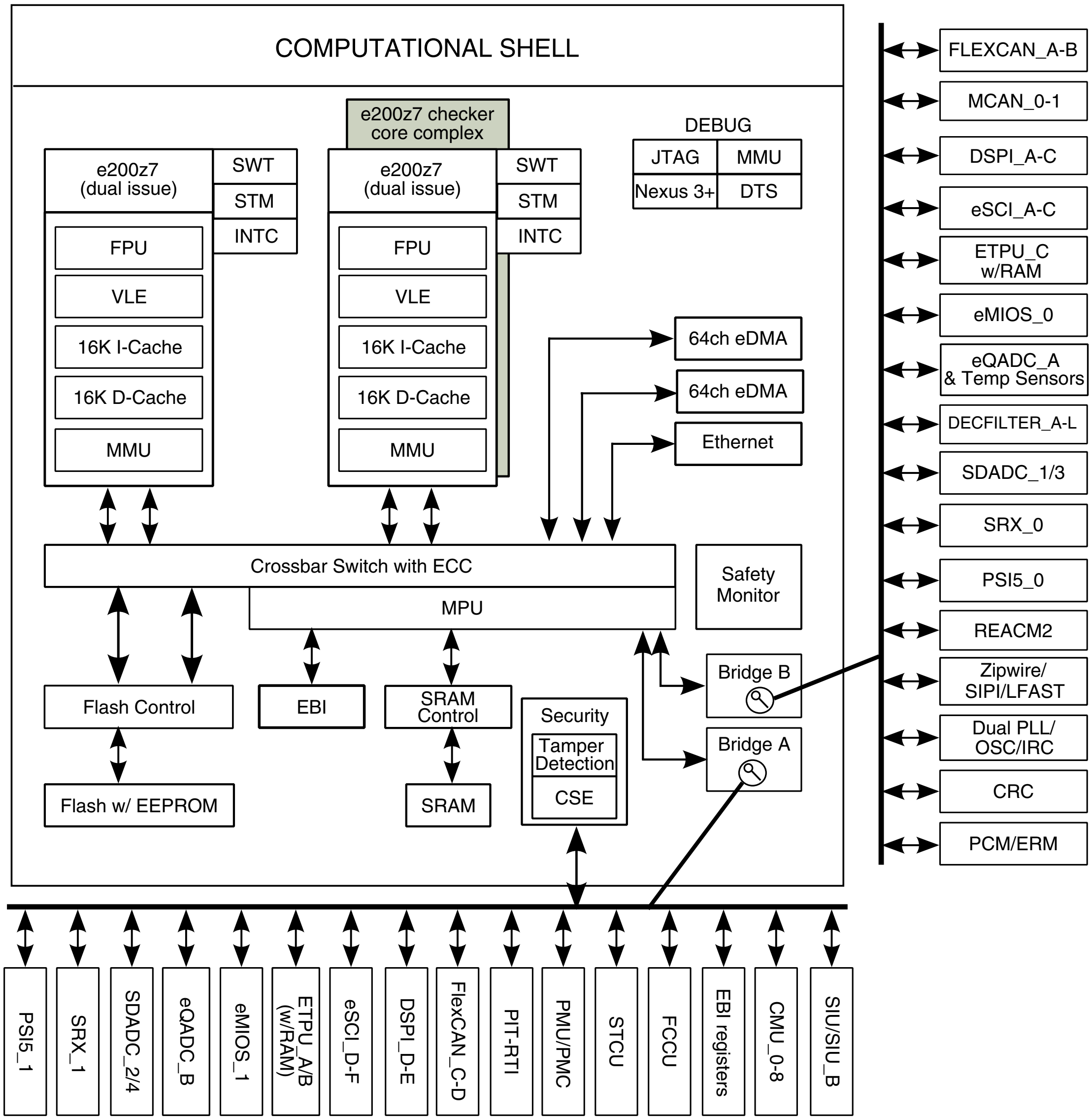
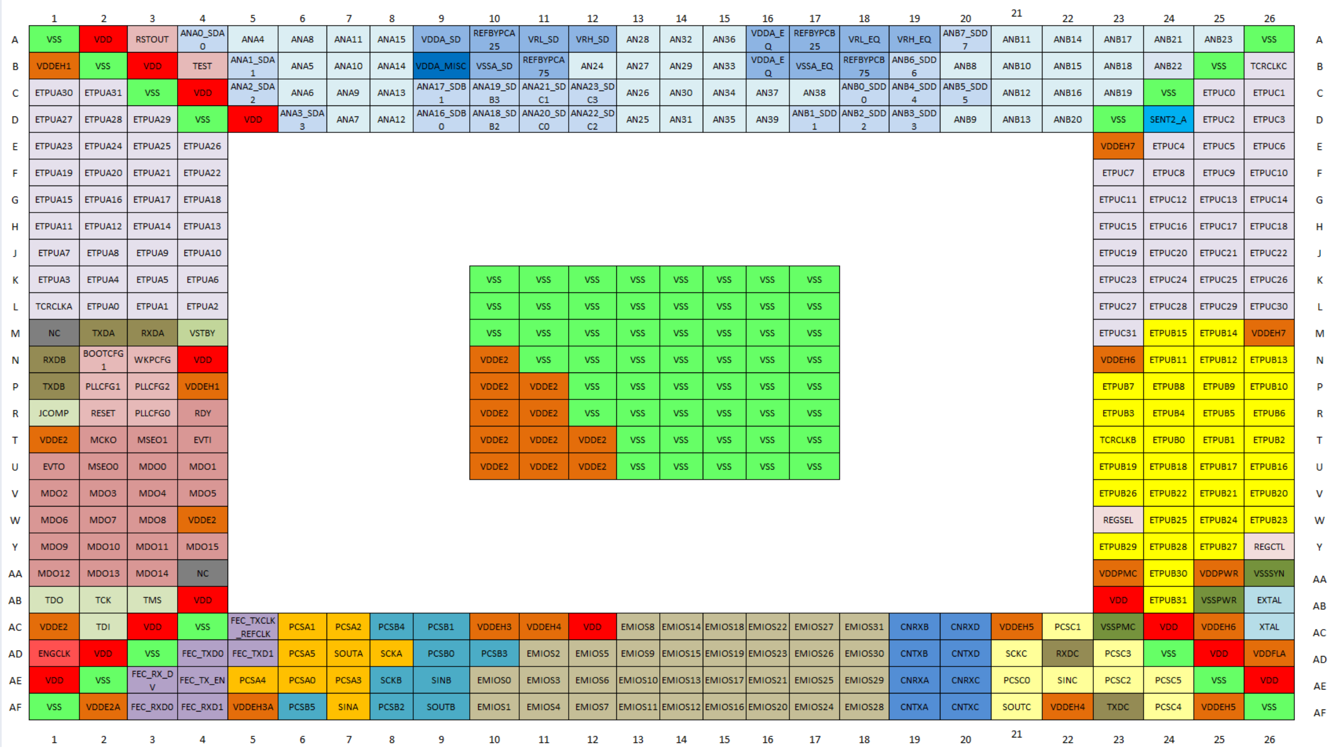


Figure 1. MPC5777C block diagram

2 Pinouts

2.1 416-ball MAPBGA pin assignments

Figure 2 shows the 416-ball MAPBGA pin assignments.

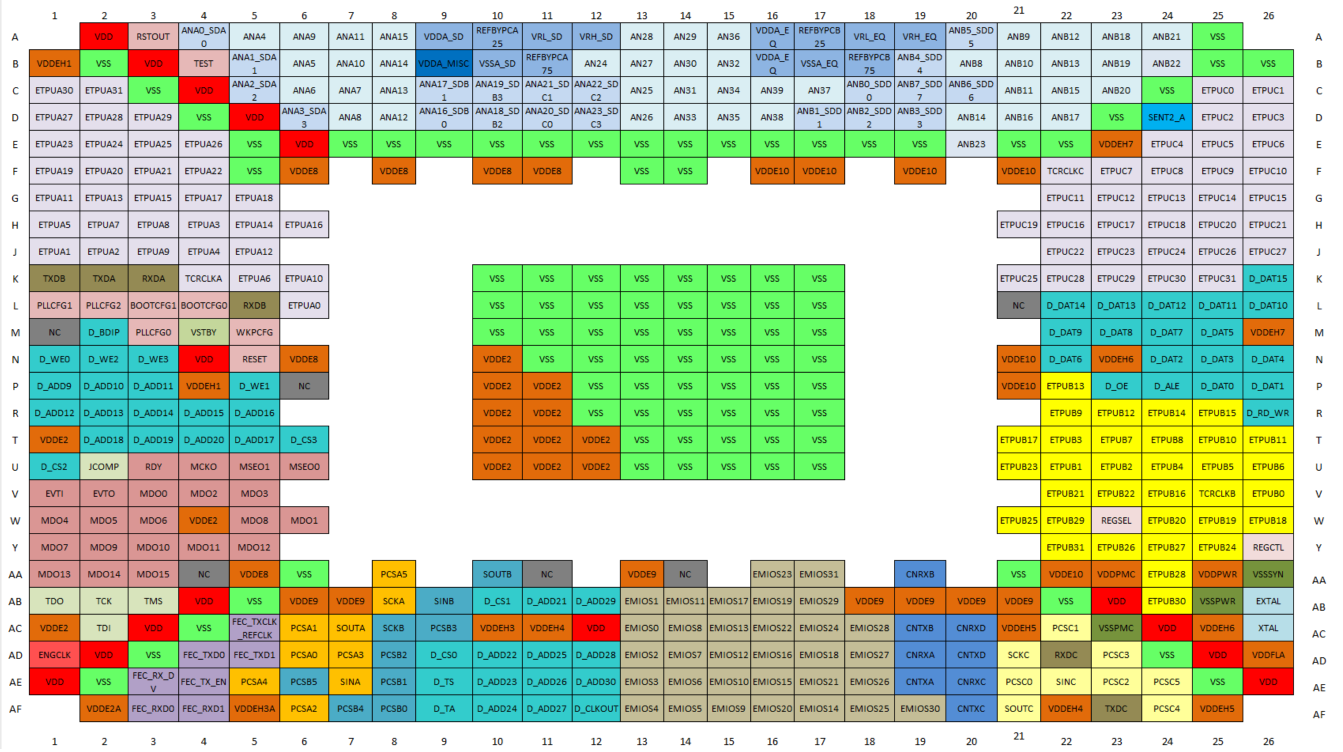


	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	VSS	VDD	RSTOUT	ANA0_SDA0	ANA4	ANA8	ANA11	ANA15	VDDA_SD	REFBYPCA25	VRL_SD	VRH_SD	AN28	AN32	AN36	VDDA_EQ	REFBYPCB25	VRL_EQ	VRH_EQ	ANB7_SDD7	ANB11	ANB14	ANB17	ANB21	ANB23	VSS	A
B	VDDEH1	VSS	VDD	TEST	ANA1_SDA1	ANA5	ANA10	ANA14	VDDA_MISC	VSSA_SD	REFBYPCA75	AN24	AN27	AN29	AN33	VDDA_EQ	VSSA_EQ	REFBYPCB75	ANB6_SDD6	ANB8	ANB10	ANB15	ANB18	ANB22	VSS	TCRCLKC	B
C	ETPUA30	ETPUA31	VSS	VDD	ANA2_SDA2	ANA6	ANA9	ANA13	ANA17_SDB1	ANA19_SDB3	ANA21_SDC1	ANA23_SDC3	AN26	AN30	AN34	AN37	AN38	ANB0_SDD0	ANB4_SDD4	ANB5_SDD5	ANB12	ANB16	ANB19	VSS	ETPUC0	ETPUC1	C
D	ETPUA27	ETPUA28	ETPUA29	VSS	VDD	ANA3_SDA3	ANA7	ANA12	ANA16_SDB0	ANA18_SDB2	ANA20_SDC0	ANA22_SDC2	AN25	AN31	AN35	AN39	ANB1_SDD1	ANB2_SDD2	ANB3_SDD3	ANB9	ANB13	ANB20	VSS	SENT2_A	ETPUC2	ETPUC3	D
E	ETPUA23	ETPUA24	ETPUA25	ETPUA26																			VDDEH7	ETPUC4	ETPUC5	ETPUC6	E
F	ETPUA19	ETPUA20	ETPUA21	ETPUA22																			ETPUC7	ETPUC8	ETPUC9	ETPUC10	F
G	ETPUA15	ETPUA16	ETPUA17	ETPUA18																			ETPUC11	ETPUC12	ETPUC13	ETPUC14	G
H	ETPUA11	ETPUA12	ETPUA14	ETPUA13																			ETPUC15	ETPUC16	ETPUC17	ETPUC18	H
J	ETPUA7	ETPUA8	ETPUA9	ETPUA10																			ETPUC19	ETPUC20	ETPUC21	ETPUC22	J
K	ETPUA3	ETPUA4	ETPUA5	ETPUA6						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS						ETPUC23	ETPUC24	ETPUC25	ETPUC26	K
L	TCRCLKA	ETPUA0	ETPUA1	ETPUA2						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS						ETPUC27	ETPUC28	ETPUC29	ETPUC30	L
M	NC	TXDA	RXDA	VSTBY						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS						ETPUC31	ETPUB15	ETPUB14	VDDEH7	M
N	RXDB	BOOTCFG1	WKPCFG	VDD						VDDE2	VSS	VSS	VSS	VSS	VSS	VSS	VSS						VDDEH6	ETPUB11	ETPUB12	ETPUB13	N
P	TXDB	PLLCFG1	PLLCFG2	VDDEH1						VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS						ETPUB7	ETPUB8	ETPUB9	ETPUB10	P
R	JCOMP	RESET	PLLCFG0	RDY						VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS						ETPUB3	ETPUB4	ETPUB5	ETPUB6	R
T	VDDE2	MCKO	MSEO1	EVTI						VDDE2	VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS						TCRCLKB	ETPUB0	ETPUB1	ETPUB2	T
U	EVTO	MSEO0	MDO0	MDO1						VDDE2	VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS						ETPUB19	ETPUB18	ETPUB17	ETPUB16	U
V	MDO2	MDO3	MDO4	MDO5																			ETPUB26	ETPUB22	ETPUB21	ETPUB20	V
W	MDO6	MDO7	MDO8	VDDE2																			REGSEL	ETPUB25	ETPUB24	ETPUB23	W
Y	MDO9	MDO10	MDO11	MDO15																			ETPUB29	ETPUB28	ETPUB27	REGCTL	Y
AA	MDO12	MDO13	MDO14	NC																			VDDPMC	ETPUB30	VDDPWR	VSSSYN	AA
AB	TDO	TCK	TMS	VDD																			VDD	ETPUB31	VSSPWR	EXTAL	AB
AC	VDDE2	TDI	VDD	VSS	FEC_TXCLK_REFCLK	PCSA1	PCSA2	PCSB4	PCSB1	VDDEH3	VDDEH4	VDD	EMIOS8	EMIOS14	EMIOS18	EMIOS22	EMIOS27	EMIOS31	CNRXB	CNRXD	VDDEH5	PCSC1	VSSPMC	VDD	VDDEH6	XTAL	AC
AD	ENGCLK	VDD	VSS	FEC_TXD0	FEC_TXD1	PCSA5	SOUTA	SCKA	PCSB0	PCSB3	EMIOS2	EMIOS5	EMIOS9	EMIOS15	EMIOS19	EMIOS23	EMIOS26	EMIOS30	CNTXB	CNTXD	SCKC	RXDC	PCSC3	VSS	VDD	VDDFLA	AD
AE	VDD	VSS	FEC_RX_DV	FEC_TX_EN	PCSA4	PCSA0	PCSA3	SCKB	SINB	EMIOS0	EMIOS3	EMIOS6	EMIOS10	EMIOS13	EMIOS17	EMIOS21	EMIOS25	EMIOS29	CNRXA	CNRXC	PCSC0	SINC	PCSC2	PCSC5	VSS	VDD	AE
AF	VSS	VDDE2A	FEC_RXD0	FEC_RXD1	VDDEH3A	PCSB5	SINA	PCSB2	SOUTB	EMIOS1	EMIOS4	EMIOS7	EMIOS11	EMIOS12	EMIOS16	EMIOS20	EMIOS24	EMIOS28	CNTXA	CNTXC	SOUTC	VDDEH4	TXDC	PCSC4	VDDEH5	VSS	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 2. MPC5777C 416-ball MAPBGA (full diagram)

2.2 516-ball MAPBGA pin assignments

Figure 3 shows the 516-ball MAPBGA pin assignments.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A		VDD	RSTOUT	ANA0_SDA0	ANA4	ANA9	ANA11	ANA15	VDDA_SD	REFBYPCA25	VRL_SD	VRH_SD	AN28	AN29	AN36	VDDA_EQ	REFBYPCB25	VRL_EQ	VRH_EQ	ANB5_SDD5	ANB9	ANB12	ANB18	ANB21	VSS		A
B	VDDEH1	VSS	VDD	TEST	ANA1_SDA1	ANA5	ANA10	ANA14	VDDA_MISC	VSSA_SD	REFBYPCA75	AN24	AN27	AN30	AN32	VDDA_EQ	VSSA_EQ	REFBYPCB75	ANB4_SDD4	ANB8	ANB10	ANB13	ANB19	ANB22	VSS	VSS	B
C	ETPUA30	ETPUA31	VSS	VDD	ANA2_SDA2	ANA6	ANA7	ANA13	ANA17_SDB1	ANA19_SDB3	ANA21_SDC1	ANA22_SDC2	AN25	AN31	AN34	AN39	AN37	ANB0_SDD0	ANB7_SDD7	ANB6_SDD6	ANB11	ANB15	ANB20	VSS	ETPUC0	ETPUC1	C
D	ETPUA27	ETPUA28	ETPUA29	VSS	VDD	ANA3_SDA3	ANA8	ANA12	ANA16_SDB0	ANA18_SDB2	ANA20_SDC0	ANA23_SDC3	AN26	AN33	AN35	AN38	ANB1_SDD1	ANB2_SDD2	ANB3_SDD3	ANB14	ANB16	ANB17	VSS	SENT2_A	ETPUC2	ETPUC3	D
E	ETPUA23	ETPUA24	ETPUA25	ETPUA26	VSS	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	ANB23	VSS	VSS	VDDEH7	ETPUC4	ETPUC5	ETPUC6	E
F	ETPUA19	ETPUA20	ETPUA21	ETPUA22	VSS	VDDE8		VDDE8		VDDE8	VDDE8		VSS	VSS		VDDE10	VDDE10		VDDE10		VDDE10	TCRCLKC	ETPUC7	ETPUC8	ETPUC9	ETPUC10	F
G	ETPUA11	ETPUA13	ETPUA15	ETPUA17	ETPUA18																	ETPUC11	ETPUC12	ETPUC13	ETPUC14	ETPUC15	G
H	ETPUA5	ETPUA7	ETPUA8	ETPUA3	ETPUA14	ETPUA16															ETPUC19	ETPUC16	ETPUC17	ETPUC18	ETPUC20	ETPUC21	H
J	ETPUA1	ETPUA2	ETPUA9	ETPUA4	ETPUA12																	ETPUC22	ETPUC23	ETPUC24	ETPUC26	ETPUC27	J
K	TXDB	TXDA	RXDA	TCRCLKA	ETPUA6	ETPUA10				VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS				ETPUC25	ETPUC28	ETPUC29	ETPUC30	ETPUC31	D_DAT15	K
L	PLLCFG1	PLLCFG2	BOOTCFG1	BOOTCFG0	RXDB	ETPUA0				VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS				NC	D_DAT14	D_DAT13	D_DAT12	D_DAT11	D_DAT10	L
M	NC	D_BDIP	PLLCFG0	VSTBY	WKPCFG					VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS					D_DAT9	D_DAT8	D_DAT7	D_DAT5	VDDEH7	M
N	D_WE0	D_WE2	D_WE3	VDD	RESET	VDDE8				VDDE2	VSS	VSS	VSS	VSS	VSS	VSS	VSS				VDDE10	D_DAT6	VDDEH6	D_DAT2	D_DAT3	D_DAT4	N
P	D_ADD9	D_ADD10	D_ADD11	VDDEH1	D_WE1	NC				VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS				VDDE10	ETPUB13	D_OE	D_ALE	D_DAT0	D_DAT1	P
R	D_ADD12	D_ADD13	D_ADD14	D_ADD15	D_ADD16					VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS					ETPUB9	ETPUB12	ETPUB14	ETPUB15	D_RD_WR	R
T	VDDE2	D_ADD18	D_ADD19	D_ADD20	D_ADD17	D_CS3				VDDE2	VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS				ETPUB17	ETPUB3	ETPUB7	ETPUB8	ETPUB10	ETPUB11	T
U	D_CS2	JCOMP	RDY	MCKO	MSEO1	MSEO0				VDDE2	VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS				ETPUB23	ETPUB1	ETPUB2	ETPUB4	ETPUB5	ETPUB6	U
V	EVTI	EVTO	MDO0	MDO2	MDO3																	ETPUB21	ETPUB22	ETPUB16	TCRCLKB	ETPUB0	V
W	MDO4	MDO5	MDO6	VDDE2	MDO8	MDO1															ETPUB25	ETPUB29	REGSEL	ETPUB20	ETPUB19	ETPUB18	W
Y	MDO7	MDO9	MDO10	MDO11	MDO12																	ETPUB31	ETPUB26	ETPUB27	ETPUB24	REGCTL	Y
AA	MDO13	MDO14	MDO15	NC	VDDE8	VSS		PCSA5		SOUTB	NC		VDDE9	NC		EMIOS23	EMIOS31		CNRXB		VSS	VDDE10	VDDPMC	ETPUB28	VDDPWR	VSSSYN	AA
AB	TDO	TCK	TMS	VDD	VSS	VDDE9	VDDE9	SCKA	SINB	D_CS1	D_ADD21	D_ADD29	EMIOS1	EMIOS11	EMIOS17	EMIOS19	EMIOS29	VDDE9	VDDE9	VDDE9	VDDE9	VSS	VDD	ETPUB30	VSSPWR	EXTAL	AB
AC	VDDE2	TDI	VDD	VSS	FEC_TXCLK_REFCLK	PCSA1	SOUTA	SCKB	PCSB3	VDDEH3	VDDEH4	VDD	EMIOS0	EMIOS8	EMIOS13	EMIOS22	EMIOS24	EMIOS28	CNTXB	CNRXD	VDDEH5	PCSC1	VSSPMC	VDD	VDDEH6	XTAL	AC
AD	ENGCLK	VDD	VSS	FEC_TXD0	FEC_TXD1	PCSA0	PCSA3	PCSB2	D_CS0	D_ADD22	D_ADD25	D_ADD28	EMIOS2	EMIOS7	EMIOS12	EMIOS16	EMIOS18	EMIOS27	CNRXA	CNTXD	SCKC	RXDC	PCSC3	VSS	VDD	VDDFLA	AD
AE	VDD	VSS	FEC_RX_DV	FEC_TX_EN	PCSA4	PCSB5	SINA	PCSB1	D_TS	D_ADD23	D_ADD26	D_ADD30	EMIOS3	EMIOS6	EMIOS10	EMIOS15	EMIOS21	EMIOS26	CNTXA	CNRXC	PCSC0	SINC	PCSC2	PCSC5	VSS	VDD	AE
AF		VDDE2A	FEC_RXD0	FEC_RXD1	VDDEH3A	PCSA2	PCSB4	PCSB0	D_TA	D_ADD24	D_ADD27	D_CLKOUT	EMIOS4	EMIOS5	EMIOS9	EMIOS20	EMIOS14	EMIOS25	EMIOS30	CNTXC	SOUTC	VDDEH4	TXDC	PCSC4	VDDEH5		AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 3. MPC5777C 516-ball MAPBGA (full diagram)

3 Electrical characteristics

The following information includes details about power considerations, DC/AC electrical characteristics, and AC timing specifications.

3.1 Absolute maximum ratings

Absolute maximum specifications are stress ratings only. Functional operation at these maxima is not guaranteed.

CAUTION

Stress beyond listed maxima may affect device reliability or cause permanent damage to the device.

See Operating conditions for functional operation specifications.

Table 1. Absolute maximum ratings

Symbol	Parameter	Conditions[1]	Value		Unit
			Min	Max	
Cycle	Lifetime power cycles	—	—	1000k	—
V_{DD}	1.2 V core supply voltage[2, 3, 4]	—	–0.3	1.5	V
V_{DDEHx}	I/O supply voltage (medium I/O pads)[5]	—	–0.3	6.0	V
V_{DDEx}	I/O supply voltage (fast I/O pads)[5]	—	–0.3	6.0	V
V_{DDPMC}	Power Management Controller supply voltage[5]	—	–0.3	6.0	V
V_{DDFLA}	Decoupling pin for flash regulator[6]	—	–0.3	4.5	V
V_{STBY}	RAM standby supply voltage[5]	—	–0.3	6.0	V
V_{SSA_SD}	SDADC ground voltage	Reference to V_{SS}	–0.3	0.3	V
V_{SSA_EQ}	eQADC ground voltage	Reference to V_{SS}	–0.3	0.3	V
$V_{DDA\_EQA/B}$	eQADC supply voltage	Reference to V_{SSA_EQ}	–0.3	6.0	V
V_{DDA_SD}	SDADC supply voltage	Reference to V_{SSA_SD}	–0.3	6.0	V
V_{RL_SD}	SDADC ground reference	Reference to V_{SS}	–0.3	0.3	V
V_{RL_EQ}	eQADC ground reference	Reference to V_{SS}	–0.3	0.3	V
V_{RH_EQ}	eQADC alternate reference	Reference to V_{RL_EQ}	–0.3	6.0	V
V_{RH_SD}	SDADC alternate reference	Reference to V_{RL_SD}	–0.3	6.0	V
$V_{REFBYPC}$	eQADC reference decoupling capacitor pins	REFBYPCA25, REFBYPCA75, REFBYPCB25, REFBYPC75	–0.3	6.0	V
V_{DDA_MISC}	TRNG and IRC supply voltage	—	–0.3	6.0	V
V_{DDPWR}	SMPS driver supply pin	—	–0.3	6.0	V
V_{SSPWR}	SMPS driver supply pin	Reference to V_{SS}	–0.3	0.3	V
$V_{SS} – V_{SSA\_EQ}$	V_{SSA_EQ} differential voltage	—	–0.3	0.3	V
$V_{SS} – V_{SSA\_SD}$	V_{SSA_SD} differential voltage	—	–0.3	0.3	V
$V_{SS} – V_{RL\_EQ}$	V_{RL_EQ} differential voltage	—	–0.3	0.3	V
$V_{SS} – V_{RL\_SD}$	V_{RL_SD} differential voltage	—	–0.3	0.3	V
V_{IN}	I/O input voltage range[7]	—	–0.3	6.0	V
		Relative to V_{DDEx}/V_{DDEHx}	—	0.3	V
		Relative to V_{SS}	–0.3	—	V
I_{INJD}	Maximum DC injection current for digital pad	Per pin, applies to all digital pins	–5	5	mA
I_{INJA}	Maximum DC injection current for analog pad	Per pin, applies to all analog pins	–5	5	mA
I_{MAXSEG}[8, 9]	Maximum current per I/O power segment	—	–120	120	mA
T_{STG}	Storage temperature range and non-operating times	—	–55	175	°C
STORAGE	Maximum storage time, assembled part programmed in ECU	No supply; storage temperature in range –40 °C to 60 °C	—	20	years
T_{SDR}	Maximum solder temperature[10] Pb-free package	—	—	260	°C

Table continues on the next page...

Table 1. Absolute maximum ratings (continued)

Symbol	Parameter	Conditions[1]	Value		Unit
			Min	Max	
MSL	Moisture sensitivity level[11]	—	—	3	—

1. Voltages are referred to V_{SS} if not specified otherwise
2. Allowed 1.45 V – 1.5 V for 60 seconds cumulative time at maximum T_J = 150 °C; remaining time as defined in note 3 and note 4
3. Allowed 1.375 V – 1.45 V for 10 hours cumulative time at maximum T_J = 150 °C; remaining time as defined in note 4
4. 1.32 V – 1.375 V range allowed periodically for supply with sinusoidal shape and average supply value below 1.275 V at maximum T_J = 150 °C
5. Allowed 5.5 V – 6.0 V for 60 seconds cumulative time with no restrictions, for 10 hours cumulative time device in reset, T_J = 150 °C; remaining time at or below 5.5 V
6. Allowed 3.6 V – 4.5 V for 60 seconds cumulative time with no restrictions, for 10 hours cumulative time device in reset, T_J = 150 °C; remaining time at or below 3.6 V
7. The maximum input voltage on an I/O pin tracks with the associated I/P supply maximum. For the injection current condition on a pin, the voltage will be equal to the supply plus the voltage drop across the internal ESD diode from I/O pin to supply. The diode voltage varies greatly across process and temperature, but a value of 0.3V can be used for nominal calculations.
8. The sum of all controller pins (including both digital and analog) must not exceed 200 mA. A V_{DDEx}/V_{DDEHx} power segment is defined as one or more GPIO pins located between two V_{DDEx}/V_{DDEHx} supply pins.
9. The average current values given in I/O pad current specifications should be used to calculate total I/O segment current.
10. Solder profile per IPC/JEDEC J-STD-020D
11. Moisture sensitivity per JEDEC test method A112

3.2 Electromagnetic interference (EMI) characteristics

Test reports with EMC measurements to IC-level IEC standards are available on request.

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions, go to nxp.com and perform a keyword search for "radiated emissions."

3.3 Electrostatic discharge (ESD) characteristics

Table 2. ESD Ratings[1, 2]

Symbol	Parameter	Conditions	Value	Unit
V_{HBM}	ESD for Human Body Model (HBM)	All pins	2000	V
V_{CDM}	ESD for Charged Device Model (CDM)	Corner pins	750	V
		Non-corner pins	500	

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements.

3.4 Operating conditions

The following table describes the operating conditions for the device, and for which all specifications in the data sheet are valid, except where explicitly noted.

If the device operating conditions are exceeded, the functionality of the device is not guaranteed.

Table 3. Device operating conditions

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
Frequency						
f_{SYS}	Device operating frequency[1]	—	—	—	264/300[2]	MHz
f_{PLATF}	Platform operating frequency	—	—	—	132/150[3]	MHz
f_{ETPU}	eTPU operating frequency	—	—	—	200/240[4]	MHz
f_{EBI}	EBI operating frequency	—	—	—	66	MHz
f_{PER}	Peripheral block operating frequency	—	—	—	132/150[3]	MHz
f_{FM_PER}	Frequency-modulated peripheral block operating frequency	—	—	—	132/150[3]	MHz
t_{CYC}	Platform clock period	—	—	—	$1/f_{PLATF}$	ns
t_{CYC_ETPU}	eTPU clock period	—	—	—	$1/f_{ETPU}$	ns
t_{CYC_PER}	Peripheral clock period	—	—	—	$1/f_{PER}$	ns
Temperature						
T_J	Junction operating temperature range	Packaged devices	–40.0	—	150.0	°C
T_A (T_L to T_H)	Ambient operating temperature range	Packaged devices	–40.0	—	125.0[5]	°C
Voltage						
V_{DD}	External core supply voltage[6, 7]	LVD/HVD enabled	1.2	—	1.32	V
		LVD/HVD disabled[8, 9, 10, 11]	1.2	—	1.38	
V_{DDA_MISC}	TRNG and IRC supply voltage	—	3.5	—	5.5	V
V_{DDEx}	I/O supply voltage (fast I/O pads)	5 V range	4.5	—	5.5	V
		3.3 V range	3.0	—	3.6	
V_{DDEHx}[11]	I/O supply voltage (medium I/O pads)	5 V range	4.5	—	5.5	V
		3.3 V range	3.0	—	3.6	
V_{DDEH1}	eTPU_A, eSCI_A, eSCI_B, and configuration I/O supply voltage (medium I/O pads)	5 V range	4.5	—	5.5	V
V_{DDPMC}[12]	Power Management Controller (PMC) supply voltage	Full functionality	3.15	—	5.5	V
V_{DDPWR}	SMPS driver supply voltage	Reference to V_{SSPWR}	3.0	—	5.5	V
V_{DDFLA}	Flash core voltage	—	3.15	—	3.6	V
V_{STBY}	RAM standby supply voltage	—	0.95[13]	—	5.5	V

Table continues on the next page...

Table 3. Device operating conditions (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{STBY_BO}	Standby RAM brownout flag trip point voltage	—	—	—	0.9[14]	V
V_{RL_SD}	SDADC ground reference voltage	—	V_{SSA_SD}			V
V_{DDA_SD}	SDADC supply voltage[15]	—	4.5	—	5.5	V
$V_{DDA\_EQA/B}$	eQADC supply voltage	—	4.75	—	5.25	V
V_{RH_SD}	SDADC reference	—	4.5	V_{DDA_SD}	5.5	V
$V_{DDA\_SD} – V_{RH\_SD}$	SDADC reference differential voltage	—	—	—	25	mV
$V_{SSA\_SD} – V_{RL\_SD}$	V_{RL_SD} differential voltage	—	–25	—	25	mV
V_{RH_EQ}	eQADC reference	—	4.75	—	5.25	V
$V_{DDA\_EQA/B} – V_{RH\_EQ}$	eQADC reference differential voltage	—	—	—	25	mV
$V_{SSA\_EQ} – V_{RL\_EQ}$	V_{RL_EQ} differential voltage	—	–25	—	25	mV
$V_{SSA\_EQ} – V_{SS}$	V_{SSA_EQ} differential voltage	—	–25	—	25	mV
$V_{SSA\_SD} – V_{SS}$	V_{SSA_SD} differential voltage	—	–25	—	25	mV
V_{RAMP}	Slew rate on power supply pins	—	—	—	100	V/ms
Current						
I_{IC}	DC injection current (per pin)[16, 17, 18]	Digital pins and analog pins	–3.0	—	3.0	mA
I_{MAXSEG}	Maximum current per power segment[19, 20]	—	–80	—	80	mA

1. Maximum operating frequency is applicable to the computational cores and platform for the device. See the Clocking chapter in the MPC5777C Microcontroller Reference Manual for more information on the clock limitations for the various IP blocks on the device.
2. If frequency modulation (FM) is enabled for the operating frequency of 264MHz, the maximum frequency still cannot exceed this value (frequency modulation must spread below nominal frequency). If frequency modulation is enabled for the operating frequency of 300MHz, this maximum frequency can be exceeded (frequency modulation can be center spread from 300MHz).
3. 132 MHz applies to the MPC5777C part number with 264 MHz operating frequency. 150 MHz applies to the version with 300 MHz operating frequency.
4. 200 MHz applies to the MPC5777C part number with 264 MHz max operating frequency. 240 MHz applies to the version with 300 MHz operating frequency.
5. The maximum specification for operating junction temperature T_J must be respected. Thermal characteristics provides details.
6. Core voltage as measured on device pin to guarantee published silicon performance
7. During power ramp, voltage measured on silicon might be lower. Maximum performance is not guaranteed, but correct silicon operation is guaranteed. See power management and reset management for description.
8. Maximum core voltage is not permitted for entire product life. See absolute maximum rating.
9. When internal LVD/HVDs are disabled, external monitoring is required to guarantee device operation. Failure to monitor externally supply voltage may result in erroneous operation of the device.
10. This LVD/HVD disabled supply voltage condition only applies after LVD/HVD are disabled by the application during the reset sequence, and the LVD/HVD are active until that point.
11. This spec does not apply to V_{DDEH1}.
12. When internal flash memory regulator is used:
    - Flash memory read operation is supported for a minimum V_{DDPMC} value of 3.15 V.
    - Flash memory read, program, and erase operations are supported for a minimum V_{DDPMC} value of 3.5 V.

When flash memory power is supplied externally (V_{DDPMC} shorted to V_{DDFLA}): The V_{DDPMC} range must be within the limits specified for LVD_FLASH and HVD_FLASH monitoring. Table 29 provides the monitored LVD_FLASH and HVD_FLASH limits.

13. If the standby RAM regulator is not used, the V_{STBY} supply input pin must be tied to ground.
14. V_{STBY_BO} is the maximum voltage that sets the standby RAM brownout flag in the device logic. The minimum voltage for RAM data retention is guaranteed always to be less than the V_{STBY_BO} maximum value.
15. For supply voltages between 3.0 V and 4.0 V there will be no guaranteed precision of ADC (accuracy/linearity). ADC will recover to a fully functional state when the voltage rises above 4.0 V.
16. Full device lifetime without performance degradation
17. I/O and analog input specifications are only valid if the injection current on adjacent pins is within these limits. See the absolute maximum ratings table for maximum input current for reliability requirements.
18. The I/O pins on the device are clamped to the I/O supply rails for ESD protection. When the voltage of the input pin is above the supply rail, current will be injected through the clamp diode to the supply rail. For external RC network calculation, assume a typical 0.3 V drop across the active diode. The diode voltage drop varies with temperature.
19. The sum of all controller pins (including both digital and analog) must not exceed 200 mA. A V_{DDEx}/V_{DDEHx} power segment is defined as one or more GPIO pins located between two V_{DDEx}/V_{DDEHx} supply pins.
20. The average current values given in I/O pad current specifications should be used to calculate total I/O segment current.

3.5 DC electrical specifications

NOTE

I_{DDA_MISC} is the sum of current consumption of IRC, I_{TRNG}, and I_{STBY} in the 5 V domain. IRC current is provided in the IRC specifications.

NOTE

I/O, XOSC, EQADC, SDADC, and Temperature Sensor current specifications are in those components' dedicated sections.

Table 4. DC electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
I_{DD}	Operating current on the V_{DD} core logic supply[1]	LVD/HVD enabled, V_{DD} = 1.2 V to 1.32 V	—	0.65	1.35	A
		LVD/HVD disabled, V_{DD} = 1.2 V to 1.38 V	—	0.65	1.4	
I_{DD_PE}	Operating current on the V_{DD} supply for flash memory program/erase	—	—	—	85	mA
I_{DDPMC}	Operating current on the V_{DDPMC} supply[2]	Flash memory read	—	—	40	mA
		Flash memory program/erase	—	—	70	
		PMC only	—	—	35	
	Operating current on the V_{DDPMC} supply (internal core regulator bypassed)	Flash memory read	—	—	10	mA
		Flash memory program/erase	—	—	40	
		PMC only	—	—	5	
I_{REGCTL}	Core regulator DC current output on V_{REGCTL} pin	—	—	—	25	mA

Table continues on the next page...

Table 4. DC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
I_{STBY}	Standby RAM supply current	1.08 V, T_J = 150°C	—	—	1140	µA
		1.25 V to 5.5 V, T_J = 150°C			1170	
		1.25 V to 5.5 V, T_J = 85°C			360	
		1.25 V to 5.5 V, T_J = 40°C	—	—	120	
I_{DD_PWR}	Operating current on the V_{DDPWR} supply	—	—	—	50	mA
I_{BG_REF}	Bandgap reference current consumption[3]		—	—	600	µA
I_{TRNG}	True Random Number Generator current	—	—	—	2.1	mA

1. I_{DD} measured on an application-specific pattern with all cores enabled at full frequency, T_J = 40°C to 150°C. Flash memory program/erase current on the V_{DD} supply not included.
2. This value is considering the use of the internal core regulator with the simulation of an external transistor with the minimum value of h_{FE} of 60.
3. This bandgap reference is for EQADC calibration and Temperature Sensors.

3.6 I/O pad specifications

The following table describes the different pad types on the chip.

Table 5. I/O pad specification descriptions

Pad type	Description
General-purpose I/O pads	General-purpose I/O and EBI data bus pads with four selectable output slew rate settings; also called SR pads
EBI pads	Provide necessary speed for fast external memory interfaces on the EBI CLKOUT, address, and control signals; also called FC pads
LVDS pads	Low Voltage Differential Signal interface pads
Input-only pads	Low-input-leakage pads that are associated with the ADC channels

NOTE

Each I/O pin on the device supports specific drive configurations. See the signal description table in the device reference manual for the available drive configurations for each I/O pin.

NOTE

Throughout the I/O pad specifications, the symbol V_{DDEx} represents all V_{DDEx} and V_{DDEHx} segments.

3.6.1 Input pad specifications

Table 6 provides input DC electrical characteristics as described in Figure 4.

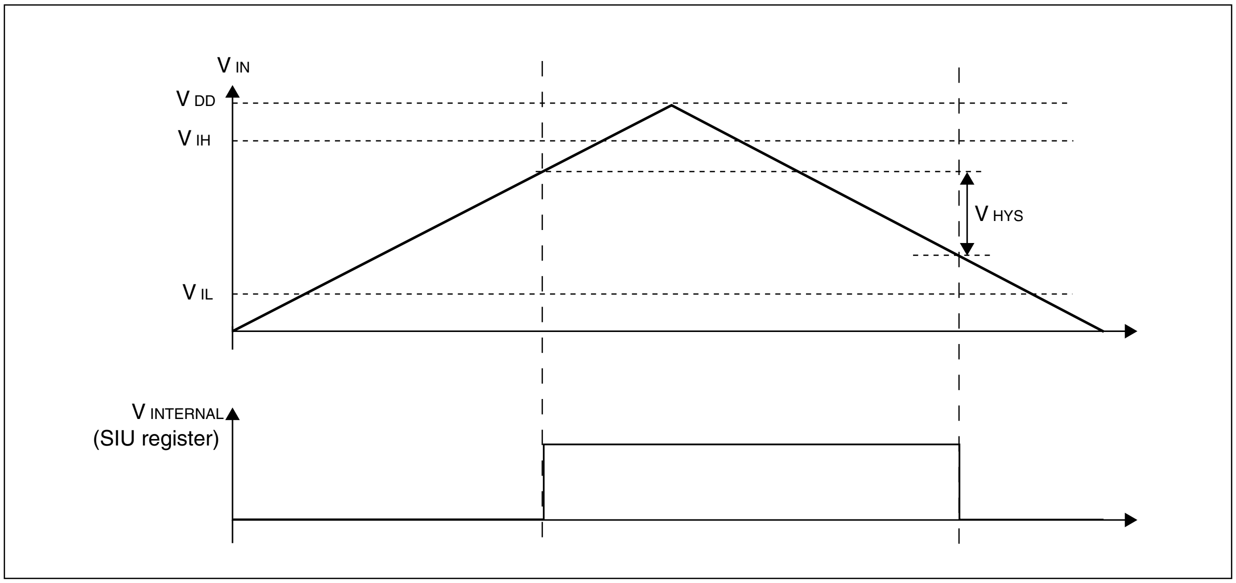


Figure 4. I/O input DC electrical characteristics definition

Table 6. I/O input DC electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{IHCMOS_H}	Input high level CMOS (with hysteresis)	3.0 V < V_{DDEx} < 3.6 V and 4.5 V < V_{DDEx} < 5.5 V	0.65 * V_{DDEx}	—	V_{DDEx} + 0.3	V
V_{IHCMOS}	Input high level CMOS (without hysteresis)	3.0 V < V_{DDEx} < 3.6 V and 4.5 V < V_{DDEx} < 5.5 V	0.55 * V_{DDEx}	—	V_{DDEx} + 0.3	V
V_{ILCMOS_H}	Input low level CMOS (with hysteresis)	3.0 V < V_{DDEx} < 3.6 V and 4.5 V < V_{DDEx} < 5.5 V	–0.3	—	0.35 * V_{DDEx}	V
V_{ILCMOS}	Input low level CMOS (without hysteresis)	3.0 V < V_{DDEx} < 3.6 V and 4.5 V < V_{DDEx} < 5.5 V	–0.3	—	0.4 * V_{DDEx}	V
$V_{HYSCMOS}$	Input hysteresis CMOS	3.0 V < V_{DDEx} < 3.6 V and 4.5 V < V_{DDEx} < 5.5 V	0.1 * V_{DDEx}	—	—	V
Input Characteristics[1]						
I_{LKG}	Digital input leakage	$V_{SS} < V_{IN} < V_{DDEx}/V_{DDEHx}$	—	—	2.5	µA
I_{LKG_FAST}	Digital input leakage for EBI address/control signal pads	$V_{SS} < V_{IN} < V_{DDEx}/V_{DDEHx}$	—	—	2.5	µA
I_{LKGA}	Analog pin input leakage (5 V range)	$V_{SSA\_SD} < V_{IN} < V_{DDA\_SD}$, $V_{SSA\_EQ} < V_{IN} < V_{DDA\_EQA/B}$	—	—	220	nA
C_{IN}	Digital input capacitance	GPIO and EBI input pins	—	—	7	pF

1. For LFAST, microsecond bus, and LVDS input characteristics, see dedicated communication module sections.

Table 7 provides current specifications for weak pullup and pulldown.

Table 7. I/O pullup/pulldown DC electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
I_{WPU}	Weak pullup current	$V_{IN} = 0.35 * V_{DDEx}$ $4.5\ V < V_{DDEx} < 5.5\ V$	40	—	120	μA
		$V_{IN} = 0.35 * V_{DDEx}$ $3.0\ V < V_{DDEx} < 3.6\ V$	25	—	80	
I_{WPD}	Weak pulldown current	$V_{IN} = 0.65 * V_{DDEx}$ $4.5\ V < V_{DDEx} < 5.5\ V$	40	—	120	μA
		$V_{IN} = 0.65 * V_{DDEx}$ $3.0\ V < V_{DDEx} < 3.6\ V$	25	—	80	

The specifications in Table 8 apply to the pins ANA0_SDA0 to ANA7, ANA16_SDB0 to ANA23_SDC3, and ANB0_SDD0 to ANB7_SDD7.

Table 8. I/O pullup/pulldown resistance electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
R_{PUPD}	Analog input bias / diagnostic pullup/ pulldown resistance	200 kΩ	130	200	280	kΩ
		100 kΩ	65	100	140	
		5 kΩ	1.4	5	7.5	
Δ_{PUPD}	R_{PUPD} pullup/pulldown resistance mismatch	—	—	—	5	%

3.6.2 Output pad specifications

Figure 5 shows output DC electrical characteristics.

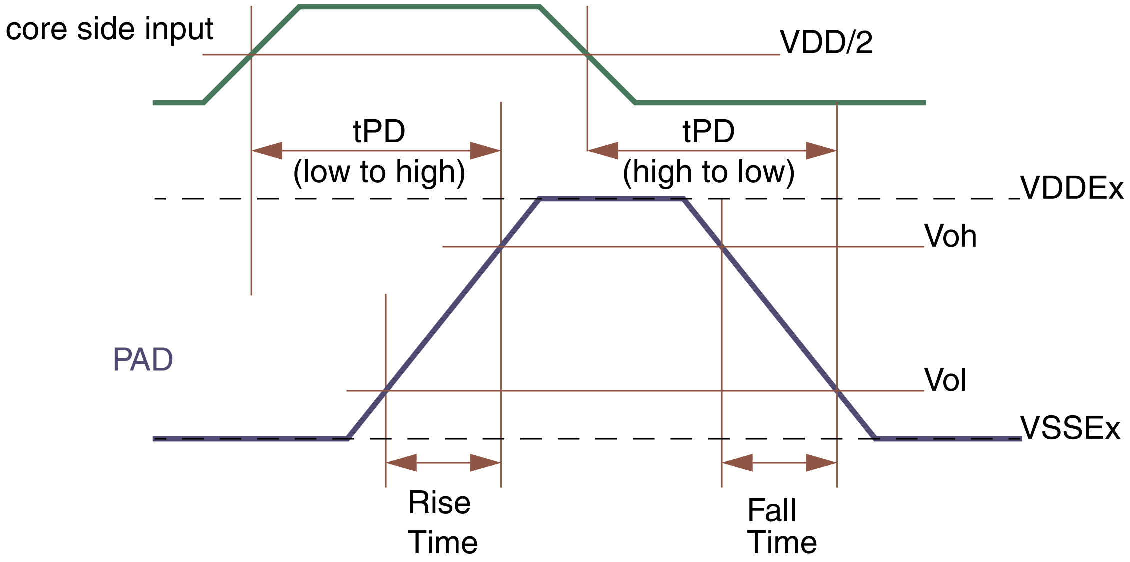


Figure 5. I/O output DC electrical characteristics definition

The following tables specify output DC electrical characteristics.

Table 9. GPIO and EBI data pad output buffer electrical characteristics (SR pads)[1]

Symbol	Parameter	Conditions[2]		Value[3]			Unit
				Min	Typ	Max	
I_{OH}	GPIO pad output high current	$V_{OH} = 0.8 * V_{DDEx}$ $4.5 V < V_{DDEx} < 5.5 V$	PCR[SRC] = 11b or 01b	25	—	—	mA
			PCR[SRC] = 10b or 00b	15	—	—	
		$V_{OH} = 0.8 * V_{DDEx}$ $3.0 V < V_{DDEx} < 3.6 V$	PCR[SRC] = 11b or 01b	13	—	—	
			PCR[SRC] = 10b or 00b	8	—	—	
I_{OL}	GPIO pad output low current	$V_{OL} = 0.2 * V_{DDEx}$ $4.5 V < V_{DDEx} < 5.5 V$	PCR[SRC] = 11b or 01b	48	—	—	mA
			PCR[SRC] = 10b or 00b	22	—	—	
		$V_{OL} = 0.2 * V_{DDEx}$ $3.0 V < V_{DDEx} < 3.6 V$	PCR[SRC] = 11b or 01b	17	—	—	
			PCR[SRC] = 10b or 00b	10.5	—	—	

Table continues on the next page...

Table 9. GPIO and EBI data pad output buffer electrical characteristics (SR pads)[1] (continued)

Symbol	Parameter	Conditions[2]		Value[3]			Unit
				Min	Typ	Max	
t_{R_F}	GPIO pad output transition time (rise/fall)	PCR[SRC] = 11b 4.5 V < V_{DDEx} < 5.5 V	C_L = 25 pF	—	—	1.2	ns
			C_L = 50 pF	—	—	2.5	
			C_L = 200 pF	—	—	8	
		PCR[SRC] = 11b 3.0 V < V_{DDEx} < 3.6 V	C_L = 25 pF	—	—	1.7	
			C_L = 50 pF	—	—	3.25	
			C_L = 200 pF	—	—	12	
		PCR[SRC] = 10b 4.5 V < V_{DDEx} < 5.5 V	C_L = 50 pF	—	—	5	
			C_L = 200 pF	—	—	18	
		PCR[SRC] = 10b 3.0 V < V_{DDEx} < 3.6 V	C_L = 50 pF	—	—	7	
			C_L = 200 pF	—	—	25	
		PCR[SRC] = 01b 4.5 V < V_{DDEx} < 5.5 V	C_L = 50 pF	—	—	13	
			C_L = 200 pF	—	—	24	
		PCR[SRC] = 01b 3.0 V < V_{DDEx} < 3.6 V	C_L = 50 pF	—	—	25	
			C_L = 200 pF	—	—	30	
		PCR[SRC] = 00b 4.5 V < V_{DDEx} < 5.5 V	C_L = 50 pF	—	—	24	
			C_L = 200 pF	—	—	50	
		PCR[SRC] = 00b 3.0 V < V_{DDEx} < 3.6 V	C_L = 50 pF	—	—	40	
			C_L = 200 pF	—	—	51	
t_{PD}	GPIO pad output propagation delay time	PCR[SRC] = 11b 4.5 V < V_{DDEx} < 5.5 V	C_L = 50 pF	—	—	6	ns
			C_L = 200 pF	—	—	13	
		PCR[SRC] = 11b 3.0 V < V_{DDEx} < 3.6 V	C_L = 50 pF	—	—	8.25	
			C_L = 200 pF	—	—	19.5	
		PCR[SRC] = 10b 4.5 V < V_{DDEx} < 5.5 V	C_L = 50 pF	—	—	9	
			C_L = 200 pF	—	—	22	
		PCR[SRC] = 10b 3.0 V < V_{DDEx} < 3.6 V	C_L = 50 pF	—	—	12.5	
			C_L = 200 pF	—	—	35	
		PCR[SRC] = 01b 4.5 V < V_{DDEx} < 5.5 V	C_L = 50 pF	—	—	27	
			C_L = 200 pF	—	—	40	
		PCR[SRC] = 01b 3.0 V < V_{DDEx} < 3.6 V	C_L = 50 pF	—	—	45	
			C_L = 200 pF	—	—	65	
		PCR[SRC] = 00b 4.5 V < V_{DDEx} < 5.5 V	C_L = 50 pF	—	—	40	
			C_L = 200 pF	—	—	65	
		PCR[SRC] = 00b 3.0 V < V_{DDEx} < 3.6 V	C_L = 50 pF	—	—	75	
			C_L = 200 pF	—	—	100	
$\|t_{SKEW\_W}\|$	Difference between rise and fall time	—		—	—	25	%

---

1. All GPIO pad output specifications are valid for 3.0 V < V_{DDEx} < 5.5 V, except where explicitly stated.

2. PCR[SRC] values refer to the setting of that register field in the SIU.
3. All values to be confirmed during device validation.

The following table shows the EBI CLKOUT, address, and control signal pad electrical characteristics. These pads can also be used for GPIO.

Table 10. GPIO and EBI CLKOUT, address, and control signal pad output buffer electrical characteristics (FC pads)

Symbol	Parameter	Conditions[1]		Value			Unit
				Min	Typ	Max	
EBI Mode Output Specifications: valid for 3.0 V < V_{DDEx} < 3.6 V							
C_{DRV}	External bus load capacitance	PCR[DSC] = 01b		—	—	10	pF
		PCR[DSC] = 10b		—	—	20	
		PCR[DSC] = 11b		—	—	30	
f_{MAX_EBI}	External bus maximum operating frequency	C_{DRV} = 10/20/30 pF		—	—	66	MHz
GPIO and EBI Mode Output Specifications							
I_{OH_EBI}	GPIO and external bus pad output high current	$V_{OH} = 0.8 * V_{DDEx}$ 4.5 V < V_{DDEx} < 5.5 V	PCR[DSC] = 11b	30	—	—	mA
			PCR[DSC] = 10b	22	—	—	
			PCR[DSC] = 01b	13	—	—	
			PCR[DSC] = 00b	2	—	—	
		$V_{OH} = 0.8 * V_{DDEx}$ 3.0 V < V_{DDEx} < 3.6 V	PCR[DSC] = 11b	16	—	—	
			PCR[DSC] = 10b	12	—	—	
			PCR[DSC] = 01b	7	—	—	
			PCR[DSC] = 00b	1	—	—	
I_{OL_EBI}	GPIO and external bus pad output low current	$V_{OL} = 0.2 * V_{DDEx}$ 4.5 V < V_{DDEx} < 5.5 V	PCR[DSC] = 11b	54	—	—	mA
			PCR[DSC] = 10b	25	—	—	
			PCR[DSC] = 01b	16	—	—	
			PCR[DSC] = 00b	2	—	—	
		$V_{OL} = 0.2 * V_{DDEx}$ 3.0 V < V_{DDEx} < 3.6 V	PCR[DSC] = 11b	17	—	—	
			PCR[DSC] = 10b	14	—	—	
			PCR[DSC] = 01b	8	—	—	
			PCR[DSC] = 00b	1	—	—	
$t_{R\_F\_EBI}$	GPIO and external bus pad output transition time (rise/fall)	PCR[DSC] = 11b	C_L = 30 pF	—	—	1.5	ns
			C_L = 50 pF	—	—	2.4	
		PCR[DSC] = 10b	C_L = 20 pF	—	—	1.5	
		PCR[DSC] = 01b	C_L = 10 pF	—	—	1.85	
		PCR[DSC] = 00b	C_L = 50 pF	—	—	45	
t_{PD_EBI}	GPIO and external bus pad output propagation delay time	PCR[DSC] = 11b	C_L = 30 pF	—	—	4.2	ns
			C_L = 50 pF	—	—	5.5	
		PCR[DSC] = 10b	C_L = 20 pF	—	—	4.2	
		PCR[DSC] = 01b	C_L = 10 pF	—	—	4.4	
		PCR[DSC] = 00b	C_L = 50 pF	—	—	59	

1. PCR[DSC] values refer to the setting of that register field in the SIU.

3.6.3 I/O pad current specifications

The I/O pads are distributed across the I/O supply segments. Each I/O supply segment is associated with a V_{DDEx} supply segment.

Table 11 provides I/O consumption figures.

To ensure device reliability, the average current of the I/O on a single segment should remain below the I_{MAXSEG} value given in Table 1.

To ensure device functionality, the average current of the I/O on a single segment should remain below the I_{MAXSEG} value given in Table 3.

NOTE

The MPC5777C I/O Signal Description and Input Multiplexing Tables are contained in a Microsoft Excel® file attached to the Reference Manual. In the spreadsheet, select the I/O Signal Table tab.

The EBI power segments have been designed to operate within the maximum per-segment current specification when the pins on the segment are used for EBI function. If the pins are used instead for GPIO function, the user must ensure the sum of the current used on each pin in the segment does not exceed the spec.

Table 11. I/O consumption

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
I_{AVG_GPIO}	Average I/O current for GPIO pads (per pad)	C_L = 25 pF, 2 MHz V_{DDEx} = 5.0 V ± 10%	—	—	0.42	mA
		C_L = 50 pF, 1 MHz V_{DDEx} = 5.0 V ± 10%	—	—	0.35	
I_{AVG_EBI}	Average I/O current for external bus output pins (per pad)	C_{DRV} = 10 pF, f_{EBI} = 66 MHz V_{DDEx} = 3.3 V ± 10%	—	—	9	mA
		C_{DRV} = 20 pF, f_{EBI} = 66 MHz V_{DDEx} = 3.3 V ± 10%	—	—	18	
		C_{DRV} = 30 pF, f_{EBI} = 66 MHz V_{DDEx} = 3.3 V ± 10%	—	—	30	

3.7 Oscillator and PLL electrical specifications

The on-chip dual PLL—consisting of the peripheral clock and reference PLL (PLL0) and the frequency-modulated system PLL (PLL1)—generates the system and auxiliary clocks from the main oscillator driver.

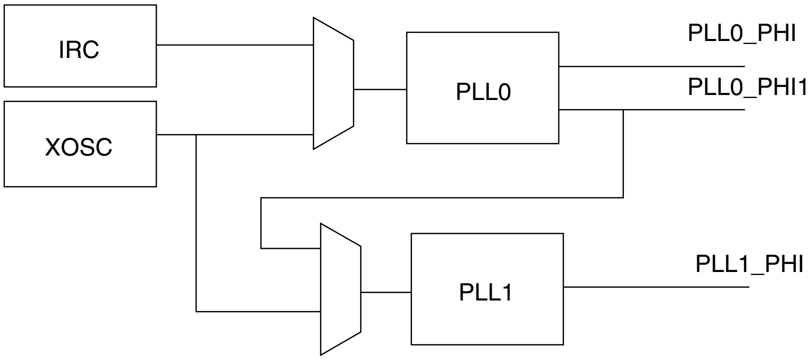


Figure 6. PLL integration

3.7.1 PLL electrical specifications

Table 12. PLL0 electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{PLL0IN}	PLL0 input clock[1, 2]	—	8	—	44	MHz
Δ_{PLL0IN}	PLL0 input clock duty cycle[2]	—	40	—	60	%
$f_{PLL0VCO}$	PLL0 VCO frequency	—	600	—	1250	MHz
$f_{PLL0PHI}$	PLL0 output frequency	—	4.762	—	200/240[3]	MHz
$t_{PLL0LOCK}$	PLL0 lock time	—	—	—	110	μs
$\lvert\Delta_{PLL0PHISPJ}\rvert$	PLL0_PHI single period jitter f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI}$ = 200 MHz, 6-sigma	—	—	200	ps
$\lvert\Delta_{PLL0PHI1SPJ}\rvert$	PLL0_PHI1 single period jitter f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI1}$ = 40 MHz, 6-sigma	—	—	300[4]	ps
$\Delta_{PLL0LTJ}$	PLL0 output long term jitter[4] f_{PLL0IN} = 20 MHz (resonator), VCO frequency = 800 MHz	10 periods accumulated jitter (80 MHz equivalent frequency), 6-sigma pk-pk	—	—	±250	ps
		16 periods accumulated jitter (50 MHz equivalent frequency), 6-sigma pk-pk	—	—	±300	ps
		long term jitter (< 1 MHz equivalent frequency), 6-sigma pk-pk)	—	—	±500	ps
I_{PLL0}	PLL0 consumption	FINE LOCK state	—	—	7.5	mA

1. Ensure that the f_{PLL0IN} frequency divided by PLLDIG_PLL0DV[PREDIV] is in the range 8 MHz to 20 MHz.
2. PLL0IN clock retrieved directly from either internal IRC or external XOSC clock. Input characteristics are granted when using internal IRC or external oscillator is used in functional mode.
3. 200 MHz applies to the MPC5777C part number with 264 MHz operating frequency. 240 MHz applies to the version with 300 MHz operating frequency

4. Noise on the V_{DD} supply with frequency content below 40 kHz and above 50 MHz is filtered by the PLL. Noise on the V_{DD} supply with frequency content in the range of 40 kHz – 50 MHz must be filtered externally to the device.

Table 13. PLL1 electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{PLL1IN}	PLL1 input clock[1]	—	38	—	78	MHz
Δ_{PLL1IN}	PLL1 input clock duty cycle[1]	—	35	—	65	%
$f_{PLL1VCO}$	PLL1 VCO frequency	—	600	—	1250	MHz
$f_{PLL1PHI}$	PLL1 output clock PHI	—	4.762	—	264/300[2]	MHz
$t_{PLL1LOCK}$	PLL1 lock time	—	—	—	100	μs
$\|\Delta_{PLL1PHISPJ}\|$	PLL1_PHI single period peak-to-peak jitter	$f_{PLL1PHI}$ = 200 MHz, 6-sigma	—	—	500[3]	ps
$f_{PLL1MOD}$	PLL1 modulation frequency	—	—	—	250	kHz
$\|\delta_{PLL1MOD}\|$	PLL1 modulation depth (when enabled)	Center spread	0.25	—	2	%
		Down spread	0.5	—	4	%
I_{PLL1}	PLL1 consumption	FINE LOCK state	—	—	6	mA

1. PLL1IN clock retrieved directly from either internal PLL0 or external XOSC clock. Input characteristics are granted when using internal PLL0 or external oscillator in functional mode.
2. 264 MHz applies to the MPC5777C part number with 264 MHz max operating frequency. 300 MHz applies to the version with 300 MHz operating frequency
3. Noise on the V_{DD} supply with frequency content below 40 kHz and above 50 MHz is filtered by the PLL. Noise on the V_{DD} supply with frequency content in the range of 40 kHz – 50 MHz must be filtered externally to the device.

3.7.2 Oscillator electrical specifications

NOTE

All oscillator specifications in Table 14 are valid for V_{DDEH6} = 3.0 V to 5.5 V.

Table 14. External oscillator (XOSC) electrical specifications

Symbol	Parameter	Conditions	Value		Unit
			Min	Max	
f_{XTAL}	Crystal frequency range	—	8	40	MHz
t_{cst}	Crystal start-up time[1, 2]	T_J = 150 °C	—	5	ms
t_{rec}	Crystal recovery time[3]	—	—	0.5	ms
V_{IHEXT}	EXTAL input high voltage (external reference)	$V_{REF} = 0.28 * V_{DDEH6}$	$V_{REF} + 0.6$	—	V
V_{ILEXT}	EXTAL input low voltage (external reference)	$V_{REF} = 0.28 * V_{DDEH6}$	—	$V_{REF} – 0.6$	V
C_{S_EXTAL}	Total on-chip stray capacitance on EXTAL pin[4]	416-ball MAPBGA	2.3	3.0	pF
		516-ball MAPBGA	2.1	2.8	
C_{S_XTAL}	Total on-chip stray capacitance on XTAL pin[4]	416-ball MAPBGA	2.3	3.0	pF
		516-ball MAPBGA	2.2	2.9	

Table continues on the next page...

Table 14. External oscillator (XOSC) electrical specifications (continued)

Symbol	Parameter	Conditions	Value		Unit
			Min	Max	
g_m	Oscillator transconductance[5]	Low	3	10	mA/V
		Medium	10	27	
		High	12	35	
V_{EXTAL}	Oscillation amplitude on the EXTAL pin after startup[6]	—	0.5	1.6	V
V_{HYS}	Comparator hysteresis	—	0.1	1.0	V
I_{XTAL}	XTAL current[6, 7]	—	—	14	mA

1. This value is determined by the crystal manufacturer and board design.
2. Proper PC board layout procedures must be followed to achieve specifications.
3. Crystal recovery time is the time for the oscillator to settle to the correct frequency after adjustment of the integrated load capacitor value.
4. See crystal manufacturer's specification for recommended load capacitor (C_L) values.The external oscillator requires external load capacitors when operating in a "low" transconductance range. Account for on-chip stray capacitance (C_{S_EXTAL}/C_{S_XTAL}) and PCB capacitance when selecting a load capacitor value. When operating in a "medium" or "high" transconductance range, the integrated load capacitor value is selected via software to match the crystal manufacturer's specification, while accounting for on-chip and PCB capacitance.
5. Select a "low," "medium," or "high" setting using the UTEST Miscellaneous DCF client's XOSC_LF_EN and XOSC_EN_HIGH fields. "Low" is the setting commonly used for crystals at 8 MHz, "medium" is commonly used for crystals greater than 8 MHz to 20 MHz, and "high" is commonly used for crystals greater than 20 MHz to 40 MHz. However, the user must characterize carefully to determine the best g_m setting for the intended application because crystal load capacitance, board layout, and other factors affect the g_m value that is needed. The user may need an additional Rshunt to optimize g_m depending on the system environment. Use of overtone crystals is not recommended.
6. Amplitude on the EXTAL pin after startup is determined by the ALC block (that is, the Automatic Level Control Circuit). The function of the ALC is to provide high drive current during oscillator startup, while reducing current after oscillation to reduce power, distortion, and RFI, and to avoid over-driving the crystal. The operating point of the ALC is dependent on the crystal value and loading conditions.
7. I_{XTAL} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded. This is the maximum current during startup of the oscillator. The current after oscillation is typically in the 2–3 mA range and is dependent on the load and series resistance of the crystal. Test circuit is shown in Figure 7.

Table 15. Selectable load capacitance

load_cap_sel[4:0] from DCF record	Load capacitance[1, 2] (pF)
00000	1.8
00001	2.8
00010	3.7
00011	4.6
00100	5.6
00101	6.5
00110	7.4
00111	8.4
01000	9.3
01001	10.2
01010	11.2

Table continues on the next page...

Table 15. Selectable load capacitance (continued)

load_cap_sel[4:0] from DCF record	Load capacitance[1, 2] (pF)
01011	12.1
01100	13.0
01101	13.9
01110	14.9
01111	15.8

1. Values are determined from simulation across process corners and voltage and temperature variation. Capacitance values vary ±12% across process, 0.25% across voltage, and no variation across temperature.
2. Values in this table do not include the die and package capacitances given by C_{S_XTAL}/C_{S_EXTAL} in Table 14.

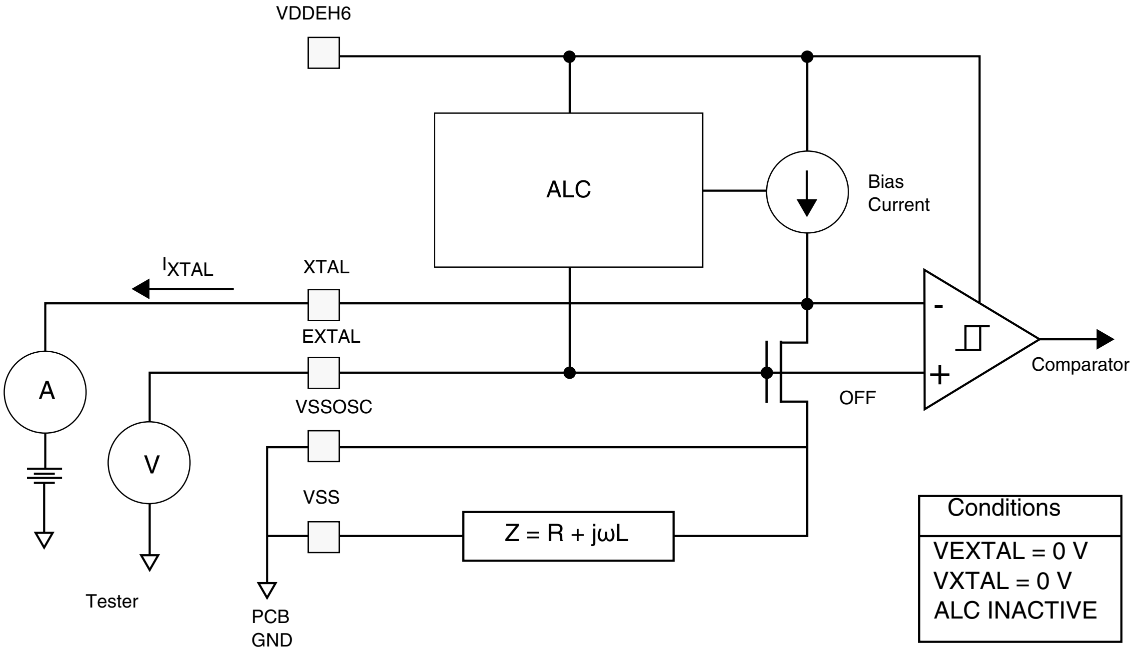


Figure 7. Test circuit

Table 16. Internal RC (IRC) oscillator electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{Target}	IRC target frequency	—	—	16	—	MHz
δf_{var_T}	IRC frequency variation	T < 150 °C	–8	—	8	%

3.8 Analog-to-Digital Converter (ADC) electrical specifications

3.8.1 Enhanced Queued Analog-to-Digital Converter (eQADC)

Table 17. eQADC conversion specifications (operating)

Symbol	Parameter	Value		Unit
		Min	Max	
f_{ADCLK}	ADC Clock (ADCLK) Frequency	2	33	MHz
CC	Conversion Cycles	2 + 13	128 + 15[1]	ADCLK cycles
T_{SR}	Stop Mode Recovery Time[2]	10	—	µs
—	Resolution[3]	1.25	—	mV
INL	INL: 16.5 MHz eQADC clock[4]	–4	4	LSB[5]
	INL: 33 MHz eQADC clock[4]	–6	6	LSB
DNL	DNL: 16.5 MHz eQADC clock[4]	–3	3	LSB
	DNL: 33 MHz eQADC clock[4]	–3	3	LSB
OFFNC	Offset Error without Calibration	0	140	LSB
OFFWC	Offset Error with Calibration	–8	8	LSB
GAINNC	Full Scale Gain Error without Calibration	–150	0	LSB
GAINWC	Full Scale Gain Error with Calibration	–8	8	LSB
I_{INJ}	Disruptive Input Injection Current[6, 7, 8, 9]	–3	3	mA
E_{INJ}	Incremental Error due to injection current[10, 11]	—	+4	Counts
TUE	TUE value[12, 13] (with calibration)	—	±8	Counts
GAINVGA1	Variable gain amplifier accuracy (gain = 1)[14]	-	-	Counts[16]
	INL, 16.5 MHz ADC	–4	4	
	INL, 33 MHz ADC	–8	8	
	DNL, 16.5 MHz ADC	–3[15]	3[15]	
	DNL, 33 MHz ADC	–3[15]	3[15]	
GAINVGA2	Variable gain amplifier accuracy (gain = 2)[14]	-	-	Counts
	INL, 16.5 MHz ADC	–5	5	
	INL, 33 MHz ADC	–8	8	
	DNL, 16.5 MHz ADC	–3	3	
	DNL, 33 MHz ADC	–3	3	
GAINVGA4	Variable gain amplifier accuracy (gain = 4)[14]	-	-	Counts
	INL, 16.5 MHz ADC	–7	7	
	INL, 33 MHz ADC	–8	8	
	DNL, 16.5 MHz ADC	–4	4	
	DNL, 33 MHz ADC	–4	4	
I_{ADC}	Current consumption per ADC (two ADCs per EQADC)	—	10	mA
I_{ADR}	Reference voltage current consumption per EQADC	—	200	µA

1. 128 sampling cycles (LST=128), differential conversion, pregain of x4
2. Stop mode recovery time is the time from the setting of either of the enable bits in the ADC Control Register to the time that the ADC is ready to perform conversions. Delay from power up to full accuracy = 8 ms.
3. At $V_{RH\_EQ} – V_{RL\_EQ} = 5.12$ V, one count = 1.25 mV without using pregain. Based on 12-bit conversion result; does not account for AC and DC errors
4. INL and DNL are tested from V_{RL} + 50 LSB to V_{RH} – 50 LSB.

5. At $V_{RH\_EQ} - V_{RL\_EQ}$ = 5.12 V, one LSB = 1.25 mV.
6. Below disruptive current conditions, the channel being stressed has conversion values of $3FF for analog inputs greater than V_{RH} and $000 for values less than V_{RL}. Other channels are not affected by non-disruptive conditions.
7. Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.
8. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA}$ + 0.5 V and $V_{NEGCLAMP}$ = –0.3 V, then use the larger of the calculated values.
9. Condition applies to two adjacent pins at injection limits.
10. Performance expected with production silicon.
11. All channels have same 10 kΩ < Rs < 100 kΩ Channel under test has Rs = 10 kΩ, $I_{INJ}=I_{INJMAX},I_{INJMIN}$.
12. The TUE specification is always less than the sum of the INL, DNL, offset, and gain errors due to cancelling errors.
13. TUE, Gain, and Offset specifications do not apply to differential conversions.
14. Variable gain is controlled by setting the PRE_GAIN bits in the ADC_ACR1-8 registers to select a gain factor of ×1, ×2, or ×4. Settings are for differential input only. Tested at ×1 gain. Values for other settings are guaranteed as indicated.
15. Guaranteed 10-bit monotonicity.
16. At $V_{RH\_EQ} - V_{RL\_EQ}$ = 5.12 V, one LSB = 1.25 mV.

3.8.2 Sigma-Delta ADC (SDADC)

The SDADC is a 16-bit Sigma-Delta analog-to-digital converter with a 333 Ksps maximum output conversion rate.

NOTE

The voltage range is 4.5 V to 5.5 V for SDADC specifications, except where noted otherwise.

Table 18. SDADC electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{IN}	ADC input signal	—	0	—	V_{DDA_SD}	V
V_{IN_PK2PK}[1]	Input range peak to peak $V_{IN\_PK2PK} = V_{INP}$[2] – V_{INM},[3]	Single ended $V_{INM} = V_{RL\_SD}$	V_{RH_SD}/GAIN			V
		Single ended $V_{INM} = 0.5*V_{RH\_SD}$ GAIN = 1	±0.5*V_{RH_SD}			
		Single ended $V_{INM} = 0.5*V_{RH\_SD}$ GAIN = 2,4,8,16	±V_{RH_SD}/GAIN			
		Differential $0 < V_{IN} < V_{DDEx}$	±V_{RH_SD}/GAIN			
f_{ADCD_M}	SD clock frequency[4]	—	4	14.4	16	MHz
f_{ADCD_S}	Conversion rate	—	—	—	333	Ksps
—	Oversampling ratio	Internal modulator	24	—	256	—
RESOLUTION	SD register resolution[5]	2's complement notation	16			bit

Table continues on the next page...

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
GAIN	ADC gain	Defined through SDADC_MCR[PGAN]. Only integer powers of 2 are valid gain values.	1	—	16	—
$\|\delta_{GAIN}\|$	Absolute value of the ADC gain error[6, 7]	Before calibration (applies to gain setting = 1)	—	—	1.5	%
		After calibration $\Delta V_{RH\_SD} < 5\%$, $\Delta V_{DDA\_SD} < 10\%$ $\Delta T_J < 50$ °C	—	—	5	mV
		After calibration $\Delta V_{RH\_SD} < 5\%$, $\Delta V_{DDA\_SD} < 10\%$ $\Delta T_J < 100$ °C	—	—	7.5	
		After calibration $\Delta V_{RH\_SD} < 5\%$, $\Delta V_{DDA\_SD} < 10\%$ $\Delta T_J < 150$ °C	—	—	10	
V_{OFFSET}	Conversion offset[6, 7]	Before calibration (applies to all gain settings: 1, 2, 4, 8, 16)	—	10*(1+1/gain)	20	mV
		After calibration $\Delta V_{DDA\_SD} < 10\%$ $\Delta T_J < 50$ °C	—	—	5	
		After calibration $\Delta V_{DDA\_SD} < 10\%$ $\Delta T_J < 100$ °C	—	—	7.5	
		After calibration $\Delta V_{DDA\_SD} < 10\%$ $\Delta T_J < 150$ °C	—	—	10	

Table continues on the next page...

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$SNR_{DIFF150}$	Signal to noise ratio in differential mode, 150 Ksps output rate	$4.5\ V < V_{DDA\_SD} < 5.5\ V$[8, 9] $V_{RH\_SD} = V_{DDA\_SD}$ GAIN = 1	80	—	—	dB
		$4.5\ V < V_{DDA\_SD} < 5.5\ V$[8, 9] $V_{RH\_SD} = V_{DDA\_SD}$ GAIN = 2	77	—	—	
		$4.5\ V < V_{DDA\_SD} < 5.5\ V$[8, 9] $V_{RH\_SD} = V_{DDA\_SD}$ GAIN = 4	74	—	—	
		$4.5\ V < V_{DDA\_SD} < 5.5\ V$[8, 9] $V_{RH\_SD} = V_{DDA\_SD}$ GAIN = 8	71	—	—	
		$4.5\ V < V_{DDA\_SD} < 5.5\ V$[8, 9] $V_{RH\_SD} = V_{DDA\_SD}$ GAIN = 16	68	—	—	
$SNR_{DIFF333}$	Signal to noise ratio in differential mode, 333 Ksps output rate	$4.5\ V < V_{DDA\_SD} < 5.5\ V$[8, 9] $V_{RH\_SD} = V_{DDA\_SD}$ GAIN = 1	71	—	—	dB
		$4.5\ V < V_{DDA\_SD} < 5.5\ V$[8, 9] $V_{RH\_SD} = V_{DDA\_SD}$ GAIN = 2	70	—	—	
		$4.5\ V < V_{DDA\_SD} < 5.5\ V$[8, 9] $V_{RH\_SD} = V_{DDA\_SD}$ GAIN = 4	68	—	—	
		$4.5\ V < V_{DDA\_SD} < 5.5\ V$[8, 9] $V_{RH\_SD} = V_{DDA\_SD}$ GAIN = 8	65	—	—	
		$4.5\ V < V_{DDA\_SD} < 5.5\ V$[8, 9] $V_{RH\_SD} = V_{DDA\_SD}$ GAIN = 16	62	—	—	

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Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
SNR_{SE150}	Signal to noise ratio in single ended mode, 150 Ksps output rate	$4.5\ V < V_{DDA\_SD} < 5.5\ V$[8, 9] $V_{RH\_SD} = V_{DDA\_SD}$ GAIN = 1	72	—	—	dB
		$4.5\ V < V_{DDA\_SD} < 5.5\ V$[8, 9] $V_{RH\_SD} = V_{DDA\_SD}$ GAIN = 2	69	—	—	
		$4.5\ V < V_{DDA\_SD} < 5.5\ V$[8, 9] $V_{RH\_SD} = V_{DDA\_SD}$ GAIN = 4	66	—	—	
		$4.5\ V < V_{DDA\_SD} < 5.5\ V$[8, 9] $V_{RH\_SD} = V_{DDA\_SD}$ GAIN = 8	62	—	—	
		$4.5\ V < V_{DDA\_SD} < 5.5\ V$[8, 9] $V_{RH\_SD} = V_{DDA\_SD}$ GAIN = 16	54	—	—	
$SINAD_{DIFF150}$	Signal to noise and distortion ratio in differential mode, 150 Ksps output rate	Gain = 1 $4.5\ V < V_{DDA\_SD} < 5.5\ V$ $V_{RH\_SD} = V_{DDA\_SD}$	72	—	—	dBFS
		Gain = 2 $4.5\ V < V_{DDA\_SD} < 5.5\ V$ $V_{RH\_SD} = V_{DDA\_SD}$	72	—	—	
		Gain = 4 $4.5\ V < V_{DDA\_SD} < 5.5\ V$ $V_{RH\_SD} = V_{DDA\_SD}$	69	—	—	
		Gain = 8 $4.5\ V < V_{DDA\_SD} < 5.5\ V$ $V_{RH\_SD} = V_{DDA\_SD}$	68.8	—	—	
		Gain = 16 $4.5\ V < V_{DDA\_SD} < 5.5\ V$ $V_{RH\_SD} = V_{DDA\_SD}$	64.8	—	—	

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Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$SINAD_{DIFF333}$	Signal to noise and distortion ratio in differential mode, 333 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V $V_{RH\_SD} = V_{DDA\_SD}$	66	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V $V_{RH\_SD} = V_{DDA\_SD}$	66	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V $V_{RH\_SD} = V_{DDA\_SD}$	63	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V $V_{RH\_SD} = V_{DDA\_SD}$	62	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V $V_{RH\_SD} = V_{DDA\_SD}$	59	—	—	
$SINAD_{SE150}$	Signal to noise and distortion ratio in single-ended mode, 150 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V $V_{RH\_SD} = V_{DDA\_SD}$	66	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V $V_{RH\_SD} = V_{DDA\_SD}$	66	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V $V_{RH\_SD} = V_{DDA\_SD}$	63	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V $V_{RH\_SD} = V_{DDA\_SD}$	62	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V $V_{RH\_SD} = V_{DDA\_SD}$	54	—	—	

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Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$THD_{DIFF150}$	Total harmonic distortion in differential mode, 150 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V $V_{RH\_SD} = V_{DDA\_SD}$	65	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V $V_{RH\_SD} = V_{DDA\_SD}$	68	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V $V_{RH\_SD} = V_{DDA\_SD}$	74	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V $V_{RH\_SD} = V_{DDA\_SD}$	80	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V $V_{RH\_SD} = V_{DDA\_SD}$	80	—	—	
$THD_{DIFF333}$	Total harmonic distortion in differential mode, 333 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V $V_{RH\_SD} = V_{DDA\_SD}$	65	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V $V_{RH\_SD} = V_{DDA\_SD}$	68	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V $V_{RH\_SD} = V_{DDA\_SD}$	74	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V $V_{RH\_SD} = V_{DDA\_SD}$	80	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V $V_{RH\_SD} = V_{DDA\_SD}$	80	—	—	

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Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
THD_{SE150}	Total harmonic distortion in single-ended mode, 150 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	66	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	
SFDR	Spurious free dynamic range	Any GAIN	60	—	—	dB
Z_{DIFF}	Differential input impedance[10, 11]	GAIN = 1	1000	1250	1500	kΩ
		GAIN = 2	600	800	1000	
		GAIN = 4	300	400	500	
		GAIN = 8	200	250	300	
		GAIN = 16	200	250	300	
Z_{CM}	Common Mode input impedance[11, 12]	GAIN = 1	1400	1800	2200	kΩ
		GAIN = 2	1000	1300	1600	
		GAIN = 4	700	950	1150	
		GAIN = 8	500	650	800	
		GAIN = 16	500	650	800	
R_{BIAS}	Bare bias resistance	—	110	144	180	kΩ
ΔV_{INTCM}	Common Mode input reference voltage[13]	—	–12	—	+12	%
V_{BIAS}	Bias voltage	—	—	$V_{RH\_SD}/2$	—	V
δV_{BIAS}	Bias voltage accuracy	—	–2.5	—	+2.5	%
CMRR	Common mode rejection ratio	—	20	—	—	dB
R_{Caaf}	Anti-aliasing filter	External series resistance	—	—	20	kΩ
		Filter capacitances	220	—	—	pF
$f_{PASSBAND}$	Pass band[9]	—	0.01	—	0.333 * f_{ADCD_S}	kHz
δ_{RIPPLE}	Pass band ripple[14]	0.333 * f_{ADCD_S}	–1	—	1	%

Table continues on the next page...

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$F_{rolloff}$	Stop band attenuation	[0.5 * f_{ADCD_S}, 1.0 * f_{ADCD_S}]	40	—	—	dB
		[1.0 * f_{ADCD_S}, 1.5 * f_{ADCD_S}]	45	—	—	
		[1.5 * f_{ADCD_S}, 2.0 * f_{ADCD_S}]	50	—	—	
		[2.0 * f_{ADCD_S}, 2.5 * f_{ADCD_S}]	55	—	—	
		[2.5 * f_{ADCD_S}, f_{ADCD_M}/2]	60	—	—	
δ_{GROUP}	Group delay	Within pass band: Tclk is f_{ADCD_M} / 2	—	—	—	—
		OSR = 24	—	—	235.5	Tclk
		OSR = 28	—	—	275	
		OSR = 32	—	—	314.5	
		OSR = 36	—	—	354	
		OSR = 40	—	—	393.5	
		OSR = 44	—	—	433	
		OSR = 48	—	—	472.5	
		OSR = 56	—	—	551.5	
		OSR = 64	—	—	630.5	
		OSR = 72	—	—	709.5	
		OSR = 75	—	—	696	
		OSR = 80	—	—	788.5	
		OSR = 88	—	—	867.5	
		OSR = 96	—	—	946.5	
		OSR = 112	—	—	1104.5	
		OSR = 128	—	—	1262.5	
		OSR = 144	—	—	1420.5	
		OSR = 160	—	—	1578.5	
		OSR = 176	—	—	1736.5	
		OSR = 192	—	—	1894.5	
		OSR = 224	—	—	2210.5	
		OSR = 256	—	—	2526.5	
		Distortion within pass band	–0.5/ f_{ADCD_S}	—	+0.5/ f_{ADCD_S}	—
f_{HIGH}	High pass filter 3 dB frequency	Enabled	—	10e–5* fADCD_S	—	—
$t_{STARTUP}$	Startup time from power down state	—	—	—	100	μs
$t_{LATENCY}$	Latency between input data and converted data when input mux does not change[15]	HPF = ON	—	—	δ_{GROUP} + f_{ADCD_S}	—
		HPF = OFF	—	—	δ_{GROUP}	

Table continues on the next page...

Table 18. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$t_{SETTLING}$	Settling time after mux change	Analog inputs are muxed HPF = ON	—	—	$2{*}\delta_{GROUP}$ + $3{*}f_{ADCD\_S}$	—
		HPF = OFF	—	—	$2{*}\delta_{GROUP}$ + $2{*}f_{ADCD\_S}$	
$t_{ODRECOVERY}$	Overdrive recovery time	After input comes within range from saturation HPF = ON	—	—	$2{*}\delta_{GROUP}$ + f_{ADCD_S}	—
		HPF = OFF	—	—	$2{*}\delta_{GROUP}$	
C_{S_D}	SDADC sampling capacitance after sampling switch[16]	GAIN = 1, 2, 4, 8	—	—	75*GAIN	fF
		GAIN = 16	—	—	600	fF
I_{BIAS}	Bias consumption	At least one SDADC enabled	—	—	3.5	mA
I_{ADV_D}	SDADC supply consumption	Per SDADC enabled	—	—	4.325	mA
I_{ADR_D}	SDADC reference current consumption	Per SDADC enabled	—	—	20	μA

1. For input voltage above the maximum and below the clamp voltage of the input pad, there is no latch-up concern, and the signal will only be "clipped."
2. VINP is the input voltage applied to the positive terminal of the SDADC
3. VINM is the input voltage applied to the negative terminal of the SDADC
4. Sampling is generated internally $f_{SAMPLING} = f_{ADCD\_M}/2$
5. For Gain = 16, SDADC resolution is 15 bit.
6. Calibration of gain is possible when gain = 1. Offset Calibration should be done with respect to $0.5{*}V_{RH\_SD}$ for differential mode and single ended mode with negative input = $0.5{*}V_{RH\_SD}$. Offset Calibration should be done with respect to 0 for single ended mode with negative input = 0. Both Offset and Gain Calibration is guaranteed for +/–5% variation of V_{RH_SD}, +/–10% variation of V_{DDA_SD}, +/–50 C temperature variation.
7. Offset and gain error due to temperature drift can occur in either direction (+/–) for each of the SDADCs on the device.
8. SDADC is functional in the range $3.6\text{ V} < V_{DDA\_SD} < 4.0\text{ V}$: SNR parameter degrades by 3 dB. SDADC is functional in the range $3.0\text{ V} < V_{RH\_SD} < 4.0\text{ V}$: SNR parameter degrades by 9 dB.
9. SNR values guaranteed only if external noise on the ADC input pin is attenuated by the required SNR value in the frequency range of $f_{ADCD\_M} – f_{ADCD\_S}$ to $f_{ADCD\_M} + f_{ADCD\_S}$, where f_{ADCD_M} is the input sampling frequency and f_{ADCD_S} is the output sample frequency. A proper external input filter should be used to remove any interfering signals in this frequency range.
10. Input impedance in differential mode $Z_{IN} = Z_{DIFF}$
11. Input impedance given at f_{ADCD_M} = 16 MHz. Impedance is inversely proportional to SDADC clock frequency. $Z_{DIFF}(f_{ADCD\_M}) = (16\text{ MHz} / f_{ADCD\_M}) * Z_{DIFF}$, $Z_{CM}(f_{ADCD\_M}) = (16\text{ MHz} / f_{ADCD\_M}) * Z_{CM}$.
12. Input impedance in single-ended mode $Z_{IN} = (2 * Z_{DIFF} * Z_{CM}) / (Z_{DIFF} + Z_{CM})$
13. V_{INTCM} is the Common Mode input reference voltage for the SDADC. It has a nominal value of $(V_{RH\_SD} - V_{RL\_SD}) / 2$.
14. The ±1% passband ripple specification is equivalent to $20 * \log_{10}(0.99) = 0.087$ dB.
15. Propagation of the information from the pin to the register CDR[CDATA] and the flags SFR[DFEF] and SFR[DFFF] is given by the different modules that must be crossed: delta/sigma filters, high pass filter, FIFO module, and clock domain synchronizers. The time elapsed between data availability at the pin and internal SDADC module registers is given by the following formula, where f_{ADCD_S} is the frequency of the sampling clock, f_{ADCD_M} is the frequency of the modulator, and $f_{FM\_PER\_CLK}$ is the frequency of the peripheral bridge clock feeds to the SDADC module:

    REGISTER LATENCY = $t_{LATENCY} + 0.5/f_{ADCD\_S} + 2\ ({\sim}{+}1)/f_{ADCD\_M} + 2({\sim}{+}1)f_{FM\_PER\_CLK}$

    The (~+1) symbol refers to the number of clock cycles uncertainty (from 0 to 1 clock cycle) to be added due to resynchronization of the signal during clock domain crossing.

Some further latency may be added by the target module (core, DMA, interrupt) controller to process the data received from the SDADC module.

16. This capacitance does not include pin capacitance, that can be considered together with external capacitance, before sampling switch.

3.9 Temperature Sensor

The following table describes the Temperature Sensor electrical characteristics.

Table 19. Temperature Sensor electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
—	Temperature monitoring range	—	–40	—	150	°C
T_{SENS}	Sensitivity	—	—	5.18	—	mV/°C
T_{ACC}	Accuracy	–40°C < T_J < 150°C	–5	—	5	°C
I_{TEMP_SENS}	V_{DDA_EQA} power supply current, per Temp Sensor	—	—	—	700	µA

3.10 LVDS Fast Asynchronous Serial Transmission (LFAST) pad electrical characteristics

The LFAST pad electrical characteristics apply to the SIPI interface on the chip. The same LVDS pad is used for the Microsecond Channel (MSC) and DSPI LVDS interfaces, with different characteristics given in the following tables.

3.10.1 LFAST interface timing diagrams

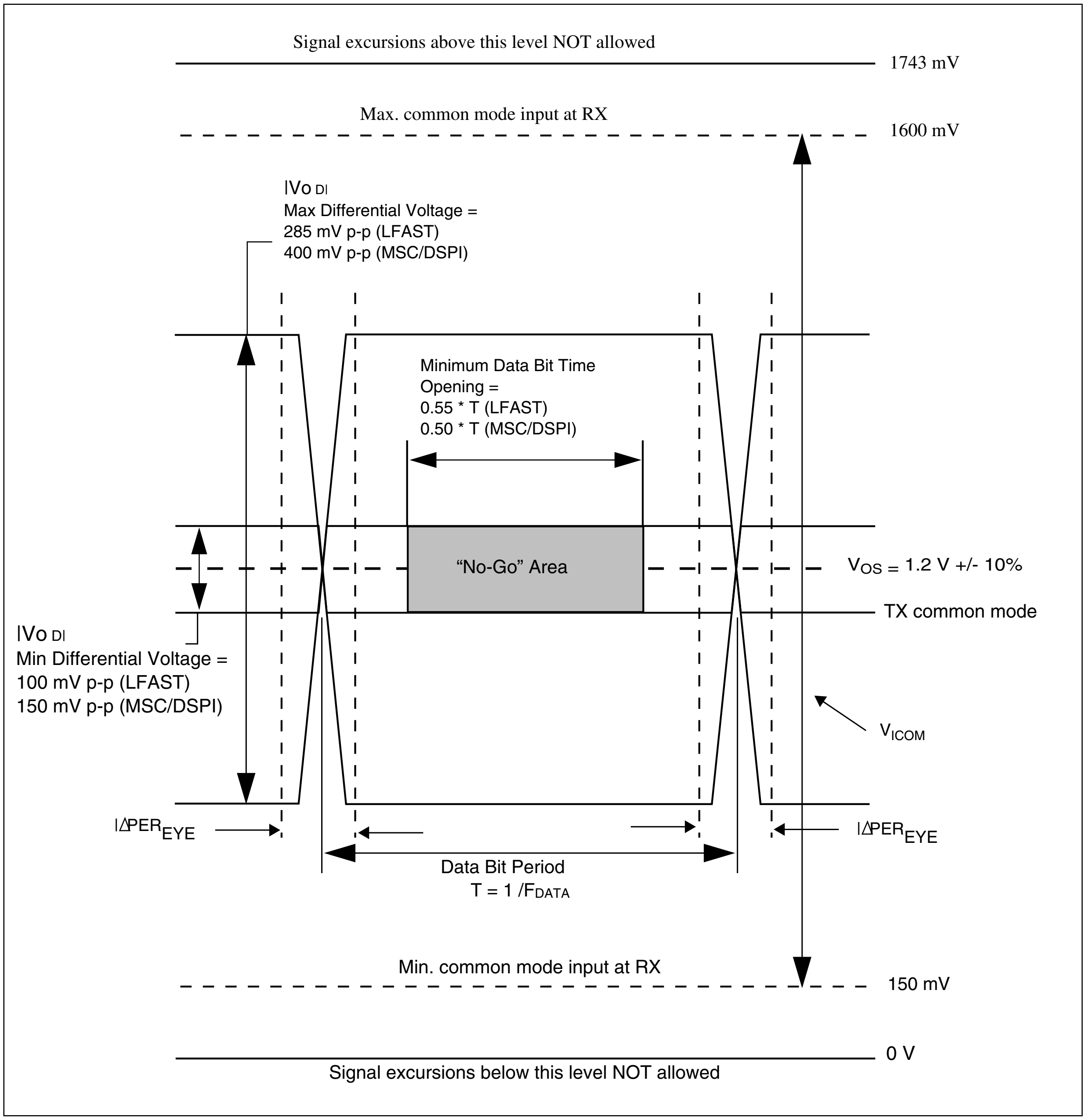


Figure 8. LFAST and MSC/DSPI LVDS timing definition

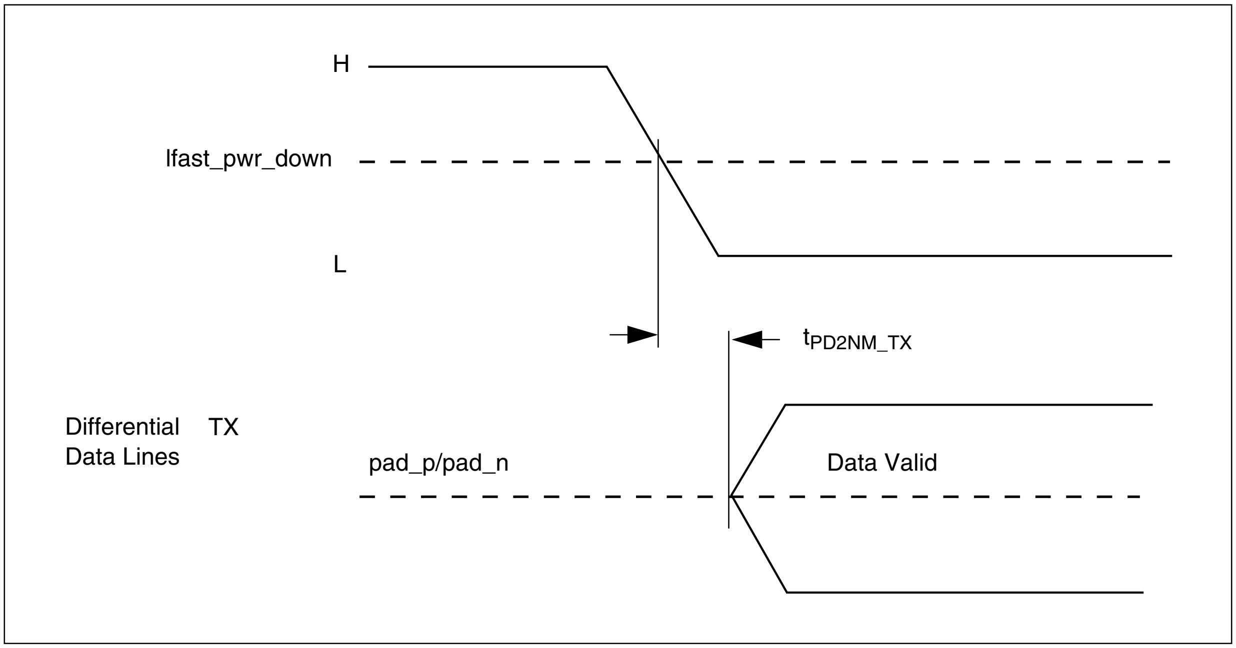


Figure 9. Power-down exit time

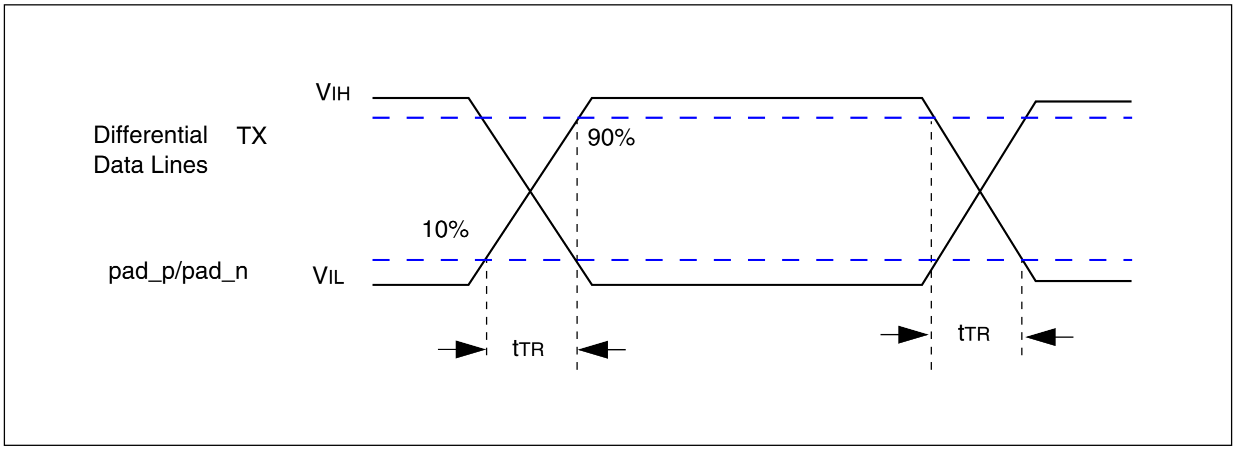


Figure 10. Rise/fall time

3.10.2 LFAST and MSC/DSPI LVDS interface electrical characteristics

The following table contains the electrical characteristics for the LFAST interface.

Table 20. LVDS pad startup and receiver electrical characteristics[1]

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
STARTUP[2],[3]						
t_{STRT_BIAS}	Bias current reference startup time[4]	—	—	0.5	4	μs

Table continues on the next page...

Table 20. LVDS pad startup and receiver electrical characteristics[1] (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
t_{PD2NM_TX}	Transmitter startup time (power down to Normal mode)[5]	—	—	0.4	2.75	μs
t_{SM2NM_TX}	Transmitter startup time (Sleep mode to Normal mode)[6]	Not applicable to the MSC/DSPI LVDS pad	—	0.2	0.5	μs
t_{PD2NM_RX}	Receiver startup time (power down to Normal mode)[7]	—	—	20	40	ns
t_{PD2SM_RX}	Receiver startup time (power down to Sleep mode)[8]	Not applicable to the MSC/DSPI LVDS pad	—	20	50	ns
I_{LVDS_BIAS}	LVDS bias current consumption	Tx or Rx enabled	—	—	0.95	mA
TRANSMISSION LINE CHARACTERISTICS (PCB Track)						
Z_0	Transmission line characteristic impedance	—	47.5	50	52.5	Ω
Z_{DIFF}	Transmission line differential impedance	—	95	100	105	Ω
RECEIVER						
V_{ICOM}	Common mode voltage	—	0.15[9]	—	1.6[10]	V
$\|\Delta VI\|$	Differential input voltage	—	100	—	—	mV
V_{HYS}	Input hysteresis	—	25	—	—	mV
R_{IN}	Terminating resistance	V_{DDEH} = 3.0 V to 5.5 V	80	125	150	Ω
C_{IN}	Differential input capacitance[11]	—	—	3.5	6.0	pF
I_{LVDS_RX}	Receiver DC current consumption	Enabled	—	—	0.5	mA

1. The LVDS pad startup and receiver electrical characteristics in this table apply to both the LFAST and the MSC/DSPI LVDS pad except where noted in the conditions.
2. All startup times are defined after a 2 peripheral bridge clock delay from writing to the corresponding enable bit in the LVDS control registers (LCR) of the LFAST and High-Speed Debug modules.
3. Startup times are valid for the maximum external loads CL defined in both the LFAST/HSD and MSC/DSPI transmitter electrical characteristic tables.
4. Bias startup time is defined as the time taken by the current reference block to reach the settling bias current after being enabled.
5. Total transmitter startup time from power down to normal mode is t_{STRT_BIAS} + t_{PD2NM_TX} + 2 peripheral bridge clock periods.
6. Total transmitter startup time from sleep mode to normal mode is t_{SM2NM_TX} + 2 peripheral bridge clock periods. Bias block remains enabled in sleep mode.
7. Total receiver startup time from power down to normal mode is t_{STRT_BIAS} + t_{PD2NM_RX} + 2 peripheral bridge clock periods.
8. Total receiver startup time from power down to sleep mode is t_{PD2SM_RX} + 2 peripheral bridge clock periods. Bias block remains enabled in sleep mode.
9. Absolute min = 0.15 V – (285 mV/2) = 0 V
10. Absolute max = 1.6 V + (285 mV/2) = 1.743 V
11. Total internal capacitance including receiver and termination, co-bonded GPIO pads, and package contributions. For bare die devices, subtract the package value given in Figure 11.

Table 21. LFAST transmitter electrical characteristics[1]

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{DATA}	Data rate	—	—	—	240	Mbps

Table continues on the next page...

Table 21. LFAST transmitter electrical characteristics[1] (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{OS}	Common mode voltage	—	1.08	—	1.32	V
$\lvert V_{OD} \rvert$	Differential output voltage swing (terminated)[2,3]	—	110	200	285	mV
t_{TR}	Rise/fall time (10% – 90% of swing)[2,3]	—	0.26	—	1.5	ns
C_L	External lumped differential load capacitance[2]	V_{DDE} = 4.5 V	—	—	12.0	pF
		V_{DDE} = 3.0 V	—	—	8.5	
I_{LVDS_TX}	Transmitter DC current consumption	Enabled	—	—	3.2	mA

1. The LFAST pad electrical characteristics are based on worst-case internal capacitance values shown in Figure 11.
2. Valid for maximum data rate f_{DATA}. Value given is the capacitance on each terminal of the differential pair, as shown in Figure 11.
3. Valid for maximum external load CL.

Table 22. MSC/DSPI LVDS transmitter electrical characteristics[1]

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{DATA}	Data rate	—	—	—	80	Mbps
V_{OS}	Common mode voltage	—	1.08	—	1.32	V
$\lvert V_{OD} \rvert$	Differential output voltage swing (terminated)[2,3]	—	150	200	400	mV
t_{TR}	Rise/Fall time (10%–90% of swing)[2,3]	—	0.8	—	4.0	ns
C_L	External lumped differential load capacitance[2]	V_{DDE} = 4.5 V	—	—	50	pF
		V_{DDE} = 3.0 V	—	—	39	
I_{LVDS_TX}	Transmitter DC current consumption	Enabled	—	—	4.0	mA

1. The MSC and DSPI LVDS pad electrical characteristics are based on the application circuit and typical worst-case internal capacitance values given in Figure 11.
2. Valid for maximum data rate f_{DATA}. Value given is the capacitance on each terminal of the differential pair, as shown in Figure 11.
3. Valid for maximum external load C_L.

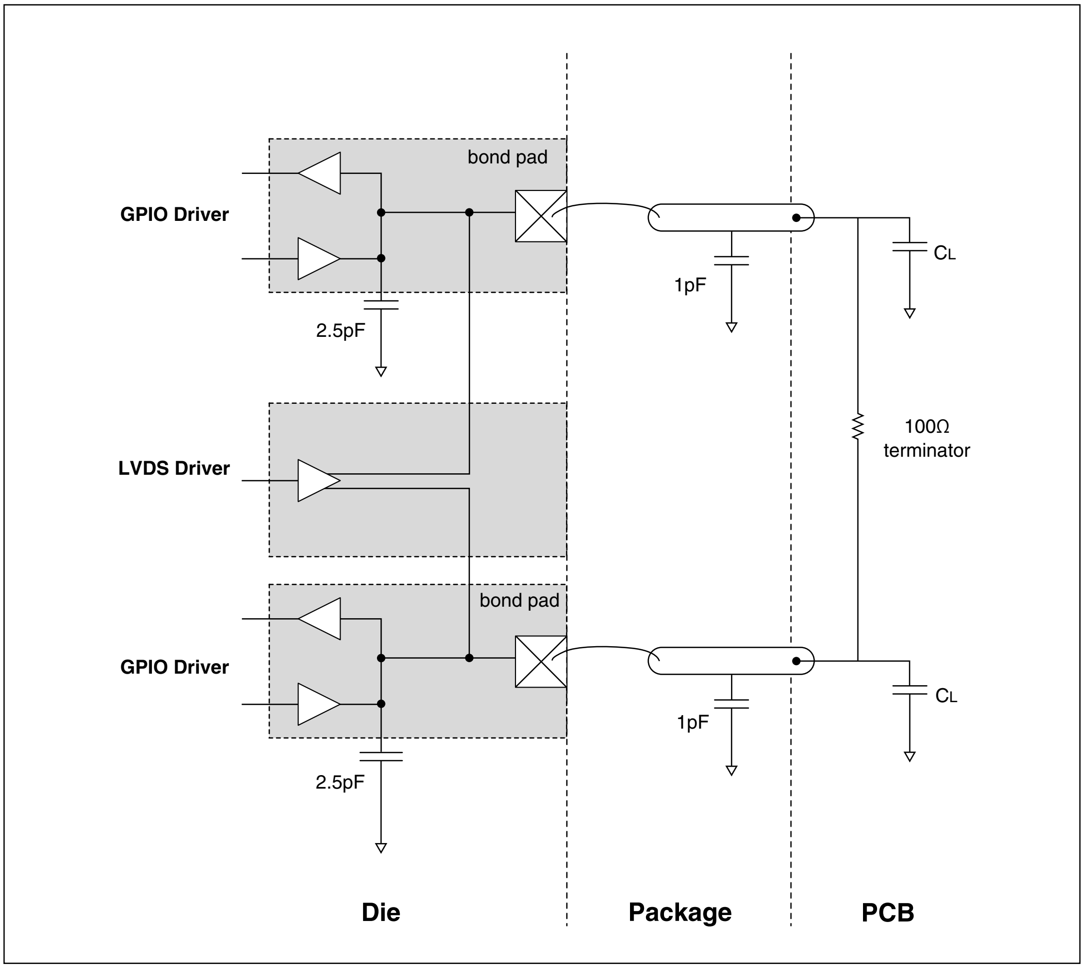


Figure 11. LVDS pad external load diagram

3.10.3 LFAST PLL electrical characteristics

The following table contains the electrical characteristics for the LFAST PLL.

Table 23. LFAST PLL electrical characteristics[1]

Symbol	Parameter	Conditions	Value			Unit
			Min	Nominal	Max	
f_{RF_REF}	PLL reference clock frequency	—	10	—	26	MHz
ERR_{REF}	PLL reference clock frequency error	—	–1	—	1	%
DC_{REF}	PLL reference clock duty cycle	—	45	—	55	%
PN	Integrated phase noise (single side band)	f_{RF_REF} = 20 MHz	—	—	–58	dBc
		f_{RF_REF} = 10 MHz	—	—	–64	
f_{VCO}	PLL VCO frequency	—	—	480[2]	—	MHz
t_{LOCK}	PLL phase lock[3]	—	—	—	40	μs

Table continues on the next page...

Table 23. LFAST PLL electrical characteristics[1] (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Nominal	Max	
ΔPER_{REF}	Input reference clock jitter (peak to peak)	Single period, f_{RF_REF} = 10 MHz	—	—	300	ps
		Long term, f_{RF_REF} = 10 MHz	–500	—	500	
ΔPER_{EYE}	Output Eye Jitter (peak to peak)[4]	—	—	—	400	ps

1. The specifications in this table apply to both the interprocessor bus and debug LFAST interfaces.
2. The 480 MHz frequency is achieved with a 10 MHz or 20 MHz reference clock. With a 13 MHz or 26 MHz reference, the VCO frequency is 468 MHz.
3. The time from the PLL enable bit register write to the start of phase locks is maximum 2 clock cycles of the peripheral bridge clock that is connected to the PLL on the device.
4. Measured at the transmitter output across a 100 Ohm termination resistor on a device evaluation board. See Figure 11.

3.11 Power management: PMC, POR/LVD, power sequencing

3.11.1 Power management electrical characteristics

The power management module monitors the different power supplies. It also generates the internal supplies that are required for correct device functionality. The power management is supplied by the V_{DDPMC} supply.

3.11.1.1 LDO mode recommended power transistors

Only specific orderable part numbers of MPC5777C support LDO regulation mode. See Ordering information for MPC5777C parts that support this regulation mode.

The following NPN transistors are recommended for use with the on-chip LDO voltage regulator controller: ON Semiconductor™ NJD2873. The collector of the external transistor is preferably connected to the same voltage supply source as the output stage of the regulator.

The following table describes the characteristics of the power transistors.

Table 24. Recommended operating characteristics

Symbol	Parameter	Value	Unit
h_{FE}	DC current gain (Beta)	60-550	—
P_D	Absolute minimum power dissipation	1.60	W
I_{CMaxDC}	Maximum DC collector current	2.0	A
VCE_{SAT}	Collector to emitter saturation voltage	300	mV
V_{BE}	Base to emitter voltage	0.95	V
V_c	Minimum voltage at transistor collector	2.5	V

The following table shows the recommended components to be used in LDO regulation mode.

Table 25. Recommended operating characteristics

Part name	Part type	Nominal	Description
Q1	NPN BJT	h_{FE} = 400	NJD2873: ON Semiconductor LDO voltage regulator controller (VRC)
CI	Capacitor	4.7 µF - 20 V	Ceramic capacitor, total ESR < 70 mΩ
CE	Capacitor	0.047–0.049 µF - 7 V	Ceramic—one capacitor for each V_{DD} pin
CV	Capacitor	22 µF - 20 V	Ceramic V_{DDPMC} (optional 0.1 µF)
CD	Capacitor	22 µF - 20 V	Ceramic supply decoupling capacitor, ESR < 50 mΩ (as close as possible to NPN collector)
CB	Capacitor	0.1 µF - 7 V	Ceramic V_{DDPWR}
R	Resistor	Application specific	Optional; reduces thermal loading on the NPN with high V_{DDPMC} levels

The following diagram shows the LDO configuration connection.

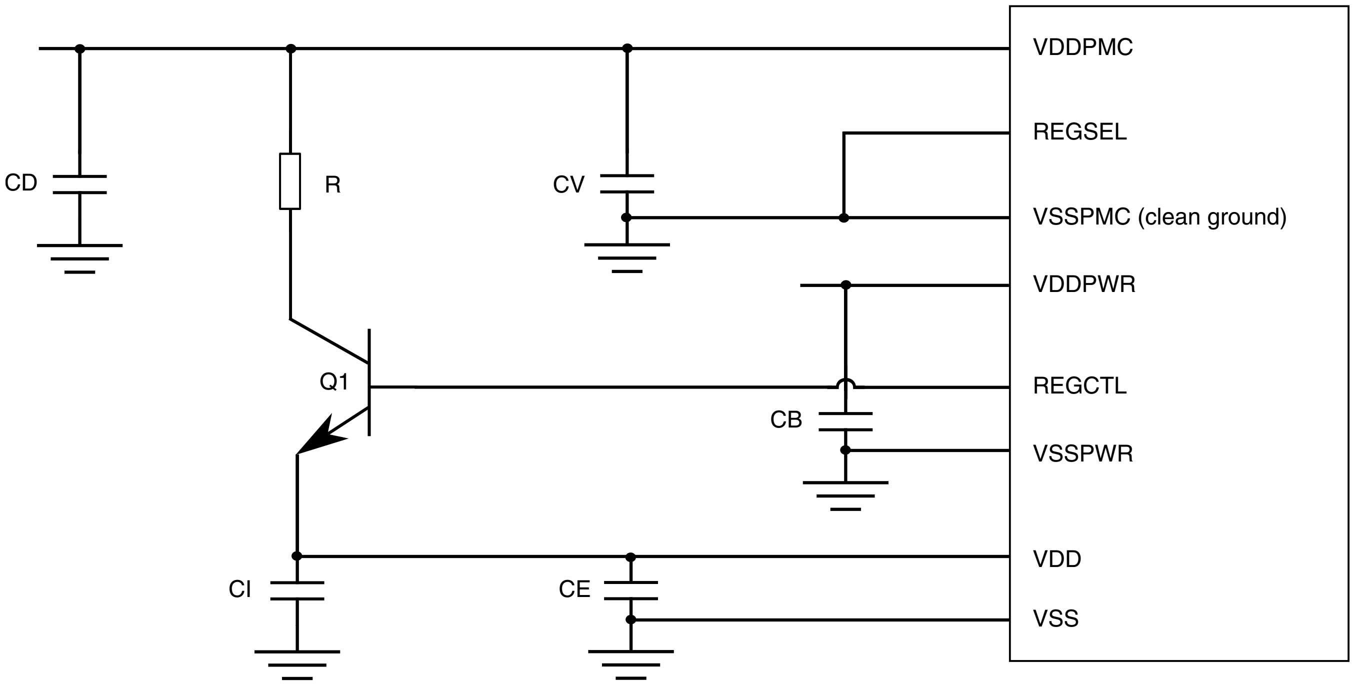


Figure 12. VRC 1.2 V LDO configuration

3.11.1.2 SMPS mode recommended external components and characteristics

The following table shows the recommended components to be used in SMPS regulation mode.

Table 26. Recommended operating characteristics

Part name	Part type	Nominal	Description
Q1	p-MOS	3 A - 20 V	SQ2301ES / FDC642P or equivalent: low threshold p-MOS, Vth < 2.0 V, Rdson @ 4.5 V < 100 mΩ, Cg < 5 nF
D1	Schottky	2 A - 20 V	SS8P3L or equivalent: Vishay™ low Vf Schottky diode
L	Inductor	3–4 μH - 1.5 A	Buck shielded coil low ESR
CI	Capacitor	22 μF - 20 V	Ceramic capacitor, total ESR < 70 mΩ
CE	Capacitor	0.1 μF - 7 V	Ceramic—one capacitor for each V_{DD} pin
CV	Capacitor	22 μF - 20 V	Ceramic V_{DDPMC} (optional 0.1 μF capacitor in parallel)
CD	Capacitor	22 μF - 20 V	Ceramic supply decoupling capacitor, ESR < 50 mΩ (as close as possible to the p-MOS source)
R	Resistor	2.0-4.7 kΩ	Pullup for power p-MOS gate
CB	Capacitor	22 μF - 20 V	Ceramic, connect 100 nF capacitor in parallel (as close as possible to package to reduce current loop from V_{DDPWR} to V_{SSPWR})

The following diagram shows the SMPS configuration connection.

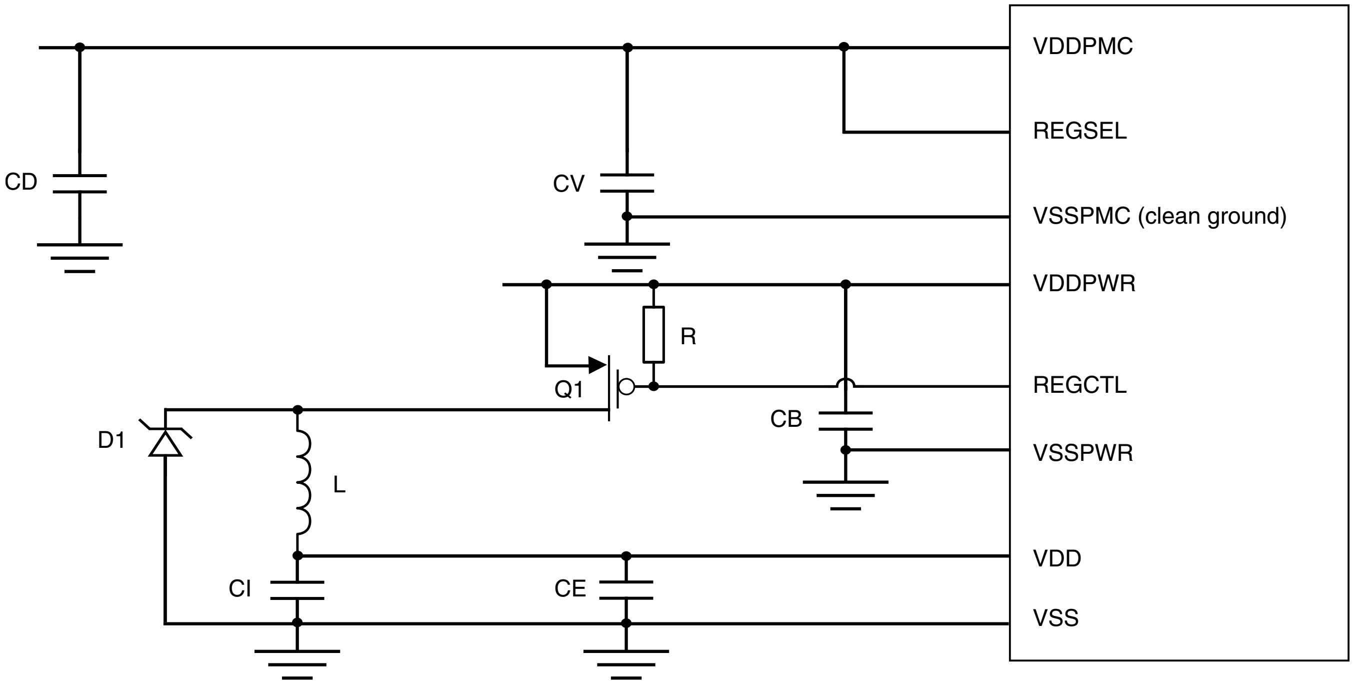


Figure 13. SMPS configuration

NOTE

The REGSEL pin is tied to V_{DDPMC} to select SMPS. If REGSEL is 0, the chip boots with the linear regulator.

See Power sequencing requirements for details about V_{DDPMC} and V_{DDPWR}.

The SMPS regulator characteristics appear in the following table.

Table 27. SMPS electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$SMPS_{CLOCK}$	SMPS oscillator frequency	Trimmed	825	1000	1220	kHz
$SMPS_{SLOPE}$	SMPS soft-start ramp slope	—	0.01	0.025	0.05	V/µs
$SMPS_{EFF}$	SMPS typical efficiency	—	—	70	—	%

3.11.2 Power management integration

To ensure correct functionality of the device, use the following recommended integration scheme for LDO mode.

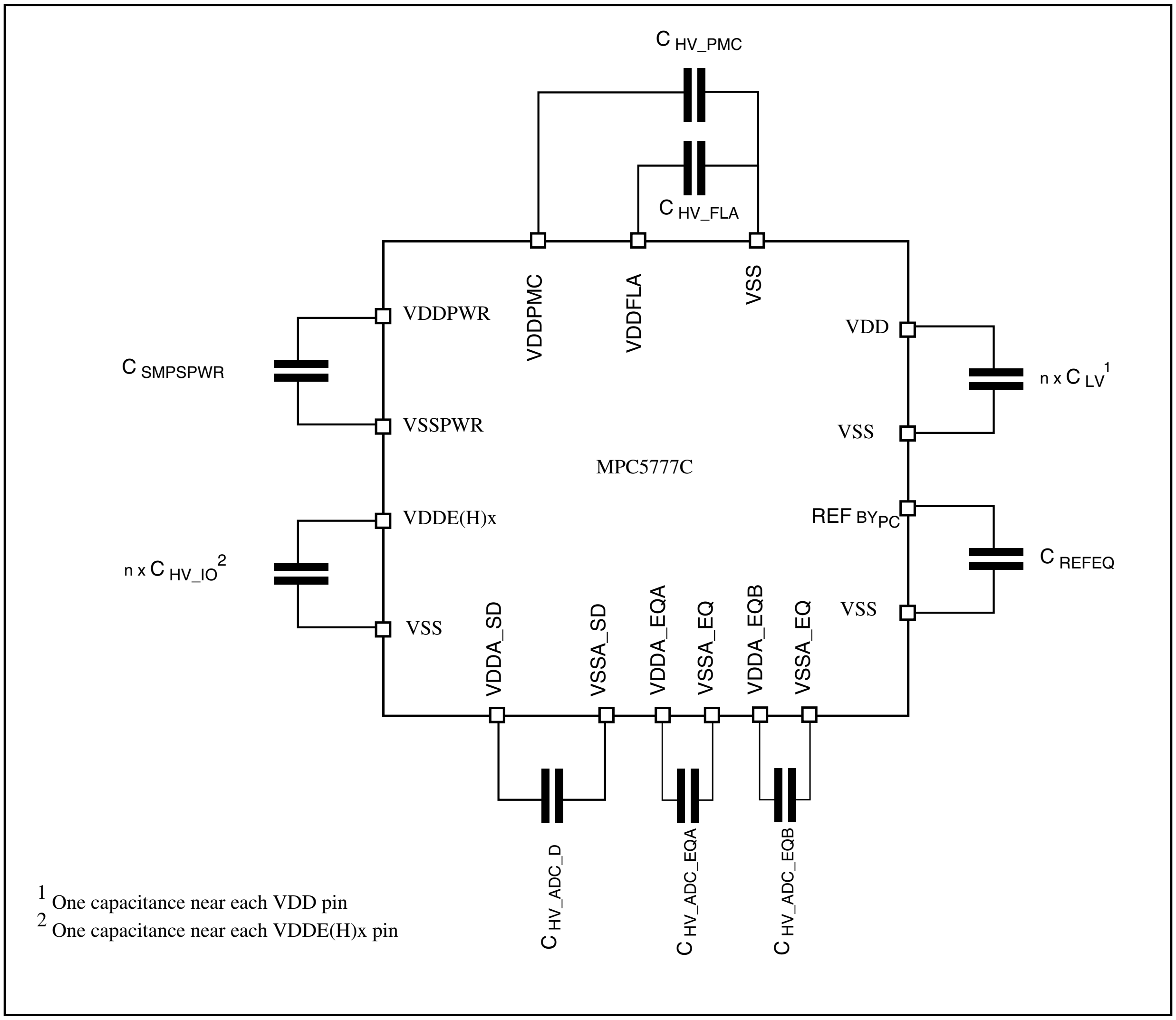


Figure 14. Recommended supply pin circuits

The following table describes the supply stability capacitances required on the device for proper operation.

Table 28. Device power supply integration

Symbol	Parameter	Conditions	Value[1]			Unit
			Min	Typ	Max	
C_{LV}	Minimum V_{DD} external bulk capacitance[2, 3]	LDO mode	4.7	—	—	µF
		SMPS mode	22	—	—	µF
$C_{SMPSPWR}$	Minimum SMPS driver supply capacitance	—	22	—	—	µF
C_{HV_PMC}	Minimum V_{DDPMC} external bulk capacitance[4, 5]	LDO mode	22	—	—	µF
		SMPS mode	22	—	—	µF
C_{HV_IO}	Minimum V_{DDEx}/V_{DDEHx} external capacitance[2]	—	—	4.7[6]	—	µF
C_{HV_FLA}	Minimum V_{DD_FLA} external capacitance[7]	—	1.0	2.0	—	µF
$C_{HV\_ADC\_EQA/B}$	Minimum $V_{DDA\_EQA/B}$ external capacitance[8]	—	0.01	—	—	µF
C_{REFEQ}	Minimum $REF_{BYPCA/B}$ external capacitance[9]	—	0.01	—	—	µF
$C_{HV\_ADC\_SD}$	Minimum V_{DDA_SD} external capacitance[10]	—	1.0	2.2	—	µF

1. See Figure 14 for capacitor integration.
2. Recommended X7R or X5R ceramic low ESR capacitors, ±15% variation over process, voltage, temperature, and aging.
3. Each V_{DD} pin requires both a 47 nF and a 0.01 µF capacitor for high-frequency bypass and EMC requirements.
4. Recommended X7R or X5R ceramic low ESR capacitors, ±15% variation over process, voltage, temperature, and aging.
5. Each V_{DDPMC} pin requires both a 47 nF and a 0.01 µF capacitor for high-frequency bypass and EMC requirements.
6. The actual capacitance should be selected based on the I/O usage in order to keep the supply voltage within its operating range.
7. The recommended flash regulator composition capacitor is 2.0 µF typical X7R or X5R, with -50% and +35% as min and max. This puts the min cap at 0.75 µF.
8. For noise filtering it is recommended to add a high frequency bypass capacitance of 0.1 µF between $V_{DDA\_EQA/B}$ and V_{SSA_EQ}.
9. For noise filtering it is recommended to add a high frequency bypass capacitance of 0.1 µF between $REF_{BYPCA/B}$ and V_{SS}.
10. For noise filtering it is recommended to add a high frequency bypass capacitance of 0.1 µF between V_{DDA_SD} and V_{SSA_SD}.

3.11.3 Device voltage monitoring

The LVD/HVDs for the device and their levels are given in the following table. Voltage monitoring threshold definition is provided in the following figure.

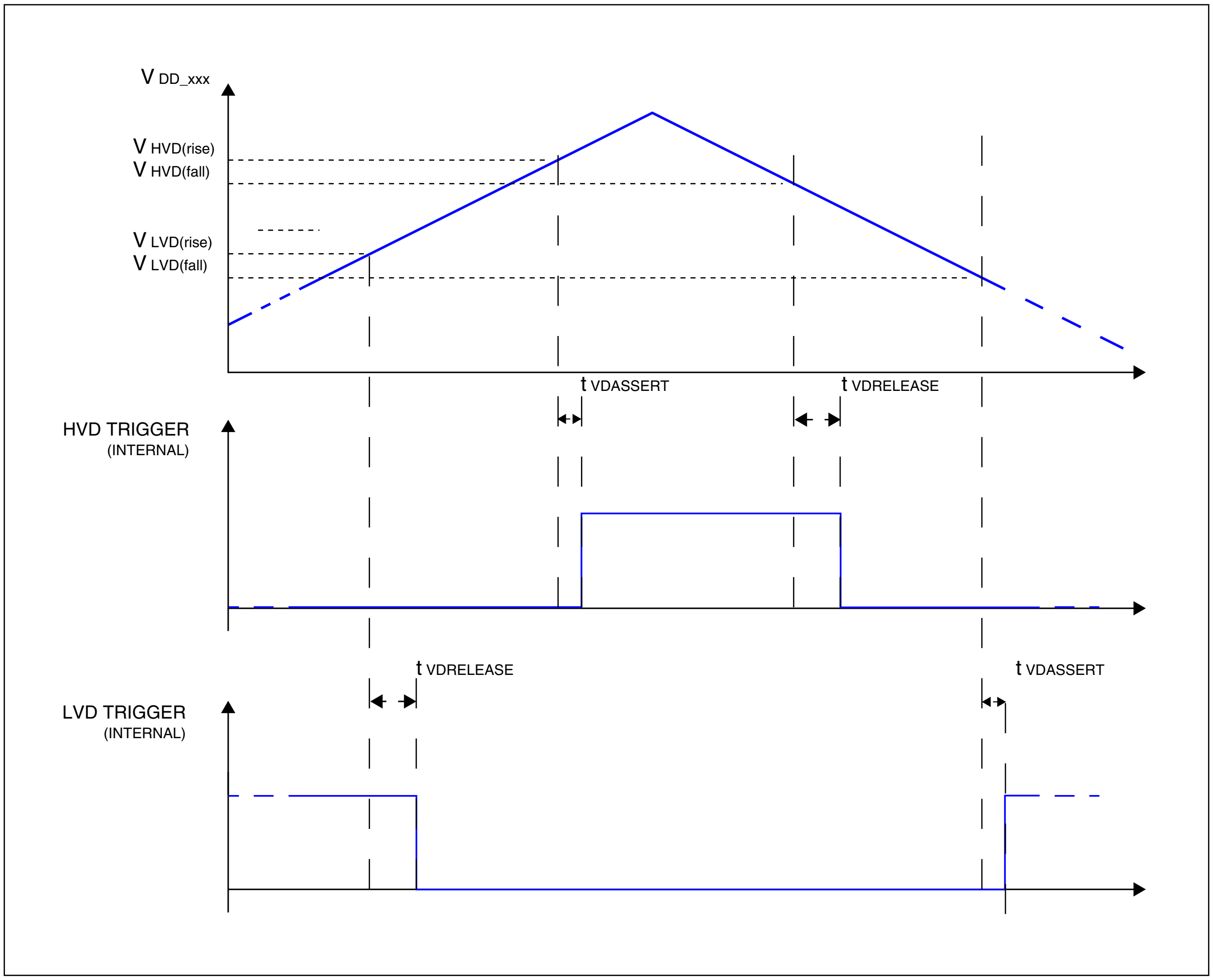


Figure 15. Voltage monitor threshold definition

Table 29. Voltage monitor electrical characteristics[1, 2]

Symbol	Parameter	Conditions	Configuration			Value			Unit
			Trim bits	Mask Opt.	Pow. Up	Min	Typ	Max	
POR098_c[3]	LV internal supply power on reset	Rising voltage (powerup)	N/A	No	Enab.	960	1010	1060	mV
		Falling voltage (power down)				940	990	1040	
LVD_core_hot	LV internal[4] supply low voltage monitoring	Rising voltage (untrimmed)	4bit	No	Enab.	1100	1140	1183	mV
		Falling voltage (untrimmed)				1080	1120	1163	
		Rising voltage (trimmed)				1142	1165	1183	
		Falling voltage (trimmed)				1122	1145	1163	
LVD_core_cold	LV external[5] supply low voltage monitoring	Rising voltage	4bit	Yes	Disab.	1165	1180	1198	mV
		Falling voltage				1136	1160	1178	
HVD_core	LV internal cold supply high voltage monitoring	Rising voltage	4bit	Yes	Disab.	1338	1365	1385	mV
		Falling voltage				1318	1345	1365	

Table continues on the next page...

Table 29. Voltage monitor electrical characteristics[1, 2] (continued)

Symbol	Parameter	Conditions	Configuration			Value			Unit
			Trim bits	Mask Opt.	Pow. Up	Min	Typ	Max	
POR_HV	HV V_{DDPMC} supply power on reset threshold	Rising voltage (powerup)	N/A	No	Enab.	2444	2600	2756	mV
		Falling voltage (power down)				2424	2580	2736	
LVD_HV	HV internal V_{DDPMC} supply low voltage monitoring	Rising voltage (untrimmed)	4bit	No	Enab.	2935	3023	3112	mV
		Falling voltage (untrimmed)				2922	3010	3099	
		Rising voltage (trimmed)				2946	3010	3066	
		Falling voltage (trimmed)				2934	2998	3044	
HVD_HV	HV internal V_{DDPMC} supply high voltage monitoring	Rising voltage	4bit	Yes	Disab.	5696	5860	5968	mV
		Falling voltage				5666	5830	5938	
LVD_FLASH	FLASH supply low voltage monitoring[6]	Rising voltage (untrimmed)	4bit	No	Enab.	2935	3023	3112	mV
		Falling voltage (untrimmed)				2922	3010	3099	
		Rising voltage (trimmed)				2956	3010	3053	
		Falling voltage (trimmed)				2944	2998	3041	
HVD_FLASH	FLASH supply high voltage monitoring[6]	Rising voltage	4bit	Yes	Disab.	3456	3530	3584	mV
		Falling voltage				3426	3500	3554	
LVD_IO	Main I/O V_{DDEH1} supply low voltage monitoring	Rising voltage (untrimmed)	4bit	No	Enab.	3250	3350	3488	mV
		Falling voltage (untrimmed)				3220	3320	3458	
		Rising voltage (trimmed)				3347	3420	3468	
		Falling voltage (trimmed)				3317	3390	3438	
$t_{VDASSERT}$	Voltage detector threshold crossing assertion	—	—	—	—	0.1	—	2.0	μs
$t_{VDRELEASE}$	Voltage detector threshold crossing de-assertion	—	—	—	—	5	—	20	μs

1. LVD is released after $t_{VDRELEASE}$ temporization when upper threshold is crossed; LVD is asserted $t_{VDASSERT}$ after detection when lower threshold is crossed.
2. HVD is released after $t_{VDRELEASE}$ temporization when lower threshold is crossed; HVD is asserted $t_{VDASSERT}$ after detection when upper threshold is crossed.
3. POR098_c threshold is an untrimmed value, before the completion of the power-up sequence. All other LVD/HVD thresholds are provided after trimming.
4. LV internal supply levels are measured on device internal supply grid after internal voltage drop.
5. LV external supply levels are measured on the die side of the package bond wire after package voltage drop.
6. V_{DDFLA} range is guaranteed when internal flash memory regulator is used.

3.11.4 Power sequencing requirements

Requirements for power sequencing include the following.

NOTE

In these descriptions, *star route layout* means a track split as close as possible to the power supply source. Each of the split tracks is routed individually to the intended end connection.

1. For both LDO mode and SMPS mode, V_{DDPMC} and V_{DDPWR} must be connected together (shorted) to ensure aligned voltage ramping up/down. In addition:
    - For SMPS mode, a star route layout of the power track is required to minimize mutual noise. If SMPS mode is not used, the star route layout is not required. V_{DDPWR} is the supply pin for the SMPS circuitry.
    - For 3.3 V operation, V_{DDFLA} must also be star routed and shorted to V_{DDPWR} and V_{DDPMC}. This triple connection is required because 3.3 V does not guarantee correct functionality of the internal V_{DDFLA} regulator. Consequently, V_{DDFLA} is supplied externally.
2. V_{DDA_MISC}: IRC operation is required to provide the clock for chip startup.
    - The V_{DDPMC}, V_{DD}, and V_{DDEH1} (reset pin pad segment) supplies are monitored. They hold IRC until all of them reach operational voltage. In other words, V_{DDA_MISC} must reach its specified minimum operating voltage before or at the same time that all of these monitored voltages reach their respective specified minimum voltages.
    - An alternative is to connect the same supply voltage to both V_{DDEH1} and V_{DDA_MISC}. This alternative approach requires a star route layout to minimize mutual noise.
3. Multiple V_{DDEx} supplies can be powered up in any order.

    During any time when V_{DD} is powered up but V_{DDEx} is not yet powered up: pad outputs are unpowered.

    During any time when V_{DDEx} is powered up before all other supplies: all pad output buffers are tristated.
4. Ramp up V_{DDA_EQ} before V_{DD}. Otherwise, a reset might occur.
5. When the device is powering down while using the internal SMPS regulator, V_{DDPMC} and V_{DDPWR} supplies must ramp down through the voltage range from 2.5 V to 1.5 V in less than 1 second. Slower ramp-down times might result in reduced lifetime reliability of the device.

3.12 Flash memory specifications

3.12.1 Flash memory program and erase specifications

NOTE

> All timing, voltage, and current numbers specified in this section are defined for a single embedded flash memory within an SoC, and represent average currents for given supplies and operations.

Table 30 shows the estimated Program/Erase times.

Table 30. Flash memory program and erase specifications

Symbol	Characteristic[1]	Typ[2]	Factory Programming[3, 4]		Field Update			Unit
			Initial Max	Initial Max, Full Temp	Typical End of Life[5]	Lifetime Max[6]		
			20°C ≤T_A ≤30°C	-40°C ≤T_J ≤150°C	-40°C ≤T_J ≤150°C	≤ 1,000 cycles	≤ 250,000 cycles	
t_{dwpgm}	Doubleword (64 bits) program time	43	100	150	55	500		μs
t_{ppgm}	Page (256 bits) program time	73	200	300	108	500		μs
t_{qppgm}	Quad-page (1024 bits) program time	268	800	1,200	396	2,000		μs
t_{16kers}	16 KB Block erase time	168	290	320	250	1,000		ms
t_{16kpgm}	16 KB Block program time	34	45	50	40	1,000		ms
t_{32kers}	32 KB Block erase time	217	360	390	310	1,200		ms
t_{32kpgm}	32 KB Block program time	69	100	110	90	1,200		ms
t_{64kers}	64 KB Block erase time	315	490	590	420	1,600		ms
t_{64kpgm}	64 KB Block program time	138	180	210	170	1,600		ms
$t_{256kers}$	256 KB Block erase time	884	1,520	2,030	1,080	4,000	—	ms
$t_{256kpgm}$	256 KB Block program time	552	720	880	650	4,000	—	ms

1. Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 150 cycles, nominal voltage.
4. Plant Programing times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: -40°C ≤ T_J ≤ 150°C, full spec voltage.

3.12.2 Flash memory Array Integrity and Margin Read specifications

Table 31. Flash memory Array Integrity and Margin Read specifications

Symbol	Characteristic	Min	Typical	Max[1]	Units [2]
$t_{ai16kseq}$	Array Integrity time for sequential sequence on 16 KB block.	—	—	512 x Tperiod x Nread	—
$t_{ai32kseq}$	Array Integrity time for sequential sequence on 32 KB block.	—	—	1024 x Tperiod x Nread	—
$t_{ai64kseq}$	Array Integrity time for sequential sequence on 64 KB block.	—	—	2048 x Tperiod x Nread	—
tai256kseq	Array Integrity time for sequential sequence on 256 KB block.	—	—	8192 x Tperiod x Nread	—
$t_{mr16kseq}$	Margin Read time for sequential sequence on 16 KB block.	73.81	—	110.7	μs
$t_{mr32kseq}$	Margin Read time for sequential sequence on 32 KB block.	128.43	—	192.6	μs
$t_{mr64kseq}$	Margin Read time for sequential sequence on 64 KB block.	237.65	—	356.5	μs
$t_{mr256kseq}$	Margin Read time for sequential sequence on 256 KB block.	893.01	—	1,339.5	μs

1. Array Integrity times need to be calculated and is dependent on system frequency and number of clocks per read. The equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and Nread (which is the number of clocks required for read, including pipeline contribution. Thus for a read setup that requires 6 clocks to read with no pipeline, Nread would equal 6. For a read setup that requires 6 clocks to read, and has the address pipeline set to 2, Nread would equal 4 (or 6 - 2).)
2. The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

3.12.3 Flash memory module life specifications

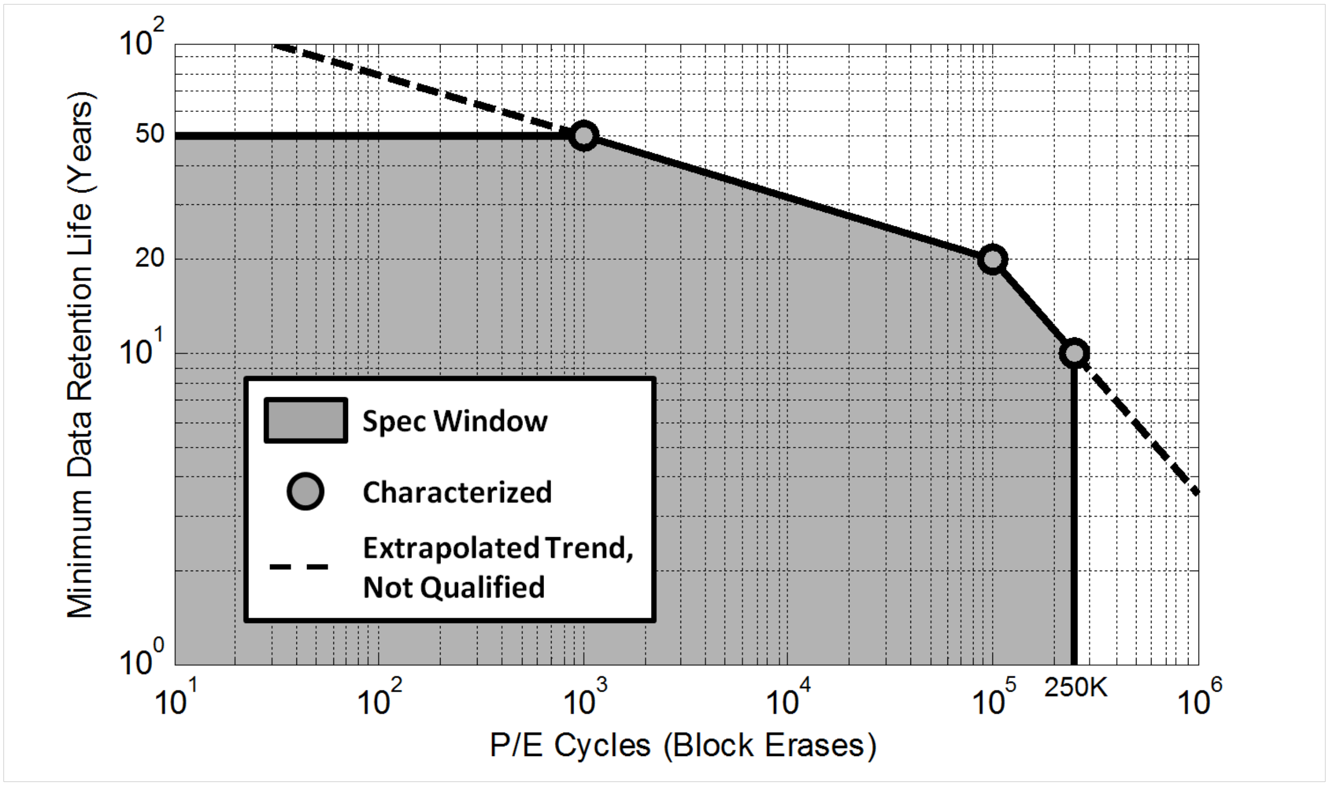
Table 32. Flash memory module life specifications

Symbol	Characteristic	Conditions	Min	Typical	Units
Array P/E cycles	Number of program/erase cycles per block for 16 KB, 32 KB and 64 KB blocks.[1]	—	250,000	—	P/E cycles
	Number of program/erase cycles per block for 256 KB blocks.[2]	—	1,000	250,000	P/E cycles
Data retention	Minimum data retention.	Blocks with 0 - 1,000 P/E cycles.	50	—	Years
		Blocks with 100,000 P/E cycles.	20	—	Years
		Blocks with 250,000 P/E cycles.	10	—	Years

1. Program and erase supported across standard temperature specs.
2. Program and erase supported across standard temperature specs.

3.12.4 Data retention vs program/erase cycles

Graphically, Data Retention versus Program/Erase Cycles can be represented by the following figure. The spec window represents qualified limits. The extrapolated dotted line demonstrates technology capability, however is beyond the qualification limits.



3.12.5 Flash memory AC timing specifications

Table 33. Flash memory AC timing specifications

Symbol	Characteristic	Min	Typical	Max	Units
t_{psus}	Time from setting the MCR-PSUS bit until MCR-DONE bit is set to a 1.	—	9.4 plus four system clock periods	11.5 plus four system clock periods	μs
t_{esus}	Time from setting the MCR-ESUS bit until MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	μs
t_{res}	Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low.	—	—	100	ns

Table continues on the next page...

Table 33. Flash memory AC timing specifications (continued)

Symbol	Characteristic	Min	Typical	Max	Units
t_{done}	Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared.	—	—	5	ns
t_{dones}	Time from 1 to 0 transition on the MCR-EHV bit aborting a program/erase until the MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	μs
t_{drcv}	Time to recover once exiting low power mode.	16 plus seven system clock periods.	—	45 plus seven system clock periods	μs
$t_{aistart}$	Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP	—	—	5	ns
t_{aistop}	Time from 1 to 0 transition of UT0-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request.	—	—	80 plus fifteen system clock periods	ns
t_{mrstop}	Time from 1 to 0 transition of UT0-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request.	10.36 plus four system clock periods	—	20.42 plus four system clock periods	μs

3.12.6 Flash memory read wait-state and address-pipeline control settings

The following table describes the recommended settings of the Flash Memory Controller's PFCR1[RWSC] and PFCR1[APC] fields at various flash memory operating frequencies, based on specified intrinsic flash memory access times of the C55FMC array at 150°C.

Table 34. Flash memory read wait-state and address-pipeline control combinations

Flash memory frequency	RWSC	APC	Flash memory read latency on mini-cache miss (# of f_{PLATF} clock periods)	Flash memory read latency on mini-cache hit (# of f_{PLATF} clock periods)
0 MHz < f_{PLATF} ≤ 33 MHz	0	0	3	1
33 MHz < f_{PLATF} ≤ 100 MHz	2	1	5	1

Table continues on the next page...

Table 34. Flash memory read wait-state and address-pipeline control combinations (continued)

Flash memory frequency	RWSC	APC	Flash memory read latency on mini-cache miss (# of f_{PLATF} clock periods)	Flash memory read latency on mini-cache hit (# of f_{PLATF} clock periods)
100 MHz < f_{PLATF} ≤ 150 MHz	3	1	6	1

3.13 AC timing

3.13.1 Generic timing diagrams

The generic timing diagrams in Figure 16 and Figure 17 apply to all I/O pins with pad types SR and FC. See the associated MPC5777C Microsoft Excel® file in the Reference Manual for the pad type for each pin.

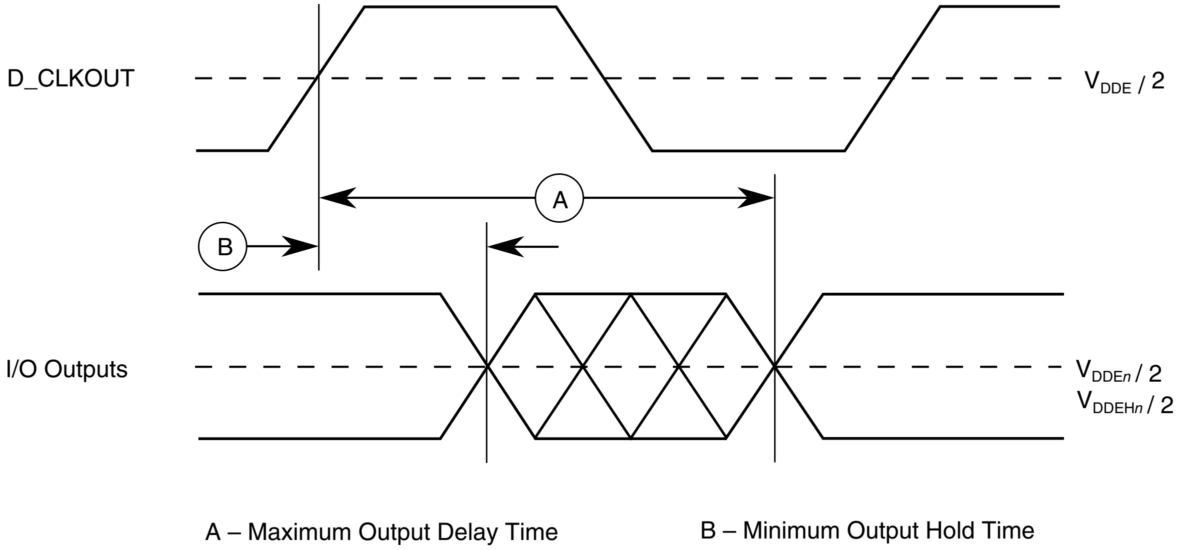
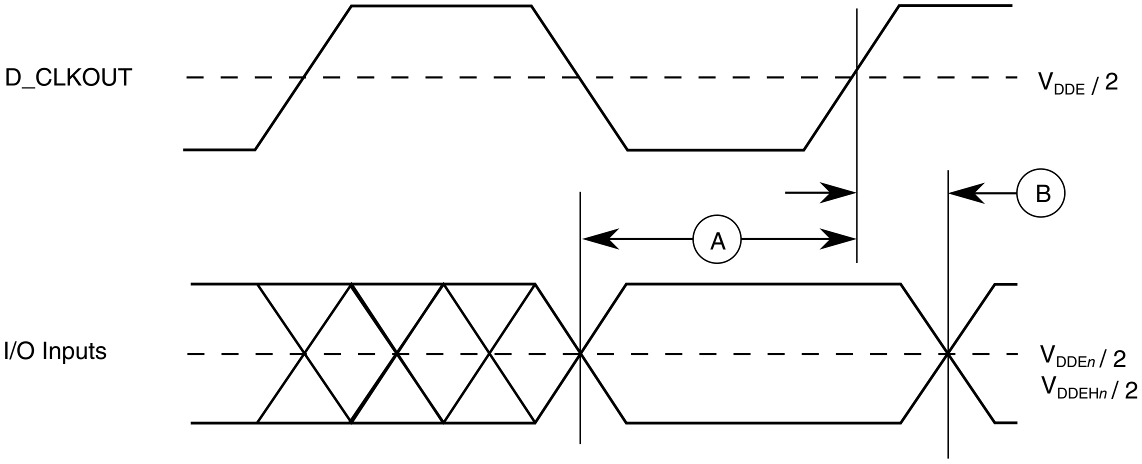


Figure 16. Generic output delay/hold timing



A – Maximum Input Delay Time B – Minimum Input Hold Time

Figure 17. Generic input setup/hold timing

3.13.2 Reset and configuration pin timing

Table 35. Reset and configuration pin timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	$\overline{\text{RESET}}$ Pulse Width	t_{RPW}	10	—	t_{cyc}[2]
2	$\overline{\text{RESET}}$ Glitch Detect Pulse Width	t_{GPW}	2	—	t_{cyc}[2]
3	PLLCFG, BOOTCFG, WKPCFG Setup Time to $\overline{\text{RSTOUT}}$ Valid	t_{RCSU}	10	—	t_{cyc}[2]
4	PLLCFG, BOOTCFG, WKPCFG Hold Time to $\overline{\text{RSTOUT}}$ Valid	t_{RCH}	0	—	t_{cyc}[2]

1. Reset timing specified at: V_{DDEH} = 3.0 V to 5.25 V, V_{DD} = 1.08 V to 1.32 V, TA = TL to TH.
2. For further information on t_{cyc}, see Table 3.

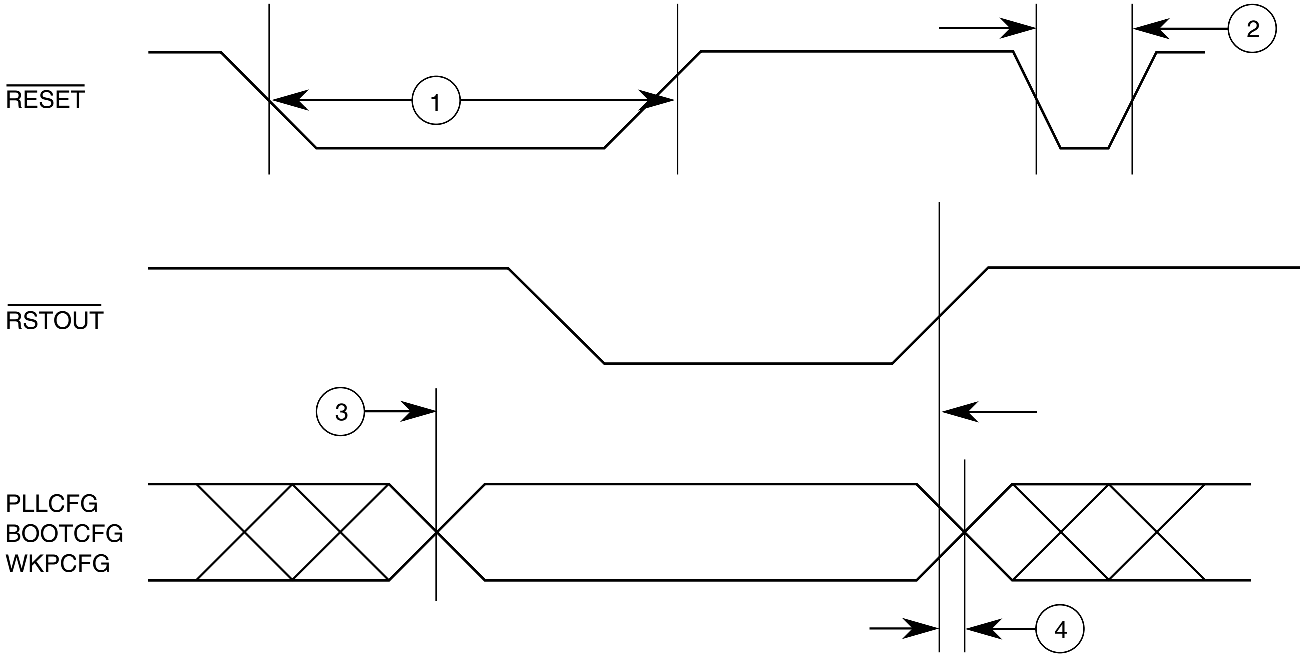


Figure 18. Reset and configuration pin timing

3.13.3 IEEE 1149.1 interface timing

Table 36. JTAG pin AC electrical characteristics[1]

#	Symbol	Characteristic	Value		Unit
			Min	Max	
1	t_{JCYC}	TCK cycle time	100	—	ns
2	t_{JDC}	TCK clock pulse width	40	60	%
3	$t_{TCKRISE}$	TCK rise and fall times (40%–70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	TMS, TDI data setup time	5	—	ns
5	t_{TMSH}, t_{TDIH}	TMS, TDI data hold time	5	—	ns
6	t_{TDOV}	TCK low to TDO data valid	—	16[2]	ns
7	t_{TDOI}	TCK low to TDO data invalid	0	—	ns
8	t_{TDOHZ}	TCK low to TDO high impedance	—	15	ns
9	t_{JCMPPW}	JCOMP assertion time	100	—	ns
10	t_{JCMPS}	JCOMP setup time to TCK low	40	—	ns
11	t_{BSDV}	TCK falling edge to output valid	—	600[3]	ns
12	t_{BSDVZ}	TCK falling edge to output valid out of high impedance	—	600	ns
13	t_{BSDHZ}	TCK falling edge to output high impedance	—	600	ns
14	t_{BSDST}	Boundary scan input valid to TCK rising edge	15	—	ns
15	t_{BSDHT}	TCK rising edge to boundary scan input invalid	15	—	ns

1. These specifications apply to JTAG boundary scan only. See Table 37 for functional specifications.
2. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
3. Applies to all pins, limited by pad slew rate. Refer to I/O delay and transition specification and add 20 ns for JTAG delay.

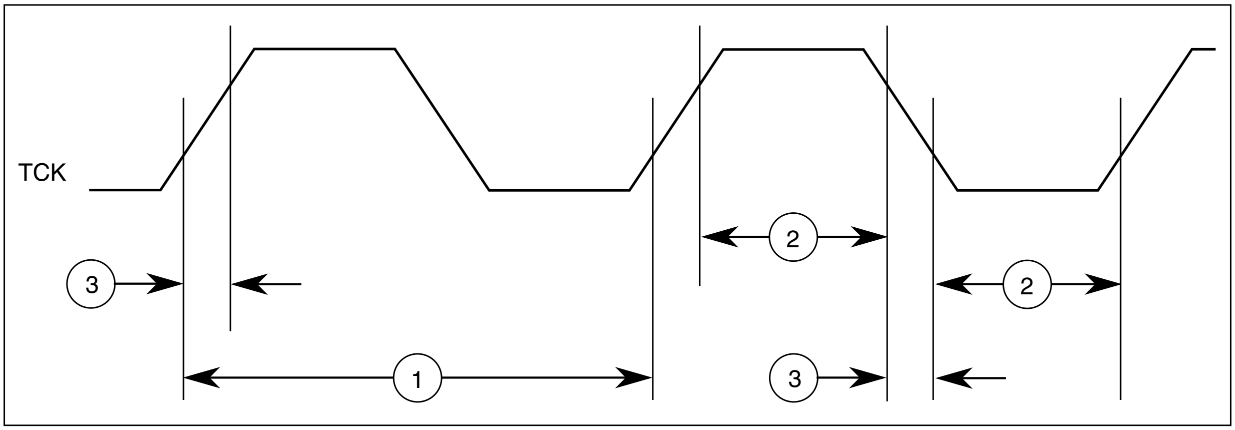


Figure 19. JTAG test clock input timing

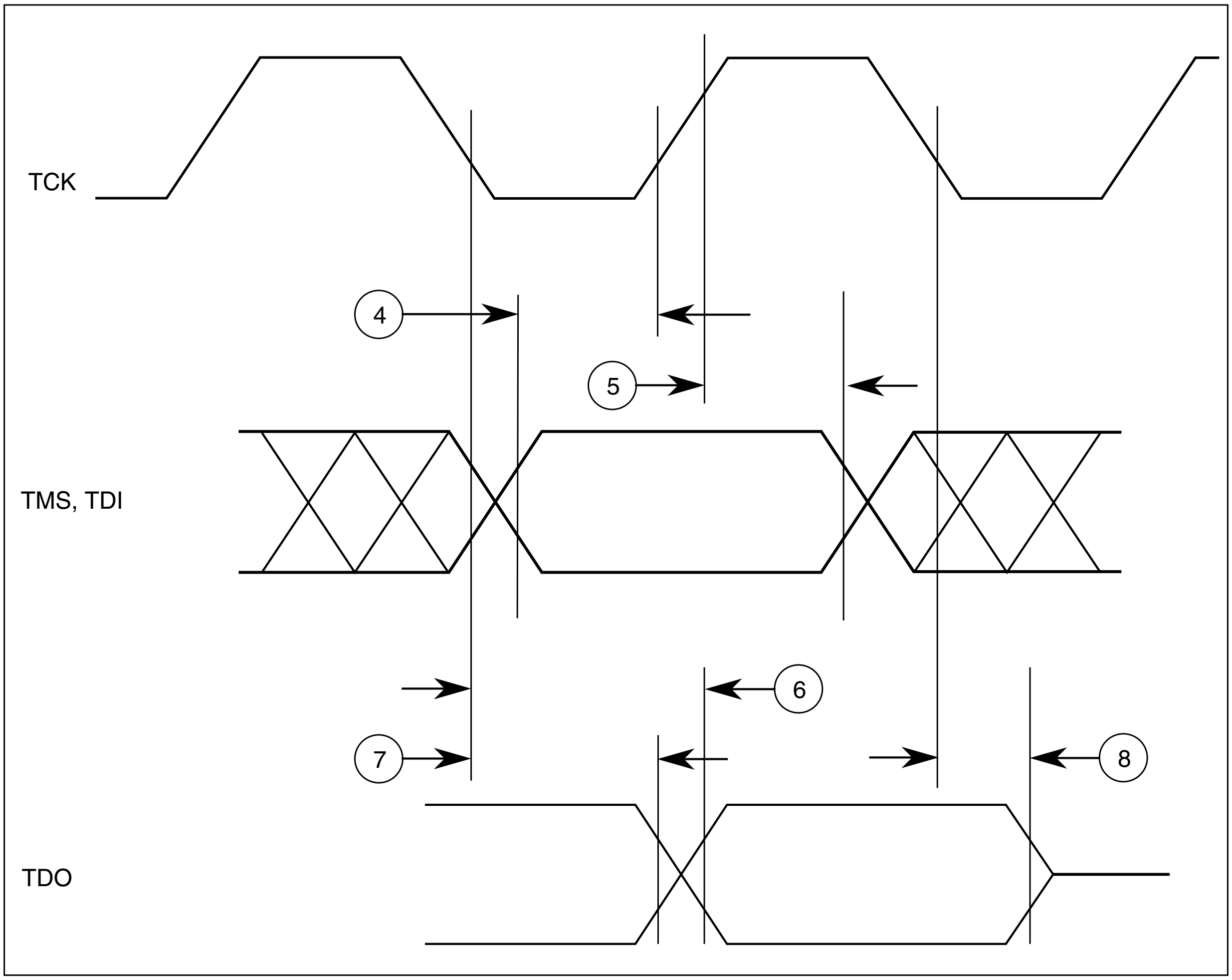


Figure 20. JTAG test access port timing

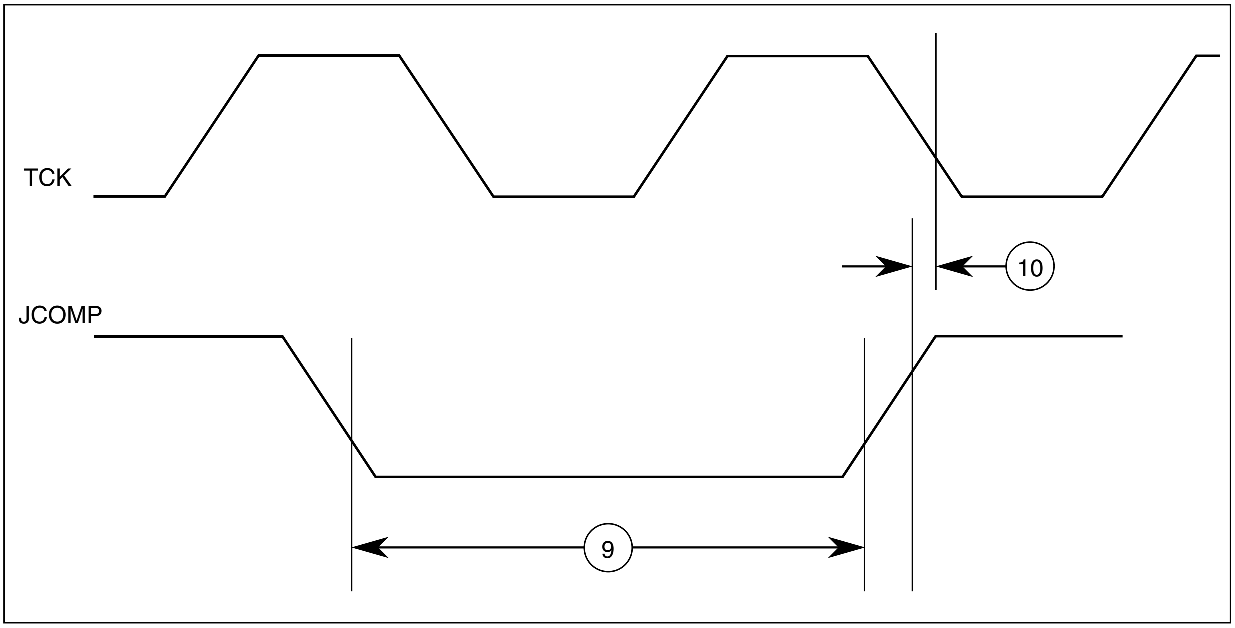


Figure 21. JTAG JCOMP timing

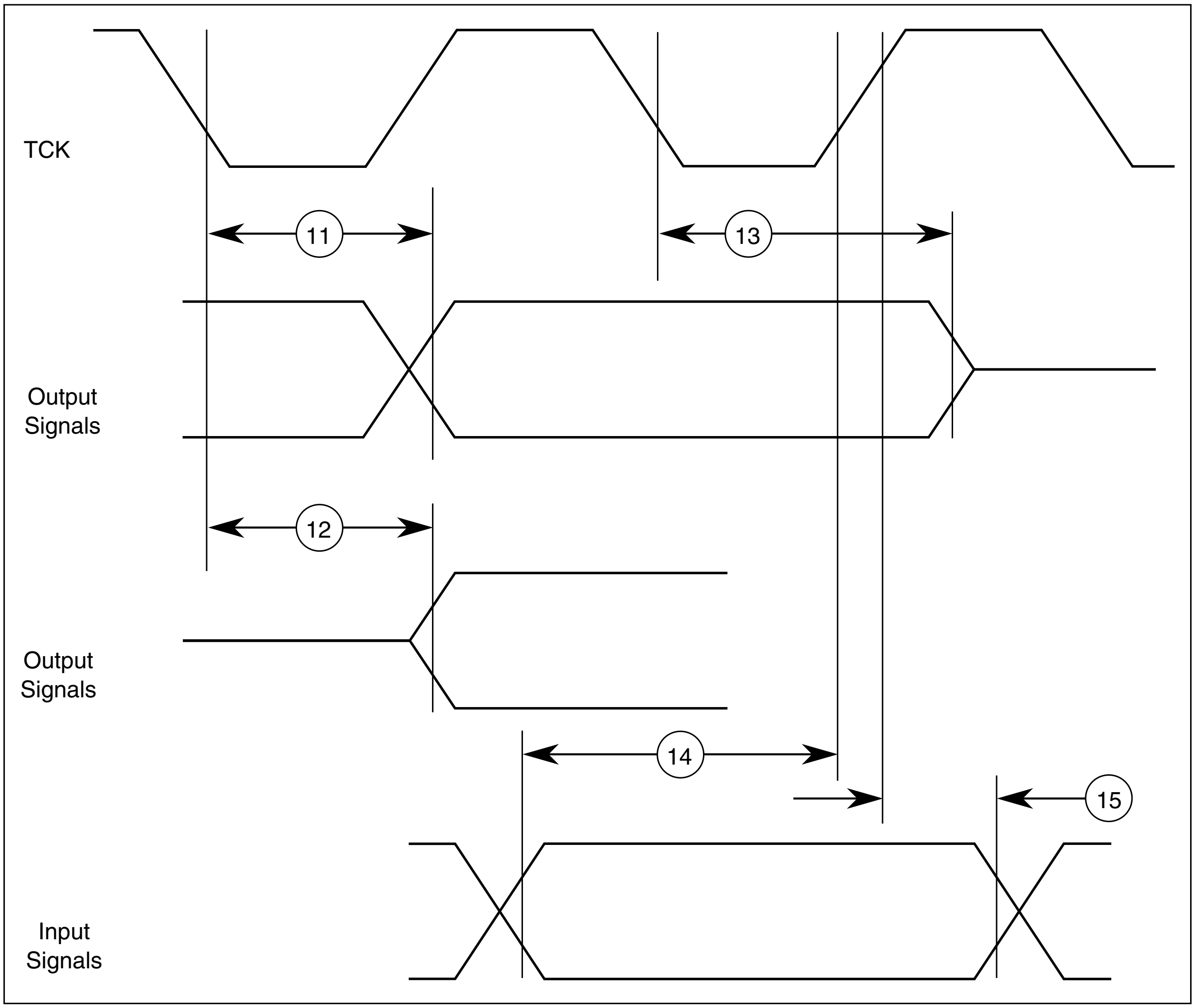


Figure 22. JTAG boundary scan timing

3.13.4 Nexus timing

Table 37. Nexus debug port timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	MCKO Cycle Time	t_{MCYC}	2	8	t_{CYC}
2	MCKO Duty Cycle	t_{MDC}	40	60	%
3	MCKO Low to MDO Data Valid[2]	t_{MDOV}	–0.1	0.2	t_{MCYC}
4	MCKO Low to $\overline{\text{MSEO}}$ Data Valid[2]	t_{MSEOV}	–0.1	0.2	t_{MCYC}
5	MCKO Low to $\overline{\text{EVTO}}$ Data Valid[2]	t_{EVTOV}	–0.1	0.2	t_{MCYC}
6	$\overline{\text{EVTI}}$ Pulse Width	t_{EVTIPW}	4.0	—	t_{TCYC}
7	$\overline{\text{EVTO}}$ Pulse Width	t_{EVTOPW}	1	—	t_{MCYC}
8	TCK Cycle Time	t_{TCYC}	2[3]	—	t_{CYC}

Table continues on the next page...

Table 37. Nexus debug port timing[1] (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
8	Absolute minimum TCK cycle time[4] (TDO sampled on posedge of TCK)	t_{TCYC}	40[5]	—	ns
	Absolute minimum TCK cycle time[4] (TDO sampled on negedge of TCK)		20[5]	—	
9	TCK Duty Cycle	t_{TDC}	40	60	%
10	TDI, TMS Data Setup Time[6]	t_{NTDIS}, t_{NTMSS}	8	—	ns
11	TDI, TMS Data Hold Time[6]	T_{NTDIH}, t_{NTMSH}	5	—	ns
12	TCK Low to TDO Data Valid[6]	t_{NTDOV}	0	18	ns
13	$\overline{\text{RDY}}$ Valid to MCKO[7]	—	—	—	—
14	TDO hold time after TCLK low[6]	t_{NTDOH}	1	—	ns

1. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10.
2. MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.
3. This is a functionally allowable feature. However, it may be limited by the maximum frequency specified by the absolute minimum TCK period specification.
4. This value is TDO propagation time plus 2 ns setup time to sampling edge.
5. This may require a maximum clock speed that is less than the maximum functional capability of the design depending on the actual system frequency being used.
6. Applies to TMS pin timing for the bit frame when using the 1149.7 advanced protocol.
7. The $\overline{\text{RDY}}$ pin timing is asynchronous to MCKO. The timing is guaranteed by design to function correctly.

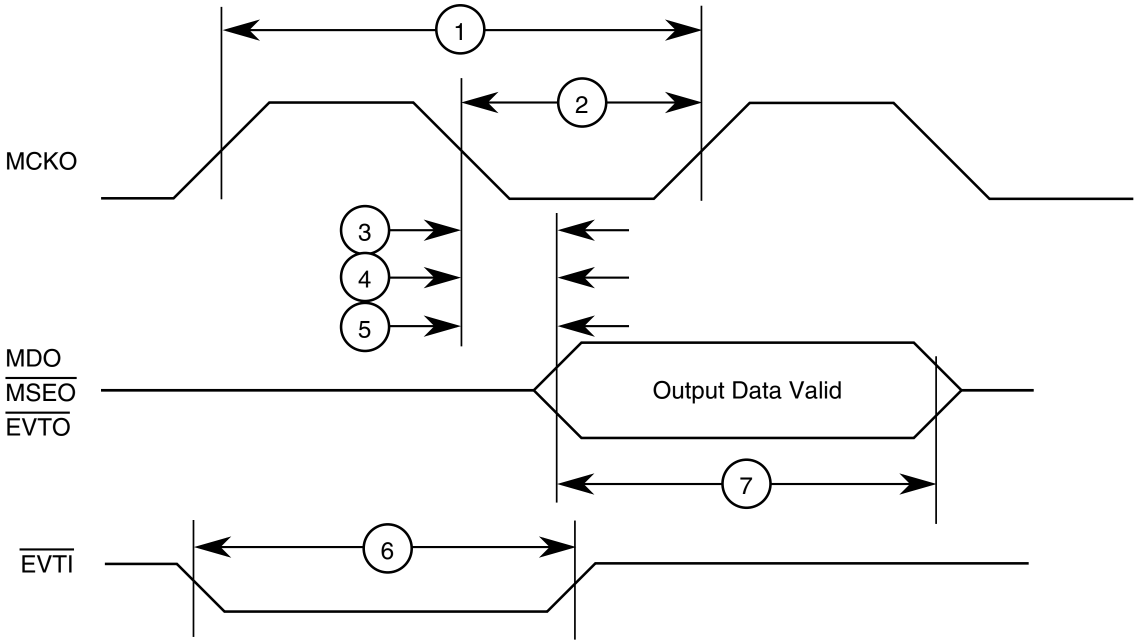


Figure 23. Nexus timings

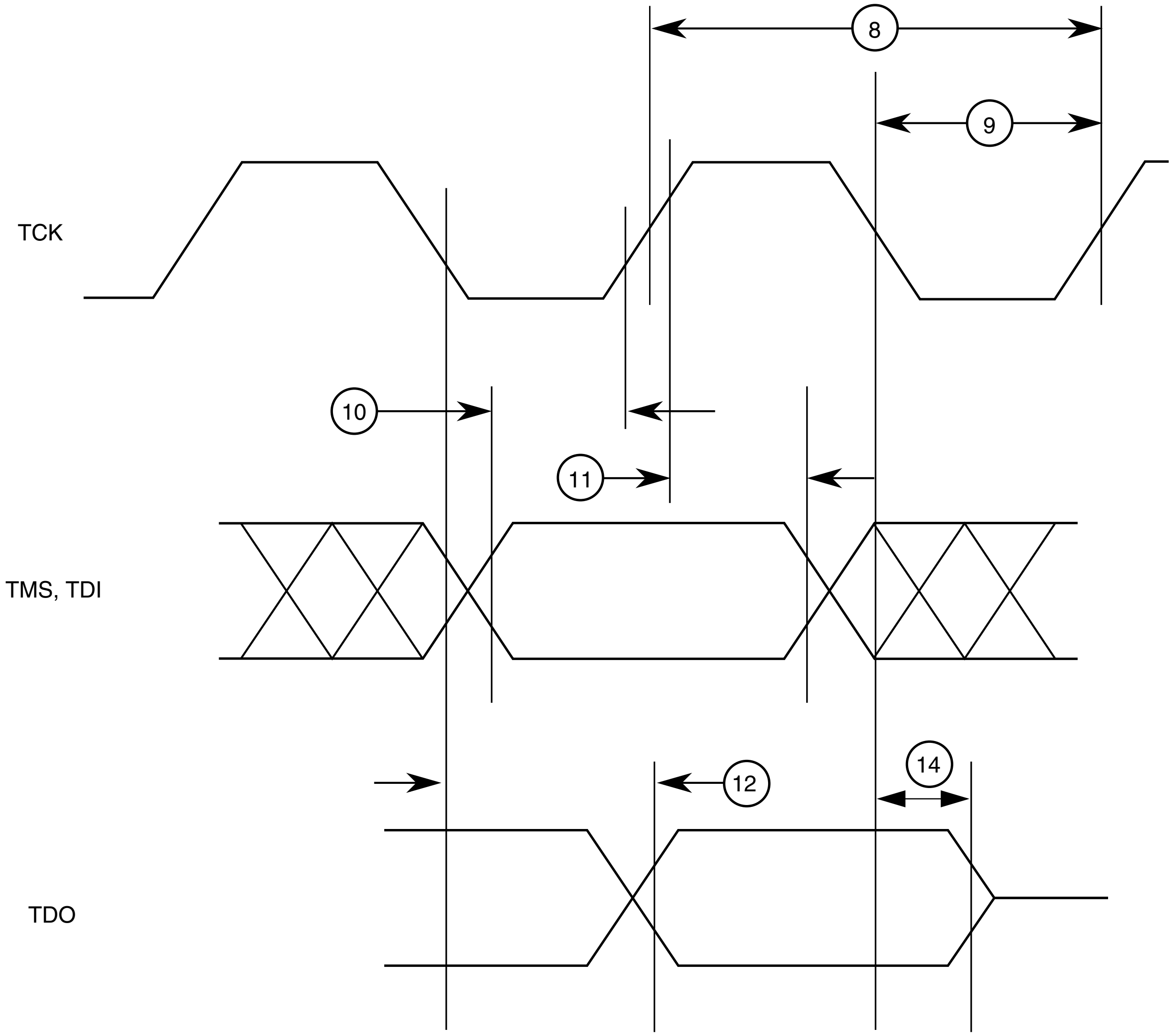


Figure 24. Nexus TCK, TDI, TMS, TDO Timing

3.13.5 External Bus Interface (EBI) timing

Table 38. Bus operation timing[1]

Spec	Characteristic	Symbol	66 MHz (Ext. bus freq.)[2, 3]		Unit	Notes
			Min	Max		
1	D_CLKOUT Period	t_C	15.2	—	ns	Signals are measured at 50% V_{DDE}.
2	D_CLKOUT Duty Cycle	t_{CDC}	45%	55%	t_C	—
3	D_CLKOUT Rise Time	t_{CRT}	—	—[4]	ns	—
4	D_CLKOUT Fall Time	t_{CFT}	—	—[4]	ns	—

Table continues on the next page...

Table 38. Bus operation timing[1] (continued)

Spec	Characteristic	Symbol	66 MHz (Ext. bus freq.)[2, 3]		Unit	Notes
			Min	Max		
5	D_CLKOUT Posedge to Output Signal Invalid or High Z (Hold Time) D_ADD[9:30] D_BDIP D_CS[0:3] D_DAT[0:15] D_OE D_RD_WR D_TA D_TS D_WE[0:3]/D_BE[0:3]	t_{COH}	1.0/1.5	—	ns	Hold time selectable via SIU_ECCR[EBTS] bit: EBTS = 0: 1.0 ns EBTS = 1: 1.5 ns
6	D_CLKOUT Posedge to Output Signal Valid (Output Delay) D_ADD[9:30] D_BDIP D_CS[0:3]	t_{COV}	—	8.5/9.0	ns	Output valid time selectable via SIU_ECCR[EBTS] bit: EBTS = 0: 8.5 ns EBTS = 1: 9.0 ns
	D_DAT[0:15]			11.5		—
	D_OE D_RD_WR D_TA D_TS D_WE[0:3]/D_BE[0:3]			8.5/9.0		Output valid time selectable via SIU_ECCR[EBTS] bit: EBTS = 0: 8.5 ns EBTS = 1: 9.0 ns
7	Input Signal Valid to D_CLKOUT Posedge (Setup Time) D_ADD[9:30] D_DAT[0:15] D_RD_WR D_TA D_TS	t_{CIS}	7.5	—	ns	—
8	D_CLKOUT Posedge to Input Signal Invalid (Hold Time) D_ADD[9:30] D_DAT[0:15] D_RD_WR D_TA D_TS	t_{CIH}	1.0	—	ns	—
9	D_ALE Pulse Width	t_{APW}	6.5	—	ns	The timing is for Asynchronous external memory system.

Table continues on the next page...

Table 38. Bus operation timing[1] (continued)

Spec	Characteristic	Symbol	66 MHz (Ext. bus freq.)[2, 3]		Unit	Notes
			Min	Max		
10	D_ALE Negated to Address Invalid	t_{AAI}	2.0/1.0 [5]	—	ns	The timing is for Asynchronous external memory system. ALE is measured at 50% of VDDE.

1. EBI timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 30 pF with SIU_PCR[DSC] = 11b for ADDR/CTRL and SIU_PCR[SRC] = 11b for DATA/ALE.
2. Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM).
3. Depending on the internal bus speed, set the SIU_ECCR[EBDF] bits correctly not to exceed maximum external bus frequency. The maximum external bus frequency is 66 MHz.
4. Refer to D_CLKOUT pad timing in Table 10.
5. ALE hold time spec is temperature dependant. 1.0 ns spec applies for temperature range -40 to 0°C. 2.0ns spec applies to temperatures > 0°C. This spec has no dependency on the SIU_ECCR[EBTS] bit.

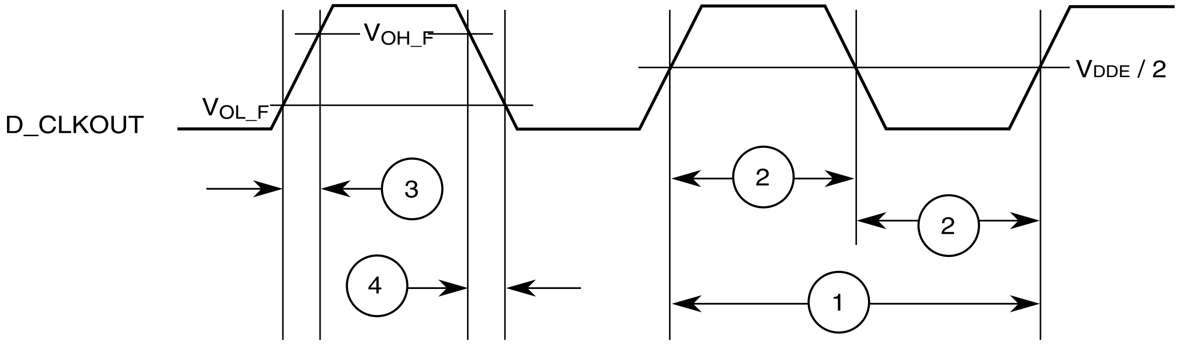


Figure 25. D_CLKOUT timing

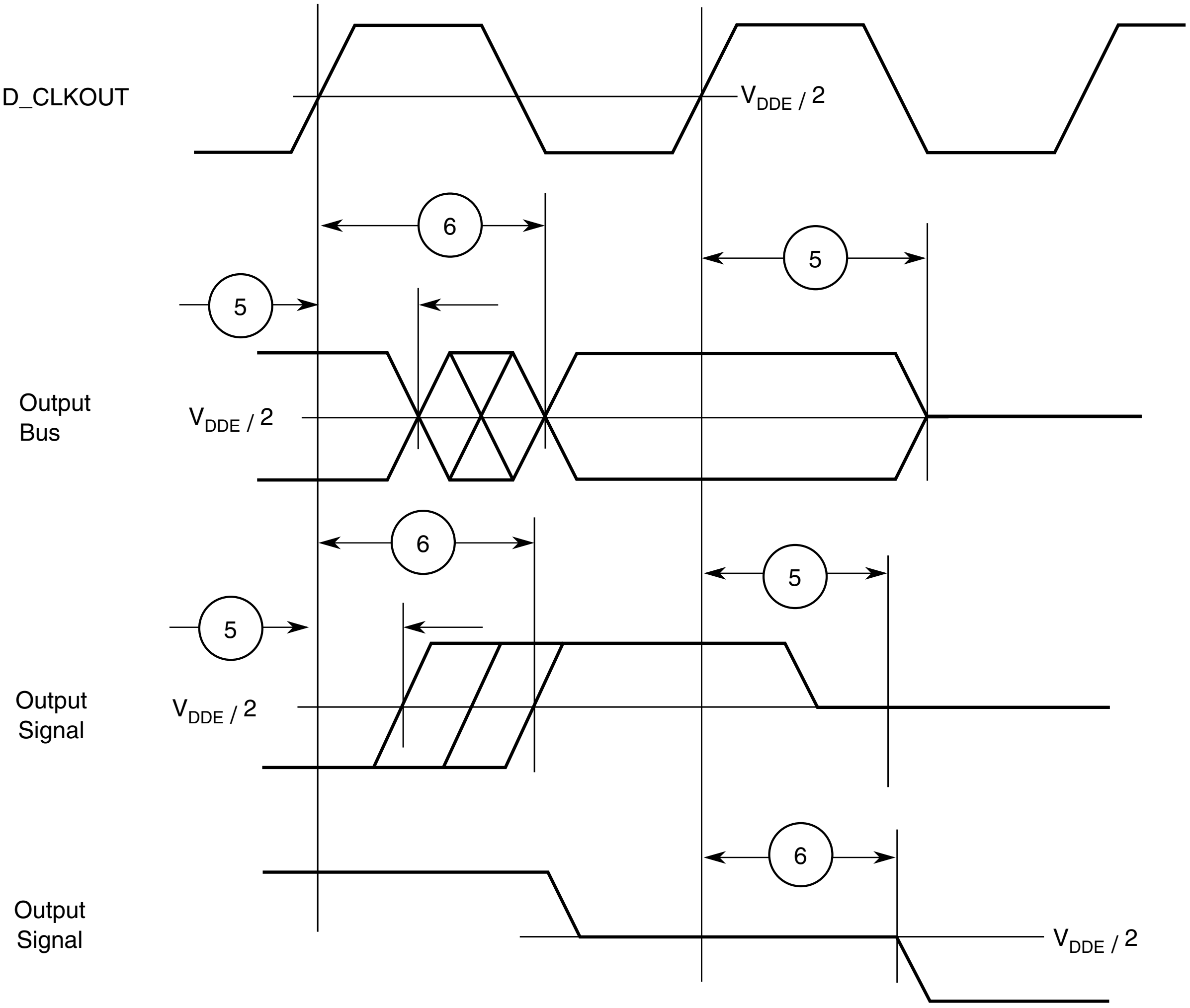


Figure 26. Synchronous output timing

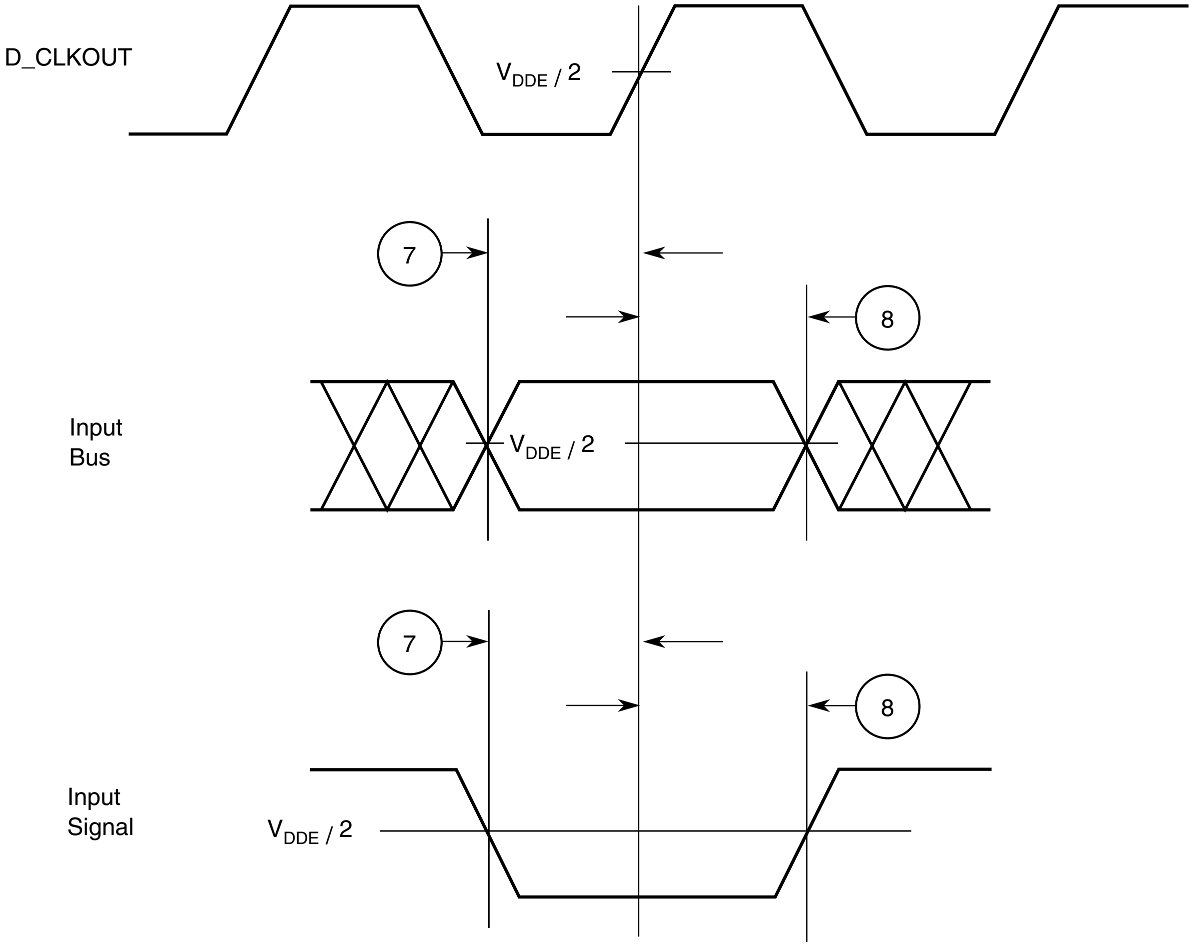


Figure 27. Synchronous input timing

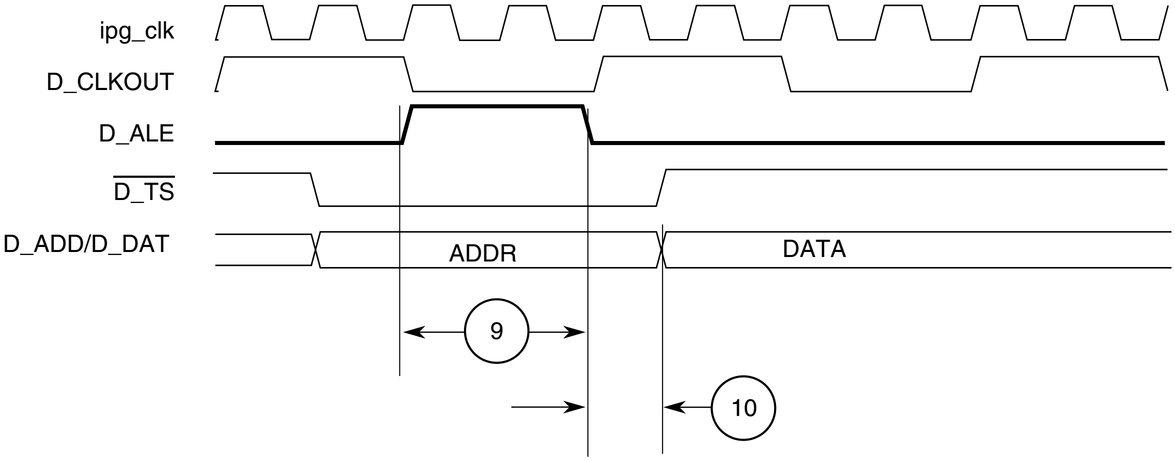


Figure 28. ALE signal timing

3.13.6 External interrupt timing (IRQ/NMI pin)

Table 39. External Interrupt timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	IRQ/NMI Pulse Width Low	t_{IPWL}	3	—	t_{cyc}[2]
2	IRQ/NMI Pulse Width High	t_{IPWH}	3	—	t_{cyc}[2]
3	IRQ/NMI Edge to Edge Time[3]	t_{ICYC}	6	—	t_{cyc}[2]

1. IRQ/NMI timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, $T_A = T_L$ to T_H.
2. For further information on t_{cyc}, see Table 3.
3. Applies when IRQ/NMI pins are configured for rising edge or falling edge events, but not both.

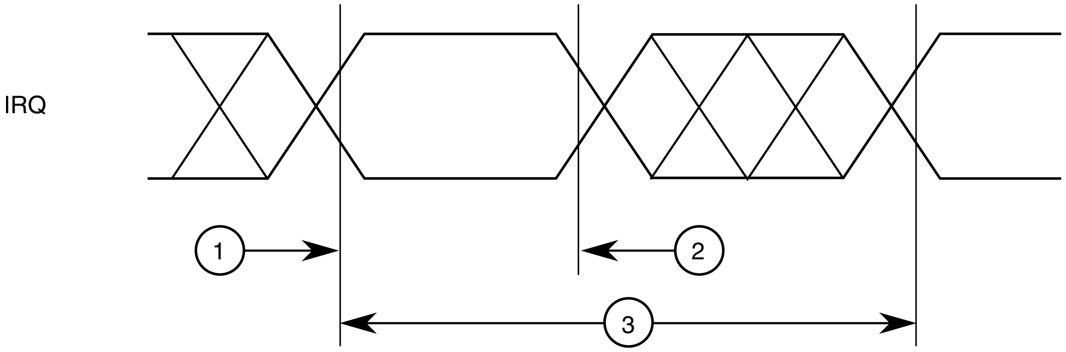


Figure 29. External interrupt timing

3.13.7 eTPU timing

Table 40. eTPU timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	eTPU Input Channel Pulse Width	t_{ICPW}	4	—	t_{CYC_ETPU}[2]
2	eTPU Output Channel Pulse Width	t_{OCPW}	1[3]	—	t_{CYC_ETPU}[2]

1. eTPU timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, $T_A = T_L$ to T_H, and C_L = 200 pF with SRC = 0b00.
2. For further information on t_{CYC_ETPU}, see Table 3.
3. This specification does not include the rise and fall times. When calculating the minimum eTPU pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

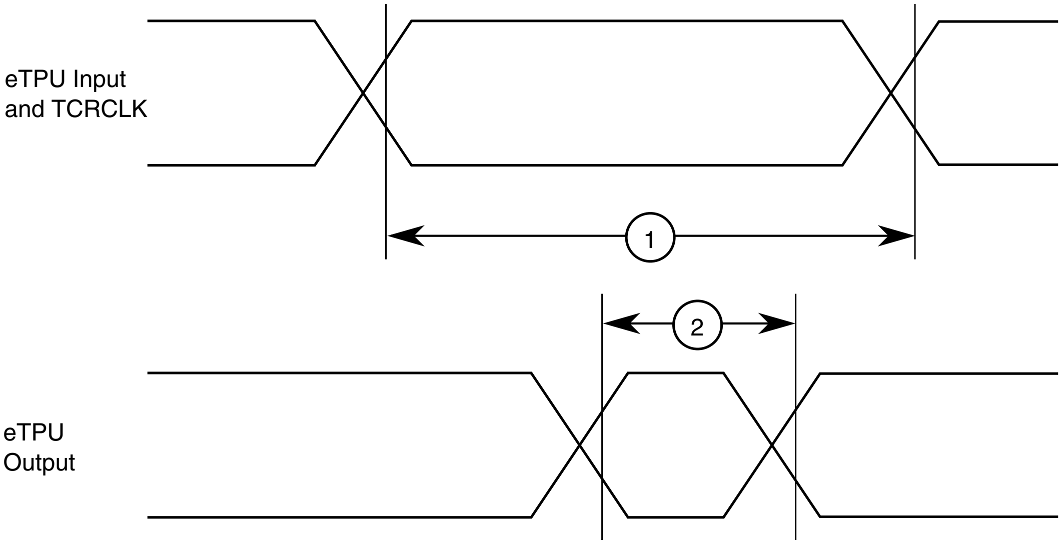


Figure 30. eTPU timing

3.13.8 eMIOS timing

Table 41. eMIOS timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	eMIOS Input Pulse Width	t_{MIPW}	4	—	t_{CYC_PER}[2]
2	eMIOS Output Pulse Width	t_{MOPW}	1[3]	—	t_{CYC_PER}[2]

1. eMIOS timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, $T_A = T_L$ to T_H, and C_L = 50 pF with SRC = 0b00.
2. For further information on t_{CYC_PER}, see Table 3.
3. This specification does not include the rise and fall times. When calculating the minimum eMIOS pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

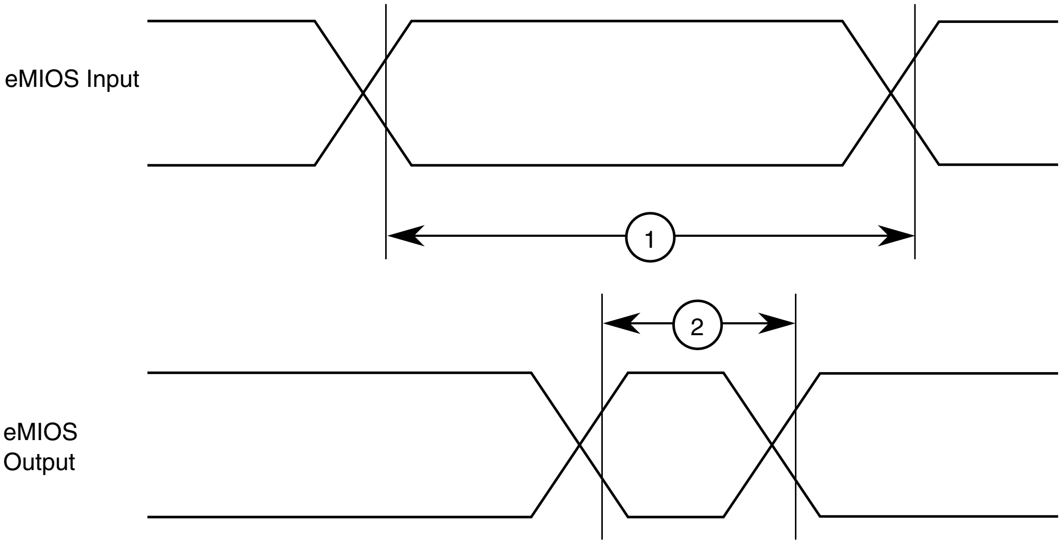


Figure 31. eMIOS timing

3.13.9 DSPI timing with CMOS and LVDS pads

NOTE

The DSPI in TSB mode with LVDS pads can be used to implement the Micro Second Channel (MSC) bus protocol.

DSPI channel frequency support is shown in Table 42. Timing specifications are shown in Table 43, Table 44, Table 45, Table 46, and Table 47.

Table 42. DSPI channel frequency support

DSPI use mode		Max usable frequency (MHz)[1, 2]
CMOS (Master mode)	Full duplex – Classic timing (Table 43)	17
	Full duplex – Modified timing (Table 44)	30
	Output only mode (SCK/SOUT/PCS) (Table 43 and Table 44)	30
	Output only mode TSB mode (SCK/SOUT/PCS) (Table 47)	30
LVDS (Master mode)	Full duplex – Modified timing (Table 45)	30
	Output only mode TSB mode (SCK/SOUT/PCS) (Table 46)	40

1. Maximum usable frequency can be achieved if used with fastest configuration of the highest drive pads.
2. Maximum usable frequency does not take into account external device propagation delay.

3.13.9.1 DSPI master mode full duplex timing with CMOS and LVDS pads

3.13.9.1.1 DSPI CMOS Master Mode — Classic Timing

Table 43. DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0, CPHA = 0 or 1[1]

#	Symbol	Characteristic	Condition[2]		Value[3]		Unit
			Pad drive[4]	Load (C_L)	Min	Max	
1	t_{SCK}	SCK cycle time	PCR[SRC]=11b	25 pF	33.0	—	ns
			PCR[SRC]=10b	50 pF	80.0	—	
			PCR[SRC]=01b	50 pF	200.0	—	
2	t_{CSC}	PCS to SCK delay	PCR[SRC]=11b	25 pF	(N[5] × t_{SYS}, [6]) – 16	—	ns
			PCR[SRC]=10b	50 pF	(N[5] × t_{SYS}, [6]) – 16	—	
			PCR[SRC]=01b	50 pF	(N[5] × t_{SYS}, [6]) – 18	—	
			PCS: PCR[SRC]=01b SCK: PCR[SRC]=10b	50 pF	(N[5] × t_{SYS}, [6]) – 45	—	

Table continues on the next page...

Table 43. DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0, CPHA = 0 or 1[1] (continued)

#	Symbol	Characteristic	Condition[2]		Value[3]		Unit
			Pad drive[4]	Load (C_L)	Min	Max	
3	t_{ASC}	After SCK delay	PCR[SRC]=11b	PCS: 0 pF SCK: 50 pF	(M[7] × t_{SYS},[6]) – 35	—	ns
			PCR[SRC]=10b	PCS: 0 pF SCK: 50 pF	(M[7] × t_{SYS},[6]) – 35	—	
			PCR[SRC]=01b	PCS: 0 pF SCK: 50 pF	(M[7] × t_{SYS},[6]) – 35	—	
			PCS: PCR[SRC]=01b SCK: PCR[SRC]=10b	PCS: 0 pF SCK: 50 pF	(M[7] × t_{SYS},[6]) – 35	—	
4	t_{SDC}	SCK duty cycle[8]	PCR[SRC]=11b	0 pF	$1/2t_{SCK} - 2$	$1/2t_{SCK} + 2$	ns
			PCR[SRC]=10b	0 pF	$1/2t_{SCK} - 2$	$1/2t_{SCK} + 2$	
			PCR[SRC]=01b	0 pF	$1/2t_{SCK} - 5$	$1/2t_{SCK} + 5$	
PCS strobe timing							
5	t_{PCSC}	PCSx to $\overline{PCSS}$ time[9]	PCR[SRC]=10b	25 pF	13.0	—	ns
6	t_{PASC}	$\overline{PCSS}$ to PCSx time[9]	PCR[SRC]=10b	25 pF	13.0	—	ns
SIN setup time							
7	t_{SUI}	SIN setup time to SCK[10]	PCR[SRC]=11b	25 pF	29.0	—	ns
			PCR[SRC]=10b	50 pF	31.0	—	
			PCR[SRC]=01b	50 pF	62.0	—	
SIN hold time							
8	t_{HI}	SIN hold time from SCK[10]	PCR[SRC]=11b	0 pF	–1.0	—	ns
			PCR[SRC]=10b	0 pF	–1.0	—	
			PCR[SRC]=01b	0 pF	–1.0	—	
SOUT data valid time (after SCK edge)							
9	t_{SUO}	SOUT data valid time from SCK[11]	PCR[SRC]=11b	25 pF	—	7.0	ns
			PCR[SRC]=10b	50 pF	—	8.0	
			PCR[SRC]=01b	50 pF	—	18.0	
SOUT data hold time (after SCK edge)							
10	t_{HO}	SOUT data hold time after SCK[11]	PCR[SRC]=11b	25 pF	–9.0	—	ns
			PCR[SRC]=10b	50 pF	–10.0	—	
			PCR[SRC]=01b	50 pF	–21.0	—	

1. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.
2. When a characteristic involves two signals, the pad drive and load conditions apply to each signal's pad, unless specified otherwise.
3. All timing values for output signals in this table are measured to 50% of the output voltage.
4. Pad drive is defined as the PCR[SRC] field setting in the SIU. Timing is guaranteed to same drive capabilities for all signals; mixing of pad drives may reduce operating speeds and may cause incorrect operation.
5. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous

SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).

6. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).
7. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
8. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
9. PCSx and $\overline{\text{PCSS}}$ using same pad configuration.
10. Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL / Automotive voltage thresholds.
11. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

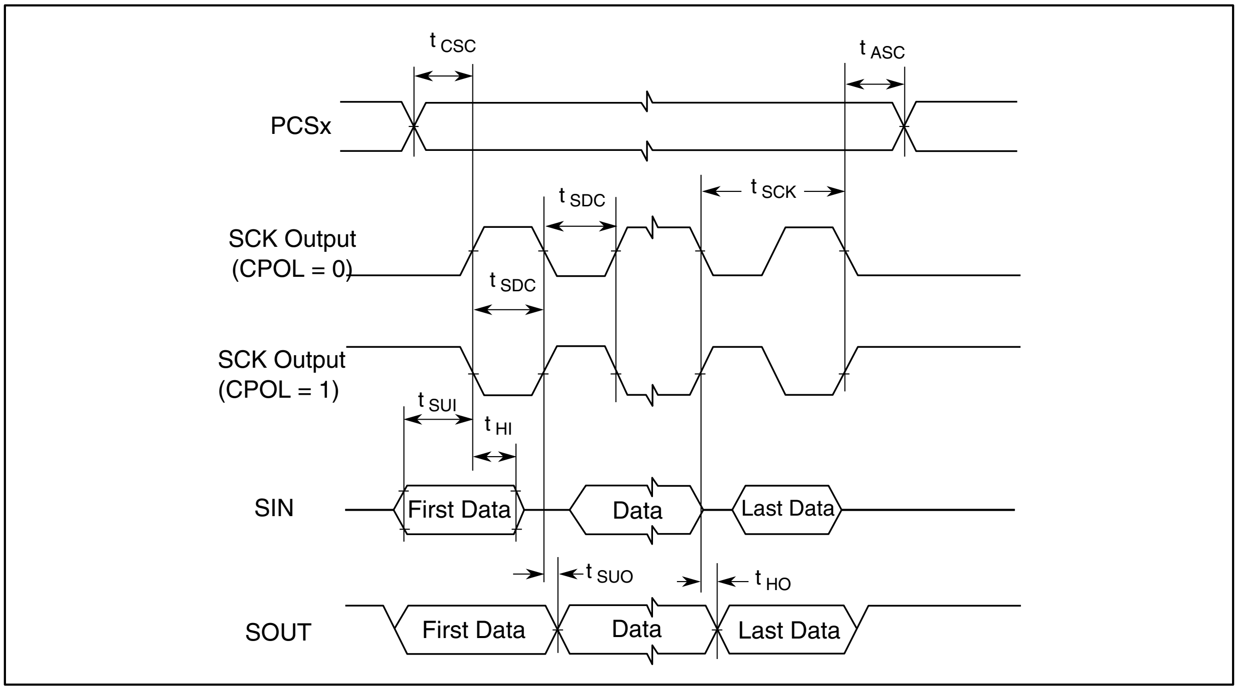


Figure 32. DSPI CMOS master mode – classic timing, CPHA = 0

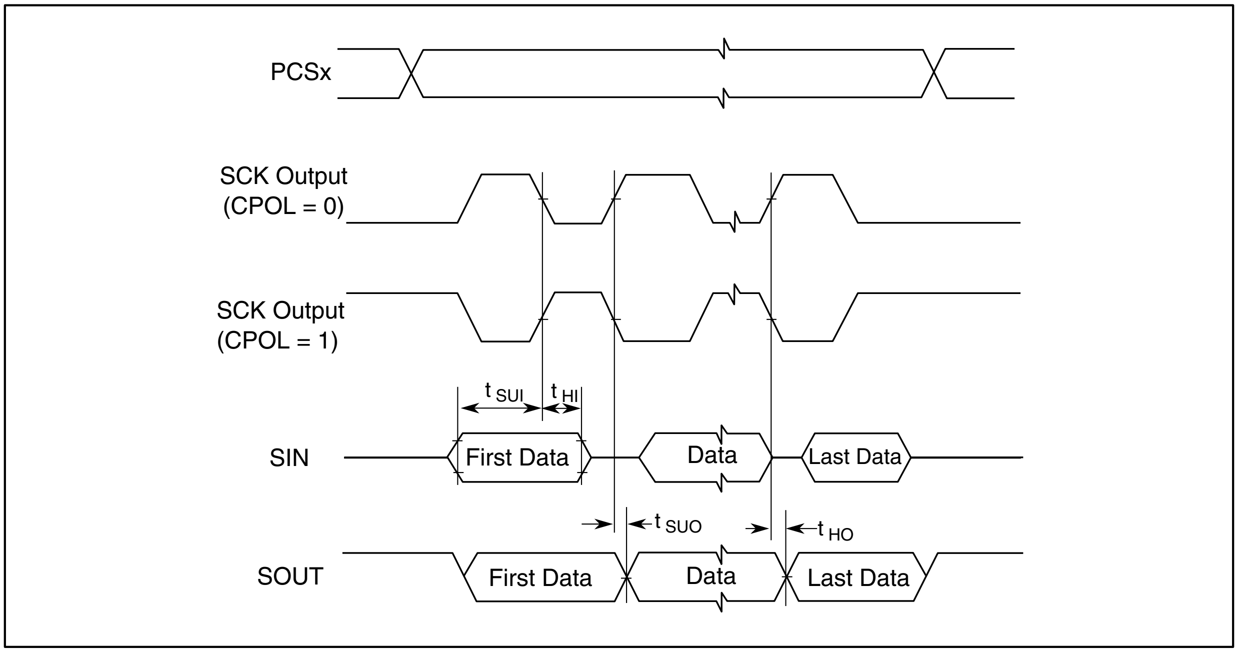


Figure 33. DSPI CMOS master mode – classic timing, CPHA = 1

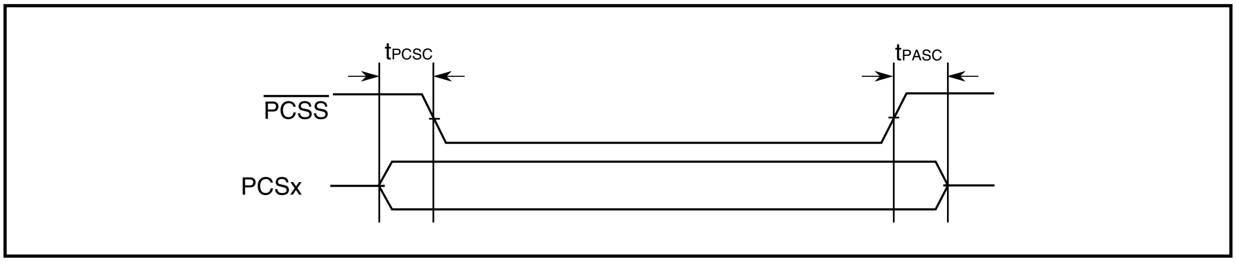


Figure 34. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing (master mode)

3.13.9.1.2 DSPI CMOS Master Mode – Modified Timing

Table 44. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1[1]

#	Symbol	Characteristic	Condition[2]		Value[3]		Unit
			Pad drive[4]	Load (C_L)	Min	Max	
1	t_{SCK}	SCK cycle time	PCR[SRC]=11b	25 pF	33.0	—	ns
			PCR[SRC]=10b	50 pF	80.0	—	
			PCR[SRC]=01b	50 pF	200.0	—	
2	t_{CSC}	PCS to SCK delay	PCR[SRC]=11b	25 pF	($N^{5} \times t_{SYS}$, [6]) – 16	—	ns
			PCR[SRC]=10b	50 pF	($N^{5} \times t_{SYS}$, [6]) – 16	—	
			PCR[SRC]=01b	50 pF	($N^{5} \times t_{SYS}$, [6]) – 18	—	
			PCS: PCR[SRC]=01b SCK: PCR[SRC]=10b	50 pF	($N^{5} \times t_{SYS}$, [6]) – 45	—	

Table continues on the next page...

Table 44. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1[1] (continued)

#	Symbol	Characteristic	Condition[2]		Value[3]		Unit
			Pad drive[4]	Load (C_L)	Min	Max	
3	t_{ASC}	After SCK delay	PCR[SRC]=11b	PCS: 0 pF SCK: 50 pF	(M[7] × t_{SYS},[6]) – 35	—	ns
			PCR[SRC]=10b	PCS: 0 pF SCK: 50 pF	(M[7] × t_{SYS},[6]) – 35	—	
			PCR[SRC]=01b	PCS: 0 pF SCK: 50 pF	(M[7] × t_{SYS},[6]) – 35	—	
			PCS: PCR[SRC]=01b SCK: PCR[SRC]=10b	PCS: 0 pF SCK: 50 pF	(M[7] × t_{SYS},[6]) – 35	—	
4	t_{SDC}	SCK duty cycle[8]	PCR[SRC]=11b	0 pF	$1/2t_{SCK} - 2$	$1/2t_{SCK} + 2$	ns
			PCR[SRC]=10b	0 pF	$1/2t_{SCK} - 2$	$1/2t_{SCK} + 2$	
			PCR[SRC]=01b	0 pF	$1/2t_{SCK} - 5$	$1/2t_{SCK} + 5$	
PCS strobe timing							
5	t_{PCSC}	PCSx to $\overline{\text{PCSS}}$ time[9]	PCR[SRC]=10b	25 pF	13.0	—	ns
6	t_{PASC}	$\overline{\text{PCSS}}$ to PCSx time[9]	PCR[SRC]=10b	25 pF	13.0	—	ns
SIN setup time							
7	t_{SUI}	SIN setup time to SCK CPHA = 0[10]	PCR[SRC]=11b	25 pF	29 – (P[11] × t_{SYS},[6])	—	ns
			PCR[SRC]=10b	50 pF	31 – (P[11] × t_{SYS},[6])	—	
			PCR[SRC]=01b	50 pF	62 – (P[11] × t_{SYS},[6])	—	
		SIN setup time to SCK CPHA = 1[10]	PCR[SRC]=11b	25 pF	29.0	—	ns
			PCR[SRC]=10b	50 pF	31.0	—	
			PCR[SRC]=01b	50 pF	62.0	—	
SIN hold time							
8	t_{HI}[12]	SIN hold time from SCK CPHA = 0[10]	PCR[SRC]=11b	0 pF	–1 + (P[11] × t_{SYS},[6])	—	ns
			PCR[SRC]=10b	0 pF	–1 + (P[11] × t_{SYS},[6])	—	
			PCR[SRC]=01b	0 pF	–1 + (P[11] × t_{SYS},[6])	—	
		SIN hold time from SCK CPHA = 1[10]	PCR[SRC]=11b	0 pF	–1.0	—	ns
			PCR[SRC]=10b	0 pF	–1.0	—	
			PCR[SRC]=01b	0 pF	–1.0	—	
SOUT data valid time (after SCK edge)							
9	t_{SUO}	SOUT data valid time from SCK CPHA = 0[13]	PCR[SRC]=11b	25 pF	—	7.0 + t_{SYS}[6]	ns
			PCR[SRC]=10b	50 pF	—	8.0 + t_{SYS}[6]	
			PCR[SRC]=01b	50 pF	—	18.0 + t_{SYS}[6]	
		SOUT data valid time from SCK CPHA = 1[13]	PCR[SRC]=11b	25 pF	—	7.0	ns
			PCR[SRC]=10b	50 pF	—	8.0	
			PCR[SRC]=01b	50 pF	—	18.0	
SOUT data hold time (after SCK edge)							

Table continues on the next page...

Table 44. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1[1] (continued)

#	Symbol	Characteristic	Condition[2]		Value[3]		Unit
			Pad drive[4]	Load (C_L)	Min	Max	
10	t_{HO}	SOUT data hold time after SCK CPHA = 0[13]	PCR[SRC]=11b	25 pF	$-9.0 + t_{SYS}$[6]	—	ns
			PCR[SRC]=10b	50 pF	$-10.0 + t_{SYS}$[6]	—	
			PCR[SRC]=01b	50 pF	$-21.0 + t_{SYS}$[6]	—	
		SOUT data hold time after SCK CPHA = 1[13]	PCR[SRC]=11b	25 pF	–9.0	—	ns
			PCR[SRC]=10b	50 pF	–10.0	—	
			PCR[SRC]=01b	50 pF	–21.0	—	

1. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.
2. When a characteristic involves two signals, the pad drive and load conditions apply to each signal's pad, unless specified otherwise.
3. All timing values for output signals in this table are measured to 50% of the output voltage.
4. Pad drive is defined as the PCR[SRC] field setting in the SIU. Timing is guaranteed to same drive capabilities for all signals; mixing of pad drives may reduce operating speeds and may cause incorrect operation.
5. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
6. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).
7. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
8. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
9. PCSx and $\overline{\text{PCSS}}$ using same pad configuration.
10. Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL / Automotive voltage thresholds.
11. P is the number of clock cycles added to delay the DSPI input sample point and is software programmable using DSPI_MCR[SMPL_PT]. The value must be 0, 1 or 2. If the baud rate divide ratio is /2 or /3, this value is automatically set to 1.
12. The 0 pF load condition given in the DSPI AC timing applies to theoretical worst-case hold timing. This guarantees worst-case operation, and additional margin can be achieved in the applications by applying a realistic load.
13. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

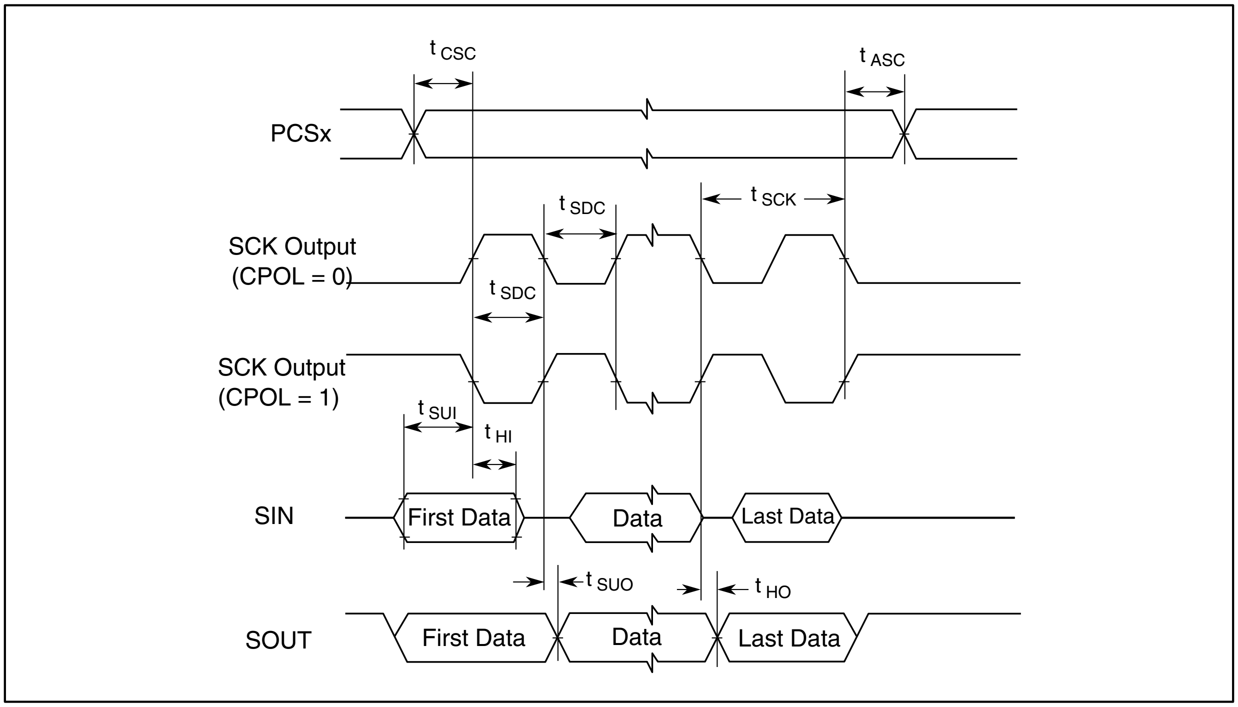


Figure 35. DSPI CMOS master mode – modified timing, CPHA = 0

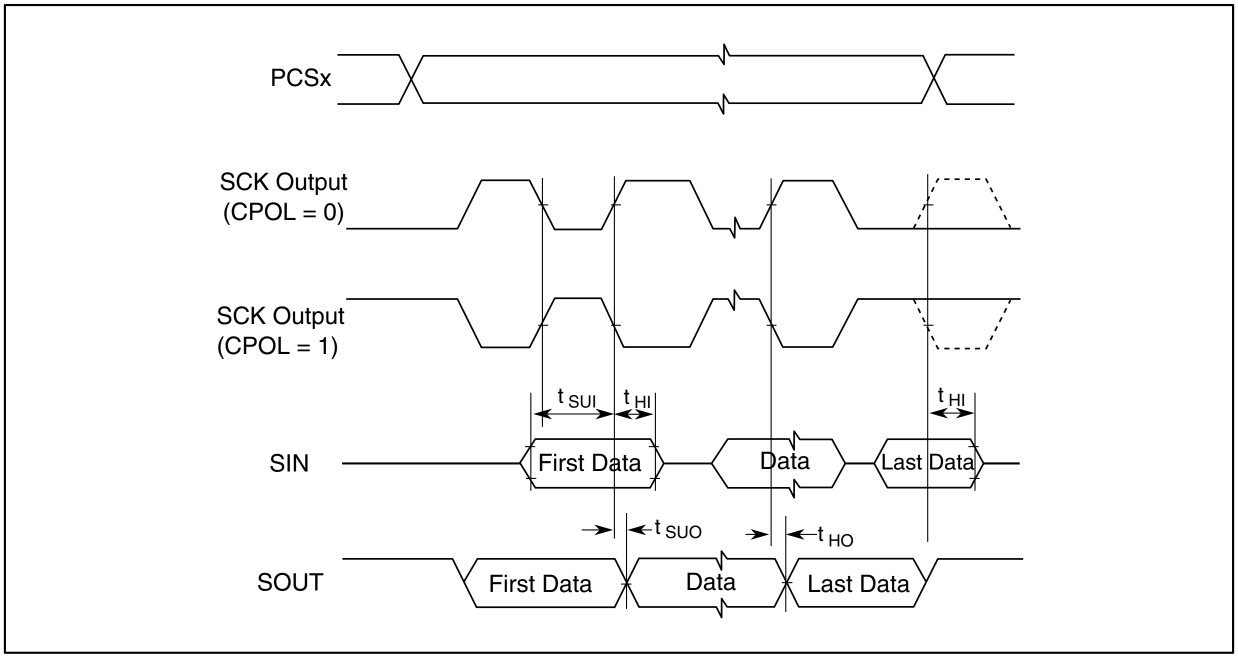


Figure 36. DSPI CMOS master mode – modified timing, CPHA = 1

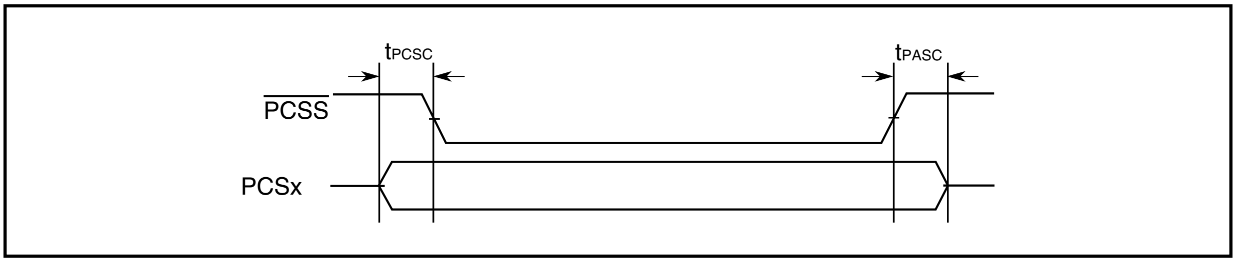


Figure 37. DSPI PCS strobe ($\overline{PCSS}$) timing (master mode)

3.13.9.1.3 DSPI LVDS Master Mode – Modified Timing

Table 45. DSPI LVDS master timing – full duplex – modified transfer format (MTFE = 1), CPHA = 0 or 1

#	Symbol	Characteristic	Condition[1]		Value[2]		Unit
			Pad drive[3]	Load (C_L)	Min	Max	
1	t_{SCK}	SCK cycle time	LVDS	15 pF to 25 pF differential	33.3	—	ns
2	t_{CSC}	PCS to SCK delay (LVDS SCK)	PCS: PCR[SRC]=11b	25 pF	(N[4] × t_{SYS}, [5]) – 10	—	ns
			PCS: PCR[SRC]=10b	50 pF	(N[4] × t_{SYS}, [5]) – 10	—	ns
			PCS: PCR[SRC]=01b	50 pF	(N[4] × t_{SYS}, [5]) – 32	—	ns
3	t_{ASC}	After SCK delay (LVDS SCK)	PCS: PCR[SRC]=11b	PCS: 0 pF SCK: 25 pF	(M[6] × t_{SYS}, [5]) – 8	—	ns
			PCS: PCR[SRC]=10b	PCS: 0 pF SCK: 25 pF	(M[6] × t_{SYS}, [5]) – 8	—	ns
			PCS: PCR[SRC]=01b	PCS: 0 pF SCK: 25 pF	(M[6] × t_{SYS}, [5]) – 8	—	ns
4	t_{SDC}	SCK duty cycle[7]	LVDS	15 pF to 25 pF differential	1/2t_{SCK} – 2	1/2t_{SCK} +2	ns
7	t_{SUI}	**SIN setup time**					
		SIN setup time to SCK CPHA = 0[8]	LVDS	15 pF to 25 pF differential	23 – (P[9] × t_{SYS}, [5])	—	ns
		SIN setup time to SCK CPHA = 1[8]	LVDS	15 pF to 25 pF differential	23	—	ns
8	t_{HI}	**SIN hold time**					
		SIN hold time from SCK CPHA = 0[8]	LVDS	0 pF differential	–1 + (P[9] × t_{SYS}, [5])	—	ns
		SIN hold time from SCK CPHA = 1[8]	LVDS	0 pF differential	–1	—	ns

Table continues on the next page...

Table 45. DSPI LVDS master timing – full duplex – modified transfer format (MTFE = 1), CPHA = 0 or 1 (continued)

#	Symbol	Characteristic	Condition[1]		Value[2]		Unit
			Pad drive[3]	Load (C_L)	Min	Max	
9	t_{SUO}	**SOUT data valid time (after SCK edge)**					
		SOUT data valid time from SCK CPHA = 0[10]	LVDS	15 pF to 25 pF differential	—	$7.0 + t_{SYS}$[5]	ns
		SOUT data valid time from SCK CPHA = 1[10]	LVDS	15 pF to 25 pF differential	—	7.0	ns
10	t_{HO}	**SOUT data hold time (after SCK edge)**					
		SOUT data hold time after SCK CPHA = 0[10]	LVDS	15 pF to 25 pF differential	$-7.5 + t_{SYS}$[5]	—	ns
		SOUT data hold time after SCK CPHA = 1[10]	LVDS	15 pF to 25 pF differential	–7.5	—	ns

1. When a characteristic involves two signals, the pad drive and load conditions apply to each signal's pad, unless specified otherwise.
2. All timing values for output signals in this table are measured to 50% of the output voltage.
3. Pad drive is defined as the PCR[SRC] field setting in the SIU. Timing is guaranteed to same drive capabilities for all signals; mixing of pad drives may reduce operating speeds and may cause incorrect operation.
4. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
5. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min tSYS = 10 ns).
6. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
7. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
8. Input timing assumes an input slew rate of 1 ns (10% – 90%) and LVDS differential voltage = ±100 mV.
9. P is the number of clock cycles added to delay the DSPI input sample point and is software programmable using DSPI_MCR[SMPL_PT]. The value must be 0, 1 or 2. If the baud rate divide ratio is /2 or /3, this value is automatically set to 1.
10. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

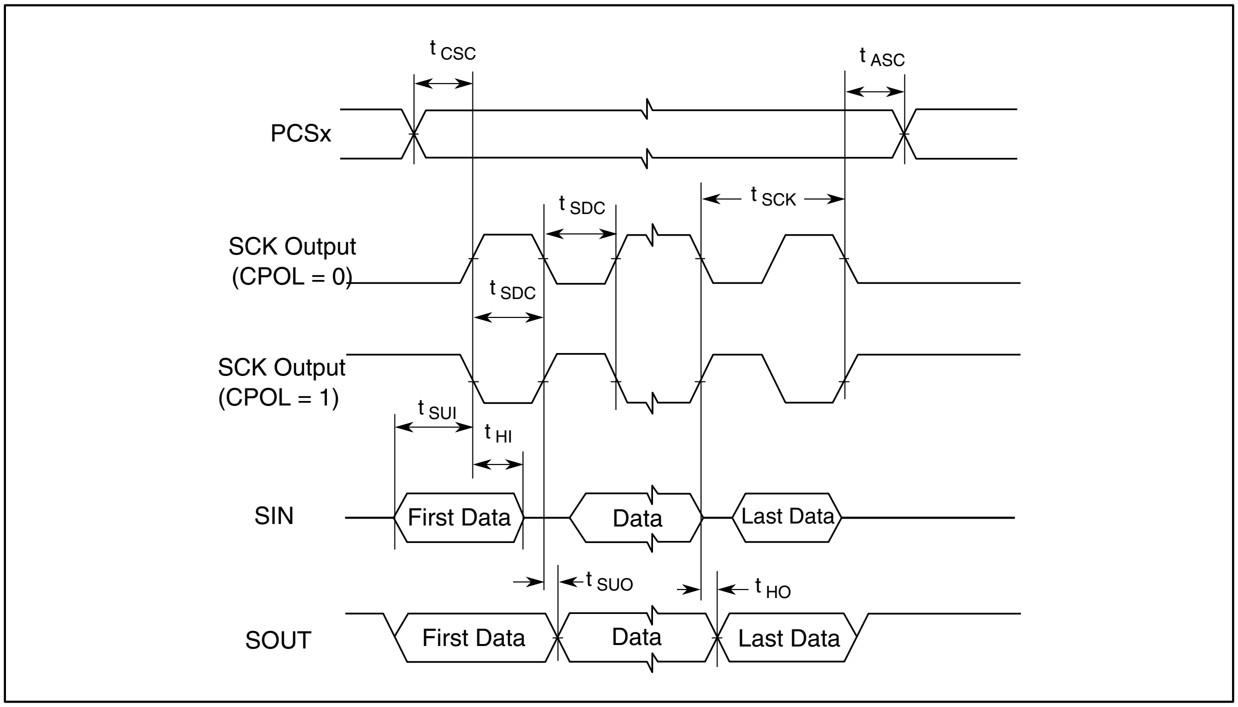


Figure 38. DSPI LVDS master mode – modified timing, CPHA = 0

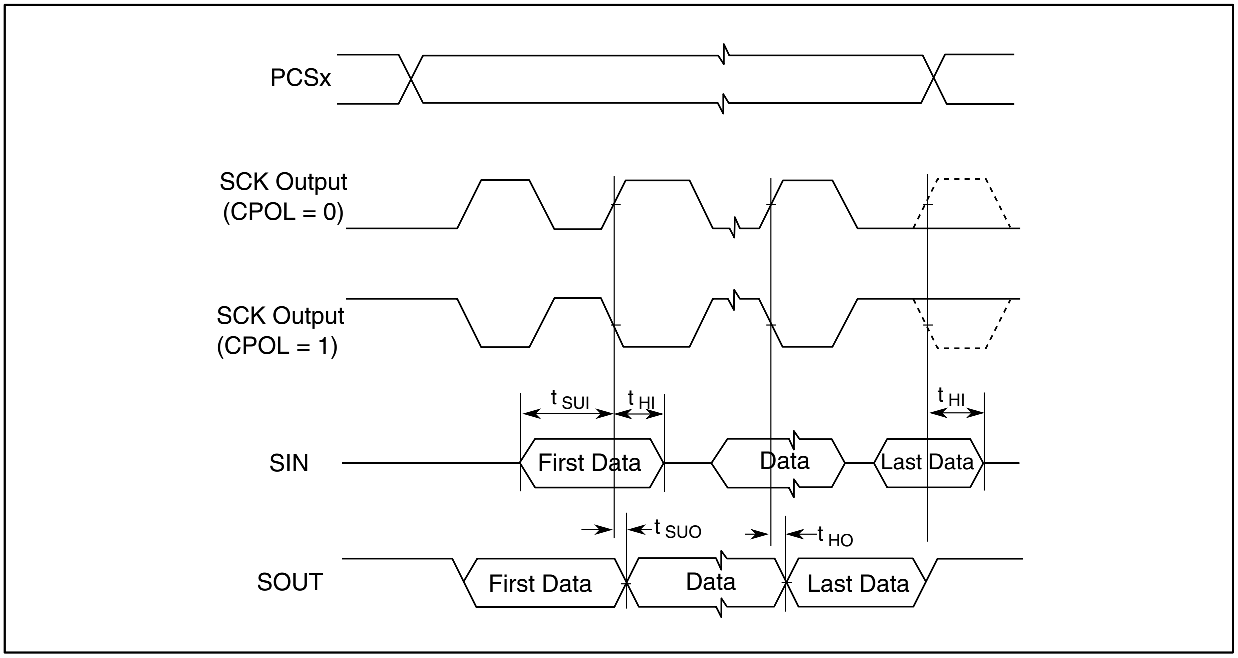


Figure 39. DSPI LVDS master mode – modified timing, CPHA = 1

3.13.9.1.4 DSPI Master Mode – Output Only

Table 46. DSPI LVDS master timing — output only — timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock[1], [2]

#	Symbol	Characteristic	Condition[3]		Value[4]		Unit
			Pad drive[5]	Load (C_L)	Min	Max	
1	t_{SCK}	SCK cycle time	LVDS	15 pF to 50 pF differential	25	—	ns
2	t_{CSV}	PCS valid after SCK[6] (SCK with 50 pF differential load cap.)	PCR[SRC]=11b	25 pF	—	8	ns
			PCR[SRC]=10b	50 pF	—	12	ns
3	t_{CSH}	PCS hold after SCK[6] (SCK with 50 pF differential load cap.)	PCR[SRC]=11b	0 pF	–4.0	—	ns
			PCR[SRC]=10b	0 pF	–4.0	—	ns
4	t_{SDC}	SCK duty cycle (SCK with 50 pF differential load cap.)	LVDS	15 pF to 50 pF differential	$1/2t_{SCK} - 2$	$1/2t_{SCK} + 2$	ns
SOUT data valid time (after SCK edge)							
5	t_{SUO}	SOUT data valid time from SCK[7]	LVDS	15 pF to 50 pF differential	—	6	ns
SOUT data hold time (after SCK edge)							
6	t_{HO}	SOUT data hold time after SCK[7]	LVDS	15 pF to 50 pF differential	–7.0	—	ns

1. All DSPI timing specifications apply to pins when using LVDS pads for SCK and SOUT and CMOS pad for PCS with pad driver strength as defined. Timing may degrade for weaker output drivers.
2. TSB = 1 or ITSB = 1 automatically selects MTFE = 1 and CPHA = 1.
3. When a characteristic involves two signals, the pad drive and load conditions apply to each signal's pad, unless specified otherwise.
4. All timing values for output signals in this table are measured to 50% of the output voltage.
5. Pad drive is defined as the PCR[SRC] field setting in the SIU. Timing is guaranteed to same drive capabilities for all signals; mixing of pad drives may reduce operating speeds and may cause incorrect operation.
6. With TSB mode or Continuous SCK clock mode selected, PCS and SCK are driven by the same edge of DSPI_CLKn. This timing value is due to pad delays and signal propagation delays.
7. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Table 47. DSPI CMOS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock [1], [2]

#	Symbol	Characteristic	Condition[3]		Value[4]		Unit
			Pad drive[5]	Load (C_L)	Min	Max	
1	t_{SCK}	SCK cycle time	PCR[SRC]=11b	25 pF	33.0	—	ns
			PCR[SRC]=10b	50 pF	80.0	—	ns
			PCR[SRC]=01b	50 pF	200.0	—	ns
2	t_{CSV}	PCS valid after SCK[6]	PCR[SRC]=11b	25 pF	7	—	ns
			PCR[SRC]=10b	50 pF	8	—	ns
			PCR[SRC]=01b	50 pF	18	—	ns
			PCS: PCR[SRC]=01b SCK: PCR[SRC]=10b	50 pF	45	—	ns

Table continues on the next page...

Table 47. DSPI CMOS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock [1], [2] (continued)

#	Symbol	Characteristic	Condition[3]		Value[4]		Unit
			Pad drive[5]	Load (C_L)	Min	Max	
3	t_{CSH}	PCS hold after SCK[6]	PCR[SRC]=11b	PCS: 0 pF SCK: 50 pF	–14	—	ns
			PCR[SRC]=10b	PCS: 0 pF SCK: 50 pF	–14	—	ns
			PCR[SRC]=01b	PCS: 0 pF SCK: 50 pF	–33	—	ns
			PCS: PCR[SRC]=01b SCK: PCR[SRC]=10b	PCS: 0 pF SCK: 50 pF	–35	—	ns
4	t_{SDC}	SCK duty cycle[7]	PCR[SRC]=11b	0 pF	$1/2t_{SCK} - 2$	$1/2t_{SCK} + 2$	ns
			PCR[SRC]=10b	0 pF	$1/2t_{SCK} - 2$	$1/2t_{SCK} + 2$	ns
			PCR[SRC]=01b	0 pF	$1/2t_{SCK} - 5$	$1/2t_{SCK} + 5$	ns
SOUT data valid time (after SCK edge)							
9	t_{SUO}	SOUT data valid time from SCK CPHA = 1[8]	PCR[SRC]=11b	25 pF	—	7.0	ns
			PCR[SRC]=10b	50 pF	—	8.0	ns
			PCR[SRC]=01b	50 pF	—	18.0	ns
SOUT data hold time (after SCK edge)							
10	t_{HO}	SOUT data hold time after SCK CPHA = 1[8]	PCR[SRC]=11b	25 pF	–9.0	—	ns
			PCR[SRC]=10b	50 pF	–10.0	—	ns
			PCR[SRC]=01b	50 pF	–21.0	—	ns

1. TSB = 1 or ITSB = 1 automatically selects MTFE = 1 and CPHA = 1.
2. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.
3. When a characteristic involves two signals, the pad drive and load conditions apply to each signal's pad, unless specified otherwise.
4. All timing values for output signals in this table are measured to 50% of the output voltage.
5. Pad drive is defined as the PCR[SRC] field setting in the SIU. Timing is guaranteed to same drive capabilities for all signals; mixing of pad drives may reduce operating speeds and may cause incorrect operation.
6. With TSB mode or Continuous SCK clock mode selected, PCS and SCK are driven by the same edge of DSPI_CLKn. This timing value is due to pad delays and signal propagation delays.
7. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
8. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

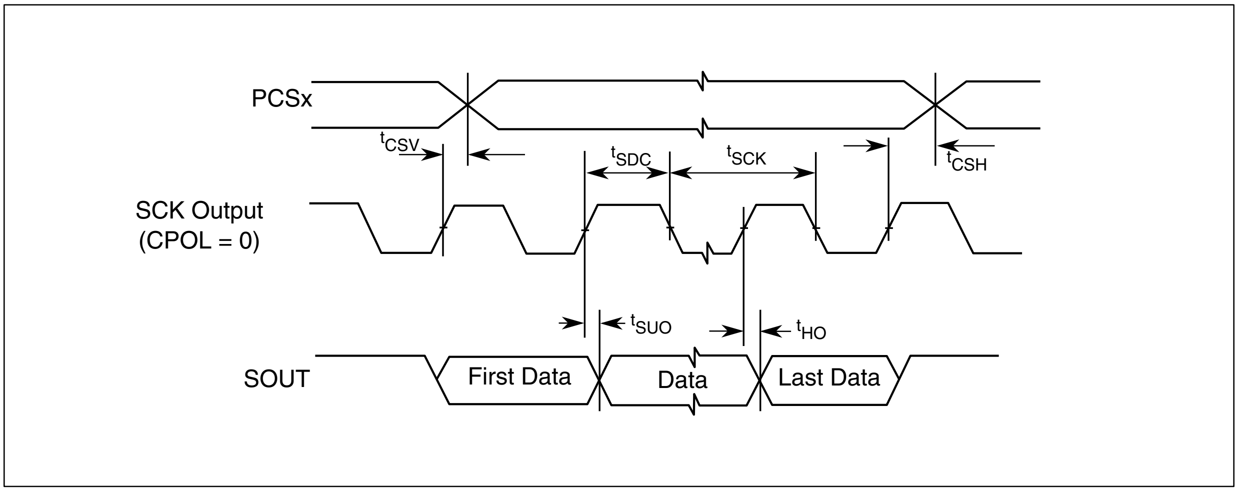


Figure 40. DSPI LVDS and CMOS master timing – output only – modified transfer format MTFE = 1, CHPA = 1

3.13.10 FEC timing

3.13.10.1 MII receive signal timing (RXD[3:0], RX_DV, and RX_CLK)

The receiver functions correctly up to a RX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the RX_CLK frequency.

Table 48. MII receive signal timing[1]

Symbol	Characteristic	Value		Unit
		Min	Max	
M1	RXD[3:0], RX_DV to RX_CLK setup	5	—	ns
M2	RX_CLK to RXD[3:0], RX_DV hold	5	—	ns
M3	RX_CLK pulse width high	35%	65%	RX_CLK period
M4	RX_CLK pulse width low	35%	65%	RX_CLK period

1. All timing specifications valid to the pad input levels defined in I/O pad current specifications.

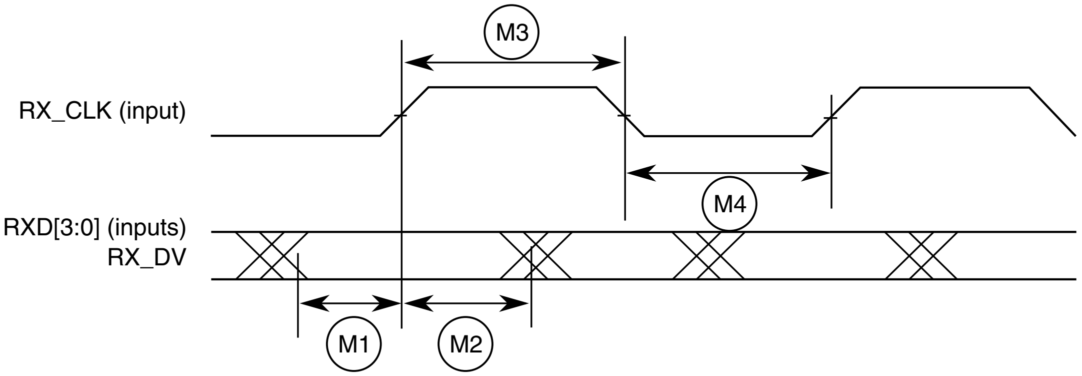


Figure 41. MII receive signal timing diagram

3.13.10.2 MII transmit signal timing (TXD[3:0], TX_EN, and TX_CLK)

The transmitter functions correctly up to a TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the TX_CLK frequency.

The transmit outputs (TXD[3:0], TX_EN) can be programmed to transition from either the rising or falling edge of TX_CLK, and the timing is the same in either case. This options allows the use of noncompliant MII PHYs.

Refer to the *MPC5777C Microcontroller Reference Manual's* Fast Ethernet Controller (FEC) chapter for details of this option and how to enable it.

Table 49. MII transmit signal timing[1]

Symbol	Characteristic	Value[2]		Unit
		Min	Max	
M5	TX_CLK to TXD[3:0], TX_EN invalid	4.5	—	ns
M6	TX_CLK to TXD[3:0], TX_EN valid	—	25	ns
M7	TX_CLK pulse width high	35%	65%	TX_CLK period
M8	TX_CLK pulse width low	35%	65%	TX_CLK period

1. All timing specifications valid to the pad input levels defined in I/O pad specifications.
2. Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.

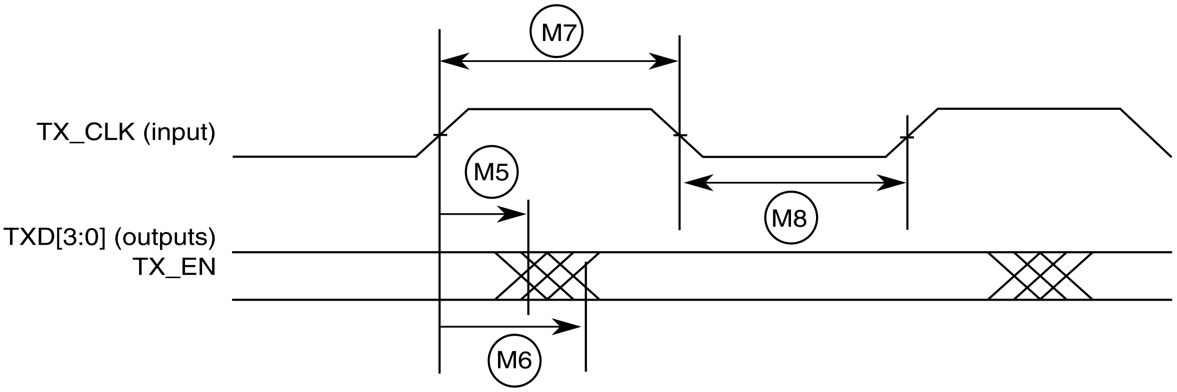


Figure 42. MII transmit signal timing diagram

3.13.10.3 MII async inputs signal timing (CRS)

Table 50. MII async inputs signal timing

Symbol	Characteristic	Value		Unit
		Min	Max	
M9	CRS minimum pulse width	1.5	—	TX_CLK period

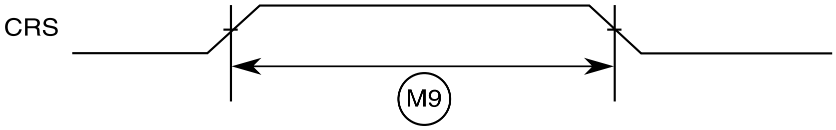


Figure 43. MII async inputs timing diagram

3.13.10.4 MII and RMII serial management channel timing (MDIO and MDC)

The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 51. MII serial management channel timing[1]

Symbol	Characteristic	Value[2]		Unit
		Min	Max	
M10	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	MDIO (input) to MDC rising edge setup	10	—	ns
M13	MDIO (input) to MDC rising edge hold	0	—	ns
M14	MDC pulse width high	40%	60%	MDC period
M15	MDC pulse width low	40%	60%	MDC period

1. All timing specifications valid to the pad input levels defined in I/O pad specifications.
2. Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value

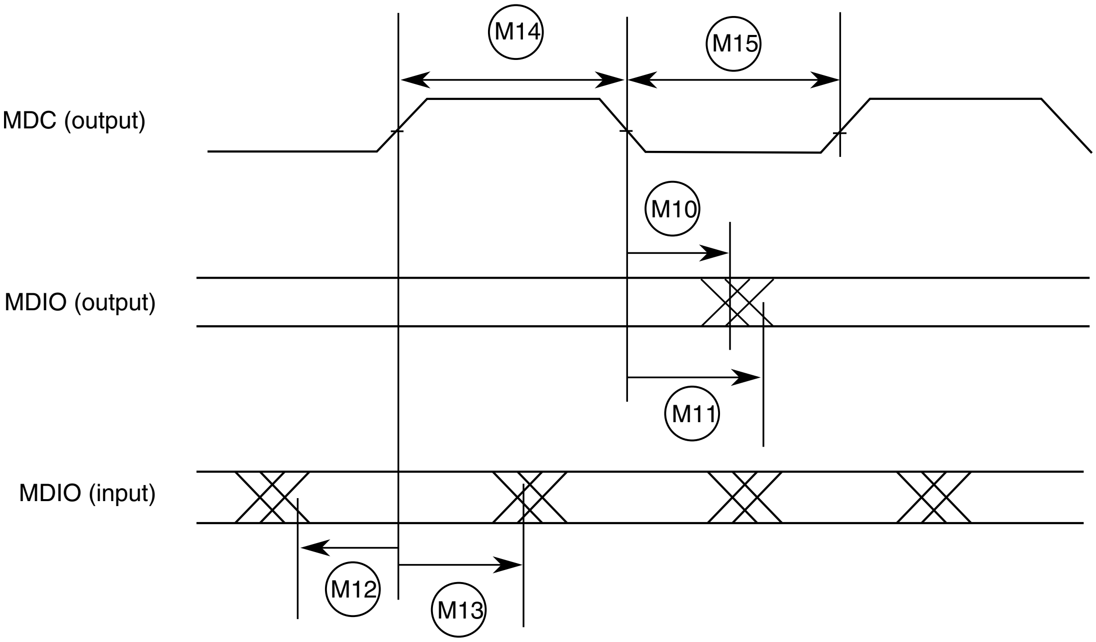


Figure 44. MII serial management channel timing diagram

3.13.10.5 RMII receive signal timing (RXD[1:0], CRS_DV)

The receiver functions correctly up to a REF_CLK maximum frequency of 50 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the RX_CLK frequency, which is half that of the REF_CLK frequency.

Table 52. RMII receive signal timing[1]

Symbol	Characteristic	Value		Unit
		Min	Max	
R1	RXD[1:0], CRS_DV to REF_CLK setup	4	—	ns
R2	REF_CLK to RXD[1:0], CRS_DV hold	2	—	ns
R3	REF_CLK pulse width high	35%	65%	REF_CLK period
R4	REF_CLK pulse width low	35%	65%	REF_CLK period

[1] All timing specifications valid to the pad input levels defined in I/O pad specifications.

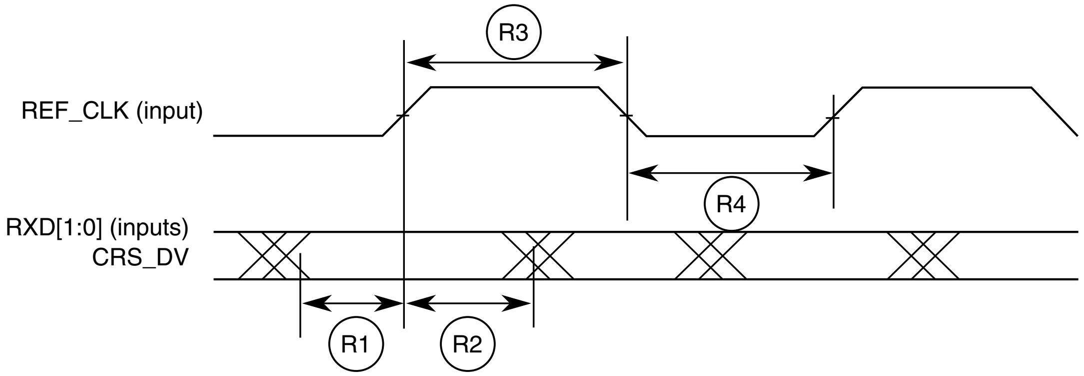


Figure 45. RMII receive signal timing diagram

3.13.10.6 RMII transmit signal timing (TXD[1:0], TX_EN)

The transmitter functions correctly up to a REF_CLK maximum frequency of 50 MHz + 1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the TX_CLK frequency, which is half that of the REF_CLK frequency.

The transmit outputs (TXD[1:0], TX_EN) can be programmed to transition from either the rising or falling edge of REF_CLK, and the timing is the same in either case. This options allows the use of non-compliant RMII PHYs.

Table 53. RMII transmit signal timing[1]

Symbol	Characteristic	Value[2]		Unit
		Min	Max	
R5	REF_CLK to TXD[1:0], TX_EN invalid	2	—	ns
R6	REF_CLK to TXD[1:0], TX_EN valid	—	16	ns
R7	REF_CLK pulse width high	35%	65%	REF_CLK period
R8	REF_CLK pulse width low	35%	65%	REF_CLK period

1. All timing specifications valid to the pad input levels defined in I/O pad specifications.
2. Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.

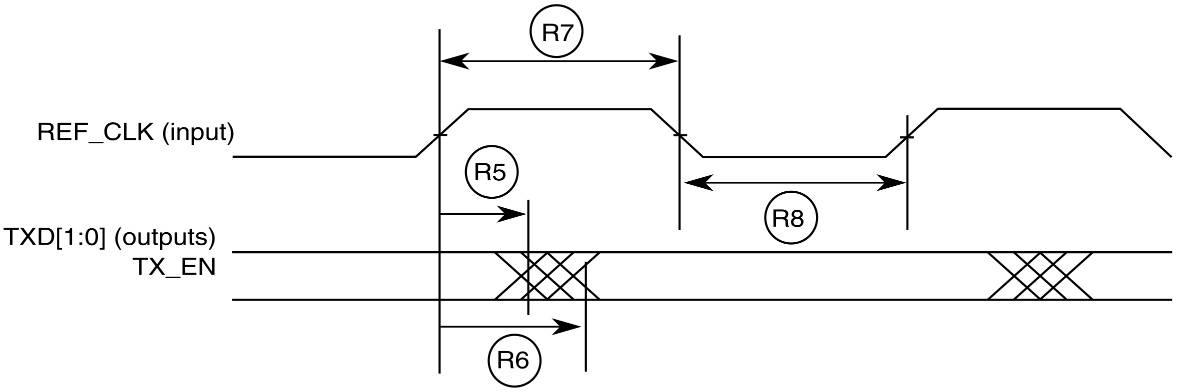


Figure 46. RMII transmit signal timing diagram

4 Package information

To find the package drawing for each package, go to http://www.nxp.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
416-ball MAPBGA	98ASA00562D
516-ball MAPBGA	98ASA00623D

4.1 Thermal characteristics

Table 54. Thermal characteristics, 416-ball MAPBGA package

Characteristic	Symbol	Value	Unit
Junction to Ambient [1, 2] Natural Convection (Single layer board)	$R_{\Theta JA}$	28.8	°C/W
Junction to Ambient [1, 3] Natural Convection (Four layer board 2s2p)	$R_{\Theta JA}$	19.6	°C/W
Junction to Ambient (@200 ft./min., Single layer board)	$R_{\Theta JMA}$	21.3	°C/W
Junction to Ambient (@200 ft./min., Four layer board 2s2p)	$R_{\Theta JMA}$	15.1	°C/W
Junction to Board [4]	$R_{\Theta JB}$	9.5	°C/W
Junction to Case [5]	$R_{\Theta JC}$	4.8	°C/W
Junction to Package Top [6] Natural Convection	Ψ_{JT}	0.2	°C/W

1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Table 55. Thermal characteristics, 516-ball MAPBGA package

Characteristic	Symbol	Value	Unit
Junction to Ambient [1, 2] Natural Convection (Single layer board)	$R_{\Theta JA}$	28.5	°C/W
Junction to Ambient [1, 3] Natural Convection (Four layer board 2s2p)	$R_{\Theta JA}$	20.0	°C/W
Junction to Ambient (@200 ft./min., Single layer board)	$R_{\Theta JMA}$	21.3	°C/W
Junction to Ambient (@200 ft./min., Four layer board 2s2p)	$R_{\Theta JMA}$	15.5	°C/W
Junction to Board [4]	$R_{\Theta JB}$	8.8	°C/W
Junction to Case [5]	$R_{\Theta JC}$	4.8	°C/W
Junction to Package Top [6] Natural Convection	Ψ_{JT}	0.2	°C/W

1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

4.1.1 General notes for thermal characteristics

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} * P_D)$$

where:

T_A = ambient temperature for the package (°C)

$R_{\Theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component

- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm^2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta \mathrm{JB}} * P_D)$$

where:

T_B = board temperature for the package perimeter (°C)

$R_{\Theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, the junction temperature is predictable if the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\Theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\Theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\Theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\Theta JC}$ is device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\Theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models. More accurate compact Flotherm models can be generated upon request.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} x P_D)$$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately

1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

When board temperature is perfectly defined below the device, it is possible to use the thermal characterization parameter (Ψ_{JPB}) to determine the junction temperature by measuring the temperature at the bottom center of the package case (exposed pad) using the following equation:

$$T_J = T_B + (\Psi_{JPB} x P_D)$$

where:

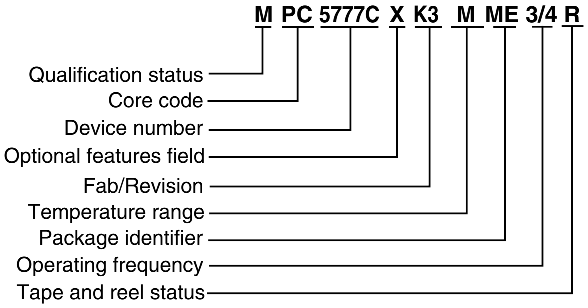
T_T = thermocouple temperature on bottom of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

5 Ordering information

Figure 47 and Table 56 describe orderable part numbers for the MPC5777C.



Temperature range
M = –40 °C to 125 °C

Operating frequency
3 = 2 x 264 MHz
4 = 2 x 300 MHz

Package identifier
ME = 416 MAPBGA Pb-Free
MO = 516 MAPBGA Pb-Free

Tape and reel status
R = Tape and reel
(blank) = Trays

Qualification status
P = Pre-qualification
M = Fully spec. qualified, general market flow
S = Fully spec. qualified, automotive flow

Optional features field
(blank) = ISO-compliant CAN FD not available, trimmed for SMPS or external regulator, and includes SHE-compliant security firmware version 2.07
A = ISO-compliant CAN FD not available, trimmed for SMPS or external regulator, and includes SHE-compliant security firmware version 2.08
R = ISO-compliant CAN FD not available, trimmed for LDO regulator, and includes SHE-compliant security firmware version 2.08
C = ISO-compliant CAN FD available, trimmed for SMPS or external regulator, and includes SHE-compliant security firmware version 2.07
D = ISO-compliant CAN FD available, trimmed for SMPS or external regulator, and includes SHE-compliant security firmware version 2.08
L = ISO-compliant CAN FD available, trimmed for LDO regulator, and includes SHE-compliant security firmware version 2.08
S = ISO-compliant CAN FD available, trimmed for SMPS or external regulator, and includes RSA-enhanced security firmware
T = ISO-compliant CAN FD available, trimmed for LDO regulator, and includes RSA-enhanced security firmware

Note: Not all options are available on all devices.

Figure 47. MPC5777C Orderable part number description

Table 56. Example orderable part numbers

Part number[1]	Package description	Speed (MHz)[2]	Operating temperature[3]	
			Min (T_L)	Max (T_H)
SPC5777CCK3MME3	MPC5777C 416 package Lead-free (Pb-free)	264	–40 °C	125 °C
SPC5777CK3MME3	MPC5777C 416 package Lead-free (Pb-free)	264	–40 °C	125 °C
SPC5777CCK3MMO3	MPC5777C 516 package Lead-free (Pb-free)	264	–40 °C	125 °C
SPC5777CK3MMO3	MPC5777C 516 package Lead-free (Pb-free)	264	–40 °C	125 °C

1. All packaged devices are PPC5777C, rather than MPC5777C or SPC5777C, until product qualifications are complete. The unpackaged device prefix is PCC, rather than SCC, until product qualification is complete.

   Not all configurations are available in the PPC parts.
2. For the operating mode frequency of various blocks on the device, see Table 3.
3. The lowest ambient operating temperature is referenced by T_L; the highest ambient operating temperature is referenced by T_H.

6 Document revision history

The following table summarizes revisions to this document since the previous release.

Table 57. Revision history

Revision	Date	Description of changes
14	01/2020	In Table 17, updated the footnote from "TUE does not apply to differential conversions" to "TUE, Gain, and Offset specifications do not apply to differential conversions". In Table 4 added Max value 120 µA for 40°C and 360 µA for 85°C for I_{STBY}.
13	08/2018	In Table 3, added information for 300 MHZ frequency: • f_{SYS} • f_{PLATF} • f_{ETPU} • f_{PER} • f_{fFM_PER} In Table 12 added Max value 240 MHz for $f_{PLL0PHI}$ and Table 13 added Max value 300 MHz for $f_{PLL1PHI}$. In Table 34 updated the row from "100 MHz > fPLATF ≤ 133 MHz" to "100 MHz > fPLATF ≤ 150 MHz" under "Flash memory frequency" column. In Figure 47 added 300 MHz frequency orderable part number.

Table continues on the next page...

Table 57. Revision history (continued)

Revision	Date	Description of changes
12	08/2018	In Table 12 of PLL electrical specifications, changed text of footnote 1: • from: "f_{PLL0IN} frequency must be scaled down using PLLDIG_PLL0DV[PREDIV] to ensure PFD input signal is in the range 8 MHz to 20 MHz." • to: "Ensure that the f_{PLL0IN} frequency divided by PLLDIG_PLL0DV[PREDIV] is in the range 8 MHz to 20 MHz." In Table 17 of Enhanced Queued Analog-to-Digital Converter (eQADC), added footnote about Max value of Conversion Cycles (CC): "128 sampling cycles (LST=128), differential conversion, pregain of x4" In Table 38 of External Bus Interface (EBI) timing, changed text of footnote 1: • from: "EBI timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, T_A = T_L to T_H, and C_L = 30 pF with SIU_PCR[DSC] = 10b for ADDR/CTRL and SIU_PCR[DSC] = 11b for CLKOUT/DATA." • to: "EBI timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, T_A = T_L to T_H, and C_L = 30 pF with SIU_PCR[DSC] = 11b for ADDR/CTRL and SIU_PCR[SRC] = 11b for DATA/ALE." In I/O pad current specifications added the text "The EBI power segments have..........segment does not exceed the spec".

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ПОСТАВКА
ЭЛЕКТРОННЫХ КОМПОНЕНТОВ

многоканальный
+7 495 668 12 70
info@moschip.ru

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9