19-5788; Rev 3; 5/12

EVALUATION KIT AVAILABLE

MAX14824

IO-Link Master Transceiver

General Description

The MAX14824 is an IO-Link® master interface that integrates an IO-Link physical layer transceiver with an auxiliary digital input and two linear regulators. High port count IO-Link master applications are supported through in-band SPI addressing, and the 12MHz SPI interface minimizes host controller access times. In-band addressing and selectable SPI addresses enable cascading up to 16 devices.

The device supports all the IO-Link data rates and features slew-rate-controlled drivers to reduce EMI. The driver is guaranteed to drive up to 300mA (min) load currents. Internal wake-up circuitry automatically determines the correct wake-up polarity, allowing for the use of simple UARTs for wake-up pulse generation.

The MAX14824 is available in a 4mm x 4mm, 24-pin TQFN package with exposed pad, and operates over the extended -40°C to +105°C temperature range.

Applications

IO-Link Master Controllers

PLC Fieldbus Gateways

High Port Count IO-Link Masters

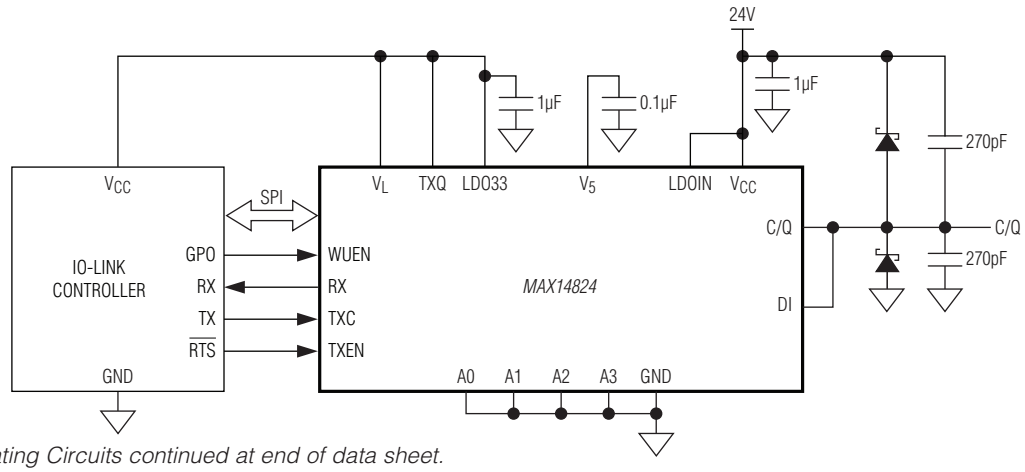
24V Digital Inputs and Outputs

***Ordering Information* appears at end of data sheet.**

Features

- **IO-Link v.1.0 and v.1.1 Physical Layer Compliant**
- **Supports COM1, COM2, and COM3 Data Rates**
- **Push-Pull, High-Side, or Low-Side Outputs**
- **300mA C/Q Output Drive**
- **1µF C/Q Load Drive Capability**
- **Generates 500mA Wake-Up Pulse**
- **Automatic Wake-Up Pulse Polarity**
- **Auxiliary Digital Input**
- **5V and 3.3V Linear Regulators**
- **SPI Interface for Configuration and Monitoring**
- **SPI-Based Chip Addressing**
- **EMI Emission Control Through Slew-Controlled Driver**
- **Reverse-Polarity Protection on DI**
- **Short-Circuit Protection on C/Q**
- **High Temperature Warning and Thermal Shutdown**
- **Extensive Fault Monitoring and Reporting**
- **-40°C to +105°C Operating Temperature Range**
- **4mm x 4mm TQFN Package**

Typical Operating Circuits



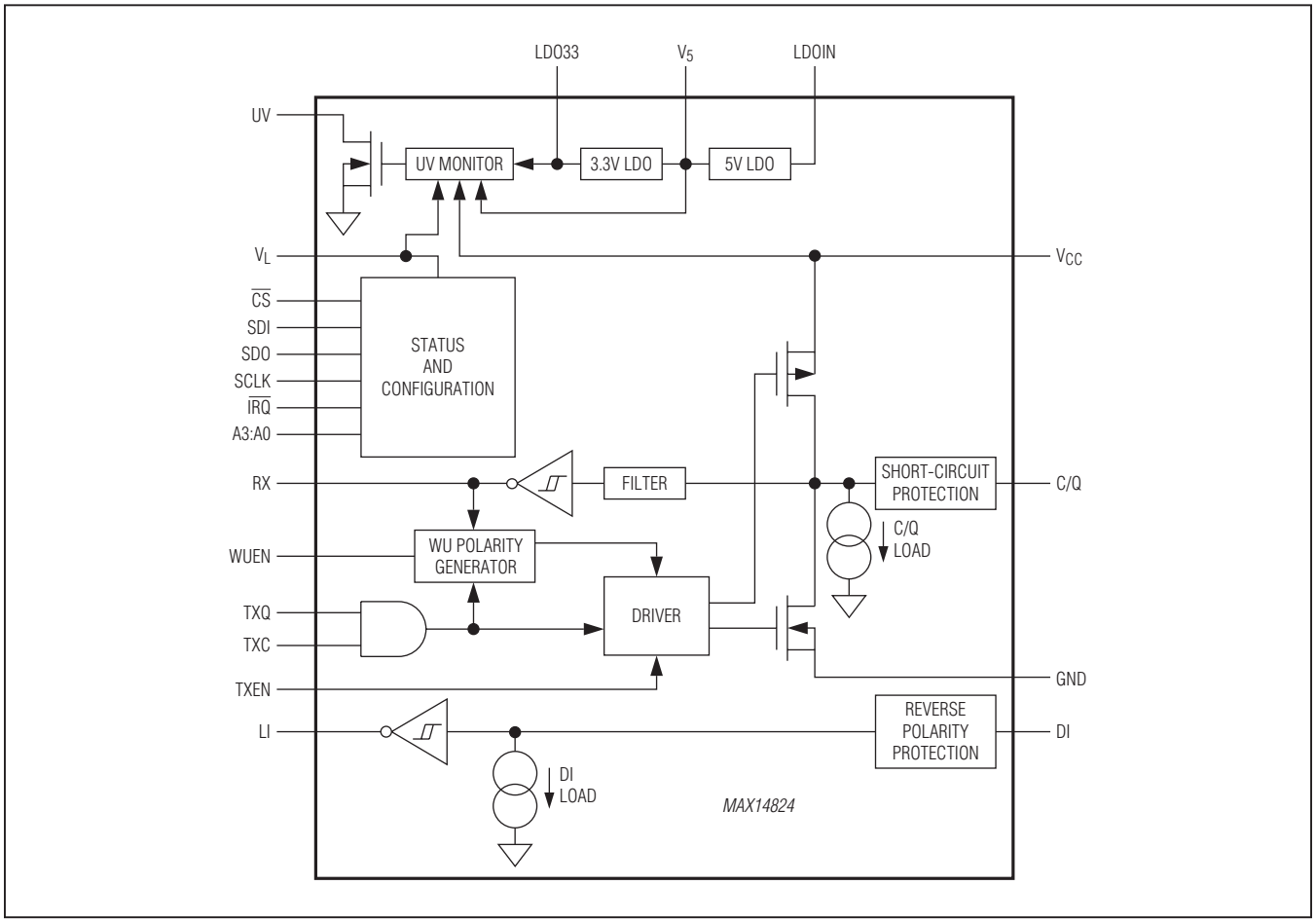
Typical Operating Circuits continued at end of data sheet.

IO-Link is a registered trademark of Profibus User Organization (PNO).

*For related parts and recommended products to use with this part, refer to: **www.maxim-ic.com/MAX14824.related***

IO-Link Master Transceiver

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND, unless otherwise specified.)

V_{CC} ..... -0.3V to +40V
LDOIN ..... -0.3V to +40V
V_5 ..... 0.3V to the lesser of (V_{LDOIN} + 0.3V) and +6V
LDO33 ..... -0.3V to the lesser of (V_5 + 0.3V) and +6V
V_L ..... -0.3V to +6V
DI ..... -40V to +40V
C/Q ..... -0.3V to (V_{CC} + 0.3V)
Logic Inputs
  TXC, TXQ, TXEN, A2, $\overline{CS}$, SDI, SCLK, WUEN .. -0.3V to (V_L + 0.3V)
  A3, A1, A0 ..... -0.3V to +6V
Logic Outputs
  RX, LI, SDO, $\overline{IRQ}$ ..... -0.3V to (V_L + 0.3V)
  UV ..... -0.3V to +6V
Continuous Current Into Any Logic Pin ..... ±50mA
Continuous Power Dissipation
  TQFN (derate 27.8mW/°C above +70°C) 2222mW
Operating Temperature Range ..... -40°C to +105°C
Maximum Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN
  Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 36°C/W
  Junction-to-Case Thermal Resistance (θ_{JC}) ..... 3°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 18V to 36V, V_L = 2.3V to 5.5V, V_{GND} = 0V; all logic inputs at V_L or GND; T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{CC} = 24V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Supply Voltage	V_{CC}	For driver operation	9		36	V
V_{CC} Supply Current	I_{CC}	V_{CC} = 24V, C/Q as input, no load on V_5 or LDO33, LDOIN not connected to V_{CC}, V_{LDOIN} = 24V		1.3	2.5	mA
V_{CC} Undervoltage Lockout Threshold	V_{CCUVLO}	V_{CC} falling	6	7.5	9	V
V_{CC} Undervoltage Lockout Threshold Hysteresis	V_{CCUVLO_HYST}			200		mV
V_5 Supply Current	I_{5_IN}	LDOIN shorted to V_5, external 5V applied to V_5, no switching, LDO33 disabled		3		mA
V_5 Undervoltage Lockout Threshold	V_{5UVLO}	V_5 falling		2.4		V
V_L Logic-Level Supply Voltage	V_L		2.3		5.5	V
V_L Logic-Level Supply Current	I_L	All logic inputs at V_L or GND			5	µA
V_L Undervoltage Threshold	V_{LUVLO}	V_L falling	0.65	0.95	1.3	V
5V LDO (V_5)						
LDOIN Input Voltage Range	V_{LDOIN}		7		36	V

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 18V to 36V, V_L = 2.3V to 5.5V, V_{GND} = 0V; all logic inputs at V_L or GND; T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{CC} = 24V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LDOIN Supply Current	I_{LDOIN}	V_{LDOIN} = 24V, C/Q as input, no load on V_5 or LDO33			3.0	5	mA
V_5 Output Voltage Range	V_5	No load on V_5, 7V ≤ V_{LDOIN} ≤ 36V		4.75	5.00	5.25	V
V_5 Load Regulation		1mA < I_{LOAD} < 10mA, V_{LDOIN} = 7V, 0.1µF bypass capacitor on V_5			0.08		%
3.3V LDO (LDO33)							
LDO33 Output Voltage	V_{LDO33}	No load on LDO33		3.1		3.5	V
LDO33 Undervoltage Lockout Threshold	$V_{LDO33UVLO}$	V_{LDO33} falling			2.4		V
LDO33 Load Regulation		1mA < I_{LOAD} < 10mA, V_{LDOIN} = 7V			0.25		%
24V INTERFACE							
C/Q Output Resistance High	$R_{OH\_C/Q}$	C/Q high-side enabled, $I_{C/Q}$ = -200mA, 9V ≤ V_{CC} ≤ 36V (Note 5)			1.8	2.9	Ω
C/Q Output Resistance Low	$R_{OL\_C/Q}$	C/Q low-side enabled, $I_{C/Q}$ = +200mA, 9V ≤ V_{CC} ≤ 36V (Note 5)			2.0	3.6	Ω
C/Q Source Current Limit	$I_{OH\_C/Q}$	C/Q high-side enabled, $V_{C/Q}$ < (V_{CC} - 3V), 9V ≤ V_{CC} ≤ 36V		+500	+670		mA
C/Q Sink Current Limit	$I_{OL\_C/Q}$	C/Q low-side enabled, $V_{C/Q}$ > 3V, 9V ≤ V_{CC} ≤ 36V			-660	-500	mA
C/Q Input Threshold High	$V_{IH\_C/Q}$	C/Q driver disabled		10.5		13.0	V
C/Q Input Threshold Low	$V_{IL\_C/Q}$	C/Q driver disabled		8.0		11.5	V
C/Q Input Hysteresis	$V_{HYS\_C/Q}$	C/Q driver disabled		1.0			V
DI Input Threshold High	V_{IH_DI}			6.8		8	V
DI Input Threshold Low	V_{IL_DI}			5.2		6.4	V
DI Input Hysteresis	V_{HYS_DI}			1			V
C/Q Weak Pulldown Current	$I_{PDC/Q}$	C/Q driver disabled, $V_{C/Q}$ = V_{CC}		100		400	µA
DI Weak Pulldown Current	I_{PDDI}	DI load disabled, V_{DI} = V_{CC}		50		300	µA
C/Q Input Capacitance	$C_{C/Q}$	C/Q driver disabled			40		pF
DI Input Capacitance	C_{DI}				20		pF
C/Q, DI INPUT LOAD							
C/Q Load Current	$I_{LLM\_C/Q}$	C/Q load enabled (C/QLoad = 1)	0 ≤ $V_{C/Q}$ ≤ 5V	0		8.1	mA
			9V ≤ $V_{C/Q}$	5	6.8	8.1	
DI Load Current	I_{LLM_DI}	DI load enabled (DiLoad = 1)	0 ≤ V_{DI} ≤ 5V	0		4.3	mA
			9V ≤ V_{DI}	2	3.5	4.3	

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 18V to 36V, V_L = 2.3V to 5.5V, V_{GND} = 0V; all logic inputs at V_L or GND; T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{CC} = 24V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS (TXC, TXQ, TXEN, $\overline{CS}$, WUEN, SDI, SCLK, A3, A2, A1, A0)						
Logic Input-Voltage Low	V_{IL}		0.3 x V_L			V
Logic Input-Voltage High	V_{IH}				0.7 x V_L	V
Logic Input Leakage Current	I_{LEAK}	Logic input = GND or V_L	-1		+1	µA
Logic Input Capacitance	C_{IN}			5		pF
A1 Pulldown Resistance	R_{A1PD}		325		800	kΩ
LOGIC OUTPUTS (RX, LI, UV, SDO, $\overline{IRQ}$)						
Logic Output-Voltage Low	V_{OL}	I_{OUT} = -5mA			0.4	V
Logic Output-Voltage High	V_{OHRX}, V_{OHWU}, V_{OHLI}, V_{OHSDO}, V_{OHIRQ},	I_{OUT} = 5mA (Note 3)	V_L - 0.6			V
SDO Leakage Current	I_{LK_SDO}	SDO disabled, SDO = GND or V_L	-1		+1	µA
THERMAL SHUTDOWN						
Thermal Warning Threshold		Die temperature rising, OTemp bit is set		+115		°C
Thermal Warning Threshold Hysteresis		Die temperature falling, OTemp bit is cleared		20		°C
Thermal Shutdown Threshold		Die temperature rising		+150		°C
Thermal Shutdown Hysteresis				20		°C

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 18V to 36V, V_L = 2.3V to 5.5V, V_{GND} = 0V; all logic inputs at V_L or GND; T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{CC} = 24V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
C/Q, DI INTERFACES							
Data Rate	DR	HiSlew = 1		4.8		230.4	kbps
		HiSlew = 0		4.8		38.4	
DRIVER (C/Q)							
Driver Low-to-High Propagation Delay	t_{PDLH}	Push-pull or high-side (PNP) configuration, Figure 1	HiSlew = 1		0.5	2	µs
			HiSlew = 0		1.6	5	
Driver High-to-Low Propagation Delay	t_{PDHL}	Push-pull or low-side (NPN) configuration, Figure 1	HiSlew = 1		0.5	2	µs
			HiSlew = 0		1.6	5	

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 18V to 36V, V_L = 2.3V to 5.5V, V_{GND} = 0V; all logic inputs at V_L or GND; T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{CC} = 24V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Driver Skew	t_{SKEW}	$\lvert t_{PDLH} - t_{PDHL} \rvert$			0.1	2	µs
Driver Rise Time	t_{RISE}	Push-pull or high-side (PNP) configuration, Figure 1	HiSlew = 1		0.4	0.85	µs
			HiSlew = 0		1.5	4	
Driver Fall Time	t_{FALL}	Push-pull or low-side (NPN) configuration, Figure 1	HiSlew = 1		0.4	0.85	µs
			HiSlew = 0		1.4	4	
Driver Enable Time High	t_{ENH}	Push-pull or high-side (PNP) configuration, Figure 3	HiSlew = 1		0.3	1.5	µs
			HiSlew = 0		0.8	7	
Driver Enable Time Low	t_{ENL}	Push-pull or low-side (NPN) configuration, Figure 2	HiSlew = 1		0.3	1.5	µs
			HiSlew = 0		0.9	7	
Driver Disable Time High	t_{DISH}	Push-pull or high-side (PNP) configuration, Figure 2 (Note 4)	HiSlew = 1		1.6	3	µs
			HiSlew = 0		1.6	3	
Driver Disable Time Low	t_{DISL}	Push-pull or low-side (NPN) configuration, Figure 3 (Note 4)	HiSlew = 1		0.1	3	µs
			HiSlew = 0		0.1	3	
RECEIVER (C/Q, DI) (Figure 4)							
Receiver Low-to-High Propagation Delay	t_{PRLH}	RxFilter = 0			0.4	2	µs
		RxFilter = 1			0.2	2	
Receiver High-to-Low Propagation Delay	t_{PRHL}	RxFilter = 0			0.5	2	
		RxFilter = 1			0.3	2	
WAKE-UP GENERATION (Figure 5)							
Wake-Up Enable Setup Time	$t_{WUEN,S}$			30			ns
Wake-Up Enable Hold Time	$t_{WUEN,H}$			30			ns
Wake-Up Pulse Rise Propagation Delay	t_1				1.5	5	µs
Wake-Up Pulse Fall Propagation Delay	t_2				1.5	3	µs
SPI TIMING ($\overline{CS}$, SCLK, SDI, SDO) (Figure 6)							
SCLK Clock Period	t_{CH+CL}			83.3			ns
SCLK Pulse-Width High	t_{CH}			41.65			ns
SCLK Pulse-Width Low	t_{CL}			41.65			ns
$\overline{CS}$ Fall to SCLK Rise Time	t_{CSS}			20			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}			20			ns
SDI Hold Time	t_{DH}			10			ns

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 18V to 36V, V_L = 2.3V to 5.5V, V_{GND} = 0V; all logic inputs at V_L or GND; T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{CC} = 24V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDI Setup Time	t_{DS}		10			ns
Output Data Propagation Delay	t_{DO}				32	ns
SDO Rise and Fall Times	t_{FT}				20	ns
Minimum $\overline{CS}$ Pulse	t_{CSW}		76.8			ns

Note 2: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

Note 3: UV is an open-drain output. Connect UV to a voltage less than 5.5V through an external pullup resistor.

Note 4: Disable time measurements are load-dependent.

Note 5: Guaranteed by design. Limits are not production tested.

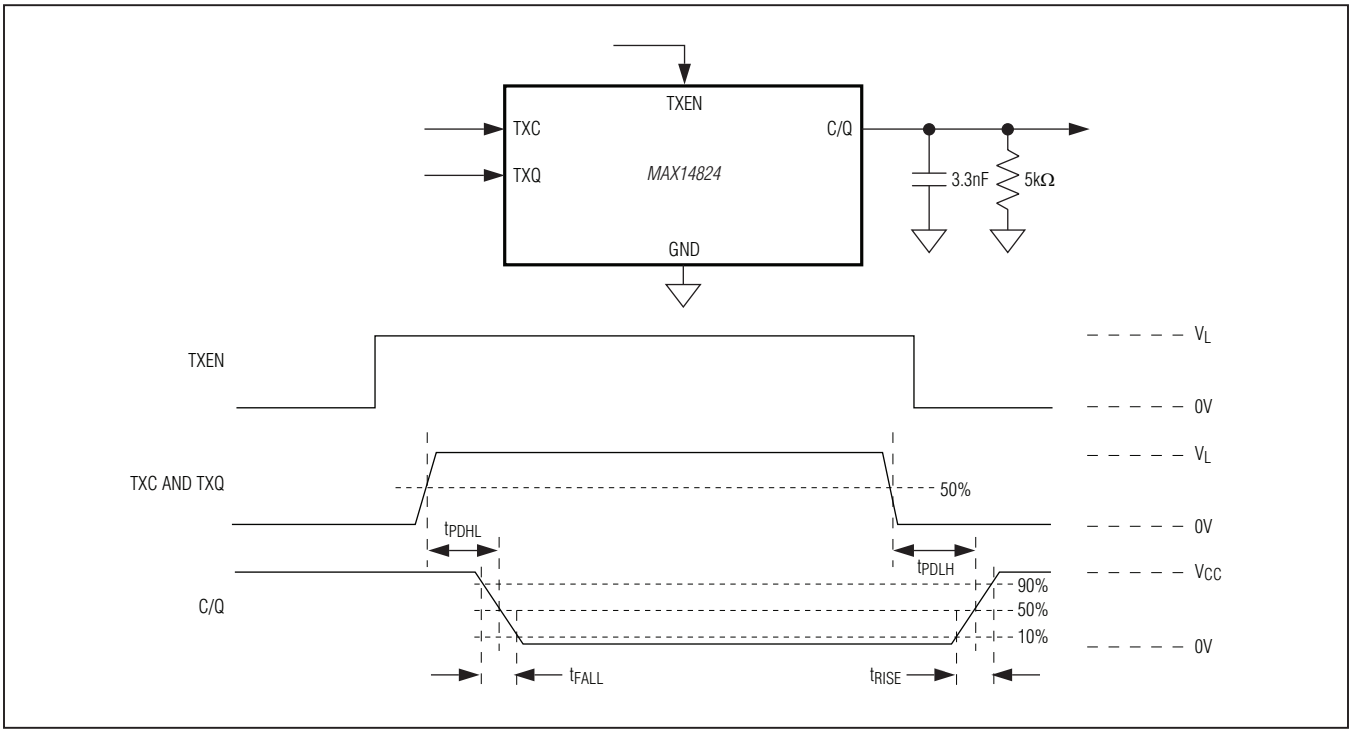


Figure 1. Driver Polarity and Timing

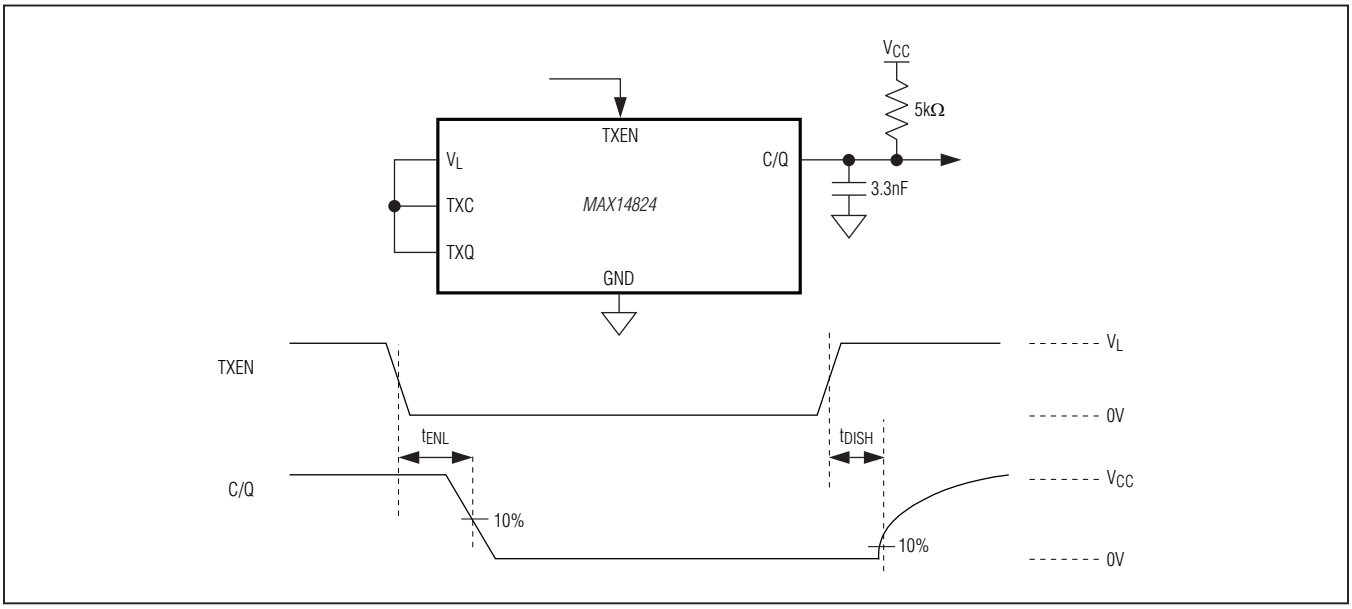


Figure 2. Driver Enable Low and Disable High Timing

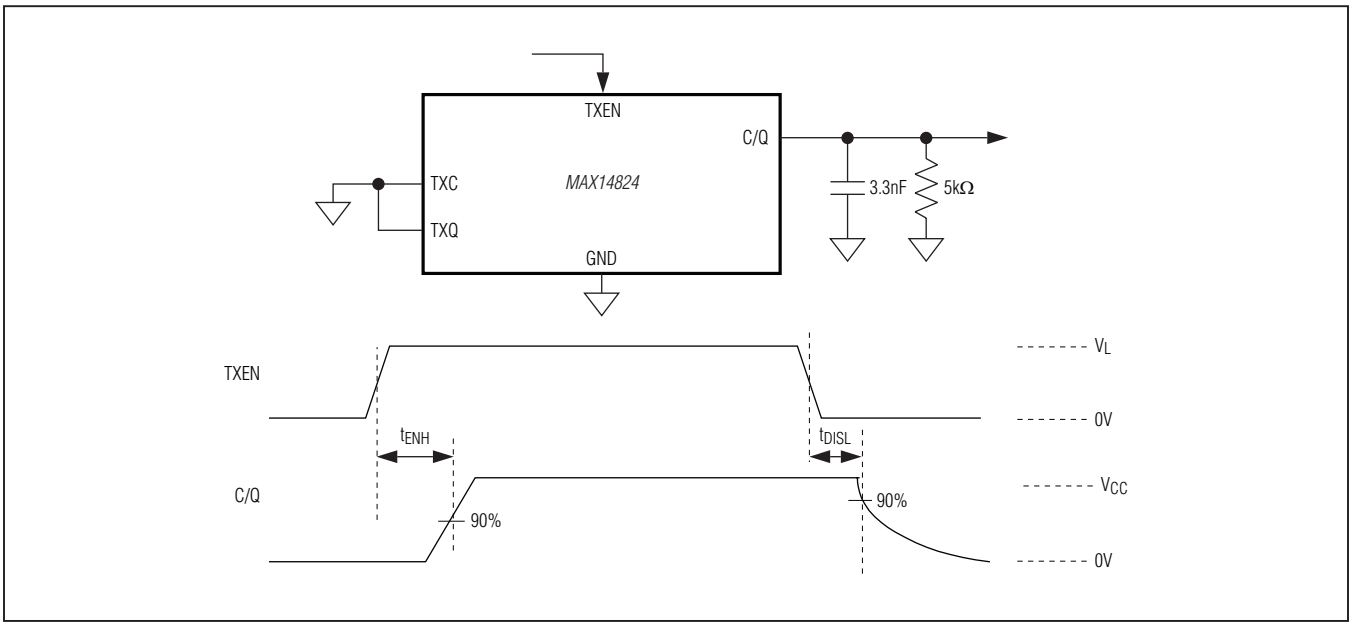


Figure 3. Driver Enable High and Disable Low Timing

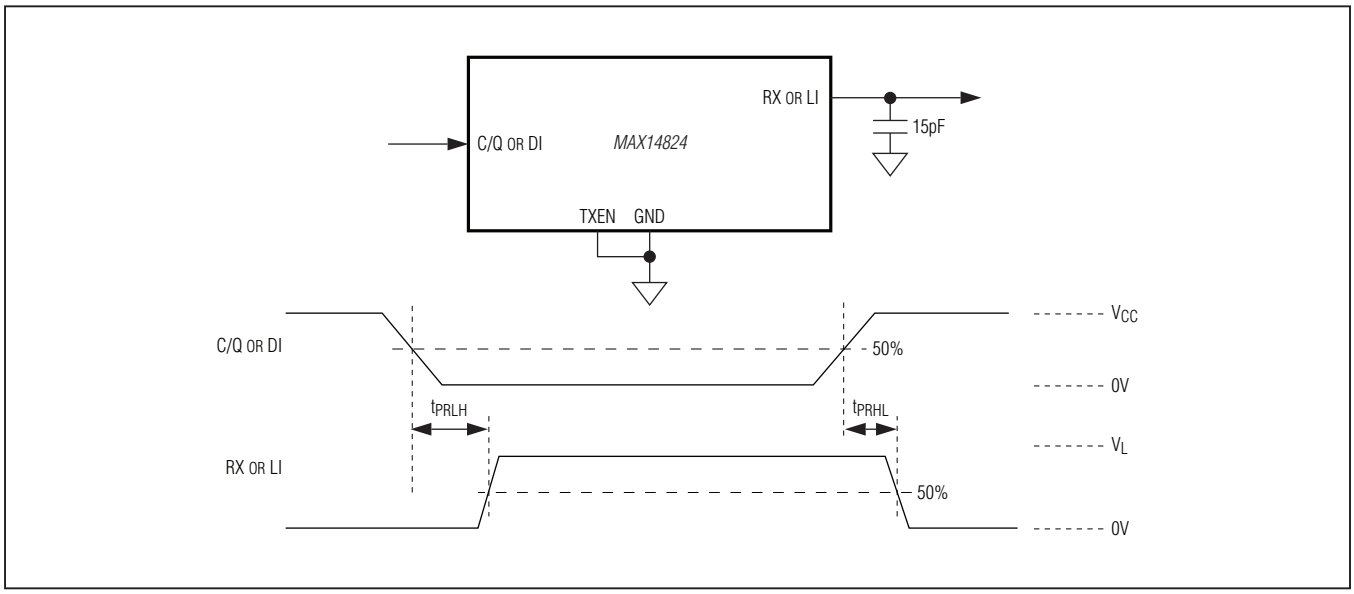


Figure 4. Receiver Polarity and Timing

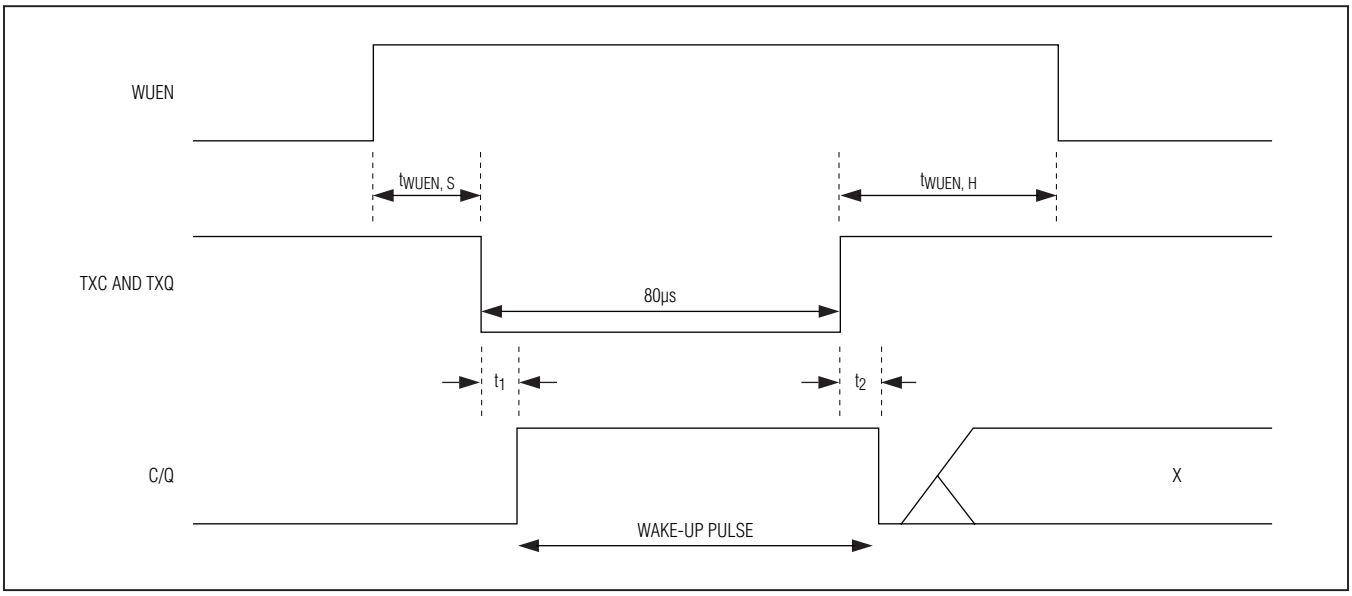


Figure 5. Wake-Up Generation

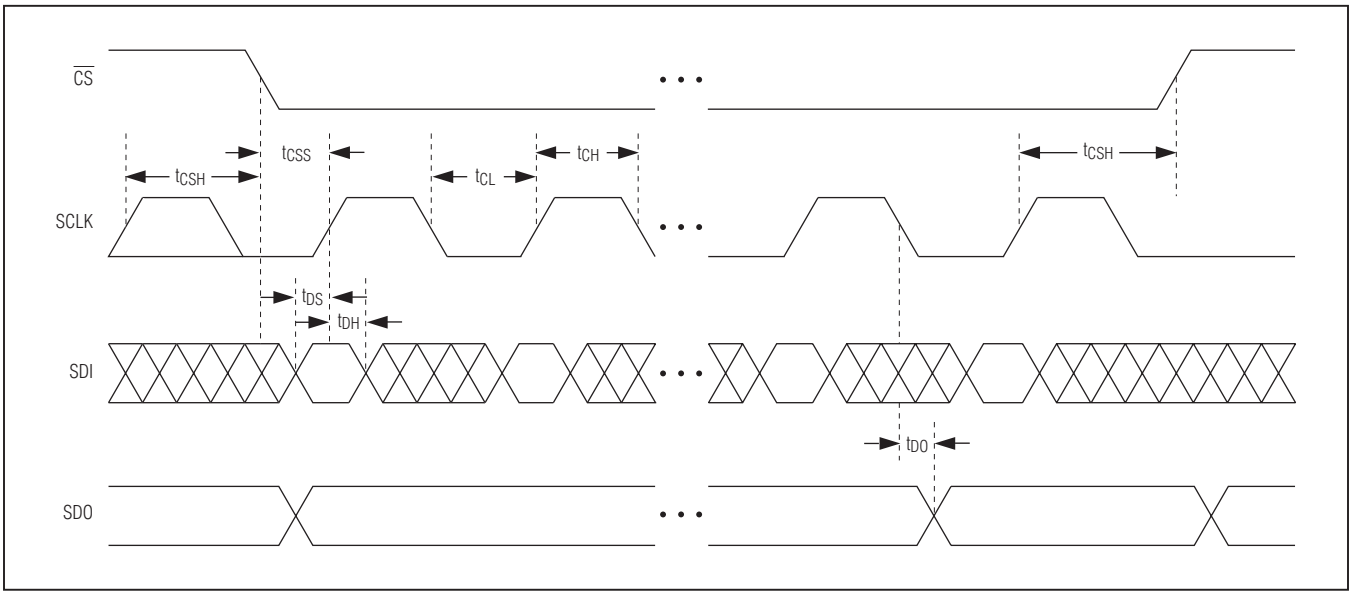
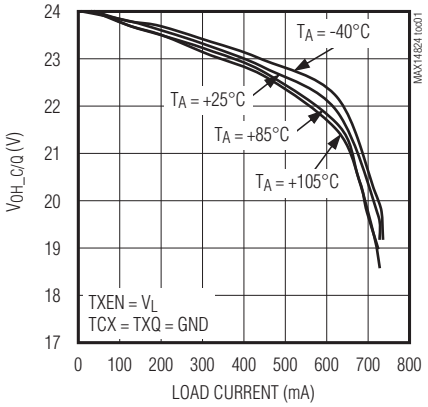


Figure 6. SPI Timing Diagram

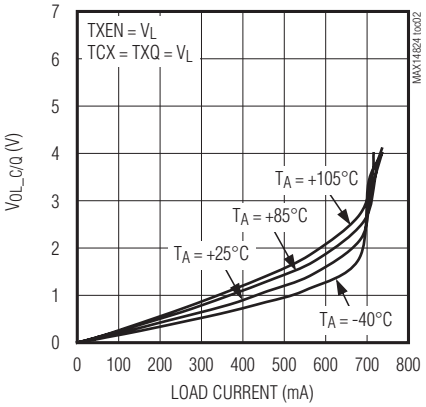
Typical Operating Characteristics

(V_{CC} = 24V, LDOIN = V_{CC}, V_L = LDO33, C/Q is in push-pull configuration, T_A = +25°C, unless otherwise noted.)

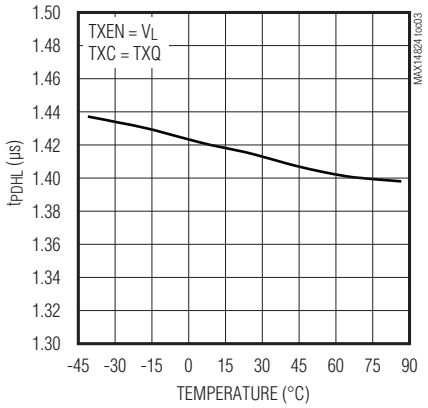
C/Q DRIVER OUTPUT HIGH vs. LOAD CURRENT



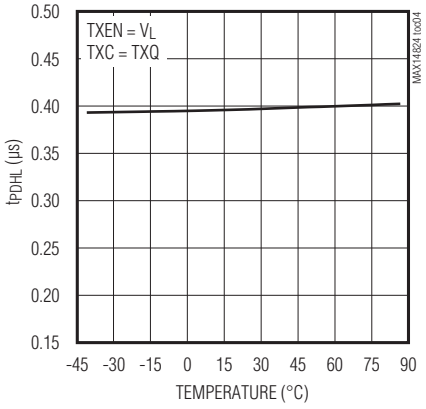
C/Q DRIVER OUTPUT LOW vs. LOAD CURRENT



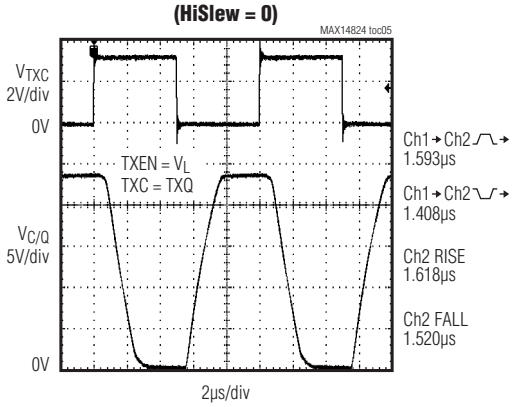
C/Q DRIVER PROPAGATION DELAY vs. TEMPERATURE (HiSlew = 0)



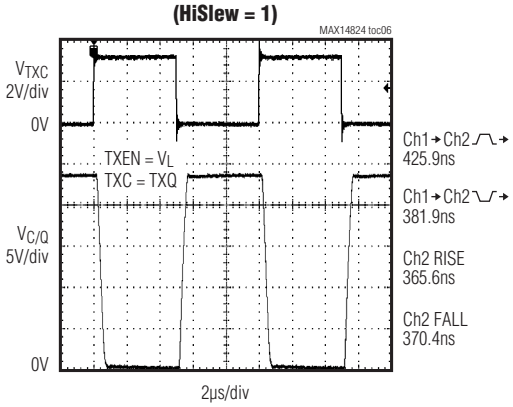
C/Q DRIVER PROPAGATION DELAY vs. TEMPERATURE (HiSlew = 1)



C/Q DRIVER OUTPUT SWITCHING (HiSlew = 0)



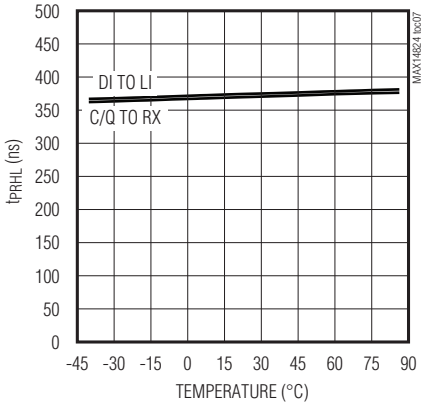
C/Q DRIVER OUTPUT SWITCHING (HiSlew = 1)



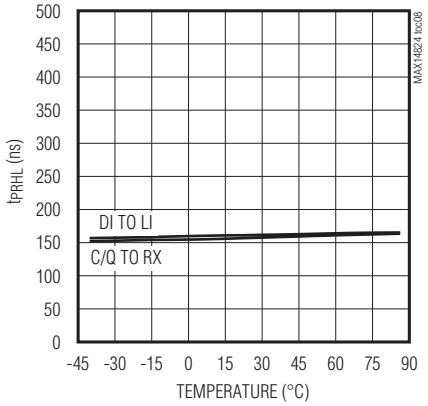
Typical Operating Characteristics (continued)

(V_{CC} = 24V, LDOIN = V_{CC}, V_L = LDO33, C/Q is in push-pull configuration, T_A = +25°C, unless otherwise noted.)

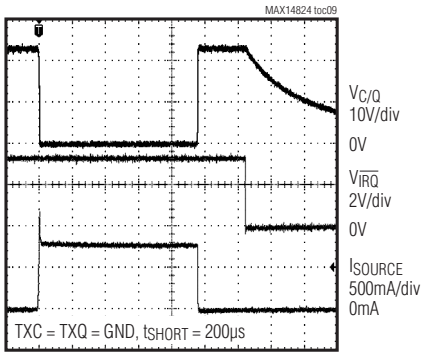
RECEIVER PROPAGATION DELAY vs. TEMPERATURE (RxFilter = 0)



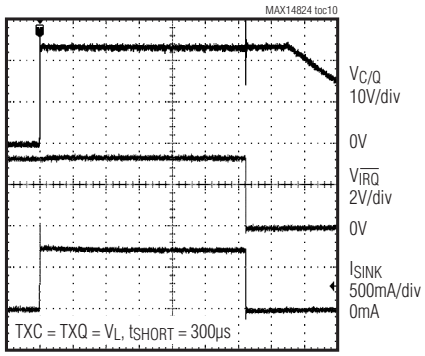
C/Q RECEIVER PROPAGATION DELAY vs. TEMPERATURE (RxFilter = 1)



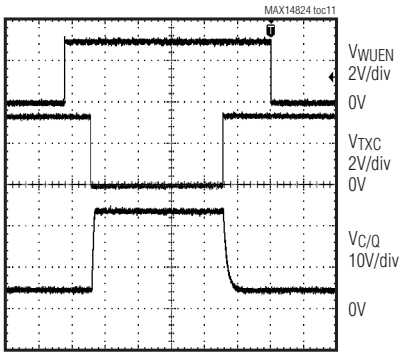
C/Q SHORT-CIRCUIT PROTECTION



C/Q SHORT-CIRCUIT PROTECTION



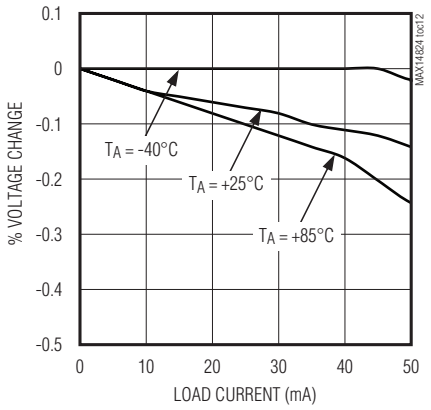
WAKE-UP GENERATION



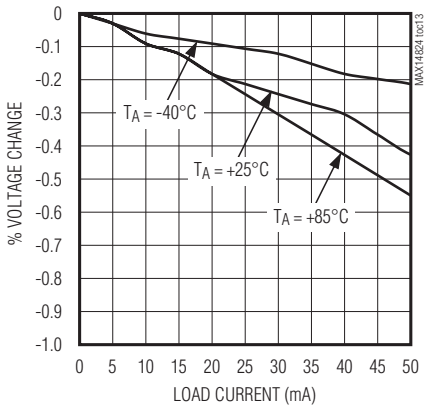
Typical Operating Characteristics (continued)

(V_{CC} = 24V, LDOIN = V_{CC}, V_L = LDO33, C/Q is in push-pull configuration, T_A = +25°C, unless otherwise noted.)

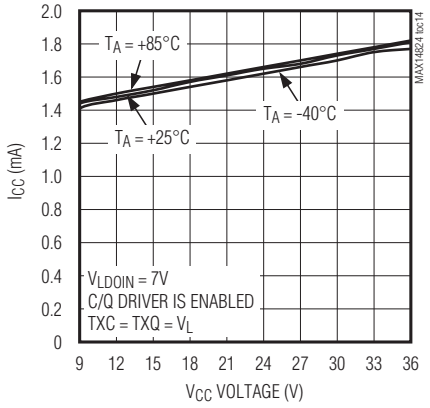
V_5 LOAD REGULATION



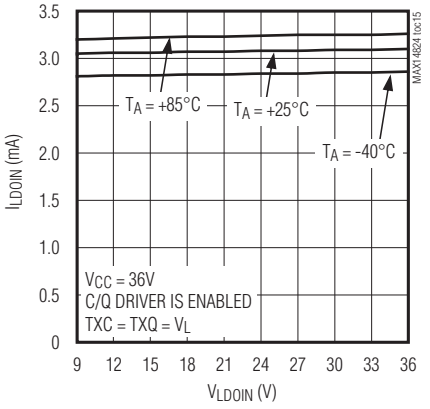
LDO33 LOAD REGULATION



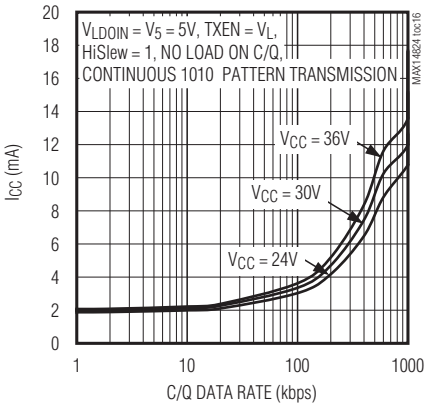
V_{CC} SUPPLY CURRENT vs. V_{CC} VOLTAGE



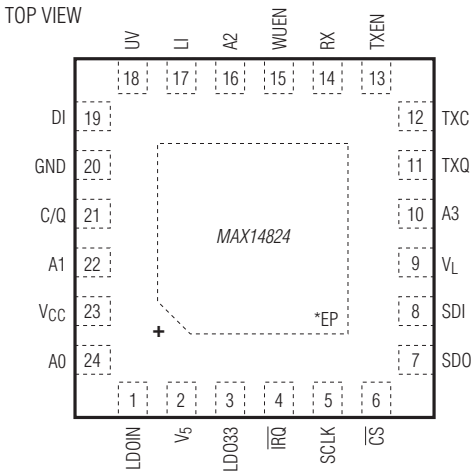
LDOIN SUPPLY CURRENT vs. LDOIN VOLTAGE



V_{CC} SUPPLY CURRENT vs. C/Q DATA RATE



Pin Configuration



TQFN
(4mm × 4mm)

*CONNECT EXPOSED PAD TO GND.

Pin Description

PIN	NAME	FUNCTION
1	LDOIN	5V Linear-Regulator Input. Bypass LDOIN to GND with a 0.1µF ceramic capacitor.
2	V_5	5V Power-Supply Input and 5V Linear-Regulator Output. Bypass V_5 to GND with a 0.1µF ceramic capacitor. See the *5V and 3.3V Linear Regulators* section for more information.
3	LDO33	3.3V Linear-Regulator Output. Bypass LDO33 to GND with a 1µF ceramic capacitor.
4	$\overline{IRQ}$	Active-Low Interrupt Request Output. $\overline{IRQ}$ is a push-pull output referenced to V_L.
5	SCLK	SPI Clock Input
6	$\overline{CS}$	SPI Chip-Select Input
7	SDO	SPI Serial-Data Output Port
8	SDI	SPI Serial-Data Input Port
9	V_L	Logic-Level Supply Input. V_L defines the logic levels on all the logic inputs and outputs. Bypass V_L to GND with a 0.1µF ceramic capacitor.
10	A3	Chip-Select Address Input 3. Do not leave A3 unconnected.
11	TXQ	Transmit Level Input. TXQ is ANDed with TXC. Drive TXQ high if not in use.
12	TXC	Transmit Communication Input. TXC is ANDed with TXQ. Drive TXC high if not in use.
13	TXEN	Transmitter Enable. Driving TXEN high enables the C/Q transmitter. While the C/Q transmitter is enabled, the C/Q current sink is turned off.

Pin Description (continued)

PIN	NAME	FUNCTION
14	RX	Receiver Output. RX is the inverse logic level of C/Q. RX is always high when the RxDis bit in the CQConfig register is set to 1.
15	WUEN	Wake-Up Enable Input. Drive WUEN high to enable automatic wake-up pulse generation.
16	A2	Chip-Select Address Input 2. Do not leave A2 unconnected.
17	LI	Logic Output of 24V DI Logic Input. LI is the inverse logic of DI. LI is referenced to V_L.
18	UV	Open-Drain Undervoltage Indicator Output. UV is active high.
19	DI	24V Logic-Level Digital Input
20	GND	Ground
21	C/Q	SIO/IO-Link Data Input/Output. Drive TXEN high to enable the C/Q driver. The logic on the C/Q output is the inverse logic level of the signals on the TXC and TXQ inputs. Drive TXEN low to disable the C/Q driver. RX is the logic inverse of C/Q.
22	A1	Chip-Select Address Input 1. Do not leave A1 unconnected.
23	V_{CC}	Power-Supply Input. Bypass V_{CC} to GND with a 1µF ceramic capacitor.
24	A0	Chip-Select Address Input 0. Do not leave A0 unconnected.
—	EP	Exposed Pad. Connect EP to GND.

Detailed Description

The MAX14824 is an IO-Link® master transceiver that integrates an IO-Link physical interface with an additional 24V digital input and two LDOs. A 12MHz SPI™ interface allows fast programming and monitoring.

The device supports COM1, COM2, and COM3 IO-Link data rates and has the option of limiting emitted EMI by selecting a lower slew rate at lower data rates. The automatic wake-up circuitry determines the correct wake-up pulse polarity, allowing the use of simple UARTs for wake-up pulse generation.

The C/Q and DI inputs have selectable current sinks that can be enabled for use in actuators.

The device is configured and monitored through an SPI interface. Extensive alarms are available through SPI.

24V Interface

The device features an IO-Link transceiver interface capable of operating with voltages up to 36V. This includes the C/Q input/output and the logic-level digital input (DI).

IO-Link is a registered trademark of Procibus User Organization (PNO).

SPI is a trademark of Motorola Inc.

DI is reverse-polarity protected. Short-circuit protection is provided on the C/Q driver.

Configurable C/Q Driver

The device's C/Q driver has a selectable push-pull, high-side (PNP), or low-side (NPN) switching driver.

Set the C/Q_N/P and C/Q_PP bits in the CQConfig register to select the driver mode for the C/Q driver. When configured as a push-pull output, C/Q switches between V_{CC} and ground. Set the C/Q_PP bit to 1 to select push-pull operation. Set the C/Q_PP bit to 0 to configure the C/Q output for open-drain operation. The C/Q_N/P bit selects NPN or PNP operation when C/Q is configured as an open-drain output.

C/Q Driver and Receiver

The C/Q driver can be enabled through hardware (TXEN) or software (C/QDEn). Drive TXEN high to enable the C/Q driver and drive TXEN low to disable the driver. The C/Q driver can be enabled through the C/QDEn bit in the C/QConfig register.

The C/Q driver on the device is specified for 300mA to drive large capacitive loads over 1µF and dynamic impedances like incandescent lamps.

The HiSlew bit increases the slew rate of the C/Q driver output. Set HiSlew to 1 for data rates of 230kbps or higher. Set HiSlew to 0 to reduce the C/Q driver slew rate and reduce EMI emission and reflections.

The C/Q receiver is always on. Disable the RX output through the RxDis bit in the CQConfig register. Set the RxDis bit to 1 to set the RX output high. Set the RxDis bit to 0 for normal receive operation.

The C/Q receiver has an analog lowpass filter to reduce high-frequency noise present on the line. Set the RxFilter bit in the CQConfig register to 0 to set the filter corner frequency to 500kHz (typ). Set the RxFilter bit to 1 to set the corner frequency of the filter to 1MHz (typ). Noise filters are present on both the C/Q and DI receivers and are controlled simultaneously by the RxFilter bit.

C/Q Fault Detection

The device registers a C/QFault condition under either of two conditions:

1) When it detects a short circuit for longer than 160µs (typ). A short condition exists when the C/Q driver's load current exceeds the 670mA (typ) current limit.
2) When it detects a voltage level error at the C/Q output. A voltage level error occurs when the C/Q driver is configured for open-drain operation (NPN or PNP), the driver is turned off, and the C/Q voltage is not pulled to exceed the C/Q receiver's threshold levels (< 8V or > 13V) by the external supply.

When a C/QFault error occurs, the C/QFault and C/QFaultInt bits are set, $\overline{IRQ}$ asserts, and the driver is turned off 240µs (typ) after the start of the fault condition.

When a short-circuit event occurs on C/Q, the driver enters autoretry mode. In autoretry mode the device periodically checks if the short is still present and attempts to correct the driver output. Autoretry attempts last for 350µs (typ) and occur every 26ms (typ).

DI Auxillary Digital Input

DI is a digital input that is Type 1 and Type 3 compliant when the internal 3.5mA DI current load is enabled. If the IO-link master system does not require auxilliary digital inputs, DI can be connected to C/Q as shown in the *Typical Operating Circuits*. This reduces the power dissipation when C/Q is operated as a digital input, by enabling the DI current load instead of the C/Q current load. Di is tolerant to reverse polarity voltages down to -40V when not connected to C/Q.

5V and 3.3V Internal Regulators

The device includes two internal current-limited regulators to generate 5V (V_5) and 3.3V (LDO33). V_5 is specified at 10mA. LDO33 is specified at 10mA. The input of V_5, LDOIN, can be connected to V_{CC} or to another voltage in the 7V to 36V range.

V_5 consitutes the supply for the logic block in the device. The device can be powered by an external 5V power supply. Disable the 5V LDO by connecting LDOIN to V_5. Apply an external voltage from 4.75V to 5.25V to V_5 when the LDO is disabled.

Use the LDO33Dis bit in the Mode register to enable/disable LDO33. See the *Mode Register [R1, R0] = [1,1]* section for more information. V_5 and LDO33 are not protected against short circuits.

Power-Up

The C/Q driver output and the UV output are high impedance when V_{CC}, V_5, V_L, and/or LDO33 voltages are below their respective undervoltage thresholds during power-up. UV goes low and the C/Q driver is enabled when all these voltages exceed their respective undervoltage lockout thresholds.

The C/Q driver is automatically disabled if V_{CC}, V_5, or V_L falls below its threshold.

Undervoltage Detection

The device monitors V_{CC}, V_5, V_L, and, optionally, LDO33 for undervoltage conditions. UV is high impedance when any monitored voltage falls below its UVLO threshold.

V_{CC}, V_5, and V_L undervoltage detection cannot be disabled. When V_{CC} falls below the V_{CCUVLO} threshold, the UV24 and UV24Int bits are set, UV asserts high, and $\overline{IRQ}$ asserts low.

The SPI register contents are unchanged while V_5 is present, regardless of the state of V_{CC} or LDO33. The SPI interface is not accessible and $\overline{IRQ}$ is not available when UV is asserted due to a V_5 or V_L undervoltage event.

When the internal 3.3V LDO regulator voltage (V_{LDO33}) falls below the LDO33 undervoltage lockout threshold, the UV33Int bit in the Status register is set and $\overline{IRQ}$ asserts. UV asserts if the UV33En bit in the Mode register is set to 1.

The UV output deasserts once the undervoltage condition is removed; however, the associated interrupts bits in the Status register and the $\overline{IRQ}$ output are not cleared until the Status register has been read.

Wake-Up Generation

The MAX14824 features automatic wake-up polarity generation functionality that can be initiated through hardware or software. The following conditions must be met prior to automatic wake-up polarity generation to ensure proper functionality:

- WUEN is low
- TXEN is low and C/QDEn = 0
- Q = 0
- TXC and TXQ are both high

Drive WUEN high to enable the automatic wake-up polarity generation circuitry in the device. When WUEN is high, apply an external pulse to TXC or TXQ from high-to-low for 80µs (typ) to generate a valid wake-up pulse. The applied pulse is independent of the logic state that the IO-Link sensor was forcing on the C/Q level (Figure 5). Drive WuEN low after the wake-up has been generated.

The C/Q driver is automatically enabled while TXC/TXQ is low and C/Q is pulled either from high-to-low or from low-to-high, depending on the previous state. The C/Q driver is automatically disabled when the TXC/TXQ inputs are pulled high again.

Wake-up polarity generation can also be enabled through software by setting the WuEnBit bit in the Mode register to 1. See the *Mode Register [R1, R0] = [1,1]* section for more information.

Thermal Protection and Considerations

The internal LDOs and C/Q driver can generate more power than the package for the device can safely dissipate. Ensure that the driver LDO loading is less than the package can dissipate. Total power dissipation for the device is calculated using the following equation:

$$P_{TOTAL} = P_{C/Q} + P_5 + P_{LDO33} + P_Q + P_{CLCQ} + P_{CLDI}$$

where $P_{C/Q}$ is the power generated in the C/Q driver, P_5 and P_{LDO33} are the power generated by the LDOs, P_Q is the quiescent power generated by the device, and P_{CLCQ} and P_{CLDI} are the power generated in the C/Q and DI current sinks.

Ensure that the total power dissipation is less than the limits listed in the *Absolute Maximum Ratings* section.

Use the following to calculate the power dissipation (in mW) due to the C/Q driver:

$$P_{C/Q} = [I_{C/Q}]^2 \times [R_O]$$

Calculate the power dissipation in the 5V LDO, V_5, using the following equation:

$$P_5 = (V_{LDOIN} - V_5) \times I_5$$

where I_5 includes the I_{LDO33} current sourced from LDO33.

Calculate the power dissipated in the 3.3V LDO, LDO33, using the following equation:

$$P_{LDO33} = 1.7V \times I_{LDO33}$$

Calculate the quiescent power dissipation in the device using the following equation:

$$P_Q = I_{CC} \times V_{CC}$$

If the current sinks are enabled, calculate their associated power dissipation as:

$$P_{CLCQ} = I_{LLM\_C/Q} \times V_{C/Q}$$

$$P_{CLDI} = I_{LLM\_DI} \times V_{DI}$$

Overtemperature Warning

Two bits in the Status and Mode registers are set when the temperature of the device exceeds +115°C (typ). The OTempInt bit in the Status register is set and $\overline{IRQ}$ asserts when the OTemp bit in the Mode register is set. Read the Status register to clear the OTempInt bit and $\overline{IRQ}$.

The OTemp bit is cleared when the die temperature falls below +95°C.

The device continues to operate normally unless the die temperature reaches the +150°C thermal shutdown threshold, when the device enters thermal shutdown.

Thermal Shutdown

When the die temperature rises above +150°C (typ) thermal shutdown threshold, the C/Q drivers and the C/Q and DI current loads are automatically turned off. The internal 3.3V and 5V LDOs remain on during thermal shutdown, if enabled. If the internal or external V5 supply remains on during thermal shutdown (which is always true in case of the internal V5 regulator), the register contents are maintained and SPI communication available.

When the die temperature falls below the thermal shutdown threshold plus hysteresis, the C/Q driver and C/Q and DI current sinks turn on automatically.

Register Functionality

The device has four 8-bit-wide registers for configuration and monitoring (Table 1). R1 and R0 are the register address.

Table 1. Register Summary

REGISTER	R1	R0	D7	D6	D5	D4	D3	D2	D1	D0
Status	0	0	X	X	DiLvl	$\overline{Q}$Lvl	C/QFaultInt	UV33Int	UV24Int	OTempInt
CQConfig	0	1	RxFilter	HiSlew	C/Q_N/P	C/Q_PP	C/QDEn	Q	RxDis	C/QLoad
DIOConfig	1	0	X	X	X	X	X	X	LiDis	DiLoad
Mode	1	1	RST	WuEnBit	X	C/QFault	UV24	OTemp	UV33En	LDO33Dis

R1/R0 = Register address, X = Unused bits.

Status Register [R1, R0] = [0,0]

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	X	X	DiLvl	$\overline{Q}$Lvl	C/QFaultInt	UV33Int	UV24Int	OTempInt
Read/Write	R	R	R	R	R	R	R	R
POR State	0	0	U	U	0	0	0	0
Reset Upon Read	Yes	Yes	No	No	Yes	Yes	Yes	Yes

X = Unused bits.
U = Unknown. These bits are dependent on the DI logic and C/Q inputs.

The Status register reflects the logic levels of C/Q and DI and shows the source of interrupts that cause an $\overline{IRQ}$ hardware interrupt. The $\overline{IRQ}$ interrupt is asserted when an alarm condition (OTemp, UV33En, UV24, C/QFault) is detected. All bits in the Status register are read-only. The interrupt bits return to the default state after the Status register is read. If a C/Q fault condition persists, the C/QFaultInt bit is immediately set after the Status register is read.

BIT	NAME	DESCRIPTION
D7:D6	X	**Unused**
D5	DiLvl	**DI Logic Level.** The DiLvl bit mirrors the current logic level at the DI input. It is the inverse of the LI output and is always active regardless of the state of the LiDis bit (Table 2). DiLvl does not affect $\overline{IRQ}$. DiLvl is not changed when the Status register is read.
D4	$\overline{Q}$Lvl	**C/Q Logic Level.** The $\overline{Q}$Lvl bit is the inverse of the logic level at C/Q. $\overline{Q}$Lvl is 1 when the C/Q input level is low (< 8V) and is 0 when the C/Q logic level is high (> 13V) (Table 3). $\overline{Q}$Lvl remains active when the C/Q receiver is disabled (RxDis = 1). $\overline{Q}$Lvl does not affect $\overline{IRQ}$. $\overline{Q}$Lvl is not changed when the Status register is read.
D3	C/QFaultInt	**C/Q Fault Interrupt.** The C/QFaultInt interrupt bit and C/QFault bit (in the Mode register) are set when a short circuit or voltage fault occurs on the C/Q driver output (see the *C/Q Fault Detection* section for more information). $\overline{IRQ}$ asserts when C/QFault is 1. Read the Status register to clear the C/QFaultInt bit and deassert $\overline{IRQ}$.

BIT	NAME	DESCRIPTION
D2	UV33Int	**Internal 3.3V LDO (LDO33) Undervoltage Warning.** Both the UV33Int interrupt bit and the UV33En bit (in the Mode register) are set when V_{LDO33} falls below the 2.4V LDO33 undervoltage threshold. If UV33En is set in the Mode register, $\overline{IRQ}$ asserts low when the UV33Int bit is 1. Read the Status register to clear the UV33Int bit and deassert $\overline{IRQ}$. Set the UV33En bit to 1 in the Mode register to enable undervoltage monitoring for UV33Int. When enabled, UV asserts high when the UV33Int bit is 1. UV deasserts when V_{LDO33} rises above the LDO33 undervoltage threshold.
D1	UV24Int	**V_{CC} Undervoltage Interrupt.** The UV24Int interrupt bit and the UV24 bit (in the Mode register) are set when the V_{CC} voltage falls below the 7.4V undervoltage threshold. $\overline{IRQ}$ asserts low when the UV24Int bit is 1. Read the Status register to clear the UV24Int bit and deassert $\overline{IRQ}$. V_{CC} undervoltage detection cannot be disabled.
D0	OTempInt	**Overtemperature Warning.** The OTempInt interrupt bit and the OTemp bit (in the Mode register) are set when a high-temperature condition is detected by the device. OTemp is set when the temperature of the die exceeds +115°C (typ). OTempInt is set and $\overline{IRQ}$ asserts when the OTemp bit is 1. The OTempInt bit is cleared and $\overline{IRQ}$ deasserts when the Status register is read. Once cleared, OTempInt is not reset if the die temperature remains above the thermal warning threshold and does not fall below +95°C.

Table 2. DiLvl and LI Output

V_{DI} (V)	DiLvl BIT	LI OUTPUT
< 5.2	0	High
> 8	1	Low

Table 3. $\overline{Q}$Lvl and RX Output

$V_{C/Q}$ (V)	$\overline{Q}$Lvl BIT	RX OUTPUT
< 8	1	High
>13	0	Low

CQConfig Register [R1, R0] = [0,1]

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RxFilter	HiSlew	C/Q_N/P	C/Q_PP	C/QDEn	Q	RxDis	C/QLoad
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	0	0	0	0	0	0	0

Use the CQConfig register to control the C/Q receiver and driver parameters. All bits in the CQConfig register are read-write and are set to 0 at power-up.

BIT	NAME	DESCRIPTION
D7	RxFilter	**C/Q and DI Receiver Filter Control.** The C/Q and DI receivers have analog lowpass filters to reduce high-frequency noise on the receiver inputs. Set the RxFilter bit to 0 to set the filter corner frequency to 500kHz. Set the RxFilter bit to 1 to set the filter corner frequency to 1MHz (this setting is used for high-speed COM3 operation). Noise filters on C/Q and DI are controlled simultaneously by the RxFilter bit.
D6	HiSlew	**Slew-Rate Control.** The HiSlew bit increases the slew rate for the C/Q driver and is used for high-speed COM3 (230kbps) data rates. Set HiSlew to 0 for COM1 and COM2 operation.
D5	C/Q_N/P	**C/Q Driver NPN/PNP Mode.** The C/Q_N/P bit selects between low-side (NPN) and high-side (PNP) modes when the C/Q driver is configured as an open-drain output (C/Q_PP = 0). Set C/Q_N/P to 1 to configure the driver for low-side (NPN) operation. Set C/Q_N/P to 0 for high-side (PNP) operation.
D4	C/Q_PP	**C/Q Driver Push-Pull Operation.** Set C/Q_PP to 1 to enable push-pull operation on the C/Q driver. The C/Q output is open drain when C/Q_PP is 0.
D3	C/QDEn	**C/Q Driver Enable/Disable.** Set the C/QDEn bit to 1 to enable the C/Q driver. Set C/QDEn to 0 for hardware (TXEN) control. See Table 4.
D2	Q	**C/Q Driver Output Logic.** The Q bit can be used to program the C/Q output driver through software. The C/Q driver must be enabled and TXC = TXQ must be high to control the C/Q driver through the Q bit (Figure 8). C/Q has the same logic polarity as the Q bit. Set the Q bit to 0 to control the C/Q driver with TXC and TXQ. The C/Q driver output state depends on the C/Q_PP and C/Q_N/P bits as shown in Table 5. Note that Table 5 assumes that the C/Q driver is enabled (TXEN = V_L or C/QDEn = 1).
D1	RxDis	**C/Q Receiver Enable/Disable.** Set the RxDis bit to 1 to disable the C/Q receiver. The RX output is high when RxDis is 1.
D0	C/QLoad	**C/Q Current Sink Enable.** Set the C/QLoad bit to 1 to enable the internal current sink at C/Q. The C/Q current sink is automatically disabled while the C/Q driver is enabled (TXEN = high or C/QDEn = 1). This saves power.

Table 4. C/QDEn and TXEN C/Q Driver Control

C/QDEn	TXEN	C/Q DRIVER
0	Low	Disabled
X	High	Enabled
1	X	Enabled

X = Don't care.

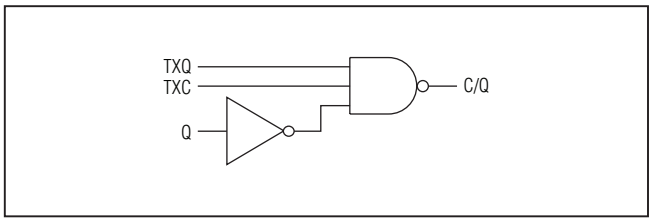


Figure 7. Equivalent C/Q Logic

Table 5. C/Q Driver Output State

TXC AND TXQ (SEE NOTE)	Q	C/Q_PP	C/Q_N/P	C/Q CONFIGURATION	C/Q STATE
High	1	0	0	PNP, open drain	On, C/Q is high
High	0	0	0	PNP, open drain	Off, C/Q is high impedance
High	1	0	1	NPN, open drain	Off, C/Q is high impedance
High	0	0	1	NPN, open drain	On, C/Q is low
High	1	1	X	Push-pull	High
High	0	1	X	Push-pull	Low

Note: *TXC and TXQ = V_L.*

X = Don't care.

DIOConfig Register [R1, R0] = [1,0]

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	X	X	X	X	X	X	LiDis	DiLoad
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	0	0	0	0	0	0	0

X = Unused bits.

Use the DIOConfig register to control the DI and DO interfaces. All bits in the DIOConfig register are read-write and are set to 0 at power-up.

BIT	NAME	DESCRIPTION
D7:D2	X	**Unused**
D1	LiDis	**LI Output Enable/Disable.** Set the LiDis bit to 1 to disable the LI output. The LI output is low when LiDis is 1.
D0	DiLoad	**DI Current Sink Enable.** Set the DiLoad bit to 1 to enable the internal current sink at the DI input.

Mode Register [R1, R0] = [1,1]

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RST	WuEnBit	X	C/QFault	UV24	OTemp	UV33En	LDO33Dis
Read/Write	R/W	R/W	R/W	R	R	R	R/W	R/W
POR State	0	0	0	0	0	0	0	0

X = Unused bits.

Use the Mode register to reset the device and manage the 3.3V LDO. The Mode register has bits that represent the current status of fault conditions. When writing to the Mode register, the contents of the fault indication bits (bits 2 to 4) do not change.

BIT	NAME	DESCRIPTION
D7	RST	**Register Reset.** Set RST to 1 to reset all registers to their default power-up state. Then set RST to 0 for normal operation. The Status register is cleared and $\overline{IRQ}$ deasserts (if asserted) when RST = 1. Interrupts are not generated while RST = 1.
D6	WuEnBit	**Auto Wake-Up Polarity Enable.** Drive the WUEN input high or set the WuEnBit bit to 1 to enable wake-up generation. When auto wake-up polarity is enabled, the device samples the logic state of C/Q and uses this as the basis for determining the subsequent wake-up pulse that is initiated through a high-to-low pulse on the TXQ and TXC inputs. Set the WuEnBit to 1 before a negative-going, 80µs (typ) wake-up pulse is transmitted to ensure that the device produces the correct polarity wake-up pulse on the C/Q output. For example, if C/Q is connected to a voltage high, then it pulls the line low for the wake-up pulse duration. If C/Q is connected to a voltage low, then it pulls the line high for the wake-up pulse duration. Clear WuEnBit after the wake-up has been generated (Table 6).
D5	X	**Unused**
D4	C/QFault	**C/Q Fault Status.** The C/QFault bit is set when a short circuit or voltage fault occurs at the C/Q driver output (see the *C/Q Fault Detection* section for more information). The C/QFault and C/QFaultInt bits are both set when a fault occurs on C/Q. C/QFault is cleared when the fault is removed.
D3	UV24	**V_{CC} Undervoltage Condition.** Both the UV24 and the UV24Int bits are set when V_{CC} falls below V_{CCUVLO}. UV24 is cleared when V_{CC} rises above the V_{CC} threshold. V_5 must be present for V_{CC} undervoltage monitoring.
D2	OTemp	**Temperature Warning.** The OTemp bit is set when a high-temperature condition occurs on the device. Both the OTempInt interrupt in the Status register and the OTemp bit are set when the junction temperature of the die rises to above +115°C (typ). The OTemp bit is cleared when the junction temperature falls below +95°C (typ).
D1	UV33En	**LDO33 UV Enable.** Set the UV33En bit to 1 to assert the UV output when LDO33 voltage falls below the 2.4V (typ) undervoltage lockout threshold. The UV33En bit does not affect the UV33Int bit in the Status register; $\overline{IRQ}$ asserts when V_{LDO33} falls below $V_{LDO33UVLO}$ regardless of the state of UV33En.
D0	LDO33Dis	**LDO33 Enable/Disable.** Set LDO33Dis to 1 to disable the 3.3V linear regulator (LDO33).

Table 6. Auto Wake-Up Polarity Generation

WuEnBit	WUEN	MODE
0	Low	Normal operation
0	High	Wake-up generation mode
1	Low	Wake-up generation mode
1	High	Wake-up generation mode

SPI Interface

The device communicates through an SPI-compatible 4-wire serial interface. The interface has three inputs—clock (SCLK), chip select (CS), and data in (SDI)—and one output, data out (SDO). The maximum SPI clock rate for the device is 12MHz. The SPI interface complies with clock polarity CPOL = 0 and clock phase CPHA = 0 (see Figure 8 and Figure 9).

The SPI interface is not available when V_5 or V_L is not present.

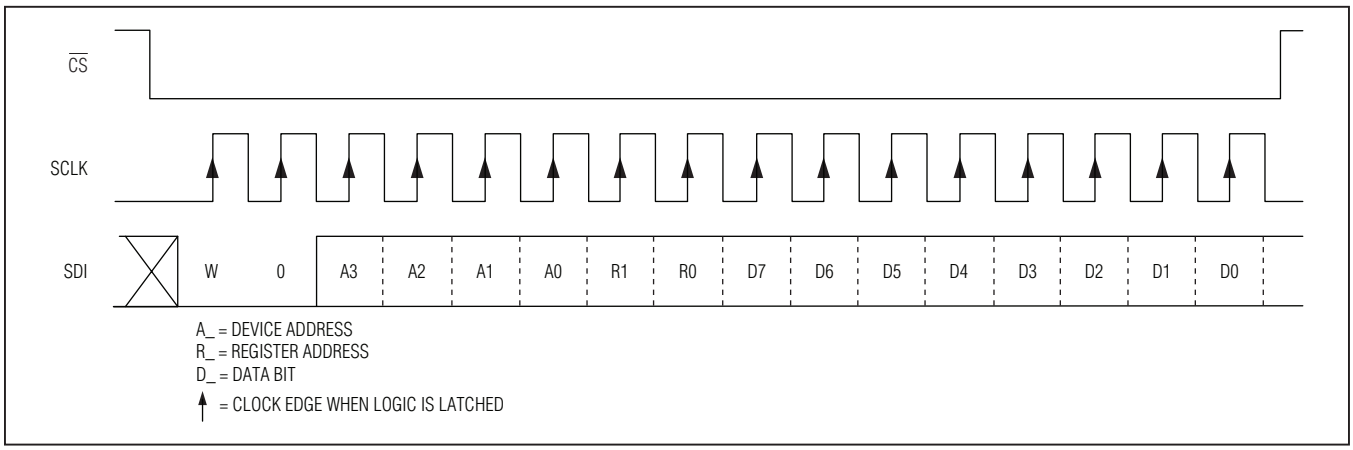


Figure 8. SPI Write Cycle

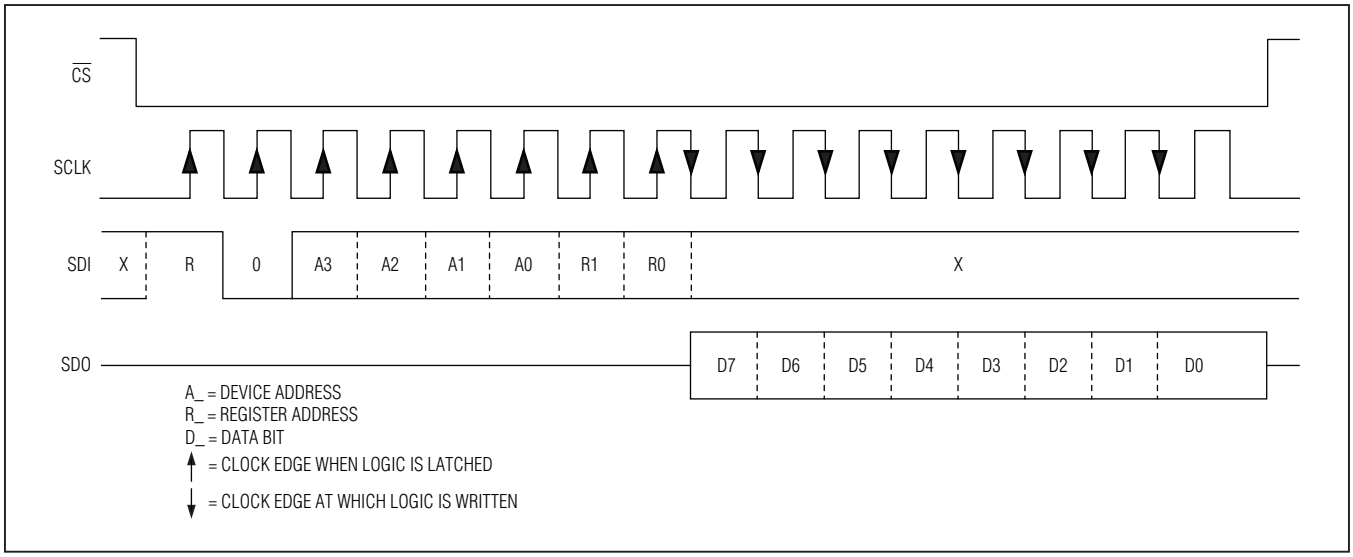


Figure 9. SPI Read Cycle

Address Selection

The device includes four chip-select address inputs, A0–A3, allowing up to 16 devices on a single bus. Drive the address inputs high or low to program the device address as shown in Table 7. Do not leave any address input unconnected.

Table 7. Address Input Selection

A3	A2	A1	A0	DEVICE ADDRESS
Low	Low	Low	Low	0x00
Low	Low	Low	High	0x01
Low	Low	High	Low	0x02
Low	Low	High	High	0x03
Low	High	Low	Low	0x04
Low	High	Low	High	0x05
Low	High	High	Low	0x06
Low	High	High	High	0x07
High	Low	Low	Low	0x08
High	Low	Low	High	0x09
High	Low	High	Low	0x0A
High	Low	High	High	0x0B
High	High	Low	Low	0x0C
High	High	Low	High	0x0D
High	High	High	Low	0x0E
High	High	High	High	0x0F

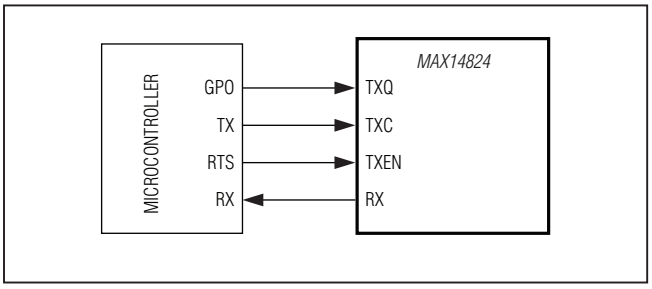


Figure 10. UART Interface

Applications Information

UART Interfacing

The logic level of the MAX14824 microcontroller's UART interface I/Os (TXC, TXQ, TXEN, and RX) is defined by V_L.

The device can be interfaced to microcontrollers whose on-board UART TX output cannot be programmed as a logic output (GPO). In this case, connect the TX output of the UART to the TXC input for IO-Link communication and connect a separate GPO output on the microcontroller to TXQ for standard IO (SIO) mode operation (Figure 10). As the TXQ and TXC inputs are internally logically ANDed, the unused input (TXC or TXQ) must be held high while the other is in operation.

Transient Protection

Inductive load switching, surges, ESD and short circuits create high transient voltages. C/Q and DI must be protected against high overvoltage and undervoltage transients. Positive voltage transients on DI must be limited to +55V relative to GND and negative voltage transients must be limited to -55V (relative to GND) on DI. Two Schottky diodes having low forward voltage, like the DLFS240, must be connected to C/Q to clamp under- and overvoltage transients. Figure 11 shows suitable protection to meet IEC 61000-4-2 ESD testing. For reduction of bit errors induced by burst transients, enable the receiver filters and add capacitors to C/Q and DI. If surge tests need to be met, a TVS diode is recommended on V_{CC}.

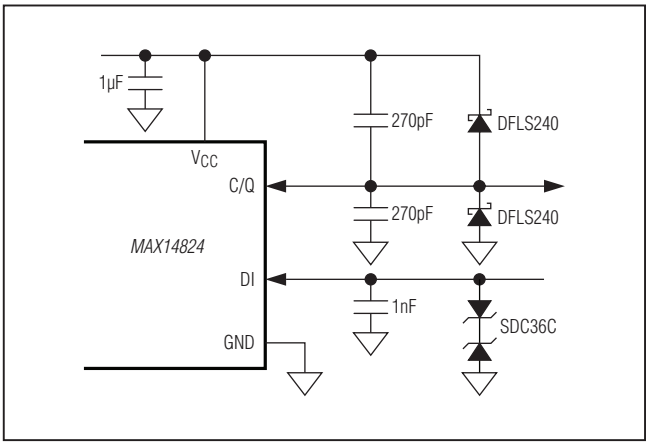


Figure 11. MAX14824 Operating Circuit with TVS Protection

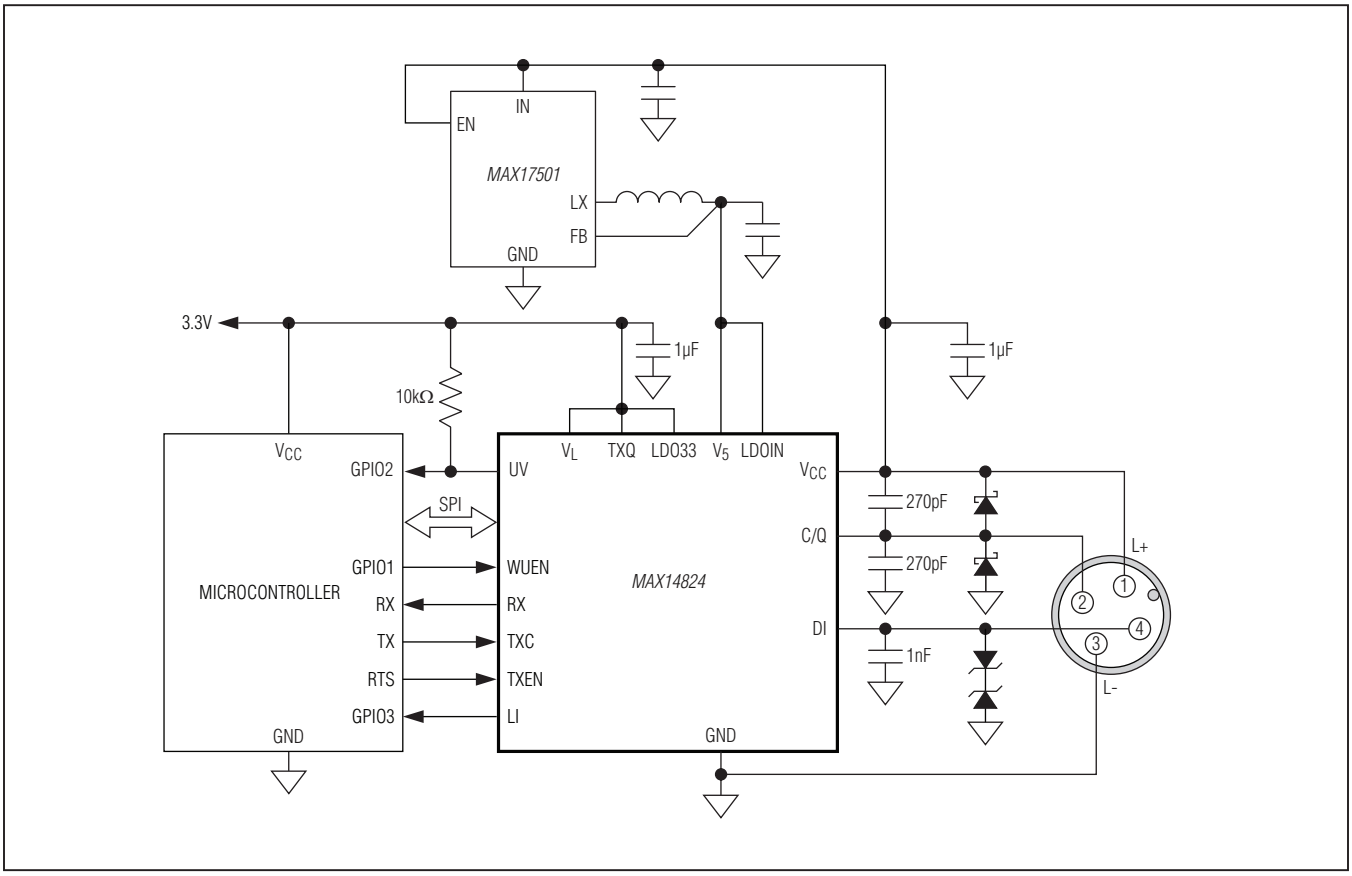


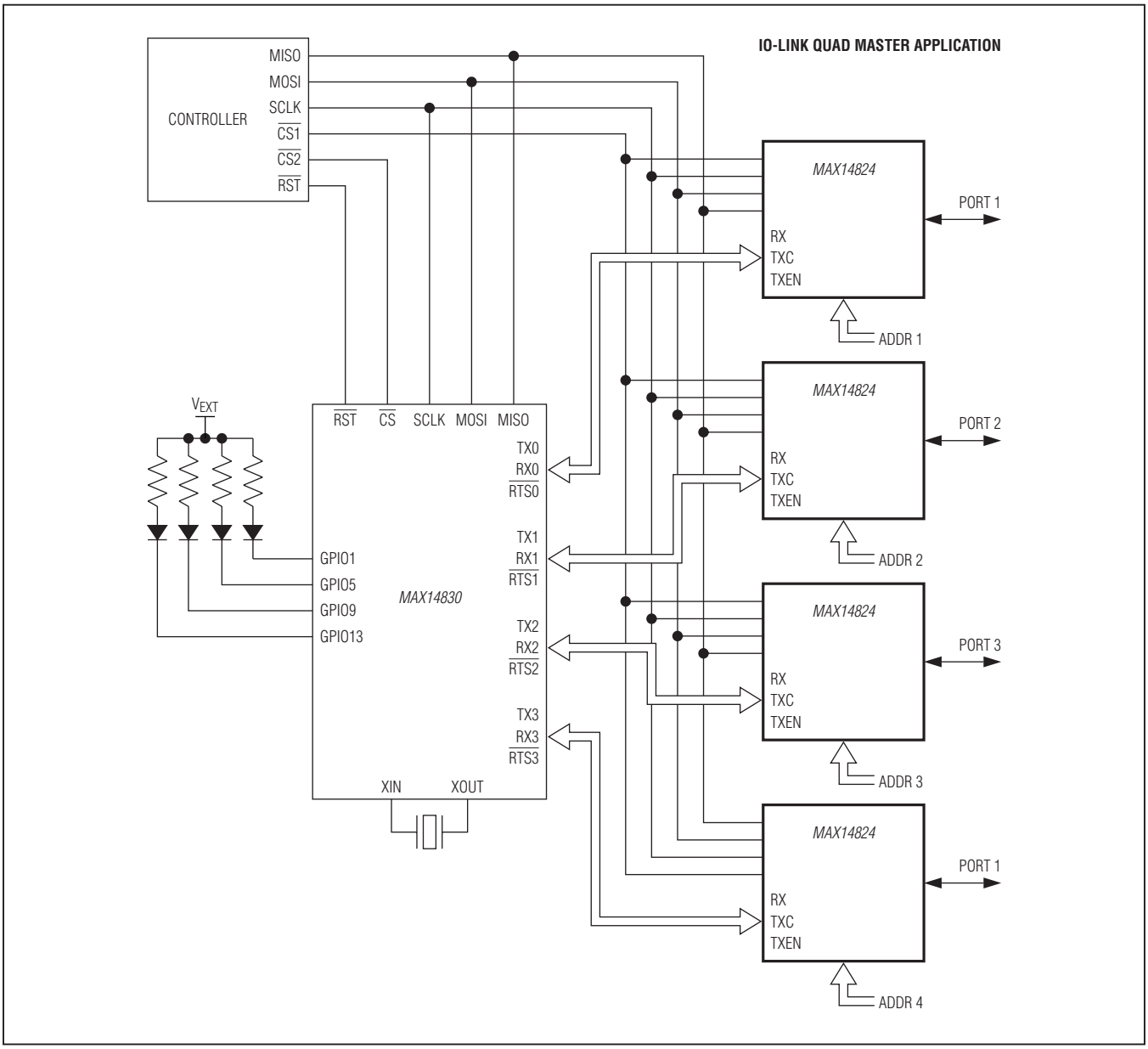
Figure 12. Use an External Supply to Power the MAX14824

External Power

The device is powered by V_{CC} and the 5V regulator, V_5. V_L is a reference voltage input to set the logic levels of the microcontroller interface. The logic and SPI interface are operational when V_5 and V_L are present even if V_{CC} is not present.

Connect LDOIN to V_5 to power the V_5 input with an external supply (Figure 12). This configuration disables operation of the internal 5V regulator and reduces power consumption.

Typical Operating Circuits (continued)



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14824GTG+	-40°C to +105°C	24 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 TQFN-EP	T2444+4	21-0139	90-0022

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/11	Initial release	—
1	6/11	Changed DI threshold to accommodate all three types of industrial sensors, added 24V supply connection in Figure 13	4, 19, 25
2	8/11	Corrected IO-Link trademark. Corrected block description in *Functional Diagram*. Corrected C/Q minimum and maximum ratings in the *Absolute Maximum Ratings* section. Corrected ICC maximum value and shuffled row parameters in the *Electrical Characteristics* Table. Replaced Figures 9 and 10. Added Maxim part number for DC-DC regulator. Corrected *Transient Protection* section.	1, 2, 3, 23, 24
3	5/12	Changed temperature rating; updated *Typical Operating Circuits*, *Functional Diagram*, and Figures 9, 11, and 12; updated TOCs 1, 2, and 16; changed parameters in *Electrical Characteristics*; updated *Detailed Description* and *Application Information*	1-7, 11, 13-17, 20, 23, 24, 24, 25, 27

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9