



PMPB48EPA

30 V, P-channel Trench MOSFET

27 March 2018

Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a leadless medium power DFN2020MD-6 (SOT1220) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Trench MOSFET technology
- Side wettable flanks for optical solder inspection
- Small and leadless ultra thin SMD plastic package: 2 x 2 x 0.65 mm
- AEC-Q101 qualified

3. Applications

- Relay driver
- High-speed line driver
- High-side load switch
- Switching circuits

4. Quick reference data

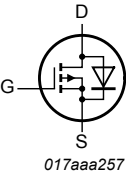
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$		-	-	-30	V
V_{GS}	gate-source voltage			-20	-	20	V
I_D	drain current	$V_{GS} = -10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-	-4.7	A
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = -10\text{ V}; I_D = -4.7\text{ A}; T_j = 25\text{ °C}$		-	40	50	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	 Transparent top view DFN2020MD-6 (SOT1220)	 017aaa257
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		
7	D	drain		
8	S	source		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMPB48EPA	DFN2020MD-6	DFN2020MD-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1220

7. Marking

Table 4. Marking codes

Type number	Marking code
PMPB48EPA	4Q

8. Limiting values

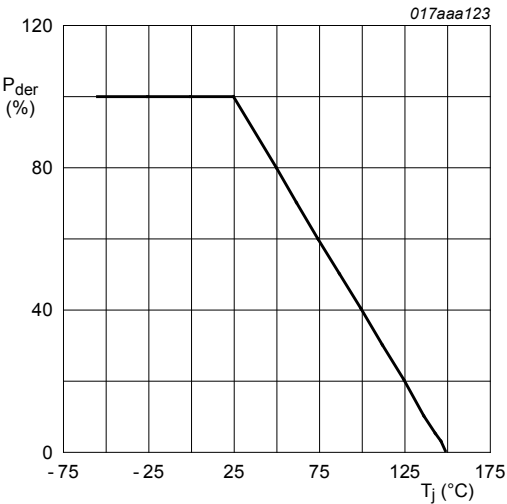
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$		-	-30	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	$V_{GS} = -10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-4.7	A
		$V_{GS} = -10\text{ V}; T_{amb} = 100\text{ °C}$	[1]	-	-3	A
I_{DM}	peak drain current	$T_{amb} = 25\text{ °C}$; single pulse; $t_p \leq 10\text{ }\mu\text{s}$		-	-19	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$	[1]	-	1.7	W
		$T_{sp} = 25\text{ °C}$		-	12.5	W
T_j	junction temperature			-55	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
Source-drain diode						
I_S	source current	$T_{amb} = 25\text{ °C}$	[1]	-	-1.8	A
ESD maximum rating						
V_{ESD}	electrostatic discharge voltage	HBM	[2]	-	500	V
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$T_{j(\text{init})} = 25\text{ °C}$; $I_D = -1.1\text{ A}$; DUT in avalanche (unclamped)		-	17.3	mJ

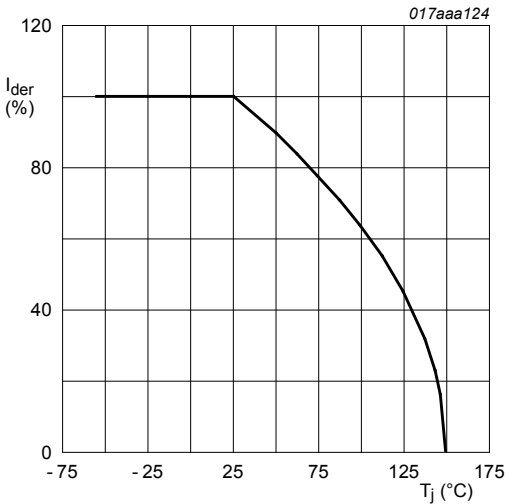
[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm^2 .

[2] Measured between all pins.



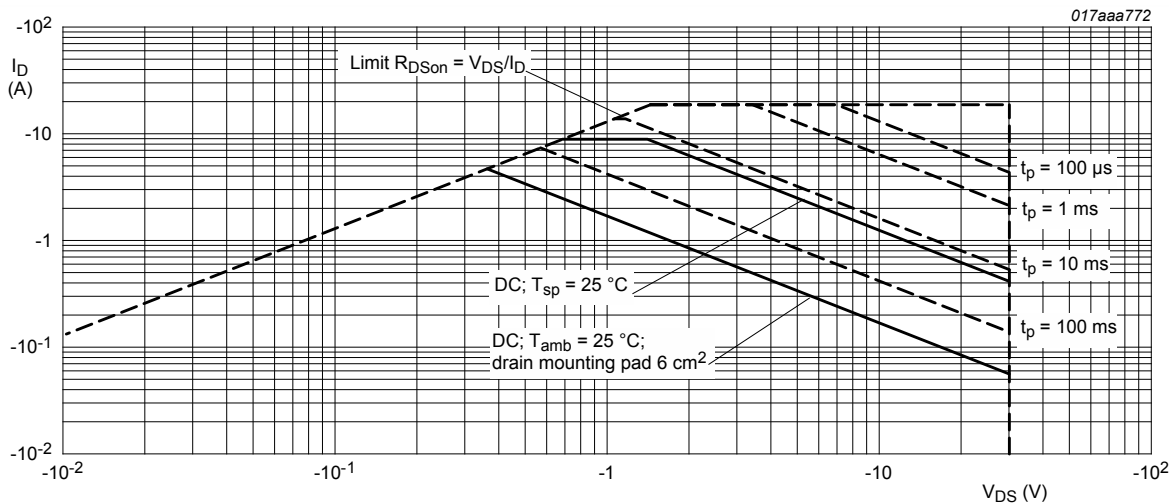
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

Fig. 1. Normalized total power dissipation as a function of junction temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100 \%$$

Fig. 2. Normalized continuous drain current as a function of junction temperature



I_{DM} = single pulse

Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	235	270	K/W
			[2]	-	67	74	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	5	10	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².

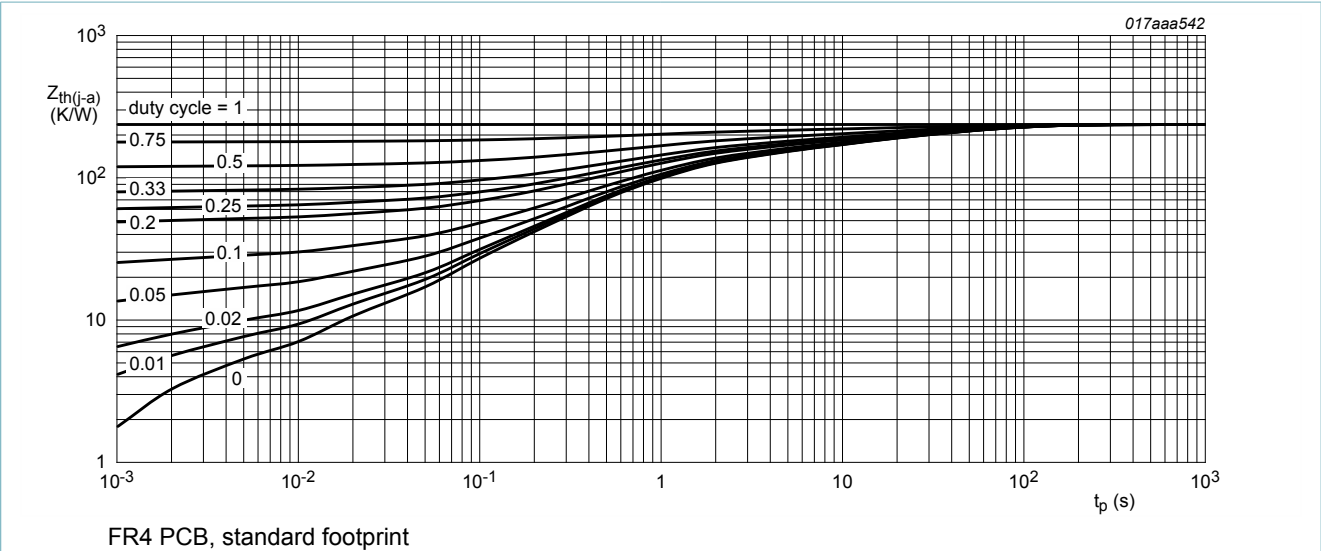


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

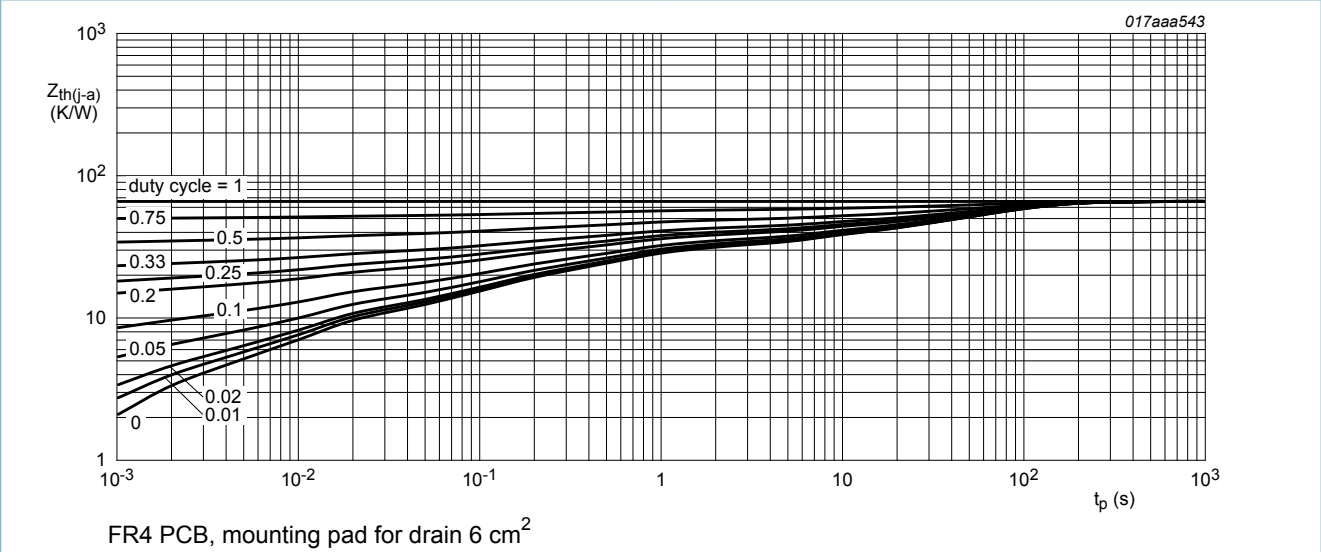


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = -250 μA; V _{GS} = 0 V; T _j = 25 °C		-30	-	-	V
V _{GSth}	gate-source threshold voltage	I _D = -250 μA; V _{DS} = V _{GS} ; T _j = 25 °C		-1	-1.5	-2.5	V
I _{DSS}	drain leakage current	V _{DS} = -30 V; V _{GS} = 0 V; T _j = 25 °C		-	-	-1	μA
I _{GSS}	gate leakage current	V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-100	nA
		V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = -10 V; I _D = -4.7 A; T _j = 25 °C		-	40	50	mΩ
		V _{GS} = -10 V; I _D = -4.7 A; T _j = 150 °C		-	60	75	mΩ
		V _{GS} = -4.5 V; I _D = -3.9 A; T _j = 25 °C		-	55	76	mΩ
g _{fs}	forward transconductance	V _{DS} = -10 V; I _D = -4.7 A; T _j = 25 °C		-	15	-	S
R _G	gate resistance	f = 1 MHz		-	6	-	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	V _{DS} = -15 V; I _D = -4.7 A; V _{GS} = -10 V; T _j = 25 °C		-	17	26	nC
Q _{GS}	gate-source charge			-	2.5	-	nC
Q _{GD}	gate-drain charge			-	3.2	-	nC
C _{iSS}	input capacitance	V _{DS} = -15 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C		-	860	-	pF
C _{oSS}	output capacitance			-	105	-	pF
C _{rSS}	reverse transfer capacitance			-	87	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = -15 V; I _D = -4.7 A; V _{GS} = -10 V; R _{G(ext)} = 6 Ω; T _j = 25 °C		-	7.4	-	ns
t _r	rise time			-	17.5	-	ns
t _{d(off)}	turn-off delay time			-	27	-	ns
t _f	fall time			-	10.4	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = -1.8 A; V _{GS} = 0 V; T _j = 25 °C		-	-0.8	-1.2	V
t _{rr}	reverse recovery time	I _S = -1.8 A; dI _S /dt = 100 A/μs; V _{GS} = 0 V; V _{DS} = -15 V; T _j = 25 °C		-	11	-	ns
Q _r	recovered charge			-	4	-	nC

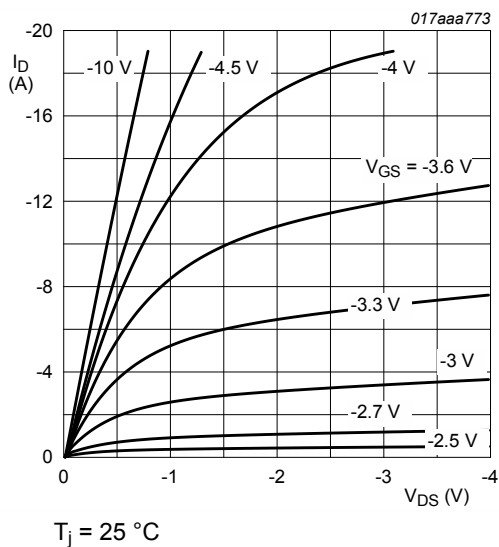


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

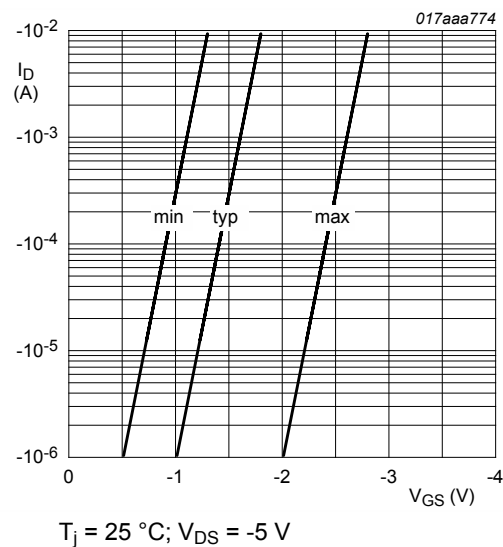


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

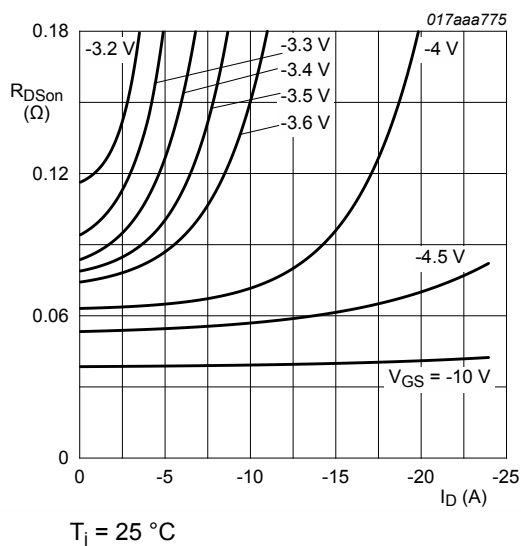


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

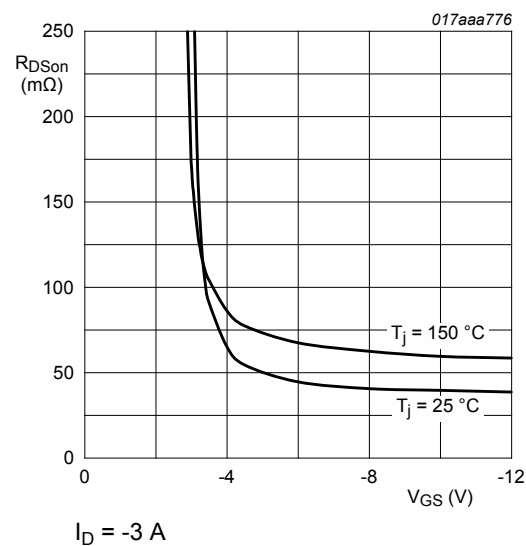


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

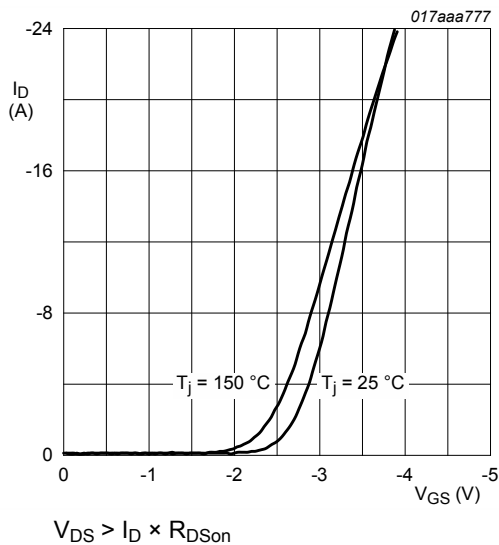


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

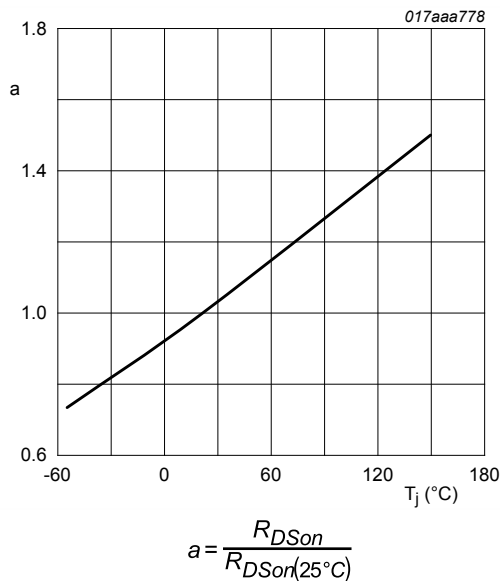


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

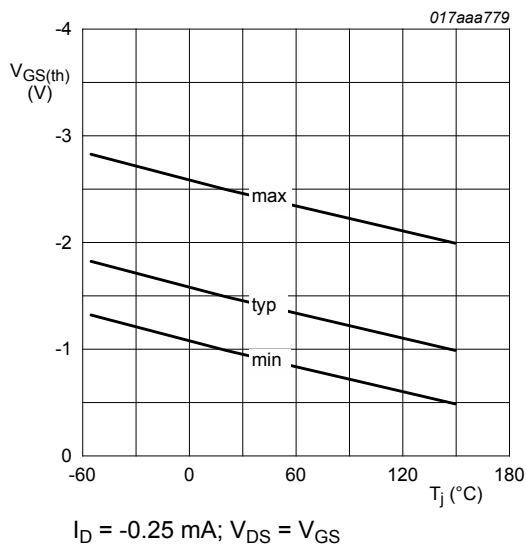


Fig. 12. Gate-source threshold voltage as a function of junction temperature

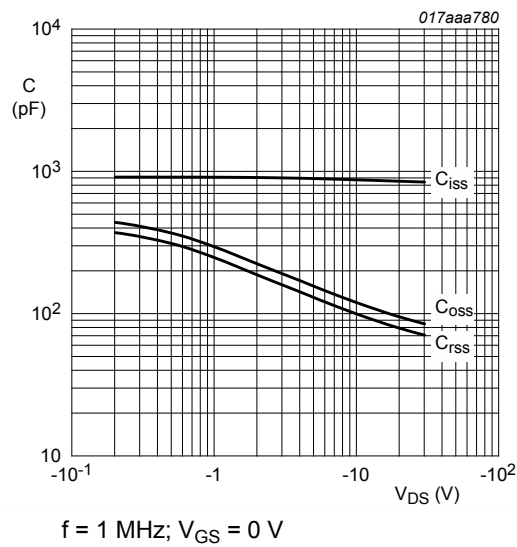


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

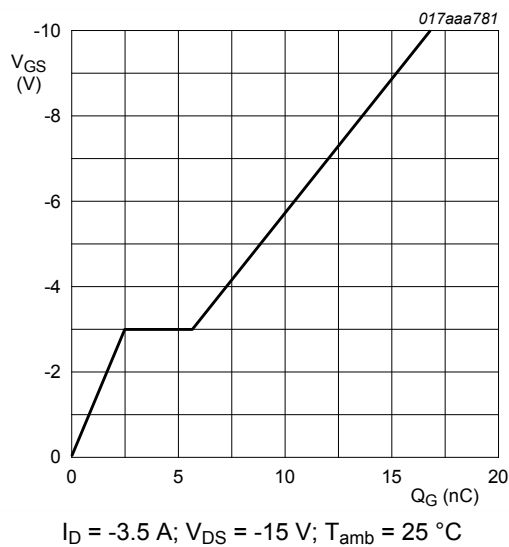


Fig. 14. Gate-source voltage as a function of gate charge; typical values

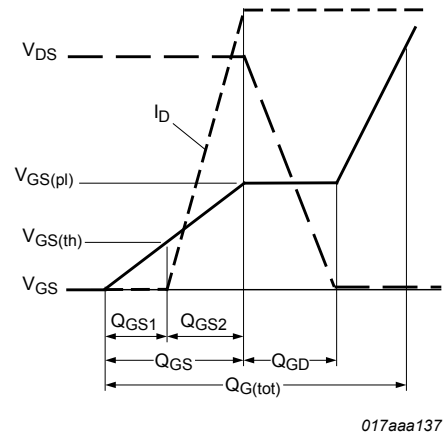


Fig. 15. Gate charge waveform definitions

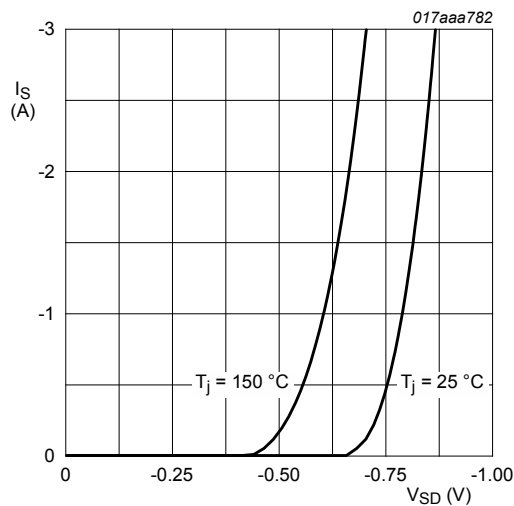


Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

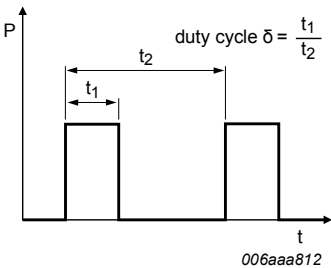


Fig. 17. Duty cycle definition

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

12. Package outline

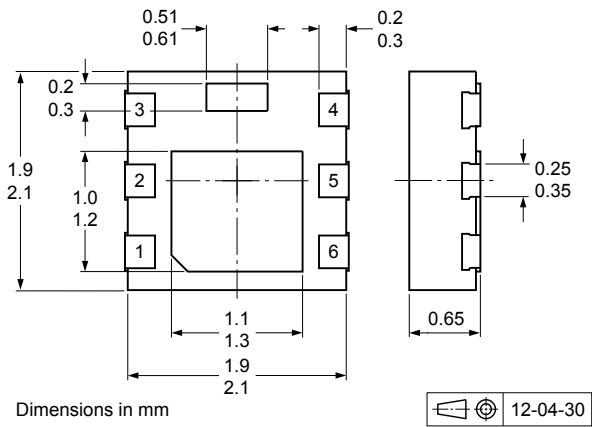


Fig. 18. Package outline DFN2020MD-6 (SOT1220)

13. Soldering

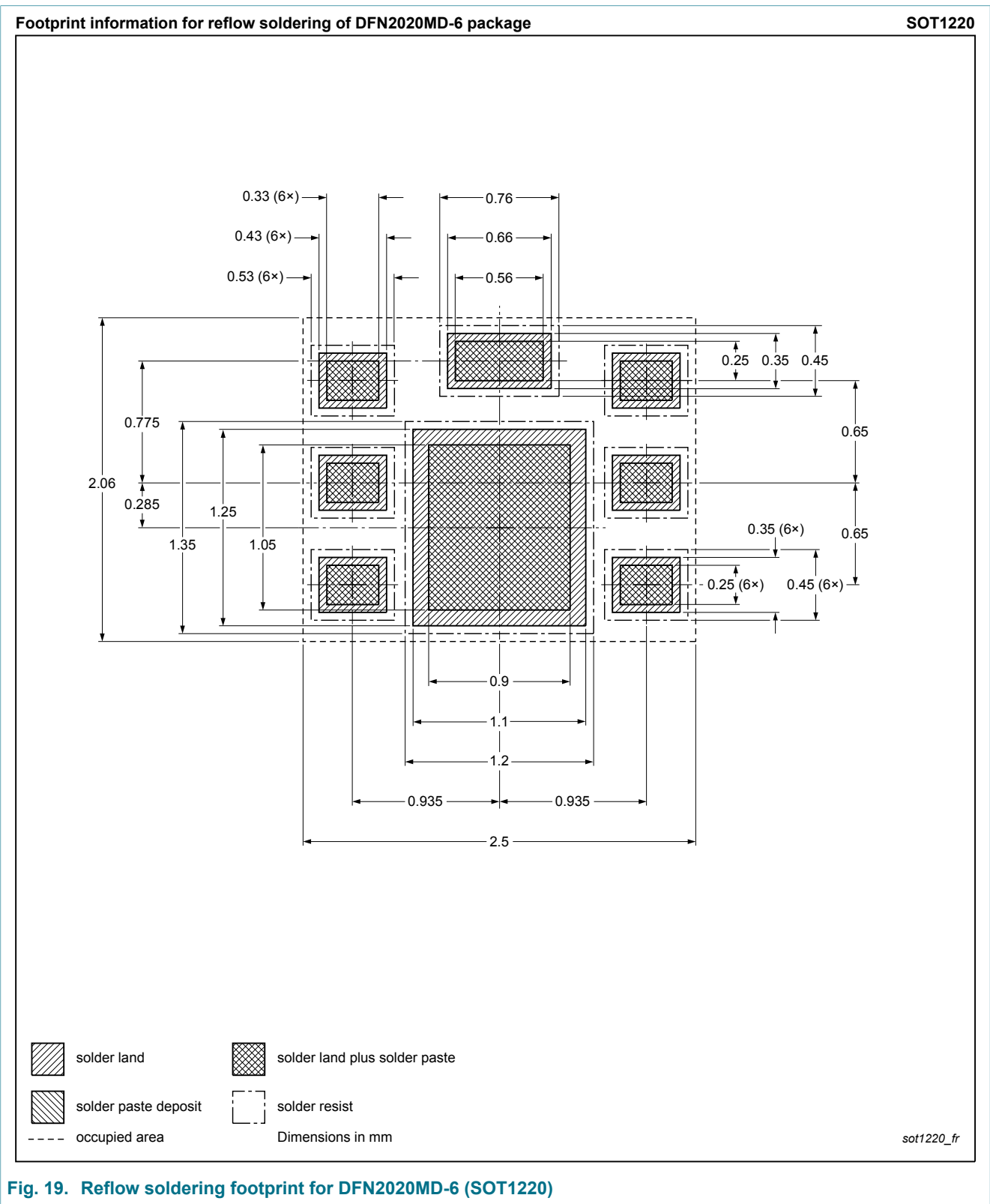


Fig. 19. Reflow soldering footprint for DFN2020MD-6 (SOT1220)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMPB48EPA v.1	20180327	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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Date of release: 27 March 2018

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