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May 2013

FDB86135

N-Channel Shielded Gate PowerTrench[®] MOSFET 100V, 176A, 3.5m Ω

Features

- · Shielded Gate MOSFET Technology
- Max $R_{DS(on)}$ = 3.5m Ω at V_{GS} = 10V, I_D = 75A
- · Fast Switching Speed
- · Low Gate Charge
- High Performance Trench Technology for Extremely Low $R_{\text{DS(on)}}$
- · High Power and Current Handling Capability
- · RoHS Compliant

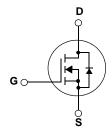
General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

Applications

- · DC-DC primary bridge
- · DC-DC Synchronous rectification
- · Hot swap





MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol		Parameter				Units
V_{DSS}	Drain to Source V	oltage			100	V
V_{GSS}	Gate to Source Vo	Gate to Source Voltage			±20	V
	Drain Curren	- Continuo	ous (Silicon Limited)	$T_{\rm C} = 25^{\rm o}{\rm C}$	176	
	- Continuous(Package Limited)			$T_{\rm C} = 25^{\rm o}{\rm C}$	120	Α
ID	- Continuous			$T_C = 25^{\circ}C(Note 1a)$	75	
	- Pulsed			704	Α	
E _{AS}	Single Pulsed Ava	lanche Energy		(Note 3)	658	mJ
П	Dawar Dissination		- T _C = 25°C	(Note 1a)	227	W
P_{D}	Power Dissipation - T _A = 25°C		(Note 1b)	2.4	W/°C	
T _J , T _{STG}	Operating and Sto	rage Temperat	ure Range		-55 to +175	°C

Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	0.66	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	62.5	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB86135	FDB86135	D2-PAK	330mm	24mm	800

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Units
Off Charac	teristics					
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A$, $V_{GS} = 0V$, $T_C = 25^{\circ}C$	100	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250μA, Referenced to 25°C	-	0.07	-	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 80V, V _{GS} = 0V	-	-	1	μА
I _{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	-	±100	nA

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	2.0	-	4.0	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10V, I _D = 75A	-	3.0	3.5	mΩ
9 _{FS}	Forward Transconductance	V _{DS} = 10V, I _D = 75A	-	167	-	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 05V V 0V	-	5485	7295	pF
C _{oss}	Output Capacitance	Output Capacitance $V_{DS} = 25V, V_{GS} = 0V$		2430	3230	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1101112	-	210	-	pF
Q _{g(tot)}	Total Gate Charge at 10V		-	89	116	nC
Q_{gs}	Gate to Source Gate Charge	V _{DS} = 80V, I _D = 75A	-	24	-	nC
Q _{gs2}	Gate Charge Threshold to Plateau	V _{GS} = 10V	-	8	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	25	-	nC

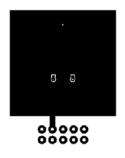
Switching Characteristics

t _{d(on)}	Turn-On Delay Time	V 50V 1 75A	-	22	54	ns
t _r	Turn-On Rise Time	$V_{DD} = 50V, I_D = 75A$	-	54	118	ns
t _{d(off)}	Turn-Off Delay Time	V_{GS} = 10V, R_{GEN} = 4.7 Ω	-	37	84	ns
t _f	Turn-Off Fall Time		-	11	32	ns

Drain-Source Diode Characteristics

V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0V, I_{SD} = 75A$ (Note 2)	-	-	1.25	V
t _{rr}	Reverse Recovery Time	$V_{GS} = 0V$, $I_{SD} = 75A$, $V_{DD} = 80V$	-	72	-	ns
Q _{rr}	Reverse Recovery Charge	$dI_F/dt = 100A/\mu s$	-	129	-	nC

1. R_{0,1A} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{0,1C} is guaranteed by design while R_{0,1C} is determined by the user's board design.



a) 40 °C/W when mounted on a 1 in² pad of 2 oz copper



b) 62.5 °C/W when mounted on a minimum pad of 2 oz copper

- 2. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0 %. 3. Starting T $_J$ = 25 °C, $\,L$ = 1 mH, I $_{AS}$ = 36.3 A, V $_{DD}$ = 100 V, V $_{GS}$ = 10 V.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

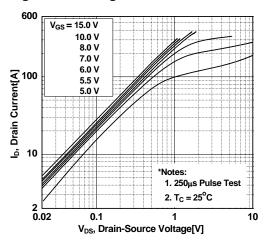


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

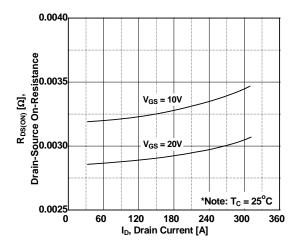


Figure 5. Capacitance Characteristics

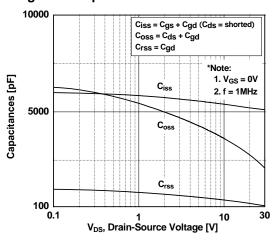


Figure 2. Transfer Characteristics

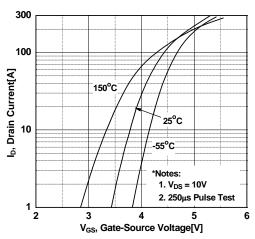


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

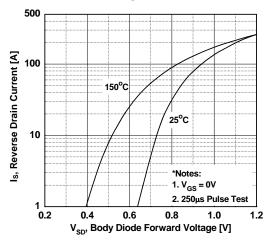
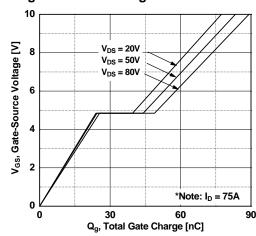


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics

Figure 7. Breakdown Voltage Variation vs. Temperature

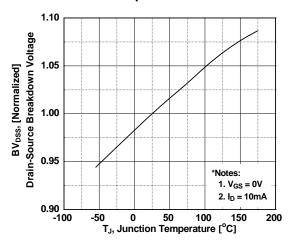


Figure 9. Maximum Safe Operating Area

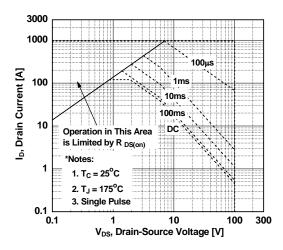


Figure 8. On-Resistance Variation vs. Temperature

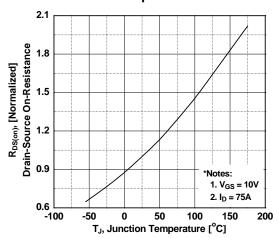


Figure 10. Maximum Drain Current vs. Case Temperature

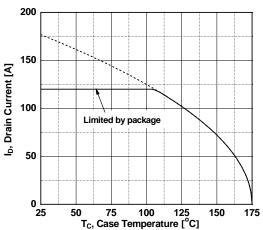
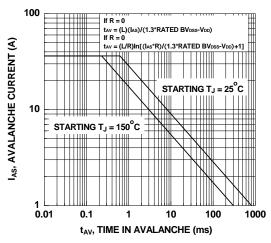
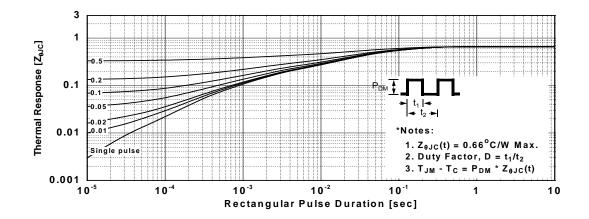


Figure 11. Unclamped Inductive Switching Capability

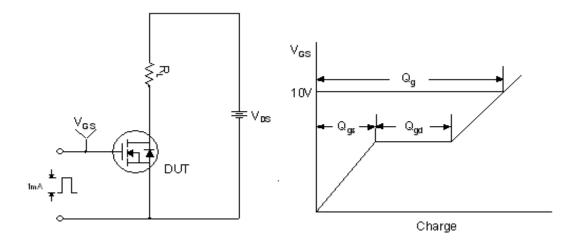


Typical Performance Characteristics

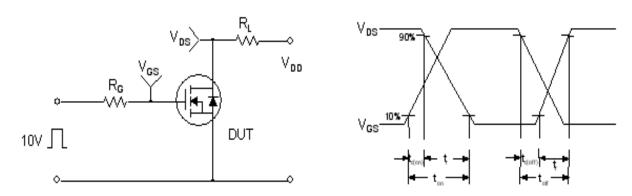
Figure 12. Transient Thermal Response Curve



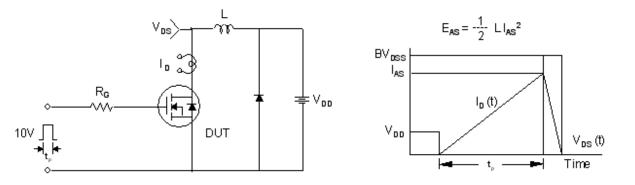
Gate Charge Test Circuit & Waveform



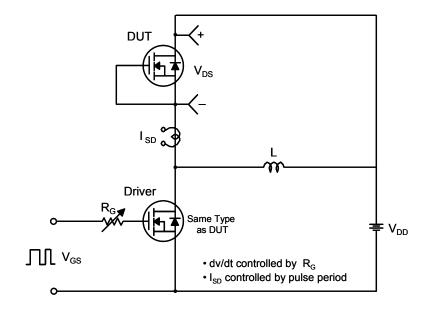
Resistive Switching Test Circuit & Waveforms

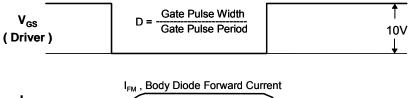


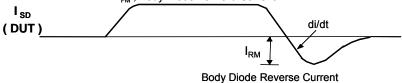
Unclamped Inductive Switching Test Circuit & Waveforms

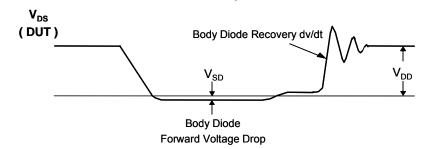


Peak Diode Recovery dv/dt Test Circuit & Waveforms



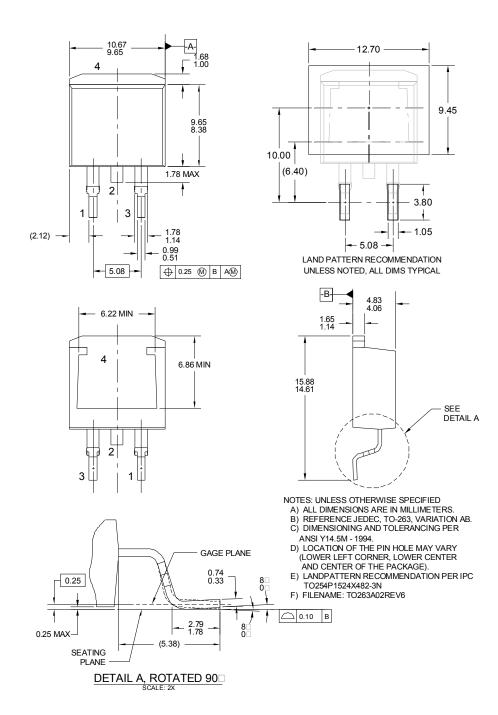






Mechanical Dimensions

D2-PAK



Dimensions in Millimeters





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