Nonvolatile Memory, Quad 64-Position Digital Potentiometer

AD5233

FEATURES

Nonvolatile memory stores wiper setting
4-channel independent programmable
64-position resolution
Power-on refreshed with EEMEM settings
EEMEM restore time: 140 µs typical
Full monotonic operation
10 kΩ, 50 kΩ, and 100 kΩ terminal resistance
Permanent memory write protection
Wiper setting readback
Predefined linear increment/decrement instructions
Predefined ±6 dB/step log taper increment/decrement instructions
SPI-compatible serial interface with readback function
2.7 V to 5.5 V single supply or ±2.5 V dual supply
11 bytes extra nonvolatile memory for user-defined data
100-year typical data retention, T_A = 55°C

APPLICATIONS

Mechanical potentiometer replacement
Instrumentation: gain, offset adjustment
Programmable voltage-to-current conversion
Programmable filters, delays, time constants
Programmable power supply
Sensor calibration

FUNCTIONAL BLOCK DIAGRAM

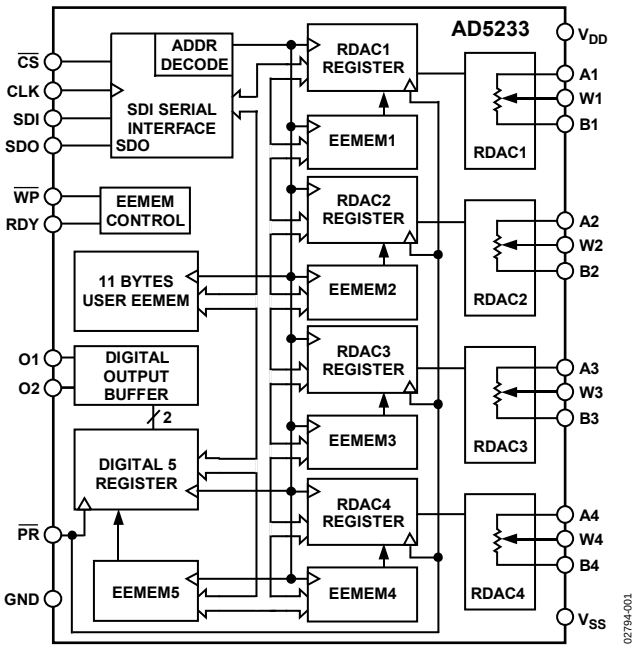

Figure 1.

GENERAL DESCRIPTION

The AD5233 is a quad-channel nonvolatile memory,[1] digitally controlled potentiometer[2] with a 64-step resolution. The device performs the same electronic adjustment function as a mechanical potentiometer with enhanced resolution, solid-state reliability, and remote controllability. The AD5233 has versatile programming using a serial peripheral interface (SPI) for 16 modes of operation and adjustment, including scratchpad programming, memory storing and restoring, increment/decrement, ±6 dB/step log taper adjustment, wiper setting readback, and extra EEMEM for user-defined information such as memory data for other components, look-up tables, or system identification information.

In the scratchpad programming mode, a specific setting can be programmed directly to the RDAC register, which sets the resistance between Terminal W to Terminal A and Terminal W to Terminal B. This setting can be stored into the EEMEM and is transferred automatically to the RDAC register during system power-on.

The EEMEM content can be restored dynamically or through external $\overline{PR}$ strobing. A $\overline{WP}$ function protects EEMEM contents. To simplify the programming, independent or simultaneous increment or decrement commands can be used to move the RDAC wiper up or down, one step at a time. For logarithmic ±6 dB step changes in wiper settings, the left or right bit shift command can be used to double or halve the RDAC wiper setting.

The AD5233 is available in a thin 24-lead TSSOP package. The part is guaranteed to operate over the extended industrial temperature range of −40°C to +85°C.

[1] The terms nonvolatile memory and EEMEM are used interchangeably.
[2] The terms digital potentiometer and RDAC are used interchangeably.

Rev. B

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3/02—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—10 kΩ, 50 kΩ, AND 100 kΩ VERSIONS

V_{DD} = 3 V ± 10% or 5 V ± 10%, V_{SS} = 0 V, $V_A = V_{DD}$, V_B = 0 V, −40°C < T_A < +85°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS, RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = NC, monotonic	−0.5	±0.1	+0.5	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = NC	−0.5	±0.1	+0.5	LSB
Nominal Resistor Tolerance	$\Delta R_{AB}/R_{AB}$	D = 0x3F	−40		+20	%
Resistance Temperature Coefficient	$(\Delta R_{WB}/R_{WB})/\Delta T \times 10^6$			600		ppm/°C
Wiper Resistance	R_W	I_W = 100 µA, code = half scale		15	100	Ω
DC CHARACTERISTICS, POTENTIOMETER DIVIDER MODE						
Resolution	N				6	Bits
Differential Nonlinearity[3]	DNL	Monotonic	−0.5	+0.1	+0.5	LSB
Integral Nonlinearity[3]	INL		−0.5	+0.1	+0.5	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = half scale		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = full scale	−1.5		0	% FS
Zero-Scale Error	V_{WZSE}	Code = zero scale	0		1.5	% FS
RESISTOR TERMINALS						
Terminal Voltage Range[4]	V_A, V_B, V_W		V_{SS}		V_{DD}	V
Capacitance A, Capacitance B[5]	C_A, C_B	f = 1 MHz, measured to GND, code = half scale		35		pF
Capacitance W[5]	C_W	f = 1 MHz, measured to GND, code = half scale		35		pF
Common-Mode Leakage Current[5, 6]	I_{CM}	$V_W = V_{DD}/2$		0.015	1	µA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	With respect to GND, V_{DD} = 5 V	2.4			V
		With respect to GND, V_{DD} = 3 V	2.1			V
		With respect to GND, V_{DD} = 2.5 V, V_{SS} = −2.5 V	2.0			V
Input Logic Low	V_{IL}	With respect to GND, V_{DD} = 5 V			0.8	V
		With respect to GND, V_{DD} = 3 V			0.6	V
		With respect to GND, V_{DD} = 2.5 V, V_{SS} = −2.5 V			0.5	V
Output Logic High (SDO, RDY)	V_{OH}	$R_{PULL-UP}$ = 2.2 kΩ to 5 V (see Figure 35)	4.9			V
Output Logic Low	V_{OL}	I_{OL} = 1.6 mA, V_{LOGIC} = 5 V (see Figure 35)			0.4	V
Input Current	I_{IL}	$V_{IN} = 0$ V or V_{DD}			±2.5	µA
Input Capacitance[5]	C_{IL}			4		pF
Output Current[5]	I_{O1}, I_{O2}	V_{DD} = 5 V, V_{SS} = 0 V, T_A = 25°C, sourcing only		50		mA
		V_{DD} = 2.5 V, V_{SS} = 0 V, T_A = 25°C, sourcing only		7		mA

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
POWER SUPPLIES						
Single-Supply Power Range	V_{DD}	V_{SS} = 0 V	2.7		5.5	V
Dual-Supply Power Range	V_{DD}/V_{SS}		±2.5		±2.75	V
Positive Supply Current	I_{DD}	$V_{IH} = V_{DD}$ or V_{IL} = GND		3.5	10	µA
Negative Supply Current	I_{SS}	$V_{IH} = V_{DD}$ or V_{IL} = GND, V_{DD} = 2.5 V, V_{SS} = −2.5 V		0.55	10	µA
EEMEM Store Mode Current	I_{DD} (store)	$V_{IH} = V_{DD}$ or V_{IL} = GND, V_{SS} = 0, $I_{SS} \approx 0$		40		mA
	I_{SS} (store)	V_{DD} = 2.5 V, V_{SS} = −2.5 V		−40		mA
EEMEM Restore Mode Current[7]	I_{DD} (restore)	$V_{IH} = V_{DD}$ or V_{IL} = GND, V_{SS} = GND, $I_{SS} \approx 0$	0.3	3	9	mA
	I_{SS} (restore)	V_{DD} = 2.5 V, V_{SS} = −2.5 V	−0.3	−3	−9	mA
Power Dissipation[8]	P_{DISS}	$V_{IH} = V_{DD}$ or V_{IL} = GND		0.018	0.05	mW
Power Supply Sensitivity[5]	P_{SS}	ΔV_{DD} = 5 V ± 10%		0.002	0.01	%/%
DYNAMIC CHARACTERISTICS[5, 9]						
Bandwidth	BW	−3 dB, R_{AB} = 10 kΩ/50 kΩ/100 kΩ		630/135/66		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz, R_{AB} = 10 kΩ		0.04		%
		V_A = 1 V rms, V_B = 0 V, f = 1 kHz, R_{AB} = 50 kΩ, 100 kΩ		0.015		%
V_W Settling Time	t_S	$V_A = V_{DD}$, V_B = 0 V, V_W = 0.50% error band, Code 0x000 to Code 0x200 for R_{AB} = 10 kΩ/50 kΩ/100 kΩ		0.6/2.2/3.8		µs
Resistor Noise Voltage	e_{N_WB}	R_{WB} = 5 kΩ, f = 1 kHz		9		nV/√Hz
Crosstalk (C_{W1}/C_{W2})	C_T	$V_A = V_{DD}$, V_B = 0 V, measure V_W with adjacent RDAC making the full-scale code change		−1		nV/sec
Analog Crosstalk (C_{W1}/C_{W2})	C_{TA}	$V_{DD} = V_{A1}$ = +2.5 V, $V_{SS} = V_{B1}$ = −2.5 V, measure V_{W1} with V_{W2} = 5 V p-p @ f = 10 kHz, Code 1 = 0x20, Code 2 = 0x3F, R_{AB} = 10 kΩ/ 50 kΩ/100 kΩ		−86/−73/−68		dB

[1] Typicals represent average readings at 25°C and V_{DD} = 5 V.
[2] Resistor position nonlinearity error (R-INL) is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. I_W > 50 µA @ V_{DD} = 2.7 V for the R_{AB} = 10 kΩ version, I_W > 50 µA for the R_{AB} = 50 kΩ, and I_W > 25 µA for the R_{AB} = 100 kΩ version (see Figure 25).
[3] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output ADC. $V_A = V_{DD}$ and $V_B = V_{SS}$. DNL specification limits of −1 LSB minimum are guaranteed monotonic operating conditions (see Figure 26).
[4] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other. Dual-supply operation enables ground-referenced bipolar signal adjustment.
[5] Guaranteed by design and not subject to production test.
[6] Common-mode leakage current is a measure of the dc leakage from Terminal B and Terminal W to a common-mode bias level of $V_{DD}/2$.
[7] EEMEM restore mode current is not continuous. Current is consumed while EEMEM locations are read and transferred to the RDAC register (see Figure 22). To minimize power dissipation, a NOP instruction should be issued immediately after Instruction 1 (0x1).
[8] Power dissipation is calculated by $P_{DISS} = (I_{DD} \times V_{DD}) + (I_{SS} \times V_{SS})$.
[9] All dynamic characteristics use V_{DD} = 2.5 V and V_{SS} = −2.5 V.

TIMING CHARACTERISTICS

V_{DD} = 3 V to 5.5 V, V_{SS} = 0 V, and −40°C < T_A < +85°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
INTERFACE TIMING CHARACTERISTICS[2, 3]						
Clock Cycle Time (t_{CYC})	t_1		20			ns
$\overline{CS}$ Setup Time	t_2		10			ns
CLK Shutdown Time to $\overline{CS}$ Rise	t_3		1			t_{CYC}
Input Clock Pulse Width	t_4, t_5	Clock level high or low	10			ns
Data Setup Time	t_6	From positive CLK transition	5			ns
Data Hold Time	t_7	From positive CLK transition	5			ns
$\overline{CS}$ to SDO-SPI Line Acquire	t_8				40	ns
$\overline{CS}$ to SDO-SPI Line Release	t_9				50	ns
CLK to SDO Propagation Delay[4]	t_{10}	$R_{PULL-UP}$ = 2.2 kΩ, C_L < 20 pF			50	ns
CLK to SDO Data Hold Time	t_{11}	R_P = 2.2 kΩ, C_L < 20 pF	0			ns
$\overline{CS}$ High Pulse Width[5]	t_{12}		10			ns
$\overline{CS}$ High to $\overline{CS}$ High[5]	t_{13}		4			t_{CYC}
RDY Rise to $\overline{CS}$ Fall	t_{14}		0			ns
$\overline{CS}$ Rise to RDY Fall Time	t_{15}			0.1	0.15	ms
Read/Store to Nonvolatile EEMEM[6]	t_{16}	Applies to Instruction 0x2, Instruction 0x3, and Instruction 0x9		25		ms
$\overline{CS}$ Rise to Clock Rise/Fall Setup	t_{17}		10			ns
Preset Pulse Width (Asynchronous)	t_{PRW}	Not shown in timing diagram	50			ns
Preset Response Time to Wiper Setting	t_{PRESP}	$\overline{PR}$ pulsed low to refresh wiper positions		70		µs
Power-On EEMEM Restore Time	t_{EEMEM1}	R_{AB} = 10 kΩ		140		µs
FLASH/EE MEMORY RELIABILITY						
Endurance[7]			100			kCycles
Data Retention[8]				100		Years

[1] Typicals represent average readings at 25°C and V_{DD} = 5 V.
[2] Guaranteed by design and not subject to production test.
[3] See the timing diagrams (Figure 2 and Figure 3) for the location of the measured values. All input control voltages are specified with $t_R = t_F$ = 2.5 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V. Switching characteristics are measured using both V_{DD} = 3 V and V_{DD} = 5 V.
[4] Propagation delay depends on the value of V_{DD}, $R_{PULL-UP}$, and C_L.
[5] Valid for commands that do not activate the RDY pin.
[6] The RDY pin is low only for Command 2, Command 3, Command 8, Command 9, Command 10, and the $\overline{PR}$ hardware pulse: CMD_8 > 1 ms; CMD_9, CMD_10 > 0.12 ms; CMD_2, CMD_3 > 20 ms. Device operation at T_A = −40°C and V_{DD} < 3 V extends the save time to 35 ms.
[7] Endurance is qualified to 100,000 cycles per JEDEC Standard 22, Method A117, and measured at −40°C, +25°C, and +85°C; typical endurance at 25°C is 700,000 cycles.
[8] Retention lifetime equivalent at junction temperature (T_J) = 55°C per JEDEC Standard 22, Method A117. Retention lifetime based on an activation energy of 0.6 eV derates with junction temperature, as shown in Figure 45 in the Flash/EEMEM Reliability section.

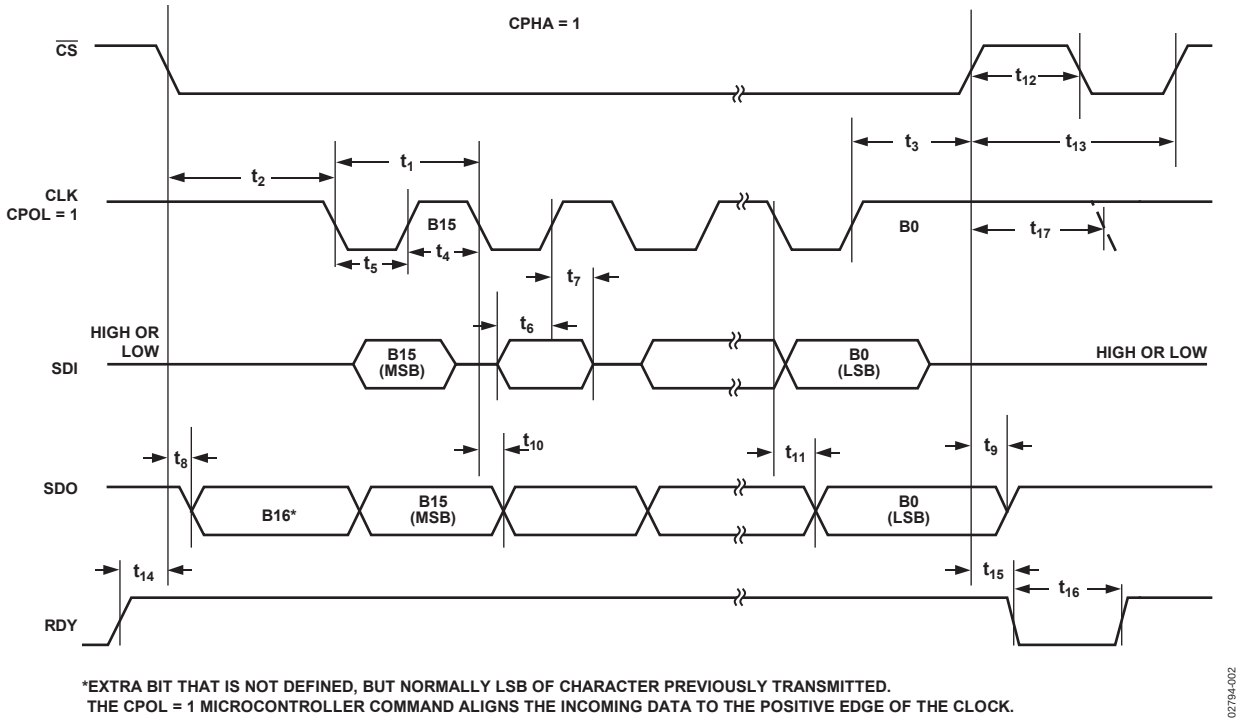

Figure 2. CPHA = 1 Timing Diagram

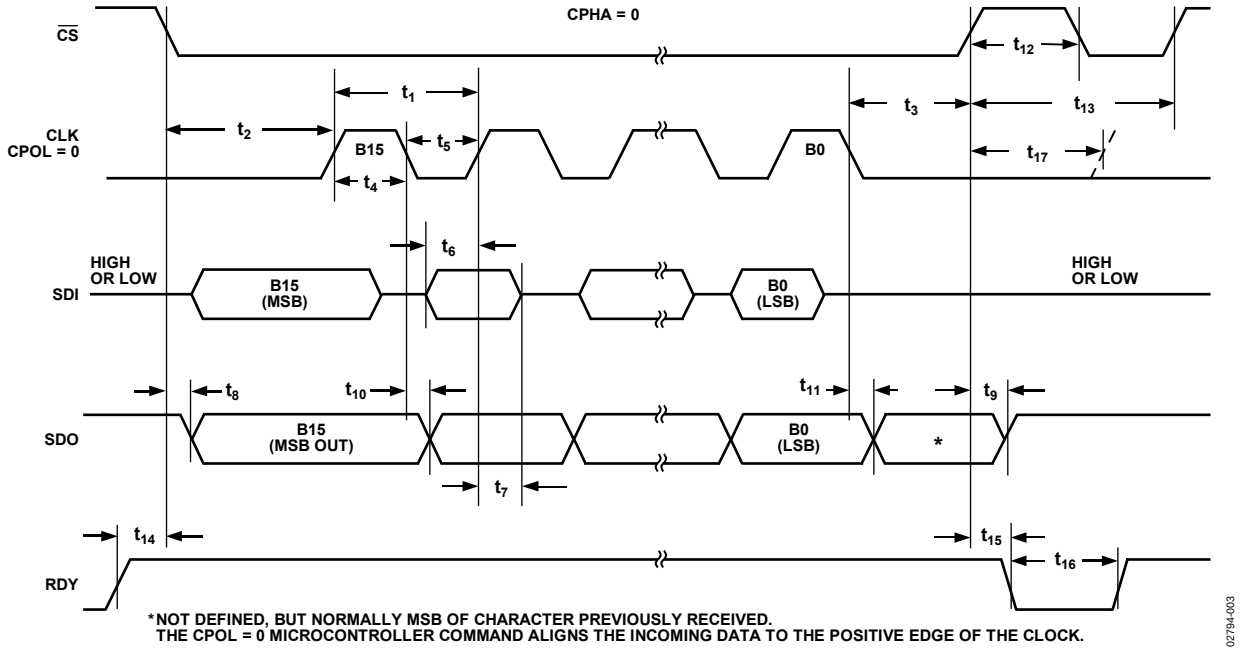

Figure 3. CPHA = 0 Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{SS} to GND	+0.3 V to −7 V
V_{DD} to V_{SS}	7 V
V_A, V_B, V_W to GND	V_{SS} − 0.3 V to V_{DD} + 0.3 V
I_A, I_B, I_W	
Pulsed[1]	±20 mA
Continuous	±2 mA
Digital Inputs and Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range[2]	−40°C to +85°C
Maximum Junction Temperature (T_J max)	150°C
Storage Temperature Range	−65°C to +150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	20 sec to 40 sec
Thermal Resistance Junction-to-Ambient, θ_{JA}[3]	50°C/W
Package Power Dissipation	(T_J max − T_A)/θ_{JA}

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.
[2] Includes programming of nonvolatile memory.
[3] Thermal Resistance (JEDEC 4-layer (2S2P) board).

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

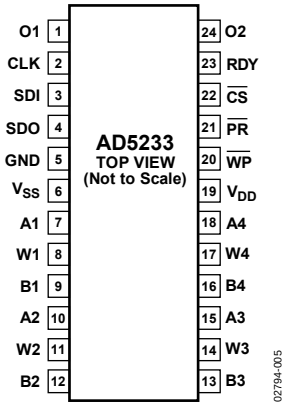

Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	O1	Nonvolatile Digital Output 1. Address (O1) = 0x4, the data bit position is D0; defaults to Logic 1 initially.
2	CLK	Serial Input Register Clock Pin. Shifts in one bit at a time on positive clock edges.
3	SDI	Serial Data Input Pin. Shifts in one bit at a time on positive CLK edges. MSB loaded first.
4	SDO	Serial Data Output Pin. Serves readback and daisy-chain functions. Command 9 and Command 10 activate the SDO output for the readback function, delayed by 16 or 17 clock pulses, depending on the clock polarity before and after the data-word (see Figure 2, Figure 3, and Table 7). In other commands, the SDO shifts out the previously loaded SDI bit pattern, delayed by 16 or 17 clock pulses, depending on the clock polarity (see Figure 2 and Figure 3). This previously shifted-out SDI can be used for daisy-chaining multiple devices. Whenever SDO is used, a pull-up resistor in the range of 1 kΩ to 10 kΩ is needed.
5	GND	Ground Pin, Logic Ground Reference.
6	V_{SS}	Negative Supply. Connect to 0 V for single-supply applications. If V_{SS} is used in dual supply, it must be able to sink 40 mA for 25 ms when storing data to EEMEM.
7	A1	Terminal A of RDAC1.
8	W1	Wiper Terminal of RDAC1, Address (RDAC1) = 0x0.
9	B1	Terminal B of RDAC1.
10	A2	Terminal A of RDAC2.
11	W2	Wiper Terminal of RDAC2, Address (RDAC2) = 0x1.
12	B2	Terminal B of RDAC2.
13	B3	Terminal B of RDAC3.
14	W3	Wiper Terminal of RDAC3, Address (RDAC3) = 0x2.
15	A3	Terminal A of RDAC3.
16	B4	Terminal B of RDAC4.
17	W4	Wiper Terminal of RDAC4, Address (RDAC4) = 0x3.
18	A4	Terminal A of RDAC4.
19	V_{DD}	Positive Power Supply Pin.
20	$\overline{WP}$	Optional Write Protect Pin. When active low, $\overline{WP}$ prevents any changes to the present contents, except $\overline{PR}$ strobe and Instruction 1 and Instruction 8, and refreshes the RDAC register from EEMEM. Execute a NOP instruction before returning to $\overline{WP}$ high. Tie $\overline{WP}$ to V_{DD} if not used.
21	$\overline{PR}$	Optional Hardware Override Preset Pin. Refreshes the scratchpad register with current contents of the EEMEM register. Factory default loads midscale 0x20 until EEMEM is loaded with a new value by the user. $\overline{PR}$ is activated at the Logic 1 transition. Tie $\overline{PR}$ to V_{DD} if not used.
22	$\overline{CS}$	Serial Register Chip Select Active Low. Serial register operation takes place when $\overline{CS}$ returns to Logic 1.
23	RDY	Ready. Active-high open-drain output. Identifies completion of Software Instruction 2, Software Instruction 3, Software Instruction 8, Software Instruction 9, Software Instruction 10, and Hardware Instruction $\overline{PR}$.
24	O2	Nonvolatile Digital Output 2. Address (O2) = 0x4, the data bit position is D1; defaults to Logic 1 initially.

TYPICAL PERFORMANCE CHARACTERISTICS

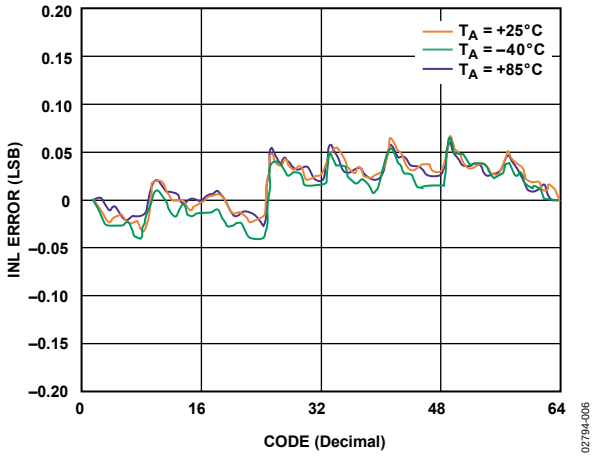

Figure 5. INL Error vs. Code, T_A = –40°C, +25°C, +85°C Overlay, R_{AB} = 10 kΩ

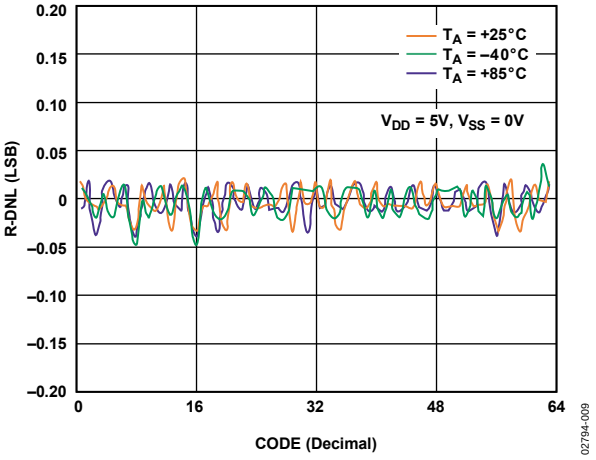

Figure 8. R-DNL vs. Code, T_A = –40°C, +25°C, +85°C Overlay, R_{AB} = 10 kΩ

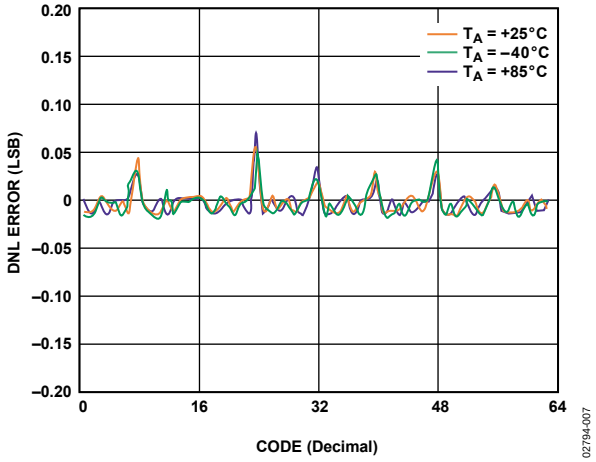

Figure 6. DNL Error vs. Code, T_A = –40°C, +25°C, +85°C Overlay, R_{AB} = 10 kΩ

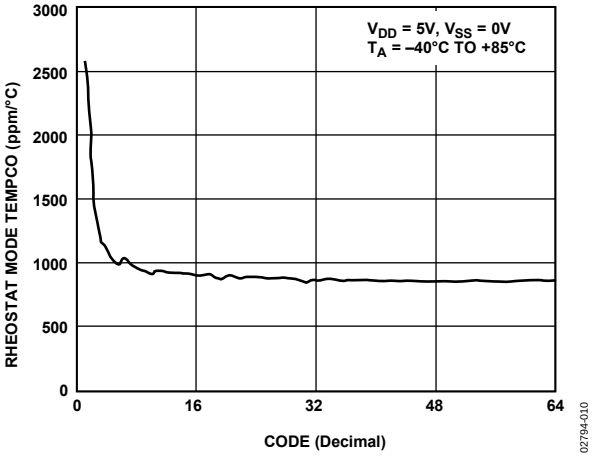

Figure 9. $(\Delta R_{WB}/R_{WB})/\Delta T \times 10^6$

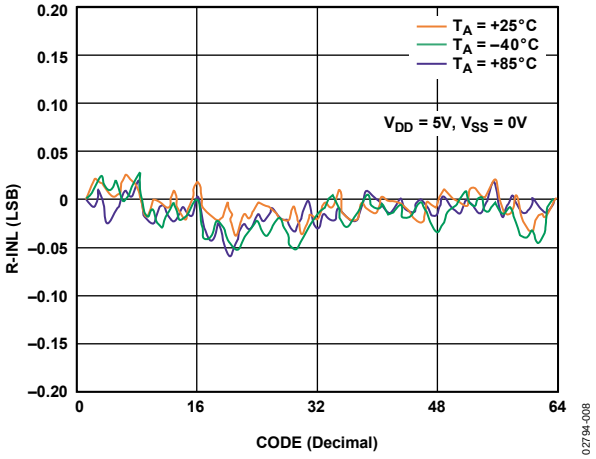

Figure 7. R-INL vs. Code, T_A = –40°C, +25°C, +85°C Overlay, R_{AB} = 10 kΩ

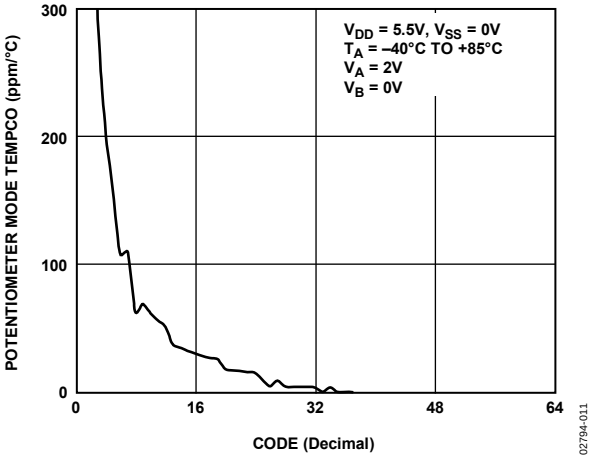

Figure 10. $(\Delta V_W/V_W)/\Delta T \times 10^6$ vs. Code, R_{AB} = 10 kΩ

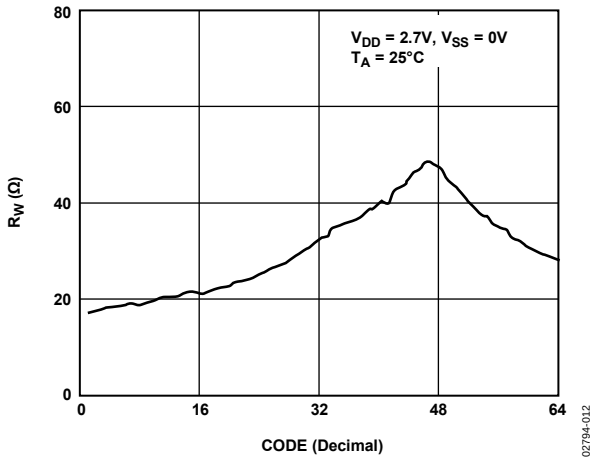

Figure 11. Wiper On Resistance vs. Code

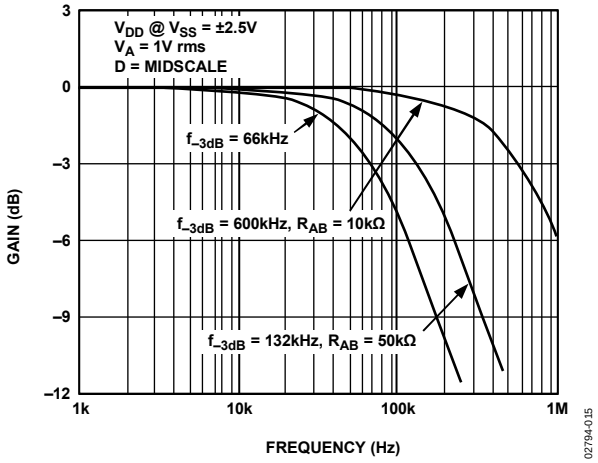

Figure 14. –3 dB Bandwidth vs. Resistance (Using the Circuit Shown in Figure 31)

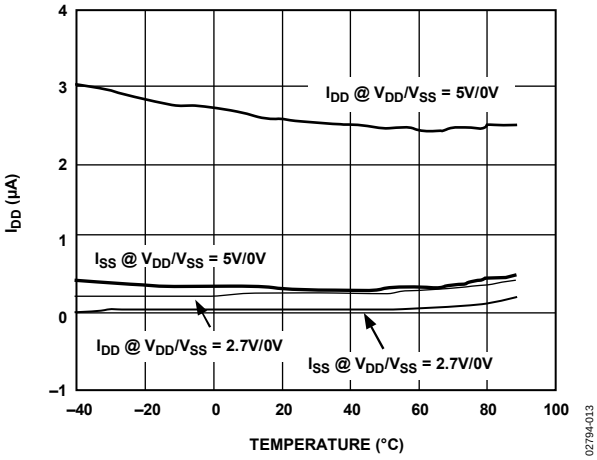

Figure 12. I_{DD} vs. Temperature, R_{AB} = 10 kΩ

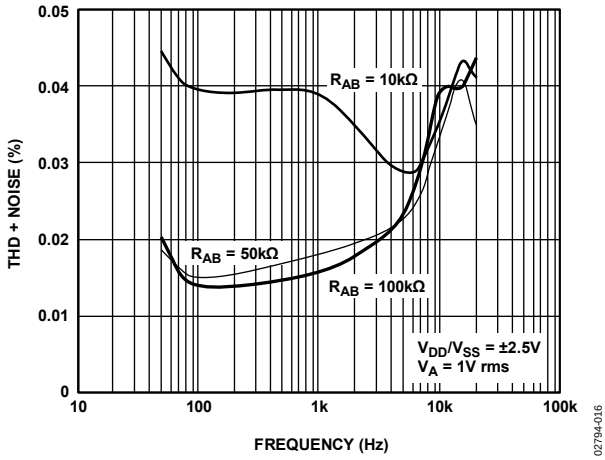

Figure 15. Total Harmonic Distortion + Noise vs. Frequency

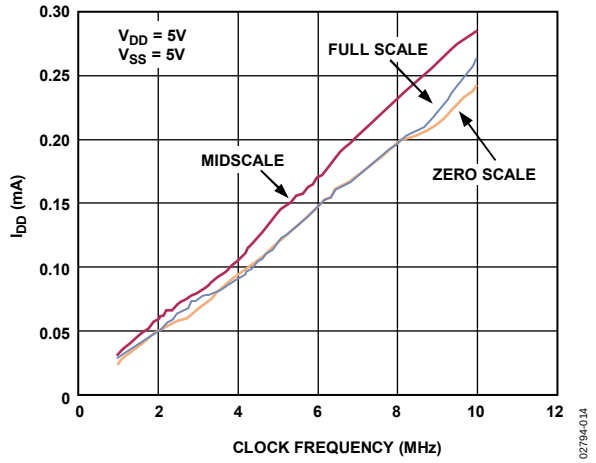

Figure 13. I_{DD} vs. Clock Frequency, R_{AB} = 10 kΩ

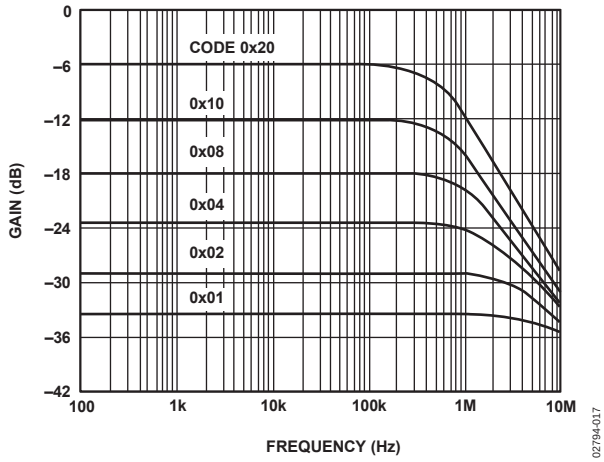

Figure 16. Gain vs. Frequency vs. Code, R_{AB} = 10 Ω (Figure 31)

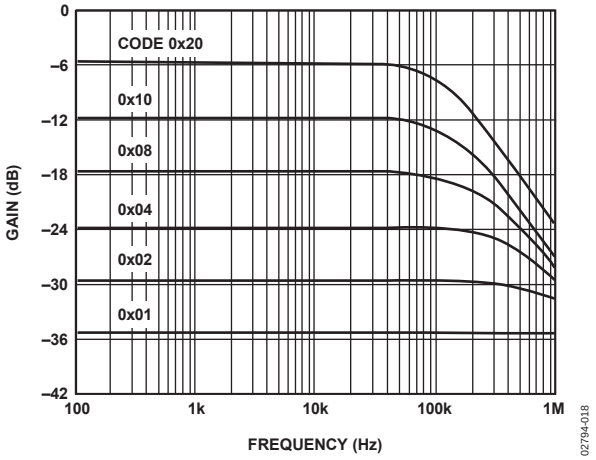

Figure 17. Gain vs. Frequency vs. Code, R_{AB} = 50 kΩ (Figure 31)

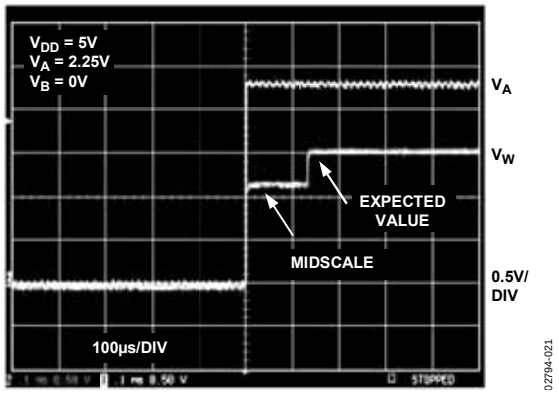

Figure 20. Power-On Reset, V_A = 2.25 V, V_B = 0 V, Code = 101010

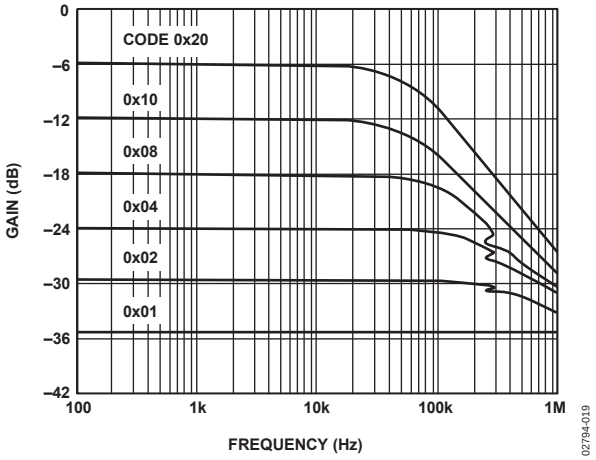

Figure 18. Gain vs. Frequency vs. Code, R_{AB} = 100 kΩ (Figure 31)

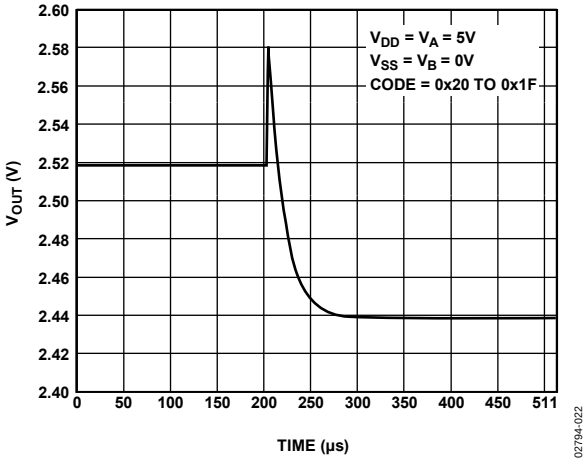

Figure 21. Midscale Glitch Energy, Code 0x20 to Code 0x1F

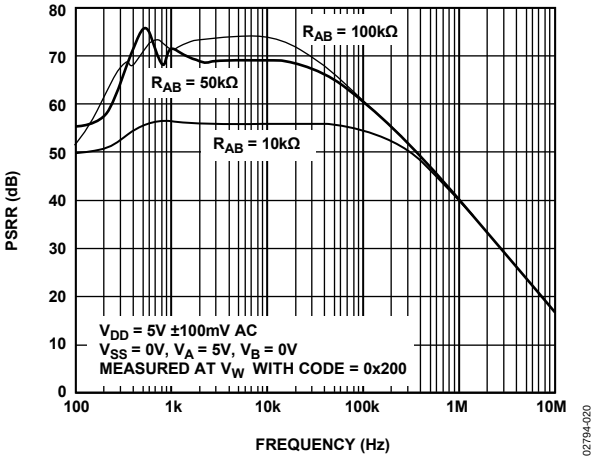

Figure 19. PSRR vs. Frequency

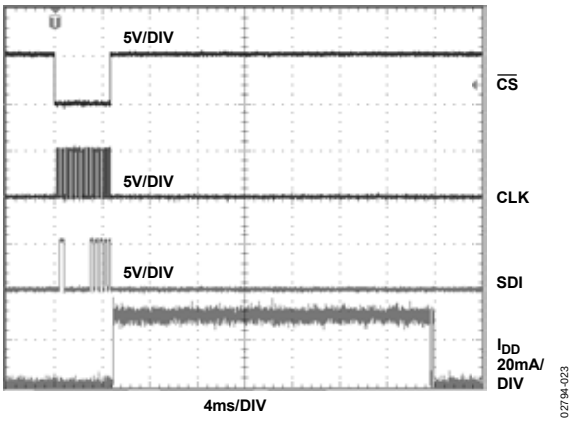

Figure 22. I_{DD} vs. Time When Storing Data to EEMEM

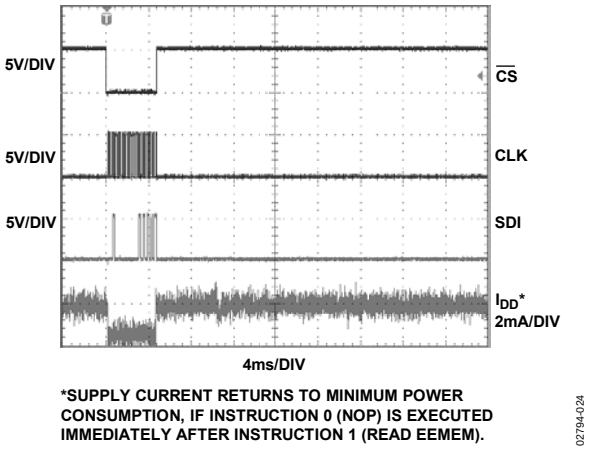

Figure 23. I_{DD} vs. Time When Reading Data from EEMEM

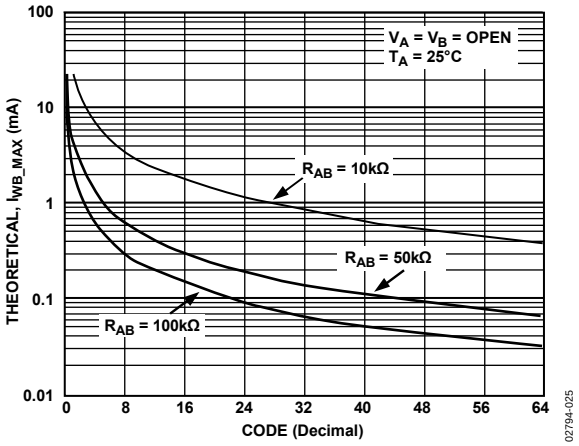

Figure 24. I_{WB_MAX} vs. Code

TEST CIRCUITS

Figure 25 to Figure 35 define the test conditions used in the specifications.

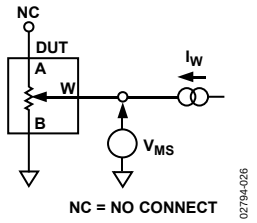

Figure 25. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

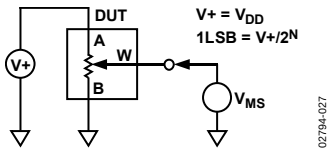

Figure 26. Potentiometer Divider Nonlinearity Error (INL, DNL)

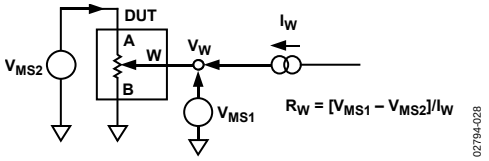

Figure 27. Wiper Resistance

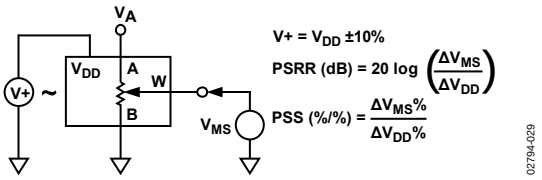

Figure 28. Power Supply Sensitivity (PSS, PSRR)

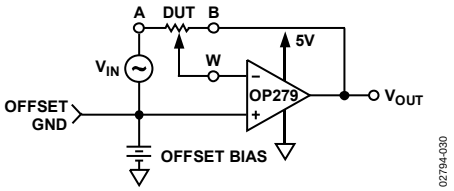

Figure 29. Inverting Gain

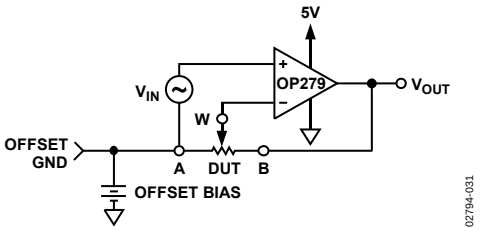

Figure 30. Noninverting Gain

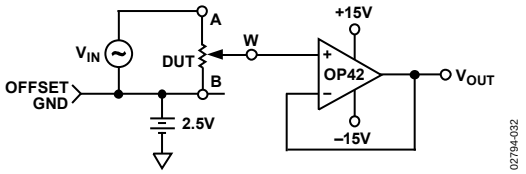

Figure 31. Gain vs. Frequency

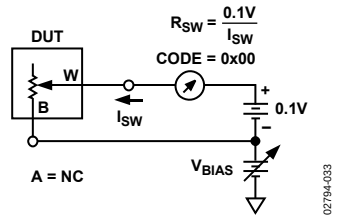

Figure 32. Incremental On Resistance

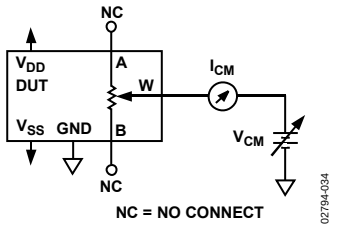

Figure 33. Common-Mode Leakage Current

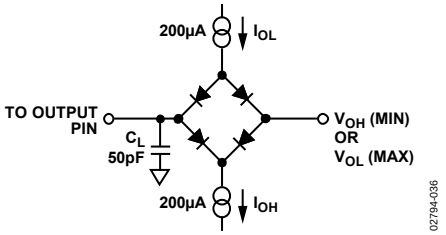

Figure 35. Load Circuit for Measuring V_{OH} and V_{OL}; the Diode Bridge Test Circuit Is Equivalent to the Application Circuit with $R_{PULL-UP}$ of 2.2 kΩ

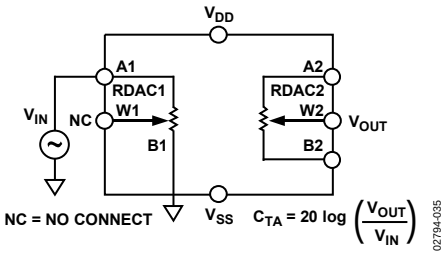

Figure 34. Analog Crosstalk

THEORY OF OPERATION

The AD5233 digital potentiometer is designed to operate as a true variable resistor replacement device for analog signals that remain within the terminal voltage range of $V_{SS} < V_{TERM} < V_{DD}$. The basic voltage range is limited to $V_{DD} - V_{SS} < 5.5$ V. The digital potentiometer wiper position is determined by the RDAC register contents.

The RDAC register acts as a scratchpad register, allowing as many value changes as necessary to place the potentiometer wiper in the correct position. The scratchpad register can be programmed with any position value using the standard SPI serial interface mode by loading the complete representative data-word. Once a desirable position is found, this value can be stored in an EEMEM register. Thereafter, the wiper position is always restored to that position for subsequent power-up.

The EEMEM data storing process takes approximately 25 ms; during this time, the shift register is locked, preventing any changes from taking place. The RDY pin pulses low to indicate the completion of this EEMEM storage.

The following instructions facilitate the user's programming needs (see Table 7 for details):

0 = Do nothing.

1 = Restore EEMEM contents to RDAC.

2 = Store RDAC setting to EEMEM.

3 = Store RDAC setting or user data to EEMEM.

4 = Decrement 6 dB.

5 = Decrement all 6 dB.

6 = Decrement one step.

7 = Decrement all one step.

8 = Reset EEMEM contents to RDACs.

9 = Read EEMEM contents from SDO.

10 = Read RDAC wiper setting from SDO.

11 = Write data to RDAC.

12 = Increment 6 dB.

13 = Increment all 6 dB.

14 = Increment one step.

15 = Increment all one step.

SCRATCHPAD AND EEMEM PROGRAMMING

The scratchpad RDAC register directly controls the position of the digital potentiometer wiper. For example, when the scratchpad register is loaded with all 0, the wiper is connected to Terminal B of the variable resistor. The scratchpad register is a standard logic register with no restriction on the number of changes allowed, but the EEMEM registers have a program erase/write cycle limitation (see the Flash/EEMEM Reliability section).

BASIC OPERATION

The basic mode of setting the variable resistor wiper position (programming the scratchpad register) is accomplished by loading the serial data input register with Instruction 11, Address A1, Address A0, and the desired wiper position data. When the proper wiper position is determined, the user can load the serial data input register with Instruction 2, which stores the wiper position data in the EEMEM register. After 25 ms, the wiper position is permanently stored in the nonvolatile memory location. Table 5 provides a programming example listing the sequence of serial data input (SDI) words with the serial data output appearing at the SDO pin in hexadecimal format.

Table 5. Set and Store RDAC Data to EEMEM Register

SDI	SDO	Action
0xB010	0xXXXX	Writes Data 0x10 to the RDAC1 register, Wiper W1 moves to ¼ full-scale position.
0x20XX	0xB010	Stores RDAC1 register content into the EEMEM1 register.

At system power-on, the scratchpad register is automatically refreshed with the value previously stored in the EEMEM register. The factory-preset EEMEM value is midscale, but it can be changed by the user thereafter.

During operation, the scratchpad (RDAC) register can be refreshed with the EEMEM register data with Instruction 1 or Instruction 8. The RDAC register can also be refreshed with the EEMEM register data under hardware control by pulsing the $\overline{PR}$ pin. The $\overline{PR}$ pulse first sets the wiper at midscale when brought to Logic 0, and then, on the positive transition to Logic 1, it reloads the RDAC wiper register with the contents of EEMEM.

Many additional advanced programming commands are available to simplify the variable resistor adjustment process (see Table 7). For example, the wiper position can be changed one step at a time using the increment/decrement instruction or by 6 dB with the shift left/right instruction. Once an increment, decrement, or shift instruction has been loaded into the shift register, subsequent $\overline{CS}$ strobes can repeat this command.

A serial data output SDO pin is available for daisy-chaining and for readout of the internal register contents.

EEMEM PROTECTION

The write protect ($\overline{WP}$) pin disables any changes to the scratchpad register contents, except for the EEMEM setting, which can still be restored using Instruction 1, Instruction 8, and the $\overline{PR}$ pulse. Therefore, $\overline{WP}$ can be used to provide a hardware EEMEM protection feature. To disable $\overline{WP}$, it is recommended to execute a NOP instruction before returning $\overline{WP}$ to Logic 1.

DIGITAL INPUT/OUTPUT CONFIGURATION

All digital inputs are ESD-protected, high input impedance that can be driven directly from most digital sources. Active at Logic 0, $\overline{PR}$ and $\overline{WP}$ must be tied to V_{DD} if they are not used. No internal pull-up resistors are present on any digital input pins. Because the device can be detached from the driving source once it is programmed, adding pull-up resistance on the digital input pins is a good way to avoid falsely triggering the floating pins in a noisy environment.

The SDO and RDY pins are open-drain digital outputs that need pull-up resistors only if these functions are used. Use a resistor in the range of 1 kΩ to 10 kΩ to balance the power and switching speed trade-off.

SERIAL DATA INTERFACE

The AD5233 contains a 4-wire SPI-compatible digital interface (SDI, SDO, $\overline{CS}$, and CLK). It uses a 16-bit serial data-word loaded MSB first. The format of the SPI-compatible word is shown in Table 6. The chip-select $\overline{CS}$ pin must be held low until the complete data-word is loaded into the SDI pin. When $\overline{CS}$ returns high, the serial data-word is decoded according to the instructions in Table 7. The command bits (Cx) control the operation of the digital potentiometer. The address bits (Ax) determine which register is activated. The data bits (Dx) are the values that are loaded into the decoded register. To program RDAC1 to RDAC4, only the 6 LSB data bits are used.

The AD5233 has an internal counter that counts a multiple of 16 bits (a frame) for proper operation. For example, the AD5233 works with a 32-bit word, but it cannot work properly with a 15-bit or 17-bit word. In addition, the AD5233 has a subtle feature that, if $\overline{CS}$ is pulsed without CLK and SDI, the part repeats the previous command (except during power-up). As a result, care must be taken to ensure that no excessive noise exists in the CLK or $\overline{CS}$ line that might alter the effective number-of-bits pattern. Also, to prevent data from locking incorrectly (due to noise, for example), the counter resets, if the count is not a multiple of four when $\overline{CS}$ goes high.

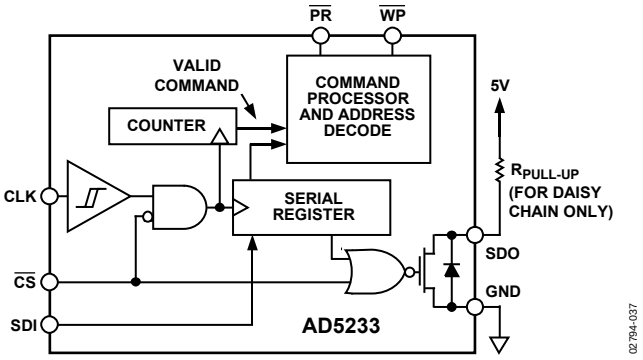

Figure 36. Equivalent Digital Input-Output Logic

The equivalent serial data input and output logic is shown in Figure 36. The open-drain output SDO is disabled whenever chip select ($\overline{CS}$) is in Logic 1. The SPI interface can be used in two slave modes: CPHA = 1, CPOL = 1 and CPHA = 0, CPOL = 0. CPHA and CPOL refer to the control bits that dictate SPI timing in the following MicroConverters® and microprocessors: ADuC812, ADuC824, M68HC11, and MC68HC16R1/MC68HC916R1. ESD protection of the digital inputs is shown in Figure 37 and Figure 38.

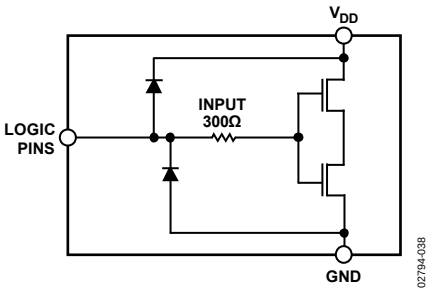

Figure 37. Equivalent ESD Digital Input Protection

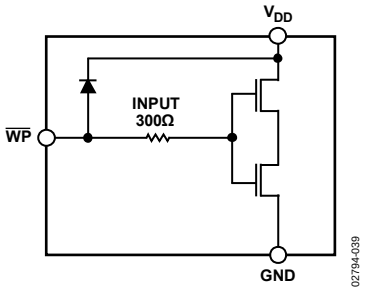

Figure 38. Equivalent $\overline{WP}$ Input Protection

DAISY-CHAIN OPERATION

The serial data output (SDO) pin serves two purposes. It can be used to read the contents of the wiper setting and EEMEM values using Instruction 10 and Instruction 9, respectively. The remaining instructions (0 to 8, 11 to 15) are valid for daisy-chaining multiple devices in simultaneous operations. Daisy-chaining minimizes the number of port pins required from the controlling IC (Figure 39). The SDO pin contains an open-drain N-channel FET that requires a pull-up resistor, if this function is used. As shown in Figure 39, users need to tie the SDO pin of one package to the SDI pin of the next package.

Users might need to increase the clock period, because the pull-up resistor and the capacitive loading at the SDO to SDI interface might require an additional time delay between subsequent packages. When two AD5233s are daisy-chained, 32 bits of data is required. The first 16 bits go to U2 and the second 16 bits go to U1. $\overline{CS}$ should be kept low until all 32 bits are clocked into their respective serial registers. $\overline{CS}$ is then pulled high to complete the operation.

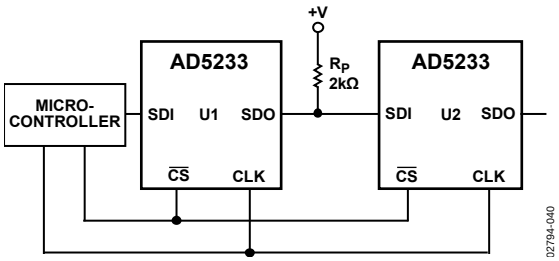

Figure 39. Daisy-Chain Configuration Using SDO

TERMINAL VOLTAGE OPERATION RANGE

The AD5233's positive V_{DD} and negative V_{SS} power supplies define the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on Terminal A, Terminal B, and Terminal W that exceed V_{DD} or V_{SS} are clamped by the internal forward-biased diodes (see Figure 40).

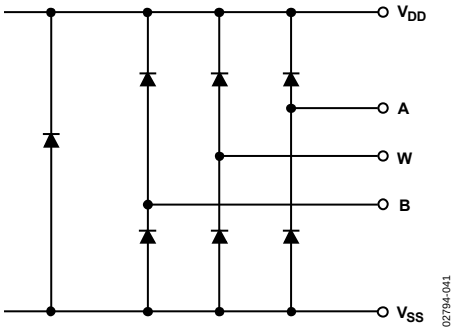

Figure 40. Maximum Terminal Voltages Set by V_{DD} and V_{SS}

The ground pin of the AD5233 device is used primarily as a digital ground reference, which needs to be tied to the PCB's common ground. The digital input control signals to the AD5233 must be referenced to the device ground pin (GND) and satisfy the logic level defined in the Specifications section. An internal level-shift circuit ensures that the common-mode voltage range of the three terminals extends from V_{SS} to V_{DD}, regardless of the digital input level.

POWER-UP SEQUENCE

Because there are diodes to limit the voltage compliance at Terminal A, Terminal B, and Terminal W (see Figure 40), it is important to power on V_{DD}/V_{SS} first before applying any voltage to Terminal A, Terminal B, and Terminal W. Otherwise, the diode is forward-biased such that V_{DD}/V_{SS} are powered unintentionally. For example, applying 5 V across the A and B terminals prior to V_{DD} causes the V_{DD} terminal to exhibit 4.3 V. It is not destructive to the device, but it might affect the rest of the system. The ideal power-up sequence is GND, V_{DD}, V_{SS}, digital inputs, and $V_A/V_B/V_W$. The order of powering V_A, V_B, V_W, and digital inputs is not important as long as they are powered after V_{DD}/V_{SS}.

Regardless of the power-up sequence and the ramp rates of the power supplies, once V_{DD}/V_{SS} are powered, the power-on preset remains effective, which restores the EEMEM values to the RDAC registers.

LATCHED DIGITAL OUTPUTS

A pair of digital outputs, O1 and O2, is available on the AD5233. These outputs provide a nonvolatile Logic 0 or Logic 1 setting. O1 and O2 are standard CMOS logic outputs, shown in Figure 41. These outputs are ideal to replace the functions often provided by DIP switches. In addition, they can be used to drive other standard CMOS logic-controlled parts that need an occasional setting change. Pin O1 and Pin O2 default to Logic 1, and they can drive up to 50 mA of load at 5 V/25°C.

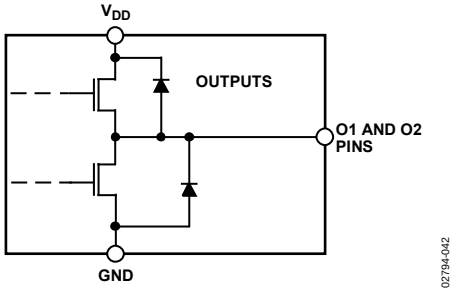

Figure 41. Logic Output O1 and Logic Output O2

In Table 6, C0 to C3 are command bits, A3 to A0 are address bits, D0 to D5 are data bits that are applicable to the RDAC wiper register, and D0 to D7 are applicable to the EEMEM register.

Table 6. 16-Bit Serial Data-Word

MSB	Instruction Byte							LSB	Data Byte							
RDAC	C3	C2	C1	C0	0	0	A1	A0	X	X	D5	D4	D3	D2	D1	D0
EEMEM	C3	C2	C1	C0	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

Command instruction codes are defined in Table 7.

Table 7. Instruction/Operation Truth Table[1, 2, 3]

Inst. No.	Instruction Byte 0								Data Byte 0								Operation
	B16							B8	B7	B6	B5	B4	B3	B2	B1	B0	
	C3	C2	C1	C0	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	NOP: Do nothing. See Table 14 for programming example.
1	0	0	0	1	0	0	A1	A0	X	X	X	X	X	X	X	X	Restore EEMEM contents to the RDAC register. This command leaves the device in read program power state. To return the part to the idle state, perform NOP instruction 0. See Table 14.
2	0	0	1	0	0	0	A1	A0	X	X	X	X	X	X	X	X	Store wiper setting: Store RDAC (ADDR) setting to EEMEM. See Table 13.
3[4]	0	0	1	1	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	Store contents of Serial Register Data Byte 0 (total eight bits) to EEMEM (ADDR). See Table 16.
4[5]	0	1	0	0	0	0	A1	A0	X	X	X	X	X	X	X	X	Decrement 6 dB: right-shift contents of RDAC register, stop at all 0s.
5[5]	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	Decrement all 6 dB: right-shift contents of all RDAC registers, stop at all 0s.
6[5]	0	1	1	0	0	0	A1	A0	X	X	X	X	X	X	X	X	Decrement content of RDAC register by 1, stop at all 0s.
7[5]	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	Decrement contents of all the RDAC registers by 1, stop at all 0s.
8	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	Reset: refresh all RDACs with their corresponding EEMEM previously stored values.
9	1	0	0	1	A3	A2	A1	A0	X	X	X	X	X	X	X	X	Read content of EEMEM (ADDR) from SDO output in the next frame. See Table 17.
10	1	0	1	0	0	0	A1	A0	X	X	X	X	X	X	X	X	Read RDAC wiper setting from SDO output in the next frame. See Table 18.
11	1	0	1	1	0	0	A1	A0	X	X	D5	D4	D3	D2	D1	D0	Write contents of Serial Register Data Byte 0 (total six bits) to RDAC. See Table 12.
12[5]	1	1	0	0	0	0	A1	A0	X	X	X	X	X	X	X	X	Increment 6 dB: Left-shift contents of RDAC register, stop at all 1s. See Table 15.
13[5]	1	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	Increment all 6 dB: left-shift contents of RDAC registers, stop at all 1s.
14[5]	1	1	1	0	0	0	A1	A0	X	X	X	X	X	X	X	X	Increment contents of the RDAC register by 1, stop at all 1s. See Table 13.
15[5]	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	Increment contents of all RDAC registers by 1, stop at all 1s.

[1] The SDO output shifts out the last 16 bits of data clocked into the serial register for daisy-chain operation. Exception: for any instruction following Instruction 9 or Instruction 10, see details of these instructions for proper usage.
[2] The RDAC register is a volatile scratchpad register that is automatically refreshed at power-on from the corresponding nonvolatile EEMEM register.
[3] Execution of these operations takes place when the $\overline{CS}$ strobe returns to Logic 1.
[4] Instruction 3 writes one data byte (eight bits of data) to EEMEM. In the case of Address 0, Address 1, Address 2, and Address 3, only the last six bits are valid for wiper position setting.
[5] The increment, decrement, and shift instructions ignore the contents of the Shift Register Data Byte 0.

ADVANCED CONTROL MODES

The AD5233 digital potentiometer includes a set of user programming features to address the wide number of applications for these universal adjustment devices.

Key programming features include

- Scratchpad programming to any desirable values
- Nonvolatile memory storage of the scratchpad RDAC register value in the EEMEM register
- Increment and decrement instructions for the RDAC wiper register
- Left- and right-bit shift of the RDAC wiper register to achieve ±6 dB level changes
- Eleven extra bytes of user-addressable nonvolatile memory

Linear Increment and Decrement Instructions

The increment and decrement instructions (14, 15, 6, and 7) are useful for linear step-adjustment applications. These commands simplify microcontroller software coding by allowing the controller to send just an increment or decrement command to the device.

For an increment command, executing Instruction 14 with the proper address automatically moves the wiper to the next resistance segment position. Instruction 15 performs the same function, except that the address does not need to be specified. All RDACs are changed at the same time.

Logarithmic Taper Mode Adjustment

Four programming instructions produce logarithmic taper increment and decrement of the wiper. These settings are activated by the 6 dB increment and 6 dB decrement instructions (12, 13, 4, and 5). For example, starting at zero scale, executing the increment Instruction 12 seven times moves the wiper in 6 dB per step from 0% to full scale, R_{AB}. The 6 dB increment instruction doubles the value of the RDAC register contents each time the command is executed. When the wiper position is near the maximum setting, the last 6 dB increment instruction causes the wiper to go to the full-scale 63_{10} code position. Further 6 dB per increment instructions do not change the wiper position beyond its full scale.

The 6 dB step increments and 6 dB step decrements are achieved by shifting the bit internally to the left or right, respectively. The following information explains the nonideal ±6 dB step adjustment under certain conditions. Table 8 illustrates the operation of the shifting function on the RDAC register data bits. Each table row represents a successive shift operation. Note that the left-shift 12 and 13 instructions were modified such that, if the data in the RDAC register is equal to zero and the data is shifted left, the RDAC register is then set to Code 1. Similarly, if the data in the RDAC register is greater than or equal to midscale and the data is shifted left, then the data in the RDAC register is automatically set to full scale. This makes the left-shift function as ideal a logarithmic adjustment as possible.

The right-shift 4 and 5 instructions are ideal only if the LSB is 0 (ideal logarithmic = no error). If the LSB is a 1, the right-shift function generates a linear half-LSB error, which translates to a number-of-bits-dependent logarithmic error, as shown in Figure 42. The plot shows the error of the odd numbers of bits for the AD5233.

Table 8. Detail Left-Shift and Right-Shift Functions for 6 dB Step Increment and Decrement

Left-Shift (+6 dB/Step)	Right-Shift (–6 dB/Step)
00 0000	11 1111
00 0001	01 1111
00 0010	00 1111
00 0100	00 0111
00 1000	00 0011
01 0000	00 0001
10 0000	00 0000
11 1111	00 0000
11 1111	00 0000

Actual conformance to a logarithmic curve between the data contents in the RDAC register and the wiper position for each right-shift 4 and 5 command execution contains an error only for odd numbers of bits. Even numbers of bits are ideal. The graph in Figure 42 shows plots of log error [$20 \times \log_{10}$ (error/code)] for the AD5233. For example, Code 3 log error = $20 \times \log_{10}(0.5/3) = -15.56$ dB, which is the worst-case scenario. The plot of log error is more significant at the lower codes.

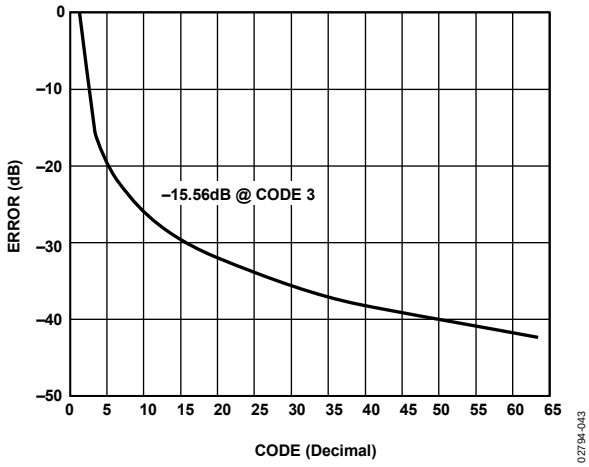

Figure 42. Plot of Log Error Conformance for Odd Numbers of Bits Only (Even Numbers of Bits are Ideal)

Using Additional Internal Nonvolatile EEMEM

The AD5233 contains additional user EEMEM registers for storing any 8-bit data. Table 9 provides an address map of the internal storage registers shown in the functional block diagram as EEMEM1, EEMEM2, and 11 bytes of user EEMEM.

Table 9. EEMEM Address Map

EEMEM Number	Address	EEMEM Content
1	0000	RDAC1[1, 2]
2	0001	RDAC2[1, 2]
3	0010	RDAC3[1, 2]
4	0011	RDAC4[1, 2]
5	0100	O1 and O2[3]
6	0101	USER1[4]
7	0110	USER2
…	…	…
15	1110	USER10
16	1111	USER11

[1] RDAC data stored in the EEMEM location is transferred to the RDAC register at power-on, or when Instruction 1, Instruction 8, and $\overline{PR}$ are executed.

[2] Execution of Instruction 1 leaves the device in the read mode power consumption state. After the last Instruction 1 is executed, the user should perform a NOP, Instruction 0, to return the device to the low power idling state.

[3] O1 and O2 data stored in EEMEM locations is transferred to the corresponding digital register at power-on, or when Instruction 1 and Instruction 8 are executed.

[4] USERx are internal nonvolatile EEMEM registers available to store and retrieve constants and other 8-bit information using Instruction 3 and Instruction 9, respectively.

RDAC STRUCTURE

The patent-pending RDAC contains multiple strings of equal resistor segments, with an array of analog switches that act as the wiper connection. The number of positions is the resolution of the device. The AD5233 has 64 connection points, allowing it to provide better than 1.5% set ability resolution. Figure 43 shows an equivalent structure of the connections between the three terminals of the RDAC. The SW_A and SW_B are always on, while the switches, SW(0) to SW(2^N–1), are on, one at a time, depending on the resistance position decoded from the data bits. Because the switch is not ideal, there is a 15 Ω wiper resistance, R_W. Wiper resistance is a function of supply voltage and temperature. The lower the supply voltage or the higher the temperature, the higher the resulting wiper resistance. Users should be aware of the wiper resistance dynamics if an accurate prediction of the output resistance is needed.

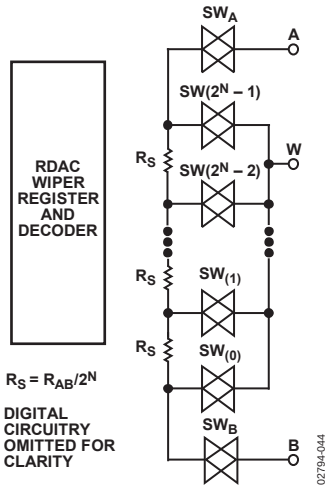

Figure 43. Equivalent RDAC Structure

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

The nominal resistance of the RDAC between Terminal A and Terminal B, R_{AB}, is available with 10 kΩ, 50 kΩ, and 100 kΩ with 64 positions (6-bit resolution). The final digit(s) of the part number determine the nominal resistance value, for example, 10 = 10 kΩ; 50 = 50 kΩ; 100 = 100 kΩ.

The 6-bit data-word in the RDAC latch is decoded to select one of the 64 possible settings. The following discussion describes the calculation of resistance (R_{WB}) at different codes of a 10 kΩ part. For V_{DD} = 5 V, the wiper's first connection starts at Terminal B for Data 0x00. $R_{WB}(0)$ is 15 Ω because of the wiper resistance and because it is independent of the nominal resistance. The second connection is the first tap point, where $R_{WB}(1)$ becomes 156 Ω + 15 Ω = 171 Ω for Data 0x01. The third connection is the next tap point, representing $R_{WB}(2)$ = 321 Ω + 15 Ω = 327 Ω for Data 0x02, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at $R_{WB}(63)$ = 9858 Ω. See Figure 43 for a simplified diagram of the equivalent RDAC circuit. When R_{WB} is used, Terminal A can be left floating or tied to the wiper.

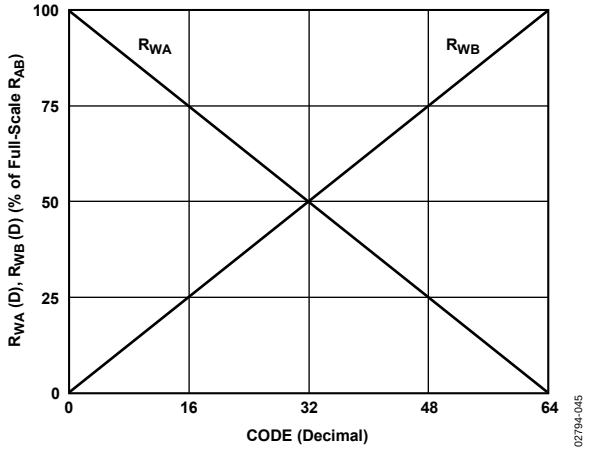

Figure 44. $R_{WA}(D)$ and $R_{WB}(D)$ vs. Decimal Code

The general equation that determines the programmed output resistance between W and B is

$$R_{WB}(D) = \frac{D}{64} \times R_{AB} + R_W \quad (1)$$

where:
D is the decimal equivalent of the data contained in the RDAC register.
R_{AB} is the nominal resistance between Terminal A and Terminal B.
R_W is the wiper resistance.

For example, the output resistance values in Table 10 are set for the given RDAC latch codes with V_{DD} = 5 V (applies to R_{AB} = 10 kΩ digital potentiometers).

Table 10. R_{WB}(D) at Selected Codes for R_{AB} = 10 kΩ

D (Decimal)	R_{WB}(D) (Ω)	Output State
63	9858	Full scale
32	5015	Midscale
1	171	1 LSB
0	15	Zero scale (wiper contact resistor)

Note that in the zero-scale condition a finite wiper resistance of 15 Ω is present. Care should be taken to limit the current flow between W and B in this state to no more than 20 mA to avoid degradation or possible destruction of the internal switches.

Like the mechanical potentiometer that the RDAC replaces, the AD5233 part is totally symmetrical. The resistance between Wiper W and Terminal A also produces a digitally controlled complementary resistance, R_{WA}. Figure 44 shows the symmetrical programmability of the various terminal connections. When R_{WA} is used, Terminal B can be left floating or tied to the wiper. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch is increased in value.

The general transfer equation for this operation is

$$R_{WA}(D) = \frac{64 - D}{64} \times R_{AB} + R_W \quad (2)$$

For example, the output resistance values in Table 11 are set for the RDAC latch codes with V_{DD} = 5 V (applies to R_{AB} = 10 kΩ digital potentiometers).

Table 11. R_{WA}(D) at Selected Codes for R_{AB} = 10 kΩ

D (Decimal)	R_{WA}(D) (Ω)	Output State
63	171	Full scale
32	5015	Midscale
1	9858	1 LSB
0	10015	Zero scale

Channel-to-channel R_{AB} matching is better than 1%. The change in R_{AB} with temperature has a 600 ppm/°C temperature coefficient.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer can be configured to generate an output voltage at the wiper terminal that is proportional to the input voltages applied to Terminal A and Terminal B. For example, connecting Terminal A to 5 V and Terminal B to ground produces an output voltage at the wiper that can be any value from 0 V to 5 V. Each LSB of voltage is equal to the voltage applied across Terminal A and Terminal B divided by the 2^N position resolution of the potentiometer divider.

Because AD5233 can also be supplied by dual supplies, the general equation defining the output voltage at V_W with respect to ground for any given input voltages applied to the A and B terminals is

$$V_W(D) = \frac{D}{64} \times V_{AB} + V_B \quad (3)$$

Equation 3 assumes that V_W is buffered so that the effect of wiper resistance is minimized. Operation of the digital potentiometer in divider mode results in more accurate operation over temperature. Here, the output voltage is dependent on the ratio of the internal resistors and not the absolute value; therefore, the drift improves to 15 ppm/°C. There is no voltage polarity restriction among the A, B, and W terminals as long as the terminal voltage (V_{TERM}) stays within $V_{SS} < V_{TERM} < V_{DD}$.

PROGRAMMING EXAMPLES

The following programming examples illustrate a typical sequence of events for various features of the AD5233. See Table 7 for the instructions and data-word format. The instruction numbers, addresses, and data appearing at the SDI and SDO pins are in hexadecimal format.

Table 12. Scratchpad Programming

SDI	SDO	Action
0xB010	0xXXXX	Writes Data 0x10 into RDAC register, Wiper W1 moves to ¼ full-scale position.

Table 13. Incrementing RDAC1 Followed by Storing the Wiper Setting to EEMEM1

SDI	SDO	Action
0xB010	0xXXXX	Writes Data 0x10 into RDAC register, Wiper W1 moves to ¼ full-scale position.
0xE0XX	0xB010	Increments the RDAC register by one to 0x11.
0xE0XX	0xE0XX	Increments the RDAC register by one to 0x12. Continues until desired wiper position is reached.
0x20XX	0xXXXX	Stores the RDAC register data into EEMEM1. Optionally tie $\overline{WP}$ to GND to protect EEMEM values.

The EEMEM1 value for RDAC1 can be restored by power-on, by strobing the $\overline{PR}$ pin, or by programming, as shown in Table 14.

Table 14. Restoring the EEMEM1 Value to the RDAC1 Register

SDI	SDO	Action
0x10XX	0xXXXX	Restores the EEMEM1 value to the RDAC1 register.
0x00XX	0x10XX	NOP. Recommended step to minimize power consumption.

Table 15. Using Left-Shift by One to Increment 6 dB Step

SDI	SDO	Action
0xC0XX	0xXXXX	Moves the wiper to double the present data contained in the RDAC1 register.

Table 16. Storing Additional User Data in EEMEM

SDI	SDO	Action
0x35AA	0xXXXX	Stores Data 0xAA in the extra EEMEM6 location, USER1. (Allowable to address in 11 locations with a maximum of eight bits of data.)
0x3655	0x35AA	Stores Data 0x55 in the extra EEMEM7 location USER2. (Allowable to address in 11 locations with a maximum of eight bits of data.)

Table 17. Reading Back Data from Memory Locations

SDI	SDO	Action
0x95XX	0xXXXX	Prepares data read from USER1 EEMEM location.
0x00XX	0x95AA	NOP Instruction 0 sends a 16-bit word out of SDO, where the last eight bits contain the contents of the USER1 location. The NOP command ensures that the device returns to the idle power dissipation state.

Table 18. Reading Back Wiper Settings

SDI	SDO	Action
0xB020	0xXXXX	Writes RDAC1 to midscale.
0xC0XX	0xB020	Doubles RDAC1 from midscale to full scale (left-shift instruction).
0xA0XX	0xC0XX	Prepares reading the wiper setting from the RDAC1 register.
0xXXXX	0xA03F	Reads back full-scale value from SDO.

FLASH/EEMEM RELIABILITY

The Flash/EE memory array on the AD5233 is fully qualified for two key Flash/EE memory characteristics, Flash/EE memory cycling endurance, and Flash/EE memory data retention.

Endurance quantifies the ability of the Flash/EE memory to be cycled through many program, read, and erase cycles. In real terms, a single endurance cycle is composed of the following four independent, sequential events:

- Initial page erase sequence
- Read/verify sequence
- Byte program sequence
- Second read/verify sequence

During reliability qualification, Flash/EE memory is cycled from 0x00 to 0x3F until a first fail is recorded, signifying the endurance limit of the on-chip Flash/EE memory.

As indicated in the Specifications section, the AD5233 Flash/EE memory endurance qualification has been carried out in accordance with JEDEC Specification A117 over the industrial temperature range of −40°C to +85°C. The results allow the specification of a minimum endurance figure over supply and temperature of 100,000 cycles, with an endurance figure of 700,000 cycles being typical of operation at 25°C.

Retention quantifies the ability of the Flash/EE memory to retain its programmed data over time. Again, the AD5233 has been qualified in accordance with the formal JEDEC Retention Lifetime Specification (A117) at a specific junction temperature (T_J = 55°C). As part of this qualification procedure, the Flash/EE memory is cycled to its specified endurance limit, described previously, before data retention is characterized. This means that the Flash/EE memory is guaranteed to retain its data for its full specified retention lifetime every time the Flash/EE memory is reprogrammed. It should also be noted that retention lifetime, based on an activation energy of 0.6 eV, derates with T_J as shown in Figure 45. For example, the data is retained for 100 years at 55°C operation, but reduces to 15 years at 85°C operation. Beyond these limits, the part must be reprogrammed so that the data can be restored.

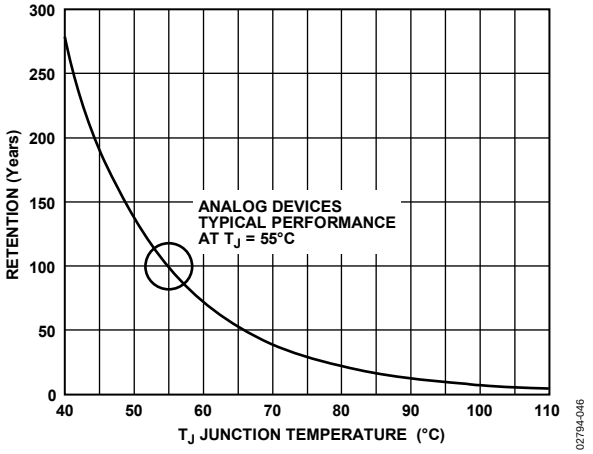

Figure 45. Flash/EE Memory Data Retention

APPLICATIONS INFORMATION

BIPOLAR OPERATION FROM DUAL SUPPLIES

The AD5233 can be operated from dual supplies ±2.5 V, which enables control of ground-referenced ac signals or bipolar operation. AC signals as high as V_{DD}/V_{SS} can be applied directly across Terminal A and Terminal B with output taken from Terminal W. See Figure 46 for a typical circuit connection.

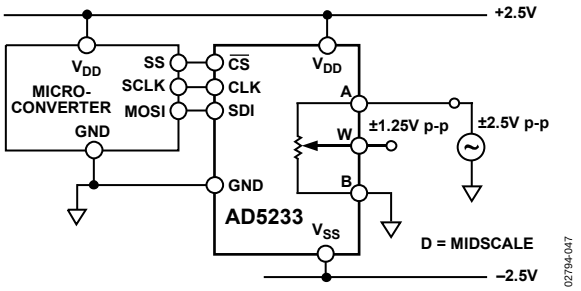

Figure 46. Bipolar Operation from Dual Supplies

GAIN CONTROL COMPENSATION

A digital potentiometer is commonly used in gain control such as the noninverting gain amplifier shown in Figure 47.

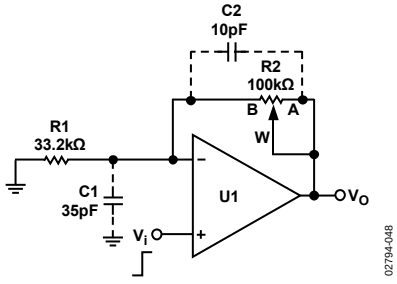

Figure 47. Typical Noninverting Gain Amplifier

When RDAC B terminal parasitic capacitance is connected to the op amp noninverting node, it introduces a 0 for the $1/b_O$ term with 20 dB/dec, while a typical op amp GBP has –20 dB/dec characteristics. A large R2 and finite C1 can cause this zero's frequency to fall well below the crossover frequency. Therefore, the rate of closure becomes 40 dB/dec, and the system as a 0° phase margin at the crossover frequency. The output can ring or oscillate if an input is a rectangular pulse or step function. Similarly, it is also likely to ring when switching between two gain values; this is equivalent to a stop change at the input.

Depending on the op amp GBP, reducing the feedback resistor might extend the zero's frequency far enough to overcome the problem. A better approach is to include a compensation capacitor, C2, to cancel the effect caused by C1. Optimum compensation occurs when R1 × C1 = R2 × C2. This is not an option because of the variation of R2.

As a result, one can use the previous relationship and scale C2 as if R2 were at its maximum value. Doing this might overcompensate and compromise the performance when R2 is set at low values. On the other hand, it avoids the ringing or oscillation at the worst case. For critical applications, C2 should be found empirically to suit the need. In general, C2 in the range of picofarads is usually adequate for the compensation.

Similarly, W and A terminal capacitances are connected to the output (not shown); their effect at this node is less significant and the compensation can be avoided in most cases.

HIGH VOLTAGE OPERATION

The digital potentiometer can be placed directly in the feedback or input path of an op amp for gain control, provided that the voltage across Terminal A and Terminal B, Terminal W and Terminal A, or Terminal W and Terminal B does not exceed |5 V|. When high voltage gain is needed, users should set a fixed gain in an op amp operated at high voltage and let the digital potentiometer control the adjustable input. Figure 48 shows a simple implementation.

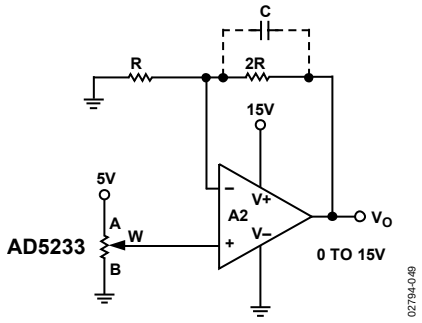

Figure 48. 5 V Voltage Span Control

Similarly, a compensation capacitor, C, might be needed to dampen the potential ringing when the digital potentiometer changes steps. This effect is prominent when stray capacitance at the inverted node is augmented by a large feedback resistor. Usually, a capacitor (C) of a few picofarads, is adequate to combat the problem.

DAC

Figure 49 shows a unipolar 8-bit DAC using the AD5233. The buffer is needed to drive various loads.

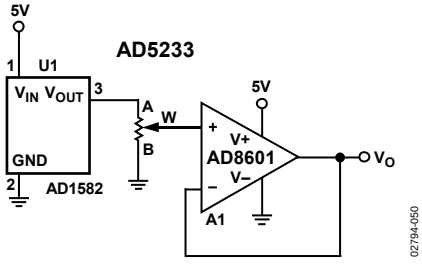

Figure 49. Unipolar 8-Bit DAC

BIPOLAR PROGRAMMABLE GAIN AMPLIFIER

There are several ways to achieve bipolar gain. Figure 50 shows one versatile implementation. Digital potentiometer, U1, sets the adjustment range; therefore, the wiper voltage, V_{W2}, can be programmed between V_i and $-KV_i$ at a given U2 setting.

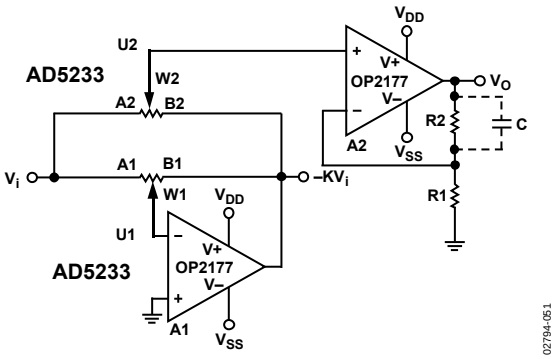

Figure 50. Bipolar Programmable Gain Amplifier

Configuring A2 as a noninverting amplifier yields a linear transfer function:

$$\frac{V_O}{V_i} = \left(1 + \frac{R2}{R1}\right) \times \left(\frac{D2}{64} \times (1 + K) - K\right) \quad (4)$$

where:
K is the ratio of R_{WB}/R_{WA} that is set by U1.
D is the decimal equivalent of the input code.

In the simpler (and much more usual) case where K is 1, a pair of matched resistors can replace U1. Equation 4 can be simplified to

$$\frac{V_O}{V_i} = \left(1 + \frac{R2}{R1}\right) \times \left(\frac{2D_2}{64} - 1\right) \quad (5)$$

Table 19 shows the result of adjusting D with A2 configured as a unity gain, a gain of 2, and a gain of 10. The result is a bipolar amplifier with linearly programmable gain and 64-step resolution.

Table 19. Result of Bipolar Gain Amplifier

D	R1 = ∞, R2 = 0	R1 = R2	R2 = 9 × R1
0	−1	−2	−10
16	−0.5	−1	−5
32	0	0	0
48	0.5	1	5
63	0.968	1.937	9.680

PROGRAMMABLE LOW-PASS FILTER

The AD5233 digital potentiometer can be used to construct a second-order Sallen-Key low-pass filter, as shown in Figure 51.

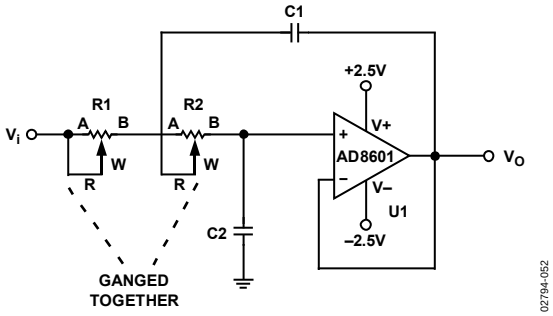

Figure 51. Sallen-Key Low-Pass Filter

The design equations are

$$\frac{V_O}{V_i} = \frac{\omega_O{}^2}{S^2 + \frac{\omega_O}{Q}S + \omega_O{}^2} \quad (6)$$

$$\omega_O = \sqrt{\frac{1}{R1 \times R2 \times C1 \times C2}} \quad (7)$$

$$Q = \frac{1}{R1 \times C1} + \frac{1}{R2 \times C2} \quad (8)$$

where:
Q is the Q factor.
V_O is the resonant frequency.
$R1$ and $R2$ are R_{WB1} and R_{WB2}, respectively.

To achieve maximal flat bandwidth where Q is 0.707, let C1 be twice the size of C2 and let R1 equal R2. Users can first select convenient values for the capacitors and then gang and move R1 and R2 together to adjust the −3 dB corner frequency. Instruction 5, Instruction 7, Instruction 13, and Instruction 15 of the AD5233 make these changes simple to implement.

PROGRAMMABLE STATE-VARIABLE FILTER

One of the standard circuits used to generate a low-pass, high-pass, or band-pass filter is the state-variable active filter. The AD5233 digital potentiometer allows full programmability of the frequency, the gain, and the Q of the filter outputs. Figure 52 shows a filter circuit using a 2.5 V virtual ground, which allows a ±2.5 V peak input and output swing. RDAC2 and RDAC3 set the low-pass, high-pass, and band-pass cutoff and center frequencies, respectively. RDAC2 and RDAC3 should be programmed with the same data (as with ganged potentiometers) to maintain the best Circuit Q.

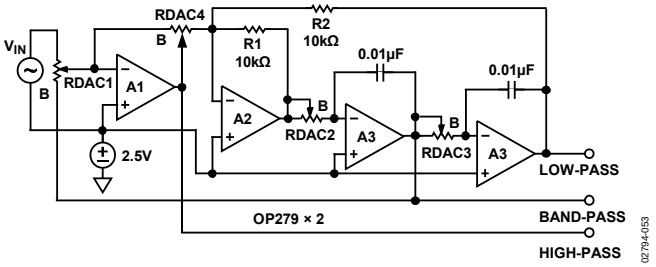

Figure 52. Programmable Stable-Variable Filter

The transfer function of the band-pass filter is

$$\frac{V_{BP}}{V_i} = \frac{A_O \frac{\omega_O}{Q} S}{S^2 + \frac{\omega_O}{Q} S + \omega_O{}^2} \quad (9)$$

where A_O is the gain.

For $R_{WB2(D2)} = R_{WB3(D3)}$, R1 = R2, and C1 = C2:

$$\omega_O = \frac{1}{R_{WB2} C1} \quad (10)$$

$$A_O = \frac{R_{WB1}}{R_{WA1}} \quad (11)$$

$$Q = \frac{R_{WA4}}{R_{WB4}} \times \frac{R_{WB1}}{R1} \quad (12)$$

Figure 53 shows the measured filter response at the band-pass output as a function of the RDAC2 and RDAC3 settings, which produce a range of center frequencies from 2 kHz to 20 kHz. The filter gain response at the band-pass output is shown in Figure 54. At a center frequency of 2 kHz, the gain is adjusted over the −20 dB to +20 dB range, determined by RDAC1. Circuit Q is adjusted by RDAC4 and RDAC1. Suitable op amps for this application are OP4177, AD8604, OP279, and AD824.

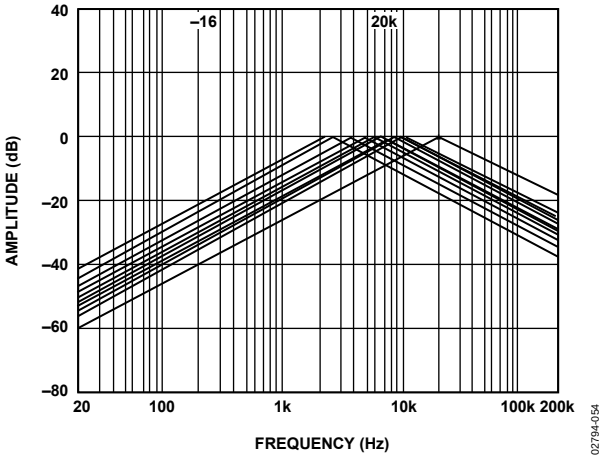

Figure 53. Programmed Center Frequency Band-Pass Response

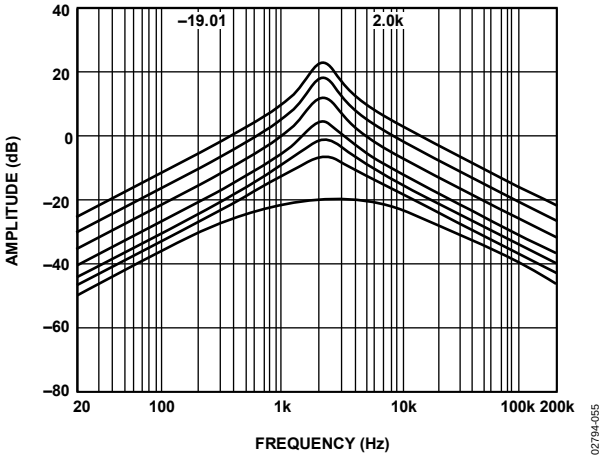

Figure 54. Programmed Amplitude Band-Pass Response

PROGRAMMABLE OSCILLATOR

In a classic Wien-bridge oscillator, shown in Figure 55, the Wien network (R, R′, C, C′) provides positive feedback, while R1 and R2 provide negative feedback. At the resonant frequency, f_O, the overall phase shift is zero, and the positive feedback causes the circuit to oscillate. If the op amp is chosen with a relatively high gain bandwidth product, the frequency response of the op amp can be neglected.

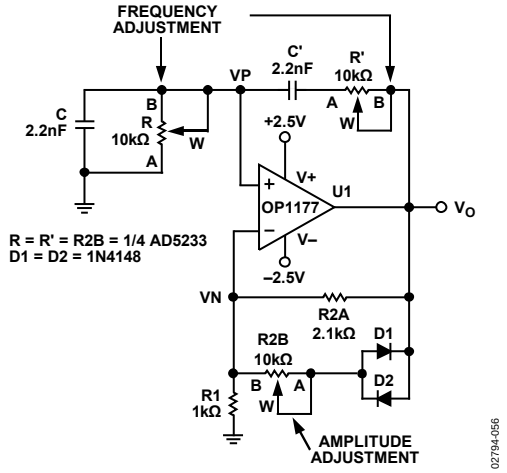

Figure 55. Programmable Oscillator with Amplitude Control

With R = R′, C = C′, and R2 = R2A||(R2B + R_{DIODE}), the oscillation frequency is

$$\omega_O = \frac{1}{RC} \text{ or } f_O = \frac{1}{2\pi RC} \quad (13)$$

where *R* is equal to R_{WA} such that

$$R = \frac{64 - D}{64} R_{AB} \quad (14)$$

At resonance, setting

$$\frac{R2}{R1} = 2 \quad (15)$$

balances the bridge. In practice, R2/R1 should be set slightly larger than 2 to ensure that the oscillation can start. On the other hand, the alternate turn-on of the diodes, D1 and D2, ensures that R1/R2 is smaller than 2 momentarily and, therefore, stabilizes the oscillation.

Once the frequency is set, the oscillation amplitude can be turned on by R2B, because

$$\frac{2}{3} V_O = I_D R2B + V_D \quad (16)$$

where V_O, I_D, and V_D are interdependent variables.

With proper selection of R2B, an equilibrium is reached such that V_O converges. R2B can be in series with a discrete resistor to increase the amplitude, but the total resistance cannot be too large or it saturates the output. In this configuration, R2B can be adjusted from minimum to full scale with amplitude varied from ±0.6 V to ±0.9 V. Using 2.2 nF for C and C′, 10 kΩ dual digital potentiometer, with R and R′ set to 8.06 kΩ, 4.05 kΩ, and 670 Ω, oscillation occurs at 8.8 kHz, 17.6 kHz, and 102 kHz, respectively (see Figure 56).

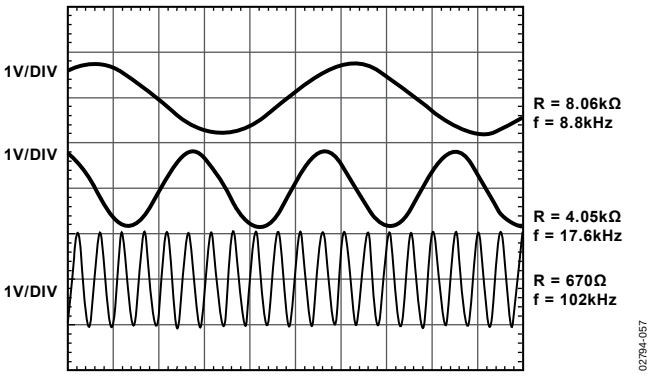

Figure 56. Programmable Oscillation

In both circuits (shown in Figure 51 and Figure 55), the frequency tuning requires that both RDACs be adjusted to the same settings. Because the two channels might be adjusted one at a time, an intermediate state occurs that might not be acceptable for some applications. Of course, the increment/decrement all instructions (5, 7, 13, and 15) can be used. Different devices can also be used in daisy-chain mode so that parts can be programmed to the same setting simultaneously.

PROGRAMMABLE VOLTAGE SOURCE WITH BOOSTED OUTPUT

For applications that require high current adjustment, such as a laser diode driver or tunable laser, a boosted voltage source can be considered (see Figure 57).

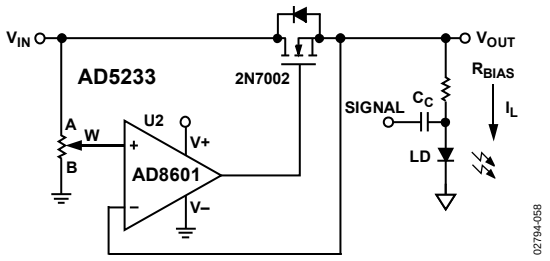

Figure 57. Programmable Boosted Voltage Source

In this circuit, the inverting input of the op amp forces the V_{OUT} to be equal to the wiper voltage set by the digital potentiometer. The load current is then delivered by the supply via the N-channel FET N_1. N_1 power handling must be adequate to dissipate (V_i – V_O) × I_L power. This circuit can source a maximum of 100 mA with a 5 V supply.

For precision applications, a voltage reference such as ADR421, ADR03, or ADR370 can be applied at Terminal A of the digital potentiometer.

PROGRAMMABLE CURRENT SOURCE

A programmable current source can be implemented with the circuit shown in Figure 58.

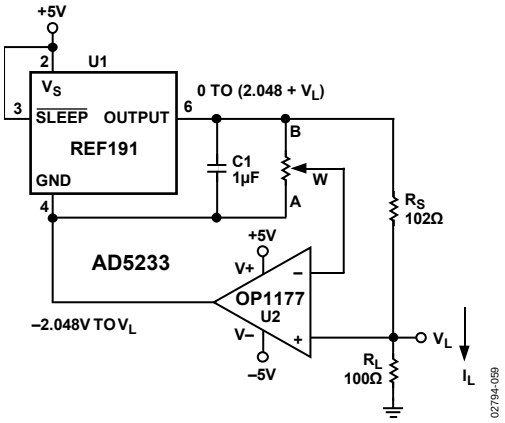

Figure 58. Programmable Current Source

REF191 is a unique low supply headroom precision reference that can deliver the 20 mA needed at 2.048 V. The load current is simply the voltage across Terminal B to Terminal W of the digital potentiometer divided by R_S.

The circuit is simple, but be aware that there are two issues. First, dual-supply op amps are ideal, because the ground potential of REF191 can swing from −2.048 V at zero scale to V_L at full scale of the potentiometer setting. Although the circuit works under single supply, the programmable resolution of the system is reduced. Second, the voltage compliance at V_L is limited to 2.5 V or equivalently a 125 Ω load. If higher voltage compliance is needed, users can consider digital potentiometers AD5260, AD5280, and AD7376. Figure 58 shows an alternative circuit for high voltage compliance.

To achieve higher current, such as when driving a high power LED, the user can replace the U1 with an LDO, reduce R_S, and add a resistor in series with the AD5233's A terminal. This limits the potentiometer's current and enhances the current adjustment resolution.

PROGRAMMABLE BIDIRECTIONAL CURRENT SOURCE

For applications that require bidirectional current control or higher voltage compliance, a Howland current pump can be used (see Figure 59).

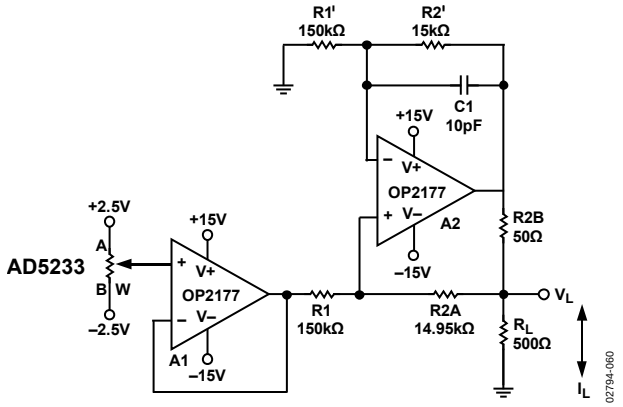

Figure 59. Programmable Bidirectional Current Source

If the resistors are matched, the load current is

$$I_L = \frac{\frac{(R2A + R2B)}{R1}}{R2B} \times V_W \quad (17)$$

R2B, in theory, can be made as small as necessary to achieve the current needed within the A2 output current-driving capability. In this circuit, OP2177 delivers ±5 mA in both directions, and the voltage compliance approaches 15 V. Without C1, it can be shown that the output impedance is

$$Z_O = \frac{R1' \times R2B\,(R1 + R2A)}{R1 \times R2' - R1'\,(R2A + R2B)} \quad (18)$$

Z_O can be infinite if the R1′ and R2′ resistors match precisely with *R1* and R2A + R2B, respectively. On the other hand, Z_O can be negative if the resistors are not matched. As a result, C1 in the range of 1 pF to 10 pF is needed to prevent oscillation from the negative impedance.

RESISTANCE SCALING

AD5233 offers 10 kΩ, 50 kΩ, and 100 kΩ nominal resistance. Users who need lower resistance but want to maintain the number of adjustment steps can parallel multiple devices. For example, Figure 60 shows a simple scheme of paralleling two AD5233 channels. To adjust half the resistance linearly per step, users need to program both devices concurrently with the same settings.

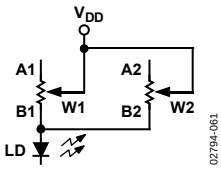

Figure 60. Reduce Resistance by Half with Linear Adjustment Characteristics

In voltage divider mode, by paralleling a discrete resistor as shown in Figure 61, a proportionately lower voltage appears at Terminal A to Terminal B. This translates into a finer degree of precision because the step size at Terminal W is smaller.

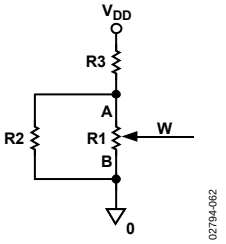

Figure 61. Lowering the Nominal Resistance

The voltage can be found as follows:

$$V_W(D) = \frac{(R_{AB} \,||\, R_2)}{R_3 + R_{AB} \,||\, R_2} \times \frac{D}{64} \times V_{DD} \quad (19)$$

Figure 60 and Figure 61 show that the digital potentiometer steps change linearly. On the other hand, log taper adjustment is usually preferred in applications such as audio control. Figure 62 shows another type of resistance scaling. In this configuration, the smaller the R2 with respect to R1, the more the pseudo log taper characteristic of the circuit behaves.

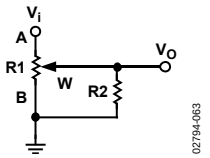

Figure 62. Resistor Scaling with Pseudo Log Adjustment Characteristics

DOUBLING THE RESOLUTION

Borrowing from Analog Devices' patented RDAC segmentation technique, the user can configure three channels of AD5233, as shown in Figure 63. By paralleling a discrete resistor, R_P ($R_P = R_{AB}/64$), with RDAC3, the user can double the resolution of AD5233 from 6 bits to 12 bits. One might think that moving RDAC1 and RDAC2 together would form the coarse 6-bit resolution, and then moving RDAC3 would form the finer 6-bit resolution. As a result, the effective resolution would become 12 bits. However, the precision of this circuit remains only 6-bit accurate and the programming can be complicated.

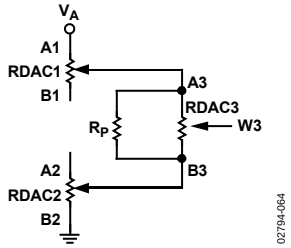

Figure 63. Doubling AD5233 from 6 Bits to 12 Bits

RESISTANCE TOLERANCE, DRIFT, AND TEMPERATURE MISMATCH CONSIDERATIONS

In a rheostat mode operation such as gain control (see Figure 64), the tolerance mismatch between the digital potentiometer and the discrete resistor can cause repeatability issues among various systems. Because of the inherent matching of the silicon process, it is practical to apply the dual- or multiple-channel device in this type of application. As such, R1 can be replaced by one of the channels of the digital potentiometer and programmed to a specific value. R2 can be used for the adjustable gain. Although it adds cost, this approach minimizes the tolerance and temperature coefficient mismatch between R1 and R2. This approach also tracks the resistance drift over time. As a result, all nonideal parameters become less sensitive to the system variations.

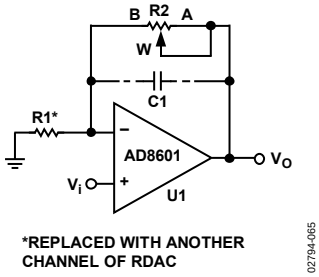

Figure 64. Linear Gain Control with Tracking Resistance Tolerance and Temperature Coefficient

RDAC CIRCUIT SIMULATION MODEL

The internal parasitic capacitances and the external load dominate the ac characteristics of the RDACs. Configured as a potentiometer divider, the −3 dB bandwidth of the AD5233 (10 kΩ resistor) measures 370 kHz at half scale. Figure 14 provides the large signal bode plot characteristics. A parasitic simulation model is shown in Figure 65.

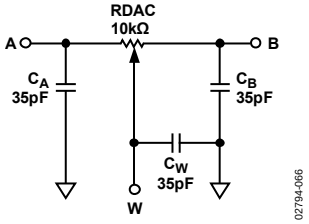

Figure 65. RDAC Circuit Simulation Model for RDAC = 10 kΩ

The following code provides a macromodel net list for the 10 kΩ RDAC:

```
Listing I. spice model net list
.PARAM D = 64, RDAC = 10E3
*
.SUBCKT DPOT (A, W, B)
*
CA   A   0   35E-12
RWA  A   W   {(1-D/64)* RDAC + 15}
CW   W   0   35-12
RWB  W   B   {D/64 * RDAC + 15}
CB   B   0   35E-12
*
.ENDS DPOT
```

OUTLINE DIMENSIONS

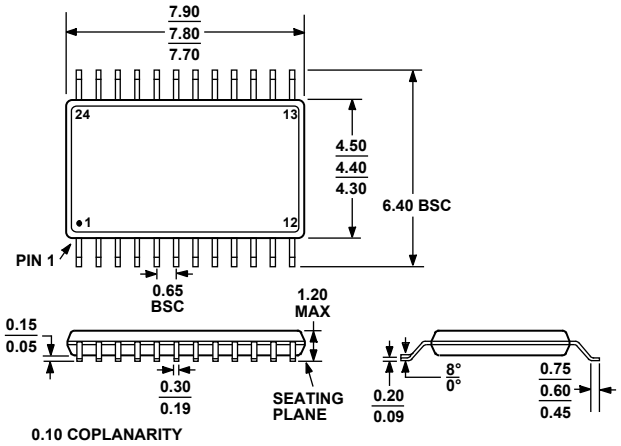

Figure 66. 24-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-24)
Dimensions shown in millimeters

ORDERING GUIDE

Model	No. of Channels	R_{AB} (kΩ)	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding[1]
AD5233BRU10	4	10	−40°C to +85°C	24-Lead TSSOP	RU-24	96	5233B10
AD5233BRU10-REEL7	4	10	−40°C to +85°C	24-Lead TSSOP	RU-24	1,000	5233B10
AD5233BRUZ10[2]	4	10	−40°C to +85°C	24-Lead TSSOP	RU-24	96	5233B10
AD5233BRUZ10-R7[2]	4	10	−40°C to +85°C	24-Lead TSSOP	RU-24	1,000	5233B10
AD5233BRU50	4	50	−40°C to +85°C	24-Lead TSSOP	RU-24	96	5233B50
AD5233BRU50-REEL7	4	50	−40°C to +85°C	24-Lead TSSOP	RU-24	1,000	5233B50
AD5233BRUZ50[2]	4	50	−40°C to +85°C	24-Lead TSSOP	RU-24	96	5233B50
AD5233BRUZ50-R7[2]	4	50	−40°C to +85°C	24-Lead TSSOP	RU-24	1,000	5233B50
AD5233BRU100	4	100	−40°C to +85°C	24-Lead TSSOP	RU-24	96	5233B100
AD5233BRU100-REEL7	4	100	−40°C to +85°C	24-Lead TSSOP	RU-24	1,000	5233B100
AD5233BRUZ100[2]	4	100	−40°C to +85°C	24-Lead TSSOP	RU-24	96	5233B100
AD5233BRUZ100-R7[2]	4	100	−40°C to +85°C	24-Lead TSSOP	RU-24	1,000	5233B100

[1] Line 1 contains the model number. Line 2 contains the Analog Devices logo followed by the end-to-end resistance value. Line 3 contains the date code, YWW or #YWW, for RoHS compliant parts.
[2] Z = RoHS Compliant Part.

NOTES

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D02794-0-5/08(B)

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