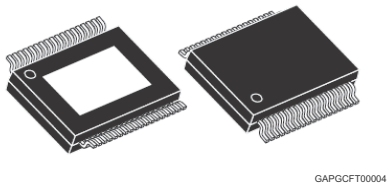
L99SD01-E

Integrated solenoid driver for automotive applications

Datasheet - production data



PowerSSO-36

Features

- Automotive qualified
- Excitation switch S_1 = 60 mΩ
- Recirculation switch S_2 = 60 mΩ
- CMOS compatible inputs
- Load current up to 14 A
- Integrated clamp structure
  - Switch S_1 clamp voltage = 45 V (minimum)
- Current sense amplifier with internal sense resistor
- S_1 switch PWM operation above 10 KHz
- I^2C standard interface for mode control and enhanced diagnostic
- Diagnostic output:
  - Open drain fault detection
  - Flag of clamp activation at the end of injection cycle
- Input for voltage monitoring and feedback
- Thermal shutdown and warning
- Overcurrent shutdown and diagnostic
- Undervoltage and overvoltage detection
- Open-load detection

Description

The L99SD01-E is a device intended for driving inductive loads such as Compressed Natural Gas (CNG) injectors.

The inputs are CMOS-compatible. The diagnostic outputs CLAMP_FLAG and FAULT provide an indication of demagnetization mode and fault conditions, respectively.

The integrated standard serial interface (I^2C) allows to digitally set peak and hold current values and other injection parameters. It also provides detailed diagnostic information. The device should work with pre-programmed peak and hold current values when values are not set by external micro. All injection parameters can be changed during operating conditions and taken into account at the first injection rising edge after the end of communication. Diagnostic information is available in case of overcurrent, overtemperature, overvoltage and open-load.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-36	L99SD01-E	L99SD01TR-E

Contents

List of tables

List of figures

1 Block diagram and pin description

Figure 1. Block diagram

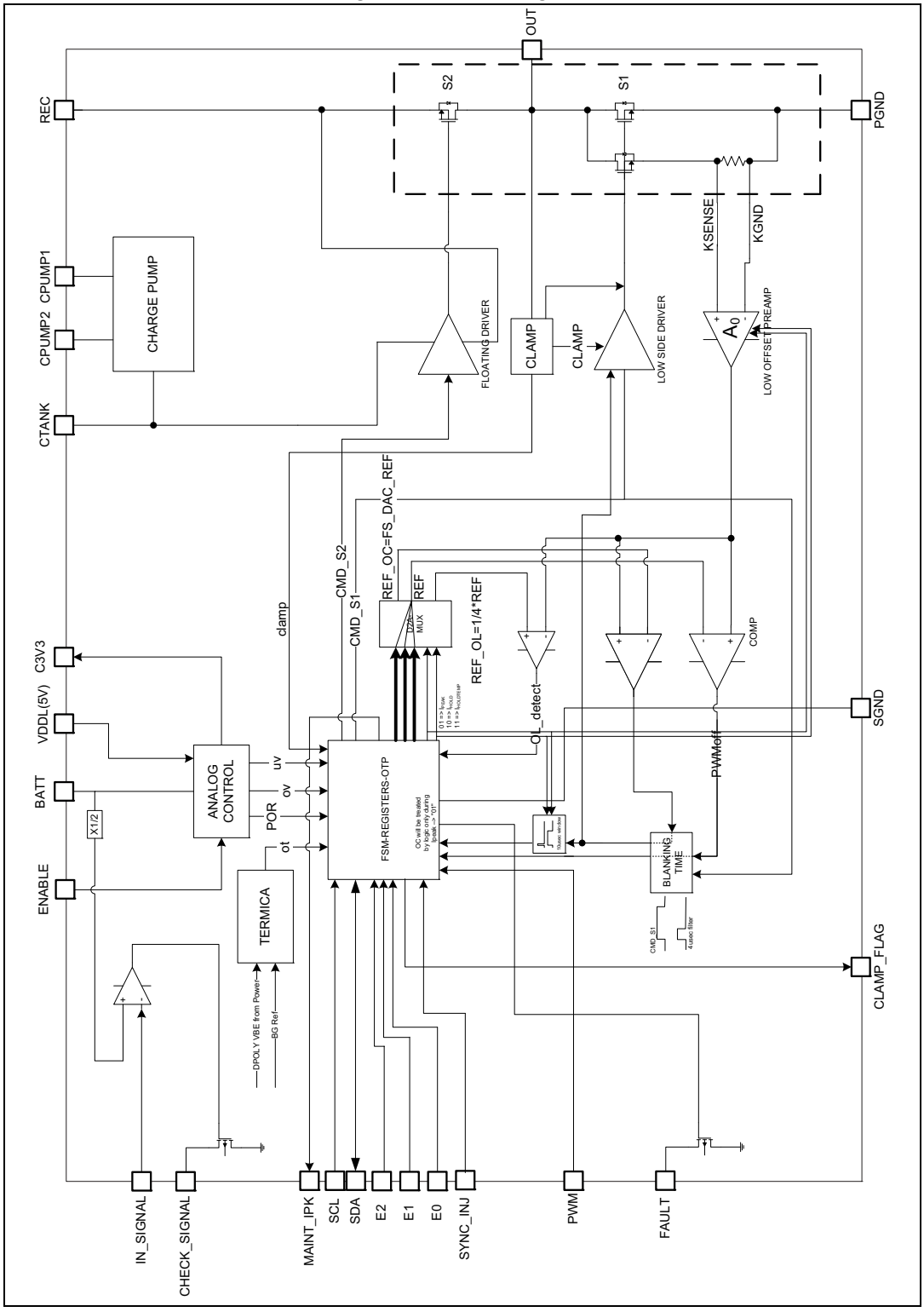


Table 2. Pin description

Pin number	Pin name	Description
1	OTP_15V	Power supply for OTP test purposes. Not connected.
2	IN_SIGNAL	This pin is used to acquire (through an external resistor) the signal coming from the Main ECU

3	CHECK_SIGNAL	The voltage on the “IN_SIGNAL” pin is compared with $V_{BATT}/2$:
		`IF IN_SIGNAL > Vbatt/2 then CHECK_SIGNAL = H`
		`IF IN_SIGNAL <= Vbatt/2 then CHECK_SIGNAL = L`

4	MAINT_IPK	Diagnostic pin going high when device is regulating Ipeak current value
5	CLAMP_FLAG	Reporting the CLAMP intervention and the end of injection cycle
6	SDA	I^2C serial interface data line
7	SCL	I^2C serial interface clock line (100 kHz)
8	FAULT	The FAULT pin is pulled low whenever a fault condition is detected.
9	PWM	External PWM clock
10	SYNC_INJ	It is used for injection synchronization and to set the single injection duration.
11	ENABLE	This pin is used to enable/disable the device. When low, device enters standby low consumption mode
12	TEST	Test activation. Not connected.
13	TEST_OUT3	Pin for test purposes. Not connected
14	SGND	Signal ground pin. Do not connect to ground module. Use for local capacitor connection
15-18	PGND	Power ground pin
19-22	REC	Recirculation path – the external recirculation diode is connected between this pin and battery.
23	TEST_OUT2	Pin for test purposes. Not connected
24	TEST_OUT1	Pin for test purposes. Not connected
25	BATT	Power supply voltage
26	CPUMP1	Charge pump pin for external capacitor connection
27	CPUMP2	Charge pump pin for external capacitor connection
28	CTANK	Supply voltage for high side driver
29	VDDL	5 V external supply voltage
30	C3V3	3.3 V supply pin for external capacitor connection
31	SGND	Signal ground pin. Do not connect to ground module. Use for local capacitor connection
32	E0	Address pin externally hard wired to ground or VDDL to address till 8 devices in parallel
33	E1	Address pin externally hard wired to ground or VDDL to address till 8 devices in parallel

Table 2. Pin description (continued)

Pin number	Pin name	Description
34	E2	Address pin externally hard wired to ground or VDDL to address till 8 devices in parallel
35	SGND	Signal ground pin. Do not connect to ground module. Use for local capacitor connection
36	OTP_0V	Power ground for OTP test purposes. Not connect
Tab	OUT	Excitation path – the injector is connected between battery and this pin

2 Injection cycle description

Figure 2 includes the main waveforms showing a typical injection cycle while *Figure 3* shows typical load connection and recirculation diode.

Figure 2. Waveforms

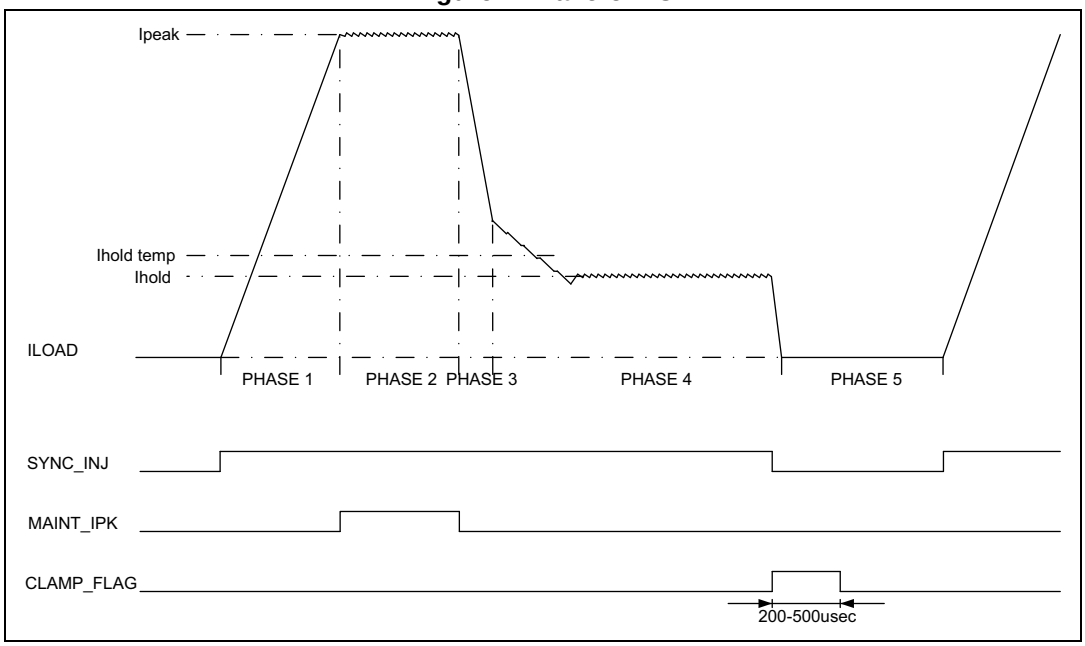
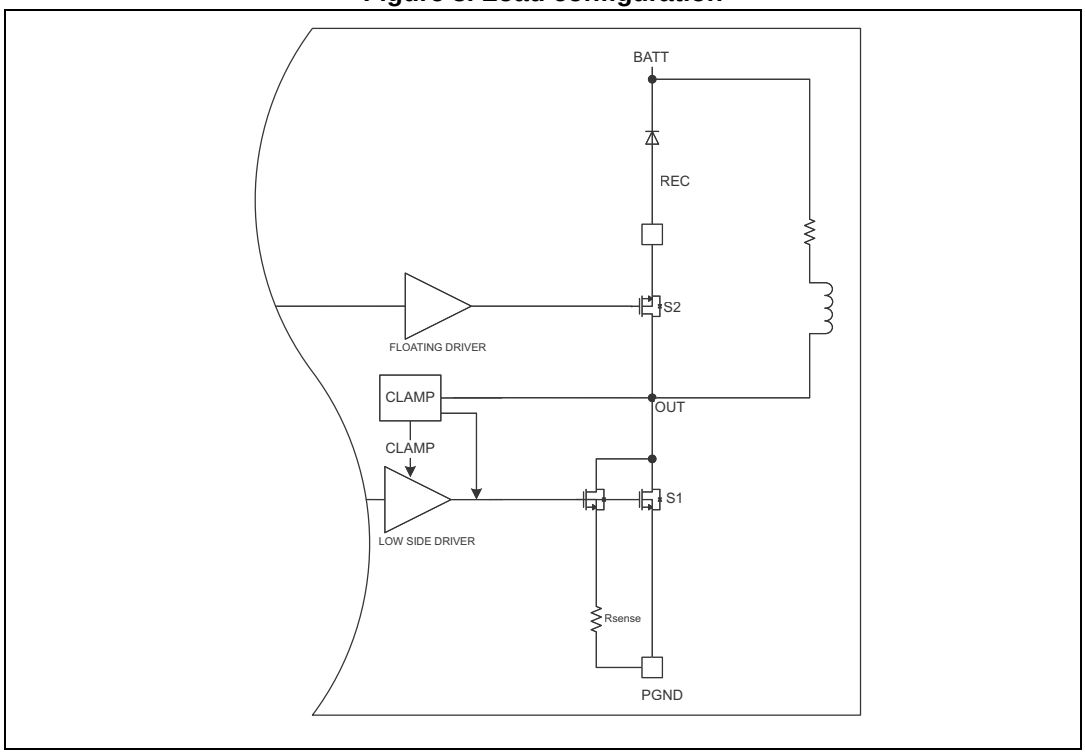


Figure 3. Load configuration



2.1 Phase 1

Injection phase starts by closing S_1 switch when there is a rising edge of SYNC_INJ signal. During this phase current on injector rises till an I_{PEAK} value set in the register A. If current doesn't reach I_{PEAK} value within a maximum time fixed in register H, the device status switches from phase 1 to phase 2.

2.2 Phase 2

If current hasn't still reached I_{PEAK} value S_1 switch continues to be ON and current continues to flow through load during all phase 2 whose length is set in register B. As soon as current reaches I_{PEAK} value it will be regulated in PWM mode at this value. PWM frequency is fixed by external clock via PWM pin.

Current is controlled by shutting-down S_1 when current reaches I_{PEAK} value. During the remaining period injector current is re-circulating through S_2 switch which should be always closed during phase 1 and phase 2. We speak about slow-recirculation during this phase.

Pin MAINT_IPK should be kept high (5 V) when current has reached and is regulated around I_{PEAK} value.

2.3 Phase 3

This is the temporary phase to go from I_{PEAK} to I_{HOLD} value. During this phase S_1 is open. Register C sets the time length of this phase. Register D sets the recirculation mode:

- Slow recirculation: S_2 closed.
- Fast recirculation: S_2 open and clamp on S_1 activated.

A particular case is when at the end of phase 2 current has not reached I_{PEAK} value yet. In this case device will go to phase 3 in slow recirculation mode whatever the value set in register D.

2.4 Phase 4

During this phase current is controlled to I_{HOLD} value. During this phase S_2 is always closed. Register E sets I_{HOLD} current value. Current is controlled by shutting-down S_1 when current reaches I_{HOLD} value. Recirculation is slow because S_2 is closed during this phase.

PWM clock signal is given externally on pin PWM.

This phase starts at the end of phase 3 when current on injector has slowed down but not below the holding value. For this reason at the beginning of this phase PWM duty cycle will be fixed by the minimum turn-on time of regulation loop, till the current reaches I_{HOLD} value.

This phase lasts till the end of injection given by the falling edge of SYNC_INJ signal. Shutting of injector is done by turning off S_1 and S_2. Fast recirculation happens through S_1 by clamp activation. CLAMP_FLAG is set to high value (5 V) during 350 µsec minimum. To minimize the current ripple during the passage from phase 3 to phase 4, a temporary hold value could be used for some PWM cycles. Register F sets this temporary hold current value, whilst Register G sets time length.

2.5 Phase 5

System is waiting for next injection cycle. No current is flowing through injector. Switches S_1 and S_2 are open.

End of injection cycle could happen everywhere during injection cycle. So device should sustain fast recirculation even during phase 2 with high current values.

If the time duration of one phase is set to zero then the corresponding phase should be skipped and device must enter the following phase.

All registers have pre-programmed values hard coded in the device. So device can operate as it is without needing of a first programming phase (for typical application). In all other applications first register writing is done automatically at the beginning of communication. All registers could be modified during the operating phase. Modified values are activated at the beginning of the first injection cycle following the end of the serial communication. Synchronization event is the rising edge of SYNC_INJ signal. In reset state all registers are cleared.

Enable pin allows device to enter standby mode with very low current consumption. Enable signal can be supplied directly by microcontroller.

Typical applications include 4 to 8 injectors which are driven via a microcontroller through a serial interface (I^2C). Each device is recognizable by a unique hard wired address code. Three pins are devoted to code up to 8 device addresses.

Each communication between microcontroller and each device is closed by an acknowledgment message. If this message does not arrive it means that something is not working in communication between microcontroller and L99SD01-E.

Figure 4. Registers (default values)

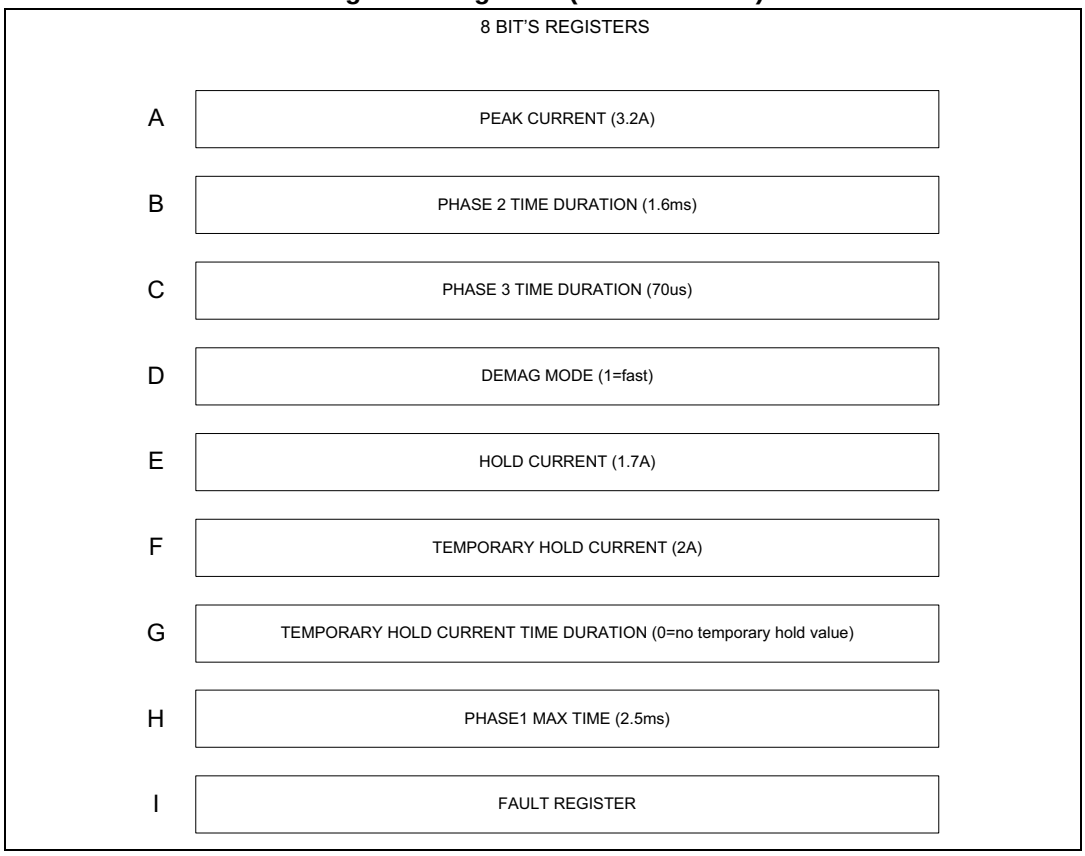
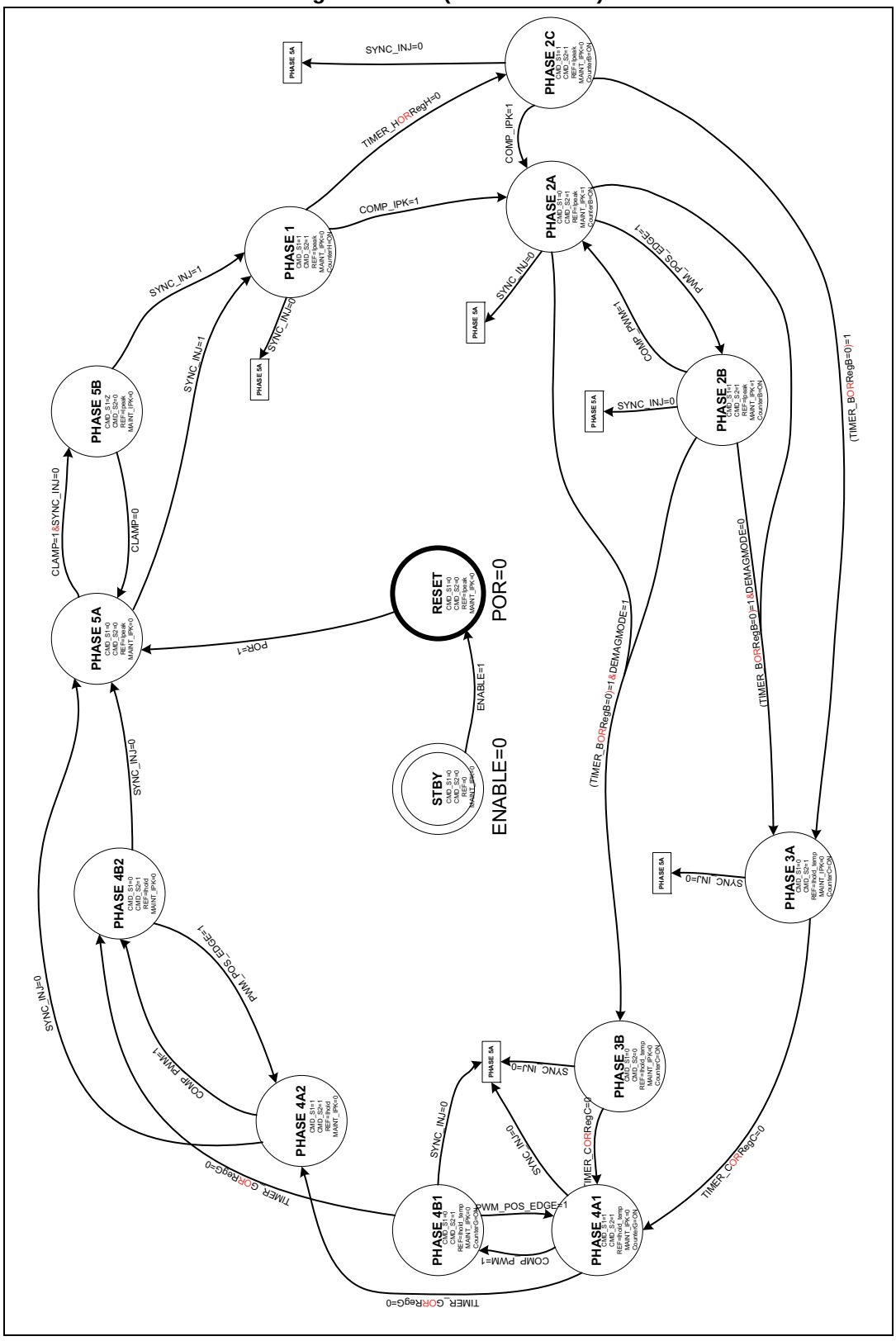


Figure 5. FSM (state machine)



3 Diagnostic

Device is auto-protected against some failures and is able to send the information fault to microcontroller via FAULT pin and serial communication line. The following table resumes all the fault conditions detected by the device and the corresponding device behavior.

Table 3. Diagnostic fault

Fault condition	Device behavior
THERMAL SHUTDOWN	Shutdown S_1 with slow recirculation (S_2 on). Fault pin low and fault register set. Device restarts when temperature slows down the reset value. Fault register reset by microcontroller.
THERMAL WARNING	Normal mode. Fault register set. Fault register reset by microcontroller. No action on Fault pin.
UNDERVOLTAGE	Normal mode. Fault pin low and fault register set. Fault register reset by microcontroller.
OVERVOLTAGE	Normal mode. Fault pin low and fault register set. Fault register reset by microcontroller.
OUTPUT SHORTED TO BATT(1)	Shut down immediately after minimum turn on time. Fault pin low and fault register set. To avoid false overcurrent detections, fault is latched in register only if happens during phase 1 or 2. In case of resistive short circuit, at the beginning of injection cycle current through load rises too fast and this will set as a short fault. Device couldn't restart until fault register is reset by microcontroller.
OPEN LOAD(2)	Normal mode. Fault pin low and fault register set. Fault register reset by microcontroller.

1. No internal current limiter. Response time of current limiter would be longer than shut-off time.
2. CHECK during PHASE 1. If max duration time of phase1 is reached (register H value) Open-load detection signal is read by control logic and validated.

Figure 6. Thermal protection

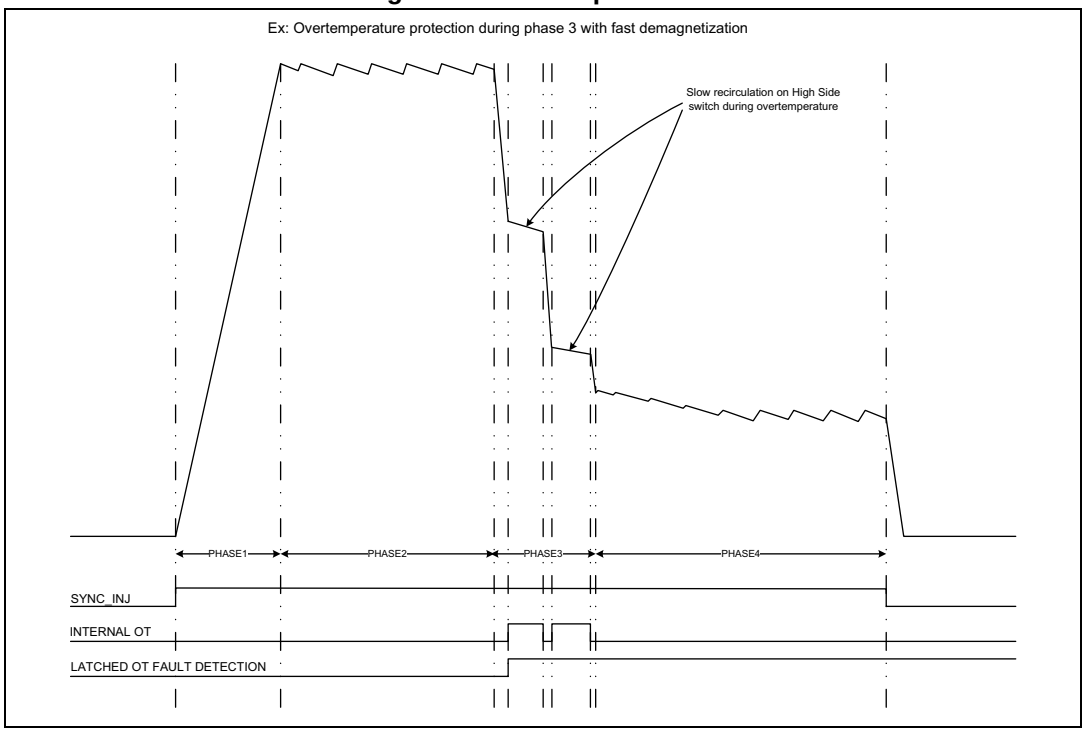


Figure 7. Short to battery protection

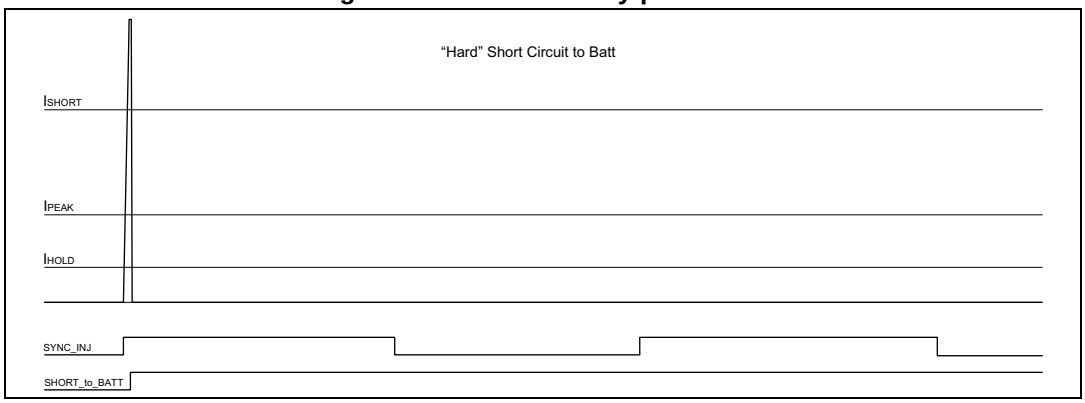


Figure 8. Soft short to battery protection

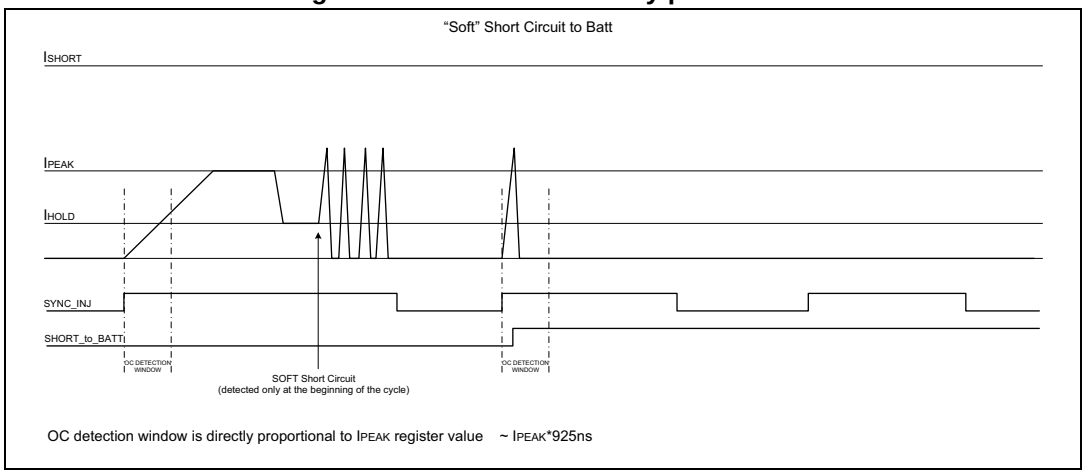
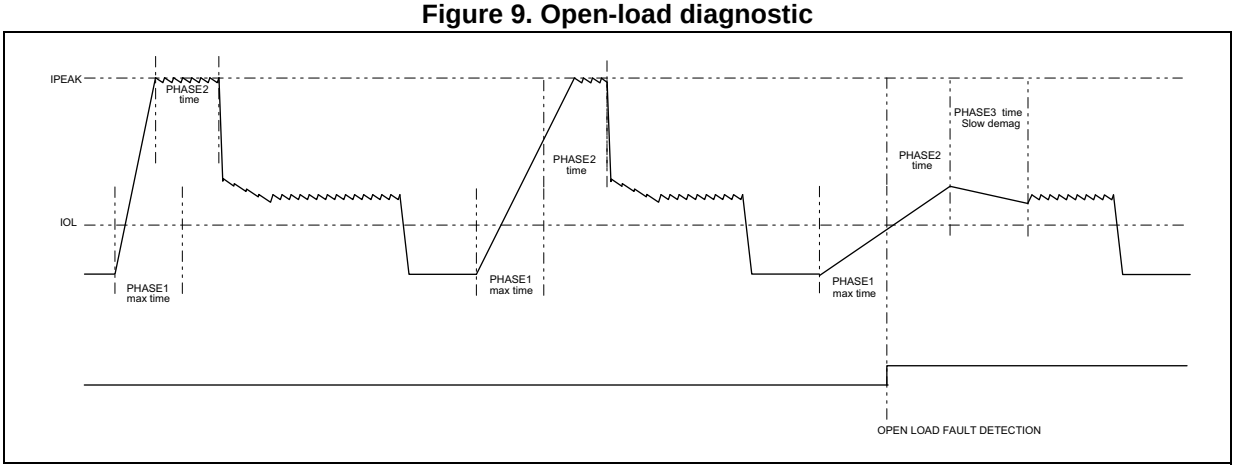


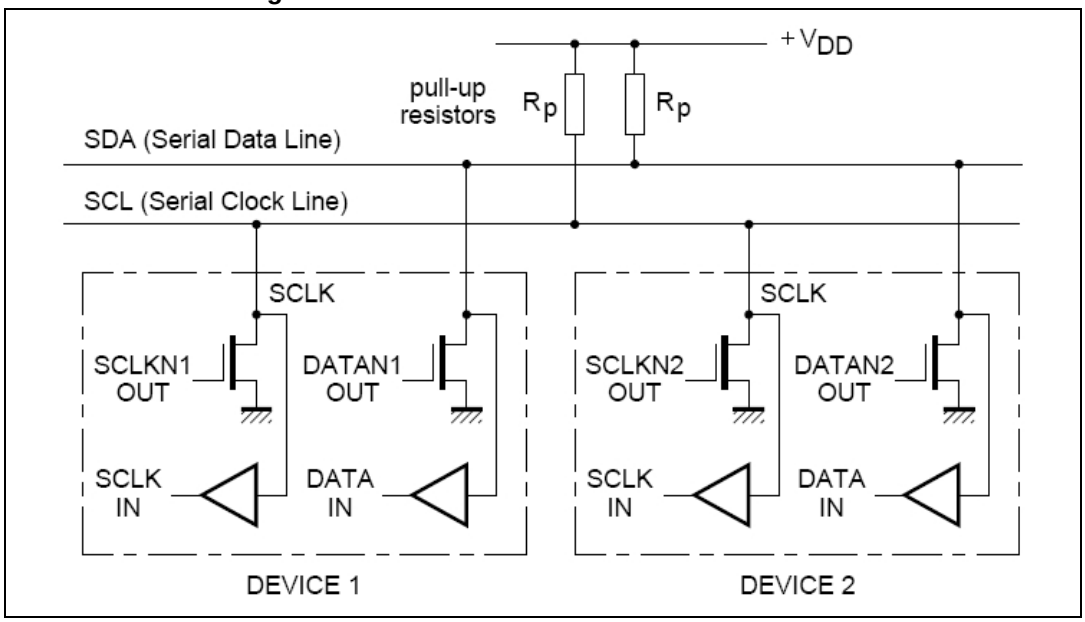
Figure 9. Open-load diagnostic



4 I²C protocol description

The L99SD01-E is compatible with the standard I²C serial bus. This is a two wire serial interface that uses a bi-directional data bus (SDA) and serial clock (SCL). Each device connected to the bus is recognized by a unique address (whether it is a microcontroller, memory or injector driver) and can operate as either a transmitter or receiver, depending on the function of the device. In addition to transmitters and receivers, devices can also be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave. L99SD01-E can only be a slave, transmitter or receiver, during communication.

Figure 10. Connection of I²C-devices to I²C-bus



4.1 SDA and SCL signals

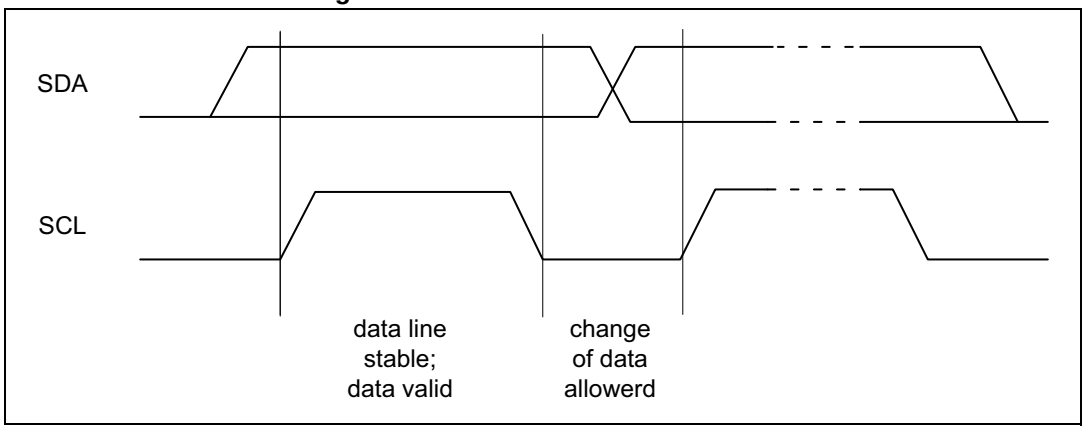
Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a current-source or pull-up resistor. When the bus is free, both lines are HIGH. The output stages of devices connected to the bus must have an open-drain or open-collector to perform the wired-AND function.

Data on the I²C bus can be transferred at rates up to 100 kbit/s in the standard-mode. The number of devices connected to the bus is limited by the max bus capacitance.

4.2 Data validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

Figure 11. Bit transfer on the I²C-bus



4.3 START and STOP conditions

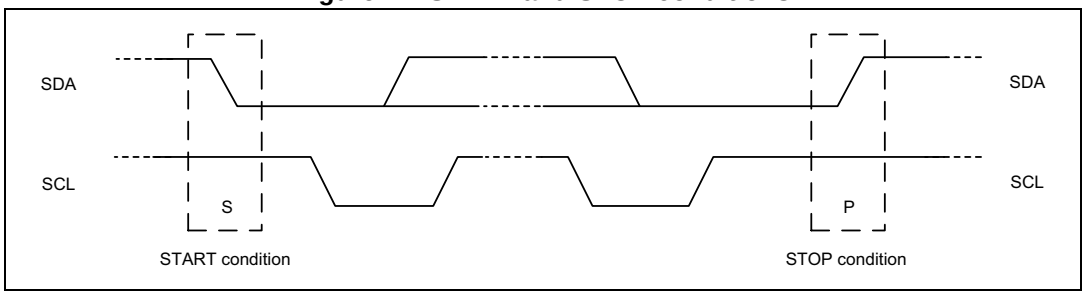
All transactions begin with a START (S) and can be terminated by a STOP (P).

A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after a STOP condition.

The bus stays busy if a repeated START (Sr) is generated instead of a STOP signal. In this respect, the START (S) and repeated START (Sr) conditions are functionally identical.

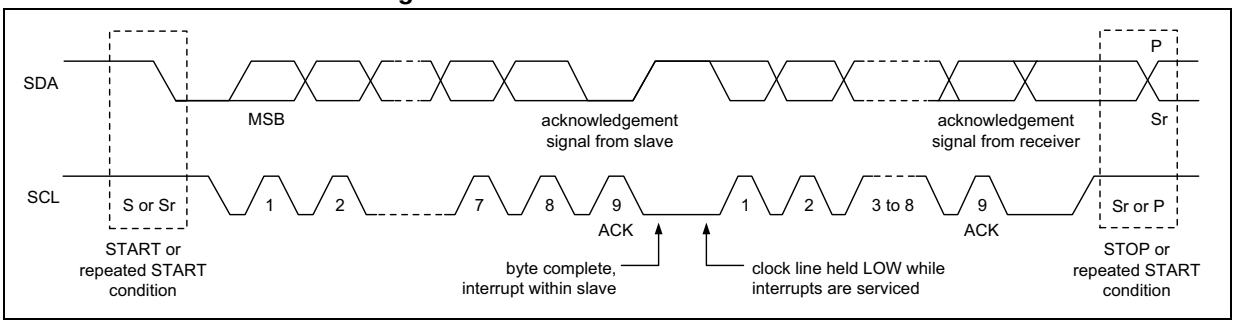
Figure 12. START and STOP conditions



4.4 Byte format

Every byte put on the SDA line must be 8 bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first.

Figure 13. Data transfer on the I²C-bus



4.5 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses including the acknowledge 9th clock pulse are generated by the master.

The acknowledge signal is defined as follows: the transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse. Setup and hold times must also be taken into account.

When the SDA remains HIGH during this 9th clock pulse, this is defined as the Not Acknowledge signal. The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

4.6 Device addressing

Data transfers follow the format shown in fig.10. After the START condition (S), a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/W). A ‘zero’ indicates a transmission (WRITE), a ‘one’ indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated START condition (Sr) and address another slave without first generating a STOP condition. Various combinations of read/write formats are then possible within such a transfer.

Figure 14. Complete data transfer

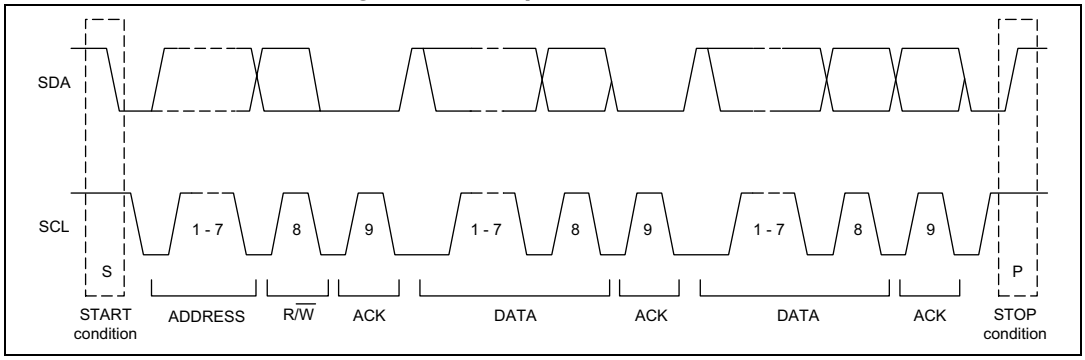
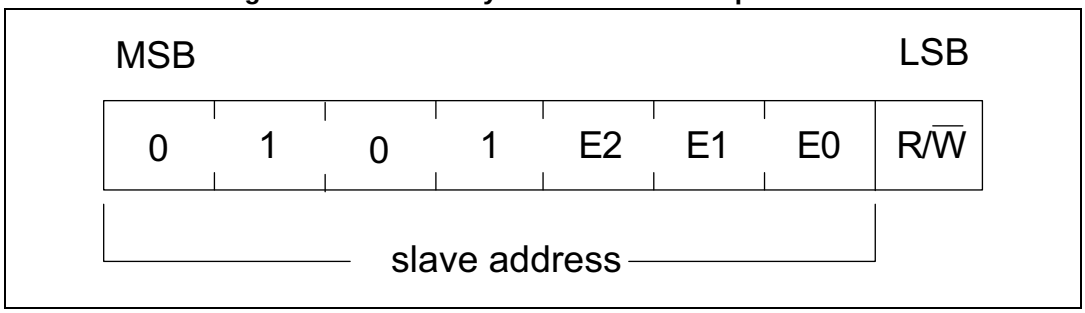


Figure 15. The first byte after the START procedure



4.7 Write operation

WRITE command in L99SD01-E is used to store data into volatile memory.

Master initiates a START condition (S) and then sends the first byte which is the slave address followed by the R/W= ‘0’. If L99SD01-E recognizes its address then it generates an ACK signal.

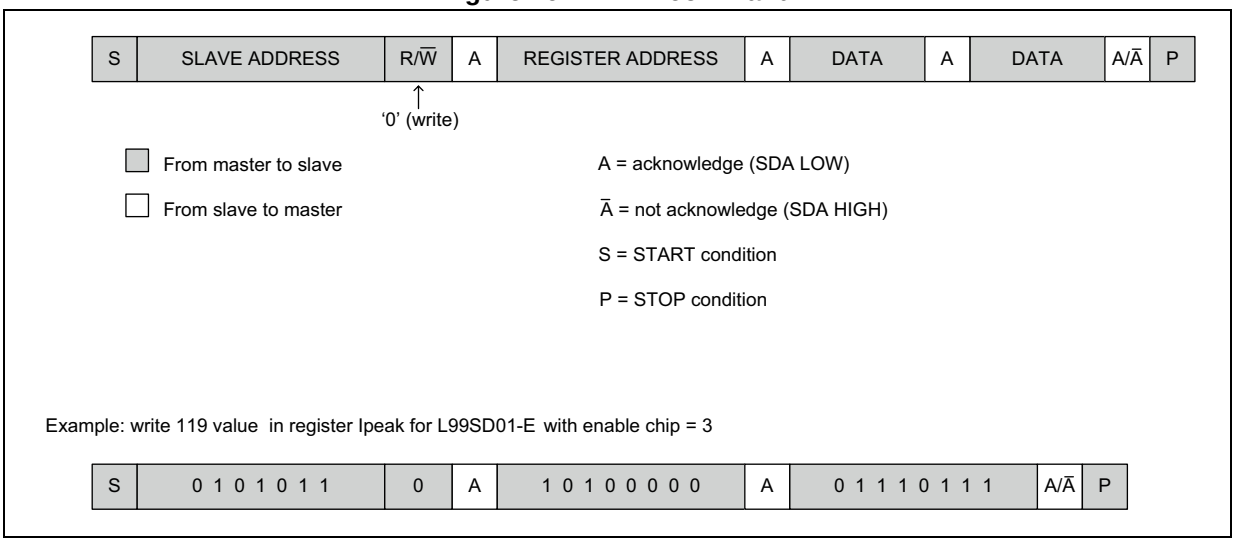
Each L99SD01-E has a different slave address. The first four bits of the address are the device type identifier and do not change for all L99SD01-E devices. The following three bits are used to address till 8 different L99SD01-E on the same bus.

Second byte sent by master in write mode is the register address where data must be written. After Acknowledge from slave, master starts to send the data, which can be one or more bytes. Eight different registers may be written in L99SD01-E. If more than eight data bytes are sent by the master, roll-over occurs.

The transfer finishes when master sends a STOP condition (P).

After the successful completion of write operations, the device internal address counter is incremented automatically, to point to the next byte address after the last one that was modified.

Figure 16. WRITE command



4.8 Read operation

READ command in L99SD01-E is used to read data contained into volatile memory. There are essentially two different Read operation modes: Current Read and Random Read.

In Random READ mode a dummy write is first performed to load the address into the address counter, then without sending a STOP condition, the Master sends another START condition, and repeats the slave address, with the R/W bit set to ‘1’ (READ). At this point slave acknowledges and starts sending data output from the addressed register. One or more bytes can be sent to master. L99SD01-E stops sending data when it receives a NACK signal from master. At this point master can decide to stop transmission by sending a STOP condition or to generate a repeated START condition to start communication with another slave. At the end of communication internal address counter is incremented automatically, to point to the next byte address after the last one that was read.

In Current READ mode, following a START condition, the master sends a slave address with a R/W bit set to ‘1’. At this point slave acknowledges and starts sending data output from the register addressed by the internal counter. One or more bytes can be sent to master. L99SD01-E stops sending data when it receives a NACK signal from master. At this point master can decide to stop transmission by sending a STOP condition or to generate a repeated START condition to start communication with another slave.

Figure 17. Current READ command

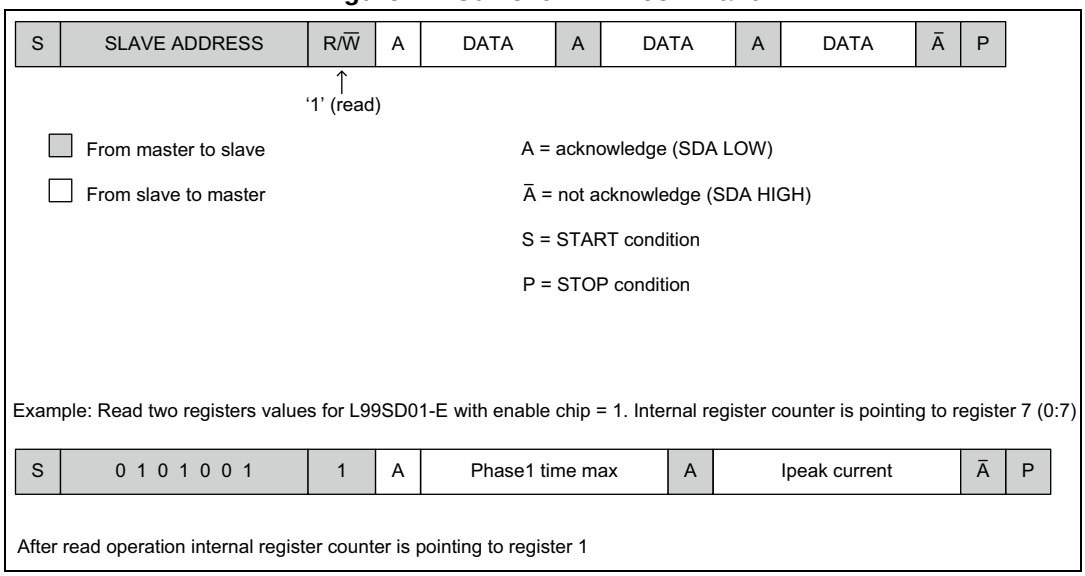
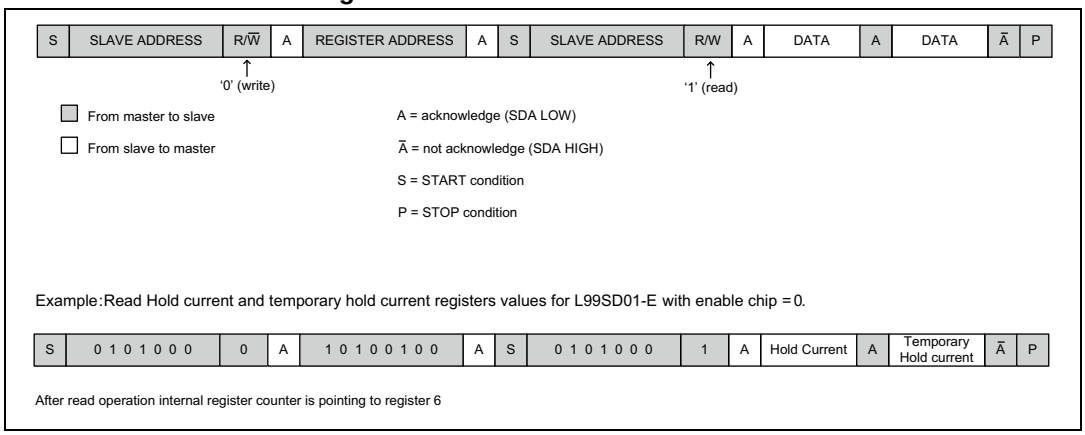


Figure 18. Random READ command



Besides the eight parameter registers, there is another eight bit register which corresponds to the fault register. It can only be reset and read via dedicated commands.

4.9 Registers Addresses and Fault register

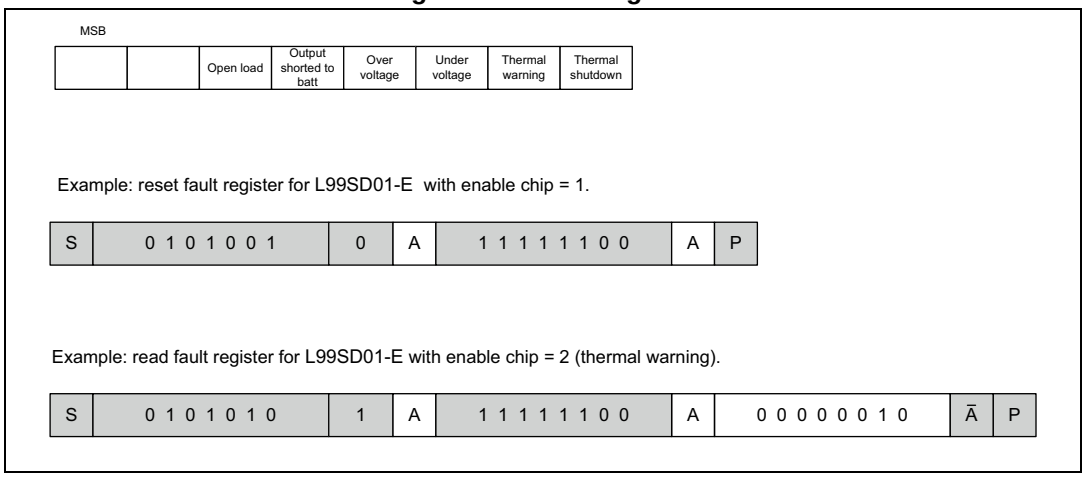
L99SD01-E does not need to be first configured via I²C-bus line. Default application parameters are hard-wired in the device. At first turn-on default application parameters are transferred inside registers which can be further modified by customer via I²C-bus if needed. In order to permit “real-time” parameter changes each register will have an equivalent temporary register to store the data until the first low-to-high transition on SYNC_INJ signal at the end of communication. At this time temporary registers are transferred into the actual parameter registers.

Each register can be read/written via serial interface. Fault register can be read and reset (fault cleared).

Table 4. Registers addresses

	Register address	Register content	Length	Access	Purpose
R0	1010 0000	I peak current	1 byte	R/W	Read/Store data
R1	1010 0001	Phase 2 duration	1 byte	R/W	Read/Store data
R2	1010 0010	Phase 3 duration	1 byte	R/W	Read/Store data
R3	1010 0011	Demag mod	1 byte	R/W	Read/Store data
R4	1010 0100	Hold Current	1 byte	R/W	Read/Store data
R5	1010 0101	Temporary hold current	1 byte	R/W	Read/Store data
R6	1010 0110	Temporary hold current time duration	1 byte	R/W	Read/Store data
R7	1010 0111	Phase 1 time max	1 byte	R/W	Read/Store data
R8	1111 1100	Fault Register	1 byte	W R	Clear Fault Read Fault

Figure 19. Fault Register



5 Register description

5.1 Register A

MSB							LSB
7	6	5	4	3	2	1	0
IPK[7]	IPK[6]	IPK[5]	IPK[4]	IPK[3]	IPK[2]	IPK[1]	IPK[0]

Address: 0xA0

Type: R/W

Reset: 0010 1000b

Description: IPK[7...0]: I_{PEAK} current value.

I_{PEAK} current in ampere can be computed as IPK[7…0] * 20.55 / 255. Value are only guaranteed between 2 A and 14 A.

5.2 Register B

MSB							LSB
7	6	5	4	3	2	1	0
TPK[7]	TPK[6]	TPK[5]	TPK[4]	TPK[3]	TPK[2]	TPK[1]	TPK[0]

Address: 0xA1

Type: R/W

Reset: 0101 0010b

Description: TPK[7...0]: Phase 2 (I_{PEAK} current) duration.

Phase 2 duration in ms can be computed as TPK[7…0] * 5 / 255.

5.3 Register C

MSB							LSB
7	6	5	4	3	2	1	0
TPH[7]	TPH[6]	TPH[5]	TPH[4]	TPH[3]	TPH[2]	TPH[1]	TPH[0]

Address: 0xA2

Type: R/W

Reset: 0010 0100b

Description: TPH[7…0]: $t_{PEAK\_TO\_HOLD}$ (Phase 3) duration.

If DEMAG_MODE bit is 0, $t_{PEAK\_TO\_HOLD}$ in microseconds can be computed as TPH[7…0] * 500 / 255.

If DEMAG_MODE bit is set to 1, $t_{PEAK\_TO\_HOLD}$ in milliseconds can be computed as TPH[7…0] * 10 / 255.

5.4 Register D

MSB							LSB
7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	DEMAG_MODE

Address: 0xA3

Type: R/W

Reset: 0000 0001b

Description: DEMAG_MODE: demagnatization during phase 3 is fast if this bit is set to 1 or slow otherwise.

Note: If at the end of phase 2 the current has not reached I_{PEAK} value, slow demagnatization mode will be applied during phase 3 whatever the value of DEMAG_MODE bit.

5.5 Register E

MSB							LSB
7	6	5	4	3	2	1	0
IH[7]	IH[6]	IH[5]	IH[4]	IH[3]	IH[2]	IH[1]	IH[0]

Address: 0xA4

Type: R/W

Reset: 0110 1001b

Description: IH[7...0]: I_{HOLD} current value.

I_{HOLD} current value in ampere can be computed as IH[7…0] * 4.11 / 255. Value are only guaranteed between 0.5 A and 3 A.

5.6 Register F

MSB							LSB
7	6	5	4	3	2	1	0
IHTMP[7]	IHTMP[6]	IHTMP[5]	IHTMP[4]	IHTMP[3]	IHTMP[2]	IHTMP[1]	IHTMP[0]

Address: 0xA5

Type: R/W

Reset: 0111 1100b

Description: IHTMP[7…0]: I_{HOLD_TEMP} current value (reference current during Phase 4).

The current value in ampere can be computed as IHTMP[7…0] * 4.11 / 255. Value are only guaranteed between 0.5 A and 3.5 A.

5.7 Register G

MSB							LSB
7	6	5	4	3	2	1	0
THTMP[7]	THTMP[6]	THTMP[5]	THTMP[4]	THTMP[3]	THTMP[2]	THTMP[1]	THTMP[0]

Address: 0xA6

Type: R/W

Reset: 0000 0000b

Description: THTMP[7..0]: I_{HOLD_TEMP} duration inside Phase 4.

Phase3 duration in ms can be computed as THTMP[7…0] * 5 / 255.

5.8 Register H

MSB							LSB
7	6	5	4	3	2	1	0
TNPM[7]	TNPM[6]	TNPM[5]	TNPM[4]	TNPM[3]	TNPM[2]	TNPM[1]	TNPM[0]

Address: 0xA7

Type: R/W

Reset: 0100 0000b

Description: TNPKM[7…0]: $t_{NO\_PEAK\_MAX}$ value.

During phase 1, if I_{PEAK} value is not reached within $t_{NO\_PEAK\_MAX}$, the device switches into Phase 2. $t_{NO\_PEAK\_MAX}$ in millisecond can be computed as TNPKM[7…0] * 10 / 255.

5.9 Fault register

MSB							LSB
7	6	5	4	3	2	1	0
Reserved	Reserved	Open Load	OUT short to battery	Over voltage	Under voltage	Thermal warning	Thermal shutdown

Address: 0xFC

Type: R/W. Any write action will result in a register clear.

Reset: 0000 0000b

Bit [4] Output shorted to battery flag.
Bit is set by HW when an over current is detected on the output at the beginning of the injection cycle (phases 1 and 2). Write the register to clear this bit.

Bit [3] Over voltage flag.
Bit is set by HW when an over voltage is detected on the battery voltage, write the register to clear this bit.

Bit [2] Under voltage flag.
Bit is set by HW when an under voltage is detected on the battery voltage, write the register to clear this bit.

Bit [1] Thermal warning flag.
Bit is set by HW when the die temperature exceeds T_{TW} threshold, write the register to clear this bit.

Bit [0] Thermal shutdown flag.
Bit is set by HW when the die temperature exceeds T_{TSD} threshold, a register writing clears this bit only if the die temperature is lower than T_{TR}.

6 Electrical specification

6.1 Absolute maximum rating

Table 5. Absolute maximum rating

Symbol	Parameter	Value	Unit
V_{BATT}	Maximum DC supply voltage	40	V
V_{BATT_REV}	Reverse DC supply voltage	-0.3	V
V_{LOAD}	Maximum DC load voltage	Internally limited	V
I_{LOAD}	Maximum DC load current	Internally limited to I_{SHORT}	A
$I_{R(LOAD)}$	Maximum reverse output current, T_C = 25°C; t = 5 ms.	-20	A
E_{AS}	Single pulse energy S1 switch; V_{BATT} = 13.5 V; T_j = 150°C; L = 6 mH; R_L = 0 Ω, typical clamp voltage	88	mJ
E_{REP1}	Repetitive energy S1 switch. V_{BATT} = 13.5 V; T_j = 125°C; L = 6 mH; R_L = 0 Ω, typical clamp voltage	38.6	mJ
E_{REP2}	Repetitive energy S1 switch. V_{BATT} = 13.5 V; T_j = -40°C; L = 6 mH; R_L = 0 Ω, typical clamp voltage	70	mJ
V_{C3V3}	3.3 V logic supply voltage range	-0.3 to 3.6	V
V_{VDDL}	5 V external supply voltage	5.5	V
V_{SYNC_INJ} V_{E0} V_{E1} V_{E2} V_{CHECK_SIGNAL} V_{SCL} V_{SDA} V_{MAINT_IPK} V_{PWM} V_{CLAMP_FLAG} V_{FAULT} V_{ENABLE}	Logic input / output voltage range	-0.3 to V_{DDL}+0.3	V
V_{IN_SIGNAL} V_{REC}	HV signal pins	-0.3 to V_{BATT}	V
V_{OUT}	Output pin	55	V
V_{CTANK}	Maximum charge pump output voltage	V_{BATT} + 15V	V
V_{CPUMP1} V_{CPUMP2}	Maximum charge pump pins voltage	V_{BATT}	V
V_{ESD}	Electrostatic discharge (R = 1.5kW, C = 100pF, all pins)	+/-2000	V
T_j	Junction operating temperature	-40 to 150	°C
T_{STG}	Storage temperature	-55 to 150	°C

6.2 Thermal data

Table 6. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	See *Figure 23*	°C/W

6.3 Electrical characteristics

6 V < V_{BATT} < 28 V; -40°C < T_j < 150°C; unless otherwise specified

Table 7. V_{BATT} supply

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{BATT}	Operating supply voltage		6		28	V
I_{SON}	V_{BATT} DC supply current	V_{BATT} = 13 V; V_{DDL} = 5 V; V_{ENABLE} = 5 V; Output floating		2		mA
I_{STBY}	V_{BATT} + V_{VDDL} quiescent supply current	V_{BATT} = 13V; V_{DDL} = 5V; V_{ENABLE} = 0V ; Output floating -40°C < T_j < 85°C			10	µA
I_{DDL}	V_{DDL} DC supply current	V_{BATT} = 13 V; V_{DDL} = 5 V; V_{ENABLE} = 5 V		8	10	mA
V_{OV}	Overvoltage threshold		34		40	V
V_{UV}	Undervoltage threshold				6	V
V_{UV_hyst}	Undervoltage threshold hysteresis		0.4	0.6		V

Table 8. Power switches S_1 – S_2

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
RON1	On state resistance (excitation path)	I_{LOAD} = 5 A; S_1 = ON; V_{BATT} = 13 V; T_j = 25°C	—	—	0.060	Ω
		I_{LOAD} = 5 A; S_1 = ON; V_{BATT} = 13 V	—	—	0.120	Ω
		I_{LOAD} = 5 A; S_1 = ON; V_{BATT} = 6 V	—	—	0.150	Ω
RON2	On state resistance Recirculation Path	I_{LOAD} = 5 A; S_2 = ON; V_{BATT} = 13 V; T_j = 25°C	—	—	0.060	Ω
		I_{LOAD} = 5 A; S_2 = ON; V_{BATT} = 13 V	—	—	0.120	Ω
		I_{LOAD} = 5 A; S_2 = ON; V_{BATT} = 6 V	—	—	0.150	Ω

Table 9. S_1 switching (excitation path)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
TD_{ON_S1}	Turn-on delay time	V_{BATT} = 13.5 V; R_{LOAD} = 2.5 Ω	100	180	300	ns
T_{R_S1}	Rise time of output voltage			500	900	ns
TD_{OFF_S1}	Turn-off delay time		600	1400	2000	ns
T_{F_S1}	Fall time of output voltage			600	1000	ns
V_{CLAMP_S1}	Switch S_1 clamp voltage	I_{LOAD} = 0.5/14 A; S_1 = off; S_2 = off	44		55	V

Table 10. Switching (recirculating path)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
TD_{ON_S2}	Turn-on delay time	V_{BATT} = 13.5 V; R_{LOAD} = 2.5Ω	—	280	600	ns
T_{R_S2}	Rise time of output voltage		—	1500	3000	ns
TD_{OFF_S2}	Turn-off delay time		—	150	600	ns
T_{F_S2}	Fall time of output voltage		—	200	800	ns

Table 11. V_{DDL} undervoltage detection

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{POR_OFF}	power-on-reset threshold	V_{DDL} increasing	3.8	4	4.2	V
V_{POR_ON}	power-on-reset threshold	V_{DDL} decreasing	3.2	3.4	3.6	V
V_{POR_hyst}	power-on-reset hysteresis	V_{POR_OFF} - V_{POR_ON}	0.3			V

Table 12. Enable

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{ENABLE\ H}$	Enable voltage threshold	V_{BATT} = 13 V	1	1.8	2.3	V
V_{ENABLE_L}	Enable voltage reset	V_{BATT} = 13 V	0.8	1.5	1.9	V
V_{ENABLE_HYST}	Enable voltage hysteresis	V_{BATT} = 13 V	0.1	0.3		V
I_{ENABLE}	Enable pull down current	V_{ENABLE} = 5 V	20	50	100	µA

Table 13. Input: SYNC_INJ

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{SYNC_L}	Input low level voltage	V_{DDL} = 5 V			1.08	V
V_{SYNC_H}	Input high level voltage	V_{DDL} = 5 V	2.1			V
V_{SYNC_HYST}	Input hysteresis voltage	V_{DDL} = 5 V	0.15			V
I_{SYNC_INJ}	pull down current at SYNC_INJ input	V_{SYNC_INJ} = 1.5 V	20	50	80	µA

Table 14. Input: PWM

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{PWM_L}	Input low level voltage	V_{DDL} = 5 V			1.08	V
V_{PWM_H}	Input high level voltage	V_{DDL} = 5 V	2.1			V
V_{PWM_HYST}	Input hysteresis voltage	V_{DDL} = 5 V	0.15			V
I_{PWM}	Pull down current at PWM input	V_{PWM} = 1.5 V	20	50	80	µA

Table 15. Inputs: E0, E1, E2

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{Ex_L}	Input low level voltage	V_{DDL} = 5V			1.08	V
V_{Ex_H}	Input high level voltage	V_{DDL} = 5V	2.1			V
V_{Ex_HYST}	Input hysteresis voltage	V_{DDL} = 5V	0.15			V
I_{Ex_IN}	Pull down current at Ex input	V_{Ex} = 1.5V	20	50	80	µA

Table 16. IN_SIGNAL VOLTAGE MONITOR, CHECK_SIGNAL

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{IN\_SIGNAL\_L}$	Input low level voltage threshold		0.4 V_{BATT}	0.45 V_{BATT}	0.5 V_{BATT}	V
$V_{IN\_SIGNAL\_H}$	Input high level voltage threshold		0.5 V_{BATT}	0.55 V_{BATT}	0.6 V_{BATT}	V
$V_{IN\_SIGNAL\_HYST}$	Input hysteresis voltage			0.1 V_{BATT}		V
V_{CHECK_SIGNAL}	Check_signal output voltage	V_{IN_SIGNAL} = 0 V; I_{CHECK_SIGNAL} = 1 mA			0.9	V

Table 17. Differential current sense amplifier

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{ICM_AMP}	Input voltage range – common mode		0		0.8	V

Table 17. Differential current sense amplifier (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{IDIFF_AMP}	Input voltage range – differential mode	Gain = 20; V_{DDL} = 5 V	10		80	mV
		Gain = 4; V_{DDL} = 5 V	20		400	mV
V_{IOFF_AMP}	Input offset voltage	V_{DDL} = 5 V	-500		500	µV
$Gain_{AMP}$	Opamp gain	$I_{LOAD} = I_{HOLD}$		20		
		$I_{LOAD} = I_{PEAK}$		4		
GBW_{AMP}	Gain bandwidth product	G = 20		2		MHz
		G = 4		0.4		MHz
$CMRR_{AMP}$	Input common mode rejection	F = 1 KHz	60			dB
$PSRR+_{AMP}$	3.3 V power supply rejection ratio			55		dB
$PSRR-_{AMP}$	GND power supply rejection ratio			40		dB
$T_{SETTLING\_R}$	Rising settling time	G = 20; (V_{RSP} - V_{RSN}) = 0 V to 10 mV in 10 ns G = 4; (V_{RSP} - V_{RSN}) = 0 V to 20 mV in 10 ns			3.5	µs
$T_{SETTLING\_F}$	Falling settling time	G = 20; (V_{RSP} - V_{RSN}) = 10 mV to 0 V in 10 ns G = 4; (V_{RSP} - V_{RSN}) = 20 mV to 0 V in 10 ns			3.5	µs

Table 18. Current sense comparator

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{ICM\_PWMCOMP}$	Input voltage range – common mode		0.05	—	2	V
$V_{IOFF\_PWMCOMP}$	Input offset voltage	V_{DDL} = 5 V	-15	—	6	mV
$TD_{PWMCOMP}$	Input to output delay	V_{INPUT} from 200 mV to 1.7 V in 10 ns		—	200	ns

Table 19. 8-bit digital to analog converter

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$VLSB_{DAC}$	Less significant bit voltage		—	4.851	—	mV

Table 20. S_1 protections and diagnostic

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
T_{TW}	Thermal warning threshold junction temperature	S_1 = ON	130			°C
T_{TSD}	Thermal shutdown threshold junction temperature	S_1 = ON	155	175		°C
T_{TR}	Thermal reset threshold junction temperature	S_1 = ON	130			°C
I_{SHORT}	Over current detection	S_1 = ON	15			A
I_{OL}	Open-load detection	S_1 = ON; I_{PEAK} = 3.2 A	0.2 * (I_{PEAK}/4)	I_{PEAK}/4	1.2 * (I_{PEAK}/4)	A
		S_1 = ON; I_{PEAK} = 5 A	0.4 * (I_{PEAK}/4)	I_{PEAK}/4	1.2 * (I_{PEAK}/4)	A
		S_1 = ON; $I_{PEAK} \geq$ 8 A	0.7 * (I_{PEAK}/4)	I_{PEAK}/4	1.3 * (I_{PEAK}/4)	A
V_{FAULT_OUT}	Status output voltage	Diagnostic output active (low); I_{FAULT} = 1 mA			0.9	V
$V_{CLAMPFLAG\_OUT}$	Clamp diagnostic pin output voltage	$I_{CLAMPFLAG}$ = 100 µA			0.1	V
		$I_{CLAMPFLAG}$ = -100µA	V_{DDL} - 0.1			V
$V_{MAINTIPK\_OUT}$	MAINT_IPK diagnostic pin voltage	$I_{MAINTIPK}$ = 100 µA			0.1	V
		$I_{MAINTIPK}$ = -100 µA	V_{DDL} - 0.1			V

Table 21. Application registers range

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{PEAK}	Register A	Application useful range = 2 → 14 A	0	3.2	20.55	A
I_{HOLD}	Register E	Application useful range = 0.5 → 3 A	0	1.7	4.11	A
I_{HOLD_TEMP}	Register F	Application useful range = 0.5 → 3.5 A	0	2	4.11	A
t_{PEAK}	Register B		0	1.6	5	ms
t_{HOLD_TEMP}	Register G		0	0	5	ms
$t_{NO\_PEAK\_MAX}$	Register H		0	2.5	10	ms
$t_{PEAK\_TO\_HOLD}$	Register C	DEMAG MODE = 0 (slow)	0		10	ms
		DEMAG MODE = 1 (fast)	0	70	500	µs

Table 22. IPEAK, IHOLD (-40 °C < T_j < 150 °C, unless otherwise specified)

Symbol	Parameter	Test conditions(1)	Min	Typ	Max	Unit
I_{PEAK}	Peak current	RegisterA = IDEFAULT	2.72	3.2	3.7	A
		RegisterA = 2 A	1.60	2	2.40	A
		T = 125°C; RegisterA = 2 A	1.70	2	2.30	A
		RegisterA = 5 A	4.25	5	5.75	A
		RegisterA = 8 A	6.8	8	9.2	A
		T = 125°C; RegisterA = 14 A	12.6	14	15.4	A
		RegisterA = 14 A	11.9	14	16.1	A
I_{HOLD}	Hold current	RegisterE = IDEFAULT	1.445	1.7	1.955	A
		T = 125°C; RegisterE = 0.5 A	0.325	0.5	0.6	A
		T = 125°C; RegisterE = 1 A	0.9	1	1.1	A
		RegisterE = 1 A	0.85	1	1.15	A
		RegisterE = 3 A	2.55	3	3.45	A
F_{PWM}	PWM frequency	Design guaranteed	10	20		KHz
D_{CYCLE}	PWM duty cycle	F_{PWM} = 20 KHz	0.15			

1. V_{BATT} > 8 V

Table 23. Charge pump

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{CP}	Charge pump output voltage(1)	I_{CP} = 200 µA	V_{BATT} + 7	V_{BATT} + 9	V_{BATT} + 13	V
C_{PUMP1}	External charge pump capacitor			4.7		nF
C_{PUMP2}	External charge pump capacitor			4.7		nF
C_{TANK}	External charge pump capacitor for S_2 driver peak current			100		nF
I_{CP1}	Charge pump output current positive	V_{BATT} + 7 V < V_{CTAK} < V_{BATT} + 13 V test mode	15	27	34	mA
I_{CP2}	Charge pump output current negative	V_{BATT} + 7 V < V_{CTAK} < V_{BATT} + 13 V test mode	-140	-100	-55	mA

1. Guaranteed by design using suggested external network:
C_{PUMP1}, C_{PUMP2}: 4.7 nF - 50 V ceramic capacitors;
C_{TANK}: 100 nF - 50 V ceramic capacitor;
Charge pump diodes: BAT41 type

Table 24. I²C-bus SDA, SCL I/O stages

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage			—	0.3 * V_{C3V3}	V
V_{IH}	High level input voltage		0.7 * V_{C3V3}	—		V
V_{HYS}	Hysteresis of Schmitt trigger inputs		0.05 * V_{C3V3}	—		V
V_{OL}	Low level output voltage	I_{SINK} = 3 mA		—	0.4	V
I_{OL}	Low level output current	V_{OL} = 0.4 V	3	—		mA
t_{OFF}	Output fall time from V_{IHmim} to V_{ILmax}			—	250	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter			—	50	ns
I_i	Input current	0.1 * V_{DDL} < V_I < 0.9 * V_{DDL}	-10	—	10	µA
C_i	I/O pin capacitance			—	10	pF

Table 25. I²C-bus SDA, SCL bus lines characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
All values are referred to $V_{IH(min)}$ (0.3 * V_{DDL}) and $V_{IL(max)}$ (0.7 * V_{DDL}). See also *Figure 20*.						
f_{SCL}	SCL clock frequency			—	100	kHz
$t_{HD;STA}$	Hold time (repeated) START condition	After this period the first clock pulse is generated	4.0	—		µs
t_{LOW}	LOW period of the SCL clock		4.7	—		µs
t_{HIGH}	HIGH period of the SCL clock		4.0	—		µs
$t_{SU;STA}$	Set-up time for a repeated START condition		4.7	—		µs
$t_{HD;DAT}$	Data hold time(1)		300(2)	—	(3)	ns
$t_{SU;DAT}$	Data set-up time		250	—		ns
t_r	Rise time of both SDA and SCL signals			—	1000	ns
t_f	Fall time of both SDA and SCL signals			—	300	ns
$t_{SU;STO}$	Set-up time for a STOP condition		4.0	—		µs
t_{BUF}	Bus free time between a STOP and START condition		4.7	—		µs

Table 25. I²C-bus SDA, SCL bus lines characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Cb	Capacitive load for each bus line			—	400	pF
$t_{VD;DAT}$	Data valid time(4)			—	3.45(3)	µs
$t_{VD;ACK}$	Data valid acknowledge time(5)			—	3.45(3)	µs
V_{nL}	Noise margin at the LOW level	For each connected device (including hysteresis)	0.1 * V_{DDL}	—		V
V_{nH}	Noise margin at the HIGH level	For each connected device (including hysteresis)	0.2 * V_{DDL}	—		V

1. $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge.
2. A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH(min)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum $t_{HD;DAT}$ could be 3.45 us, but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time.
4. $t_{VD;DAT}$ = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse)
5. $t_{VD;ACK}$ = time for acknowledgment signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse)

Figure 20. Definition of timing on the I²C-bus

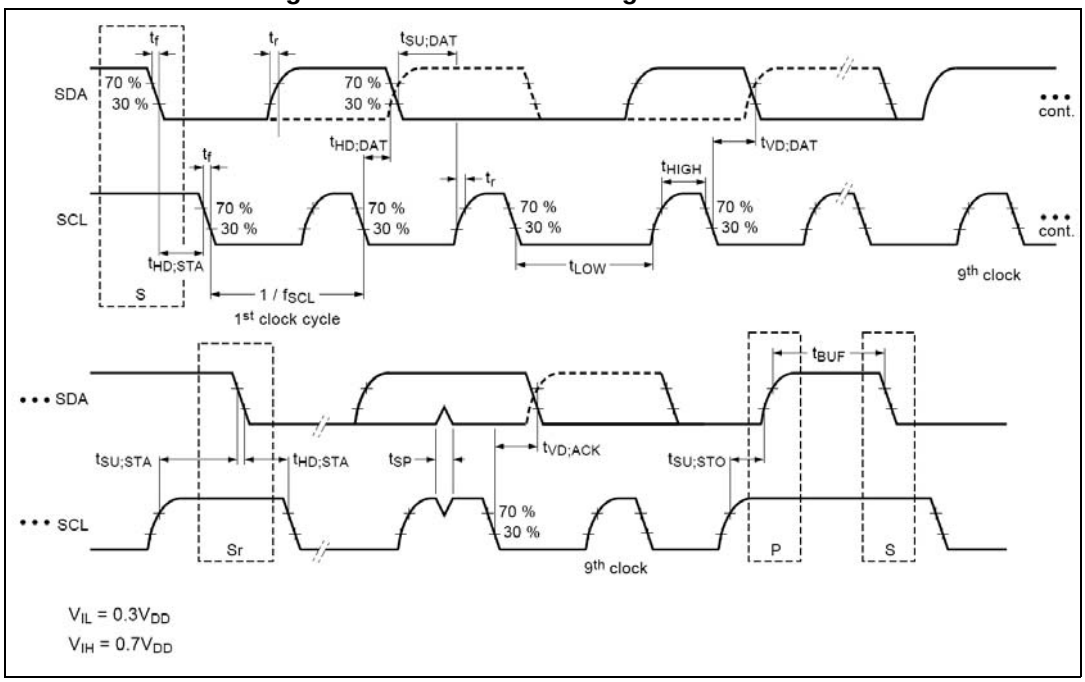


Table 26. Electrical transient requirements (part 1)

ISO 7637-2: 2004(E) Test Pulse	Test levels(1)		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and impedance
	III	IV				
1	-75 V	-100 V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37 V	+50 V	5000 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	-100 V	-150 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
3b	+75 V	+100 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
4	-6 V	-7 V	1 pulse			100 ms, 0.01 Ω
5b(2)	+65 V	+87 V	1 pulse			400 ms, 2 Ω

1. The above test levels must be considered referred to V_{CC} = 13.5V except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to OUT.

Table 27. Electrical transient requirements (part 2)

ISO 7637-2: 2004(E) test pulse	Test level results(1)	
	III	IV
1	C	E
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b (2)	C	C

1. The above test levels must be considered referred to V_{CC} = 13.5 V except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to OUT.

Table 28. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the

7 OTP (One Time Programmable Memory)

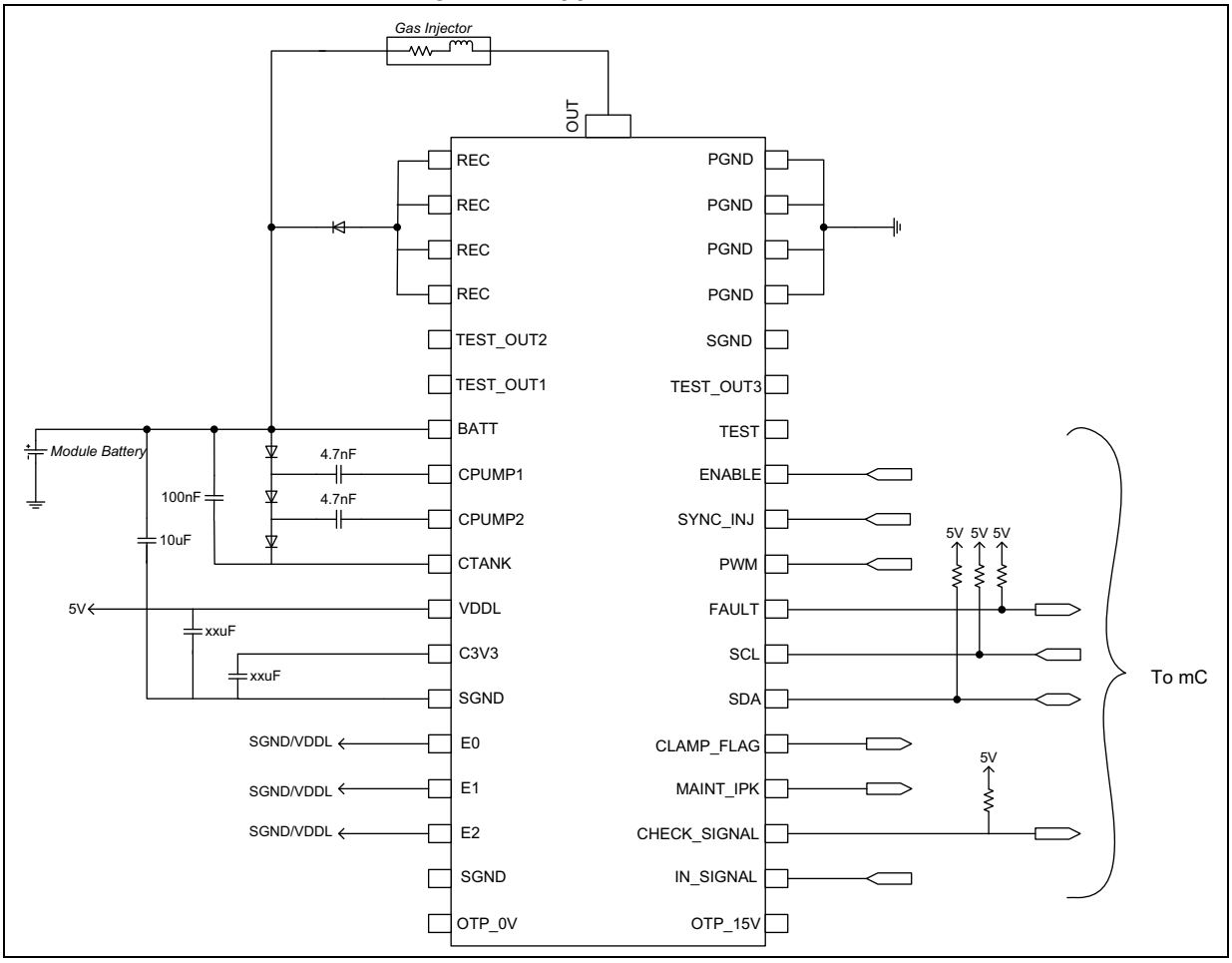
L99SD01-E provides two 16 bit OTP modules for internal parameter trimming. Default application parameters are hard coded into the device. OTP use is reserved to ST and other access will be hardware forbidden.

Table 29. 16 bit OTP modules

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OTP_0				Osc trimming			Current reference trimming					Bandgap trimming				
OTP_1				Reference slope				Blanking			IHOLD current trimming					

8 Application schematic

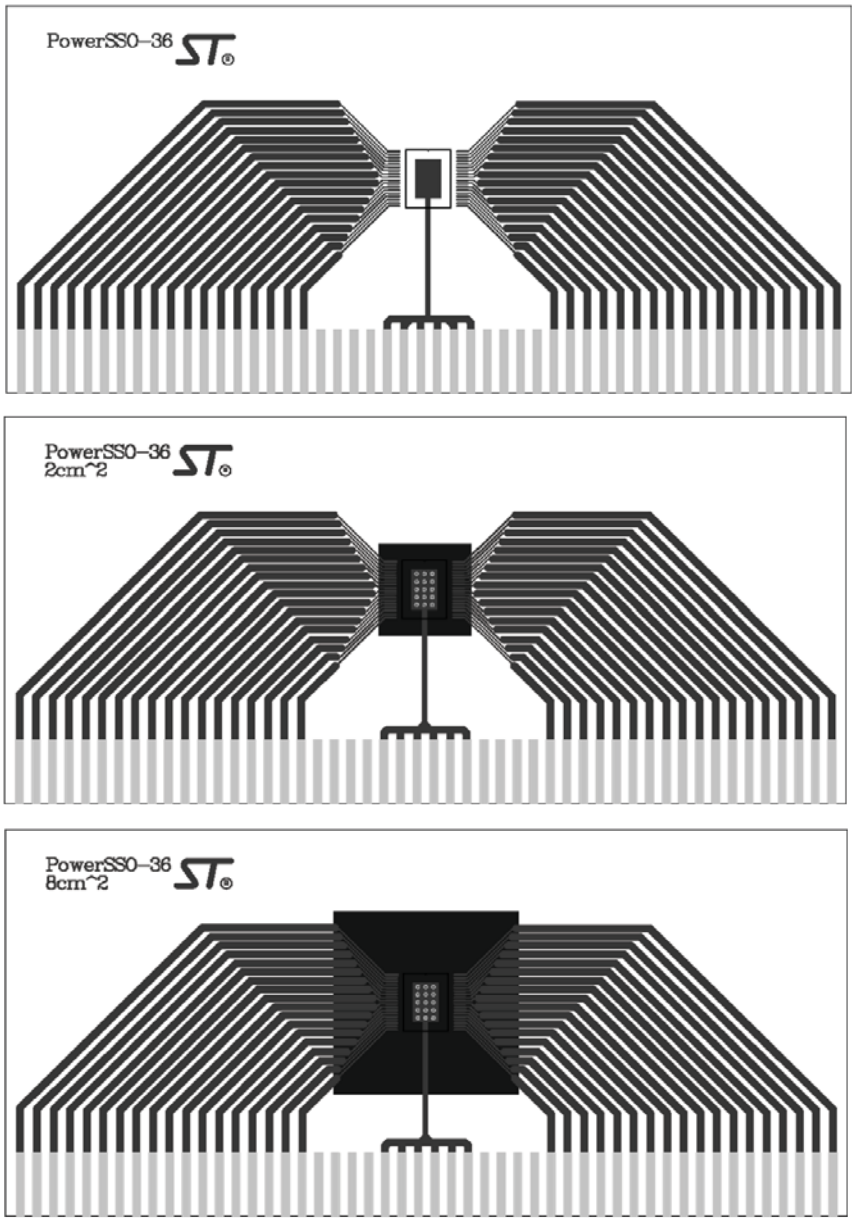
Figure 21. Application schematic



9 Package and PCB thermal data

9.1 PowerSSO-36 thermal data

Figure 22. PowerSSO-36 PC board



1. Board finish thickness 1.6 mm +/- 10%; Board double layer; Board dimension 129 mm x 60 mm; Board Material FR4; Cu thickness 0.070 mm; Thermal vias separation 1.2 mm; Thermal via diameter 0.3 mm +/-0.08 mm; Cu thickness on vias 0.025 mm; Footprint dimension 4.1 mm x 6.5 mm.

Figure 23. Rthj-amb vs PCB copper area in open box free air condition

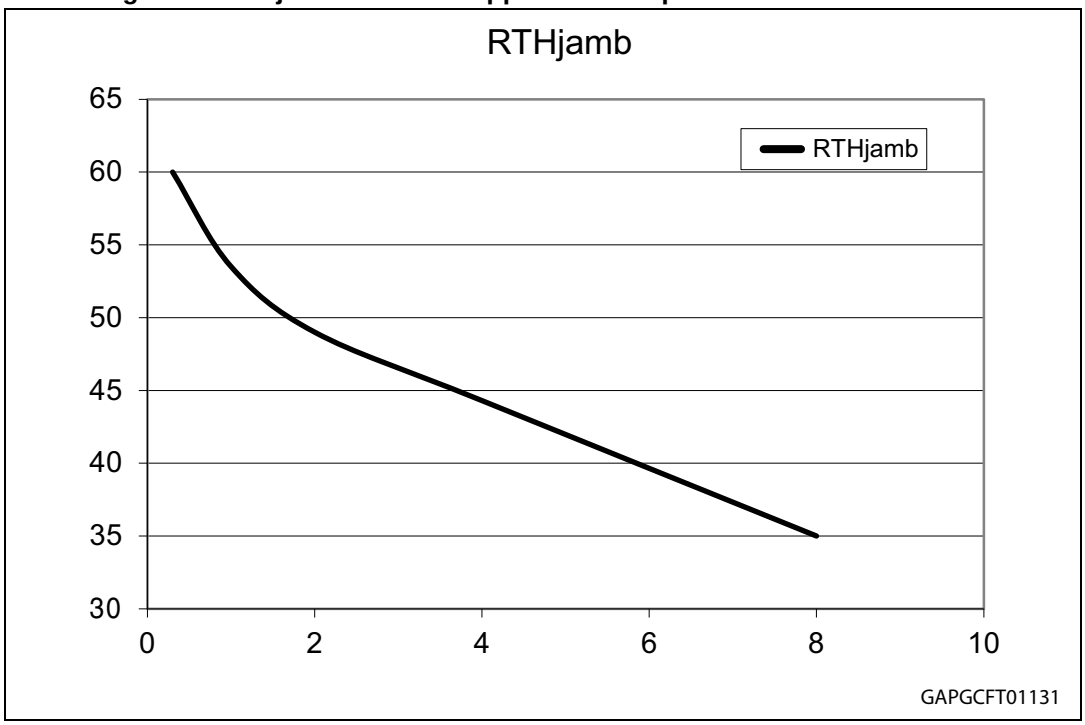


Figure 24. PowerSSO-36 thermal impedance junction ambient

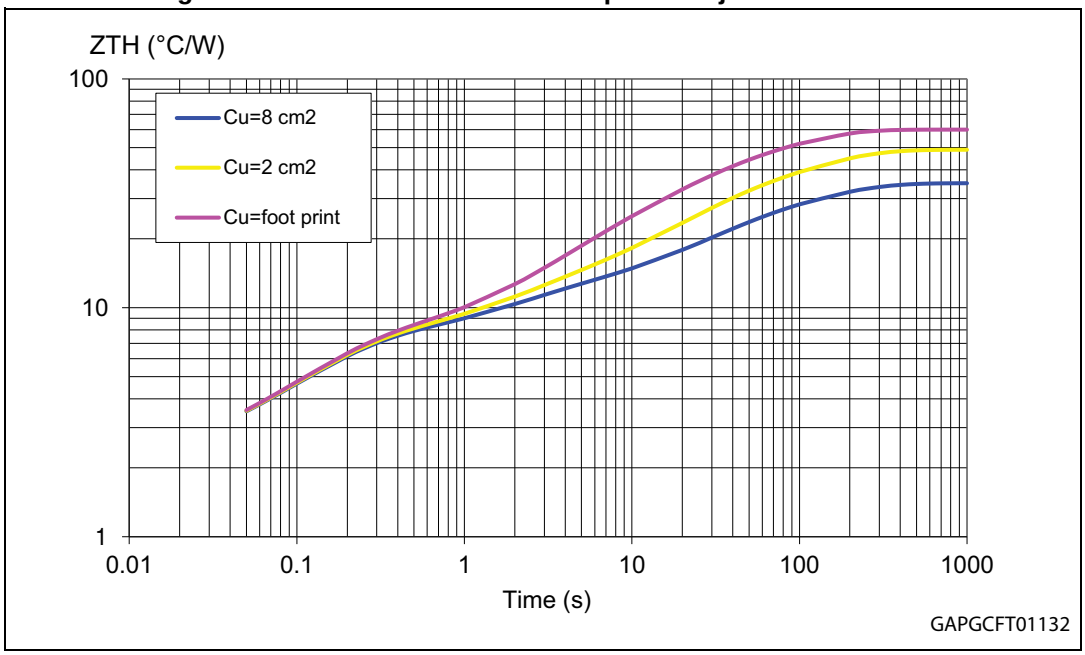


Figure 25. Thermal fitting model of a HSD in PowerSSO-36

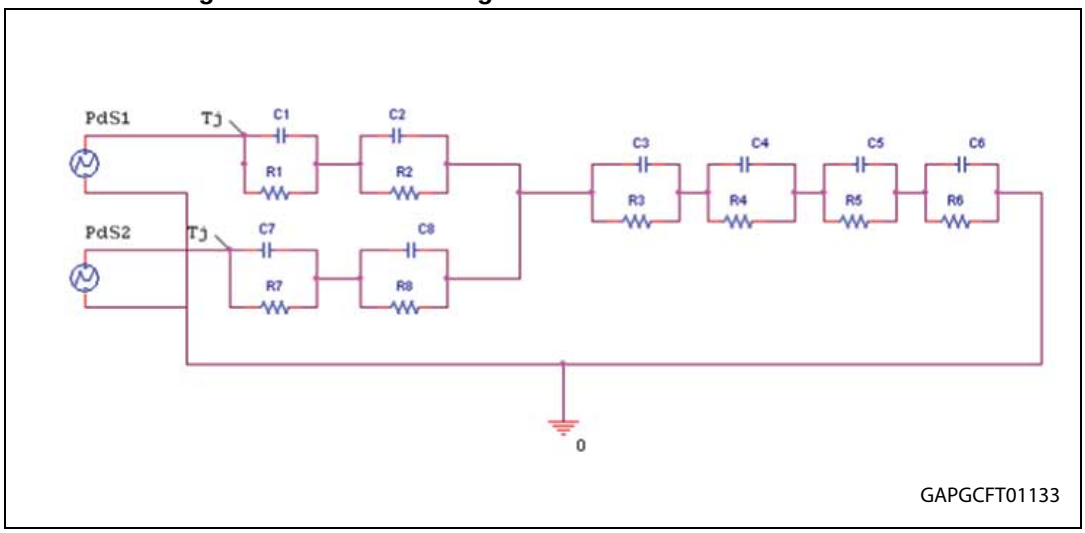


Table 30. Thermal parameters

Area/island (cm^2)	FP	2	8
R1 = R7 (°C/W)	0.8		
R2 = R8 (°C/W)	1.2		
R3 (°C/W)	5		
R4 (°C/W)	8		
R5 (°C/W)	18	15	10
R6 (°C/W)	27	23	14
C1 = C7 (W·s/°C)	0.0005		
C2 = C8 (W·s/°C)	0.002		
C3 (W·s/°C)	0.03		
C4 (W·s/°C)	0.5		
C5 (W·s/°C)	1	1.5	3
C6 (W·s/°C)	3	5	9

10 Package and packing Information

10.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

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10.2 PowerSSO-36 package information

Figure 26. PowerSSO-36 package dimensions

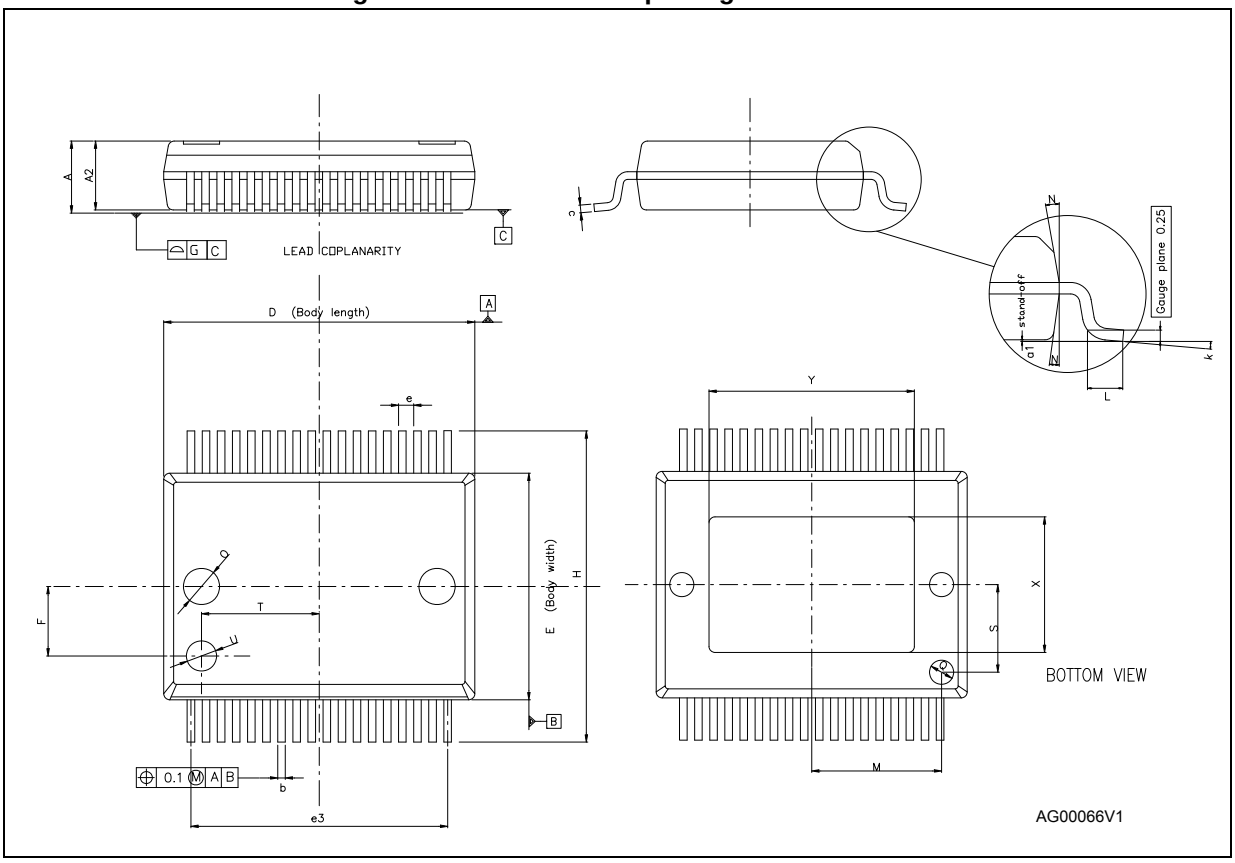

Table 31. PowerSSO-36 mechanical data

Symbol	Millimeters		
	Min	Typ.	Max
A	2.15		2.47
A2	2.15		2.40
a1	0		0.1
b	0.18		0.36

Table 31. PowerSSO-36 mechanical data

Symbol	Millimeters		
	Min	Typ.	Max
c	0.23		0.32
D(1)	10.10		10.50
E	7.4		7.6
e		0.5	
e3		8.5	
F		2.3	
G			0.1
G1			0.06
H	10.1		10.5
h			0.4
k	0°		8°
L	0.55		0.90
M		4.3	
N			10°
O		1.2	
Q		0.8	
S		2.9	
T		3.65	
U		1	
X	4.1		4.7
Y	6.5		7.1

1. “D” and “E“ do not include mold Flash or protrusions. Mold Flash or protrusion shall not exceed 0.15 mm per side (0.006”).

11 Revision history

Table 32. Document revision history

Date	Revision	Changes
05-Dec-2011	1	Initial release
12-Sep-2013	2	*Table 2: Pin description*: – SCL: updated description Updated *Section 4.1: SDA and SCL signals* Added *Chapter 5: Register description* *Table 5: Absolute maximum rating*: – I_{LOAD}, $I_{R(LOAD)}$: updated value – EC: deleted rows – E_{AS}, E_{REP1}, E_{REP2}: added rows Updated *Table 6: Thermal data* *Table 18: Current sense comparator*: – $V_{IOFF\_PWMCOMP}$: updated min value *Table 20: S1 protections and diagnostic*: – I_{OL}: added test condition and values *Table 22: IPEAK, IHOLD (-40 °C < Tj < 150 °C, unless otherwise specified)*: – I_{PEAK}, I_{HOLD}: added test condition and values *Table 23: Charge pump*: – added note – I_{CP1}, I_{CP2}: added rows *Table 24: I2C-bus SDA, SCL I/O stages*: – I_{OL}: removed test condition – t_{OFF}: updated parameter, removed test condition and min value *Table 25: I2C-bus SDA, SCL bus lines characteristics*: – f_{SCL}, $t_{HD;STA}$, t_{LOW}, t_{HIGH}, $t_{SU;STA}$, $t_{HD;DAT}$, $t_{SU;DAT}$, t_r, t_f, $t_{SU;STO}$, t_{BUF}, Cb, $t_{VD;DAT}$, $t_{VD;ACK}$: updated values Added *Table 26: Electrical transient requirements (part 1)*, *Table 27: Electrical transient requirements (part 2)* and *Table 28: Electrical transient requirements (part 3)* Added *Chapter 9: Package and PCB thermal data*
18-Sep-2013	3	Updated disclaimer.
11-Apr-2014	4	Updated document title.
18-Dec-2014	5	Updated document title, *Features* and *Description*.

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