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**July 2015** 

## **FDMS86200DC**

# N-Channel Dual Cool $^{TM}$ 56 Shielded Gate PowerTrench $^{@}$ MOSFET 150 V, 40 A, 17 $m\Omega$

#### **Features**

- Shielded Gate MOSFET Technology
- Dual Cool<sup>TM</sup> Top Side Cooling PQFN package
- Max  $r_{DS(on)} = 17 \text{ m}\Omega$  at  $V_{GS} = 10 \text{ V}$ ,  $I_D = 9.3 \text{ A}$
- Max  $r_{DS(on)} = 25 \text{ m}\Omega$  at  $V_{GS} = 6 \text{ V}$ ,  $I_D = 7.8 \text{ A}$
- High performance technology for extremely low r<sub>DS(on)</sub>
- 100% UIL tested
- RoHS Compliant

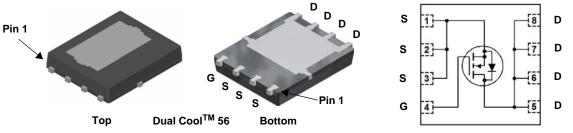


#### **General Description**

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. Advancements in both silicon and Dual Cool  $^{TM}$  package technologies have been combined to offer the lowest  $r_{DS(on)}$  while maintaining excellent switching performance by extremely low Junction-to-Ambient thermal resistance.

#### **Applications**

- Primary MOSFET in DC DC converters
- Secondary Synchronous rectifier
- Load switch



#### MOSFET Maximum Ratings TA = 25 °C unless otherwise noted

Symbol	Paramo	eter		Ratings	Units
V <sub>DS</sub>	Drain to Source Voltage			150	V
V <sub>GS</sub>	Gate to Source Voltage			±20	V
	Drain Current -Continuous	T <sub>C</sub> = 25 °C		40	
$I_D$	-Continuous	T <sub>A</sub> = 25 °C	(Note 1a)	9.3	Α
	-Pulsed		(Note 4)	100	
E <sub>AS</sub>	Single Pulse Avalanche Energy		(Note 3)	294	mJ
ר	Power Dissipation	T <sub>C</sub> = 25 °C		125	w
$P_{D}$	Power Dissipation	T <sub>A</sub> = 25 °C	(Note 1a)	3.2	VV
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Tempera	ature Range		-55 to +150	°C

#### **Thermal Characteristics**

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Top Source)	2.5	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Bottom Drain)	1.0	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	81	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1i)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1j)	23	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1k)	11	

#### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
86200	FDMS86200DC	Dual Cool <sup>TM</sup> 56	13"	12 mm	3000 units

# **Electrical Characteristics** $T_J = 25$ °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	acteristics					
$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	150			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu A$ , referenced to 25°C		105		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 120 V, V <sub>GS</sub> = 0 V			1	μΑ
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA

#### **On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	2.0	3.3	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu A$ , referenced to 25 °C		-11		mV/°C
		$V_{GS} = 10 \text{ V}, I_D = 9.3 \text{ A}$		14	17	
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	$V_{GS} = 6 \text{ V}, I_D = 7.8 \text{ A}$		17	25	mΩ
, ,		$V_{GS} = 10 \text{ V}, I_D = 9.3 \text{ A}, T_J = 125 \text{ °C}$		29	35	
9 <sub>FS</sub>	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_D = 9.3 \text{ A}$		32		S

#### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V 75 V V 0 V		2110	2955	pF
Coss	Output Capacitance	$V_{DS} = 75 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1  MHz		205	290	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 1 101112		8.1	15	pF
$R_g$	Gate Resistance		0.1	1.5	3.0	Ω

### **Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time			16	29	ns
t <sub>r</sub>	Rise Time	V <sub>DD</sub> = 75 V , I <sub>D</sub> = 9	9.3 A,	4	10	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	V <sub>GS</sub> = 10 V, R <sub>GEN</sub>	= 6 Ω	23	37	ns
t <sub>f</sub>	Fall Time			5	10	ns
0	Total Gate Charge	$V_{GS} = 0 V to 10 V$		30	42	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0 V to 6 V$	V <sub>DD</sub> = 75 V	19	27	nC
$Q_{gs}$	Gate to Source Charge		$I_D = 9.3 A$	9.7		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			5.6		nC

#### **Drain-Source Diode Characteristics**

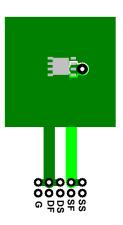
V	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 9.3 \text{ A}$ (Note 2)	0.8	1.3	\/
$v_{SD}$	Source to Drain blode Polward Voltage	$V_{GS} = 0 \text{ V}, I_S = 2.6 \text{ A}$ (Note 2)	0.7	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 9.3 A, di/dt = 100 A/μs	79	126	ns
Q <sub>rr</sub>	Reverse Recovery Charge	iF = 9.5 A, αί/αι = 100 A/μS	126	176	nC

#### **Thermal Characteristics**

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Top Source)	2.5	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Bottom Drain)	1.0	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1c)	27	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1d)	34	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1e)	16	°C/M
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1f)	19	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1g)	26	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1h)	61	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1i)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1j)	23	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1k)	11	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1I)	13	

#### NOTES

1. R<sub>0JA</sub> is determined with the device mounted on a FR-4 board using a specified pad of 2 oz copper as shown below. R<sub>0JC</sub> is guaranteed by design while R<sub>0CA</sub> is determined by the user's board design.



a. 38 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 81 °C/W when mounted on a minimum pad of 2 oz copper

- c. Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
- d. Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper
- e. Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
- f. Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper
- g. 200FPM Airflow, No Heat Sink,1 in<sup>2</sup> pad of 2 oz copper
- h. 200FPM Airflow, No Heat Sink, minimum pad of 2 oz copper
- i. 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
- j. 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper
- k. 200FPM Airflow, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
- I. 200FPM Airflow, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper
- 2. Pulse Test: Pulse Width < 300  $\mu\text{s},$  Duty cycle < 2.0%.
- 3.  $E_{AS}$  of 294 mJ is based on starting  $T_J$  = 25 °C; N-ch: L = 3 mH,  $I_{AS}$  = 14 A,  $V_{DD}$  = 150 V,  $V_{GS}$  = 10 V. 100% test at L = 0.1 mH,  $I_{AS}$  = 42 A.
- ${\it 4. Pulsed Id limited by junction temperature, td} <= 10 uS, please refer to SOA curve for more details. \\$

## **Typical Characteristics** $T_J = 25$ °C unless otherwise noted

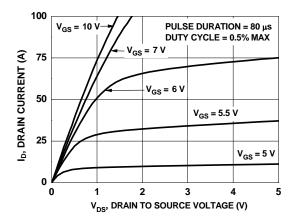


Figure 1. On-Region Characteristics

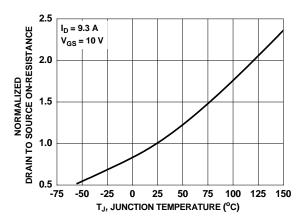


Figure 3. Normalized On-Resistance vs Junction Temperature

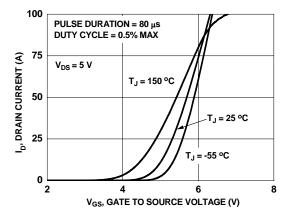


Figure 5. Transfer Characteristics

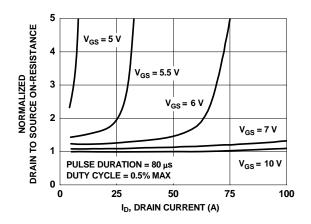


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

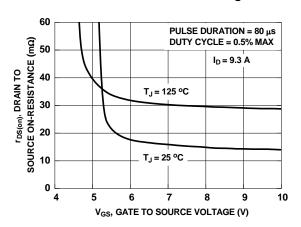


Figure 4. On-Resistance vs Gate to Source Voltage

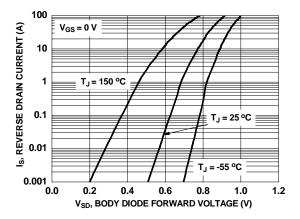


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

# **Typical Characteristics** $T_J = 25$ °C unless otherwise noted

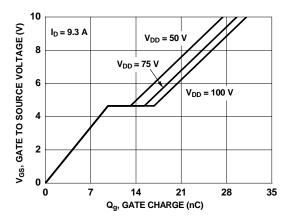


Figure 7. Gate Charge Characteristics

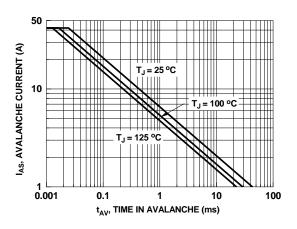


Figure 9. Unclamped Inductive Switching Capability

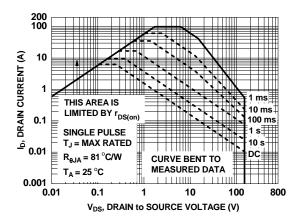


Figure 11. Forward Bias Safe Operating Area

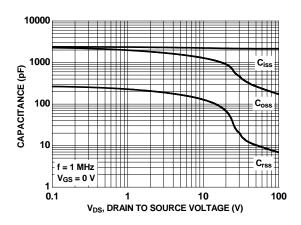


Figure 8. Capacitance vs Drain to Source Voltage

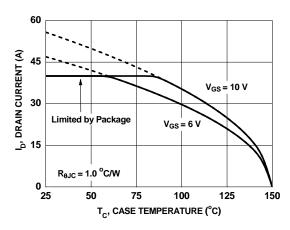


Figure 10. Maximum Continuous Drain Current vs Case Temperature

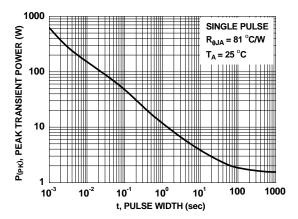


Figure 12. Single Pulse Maximum Power Dissipation

# Typical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted

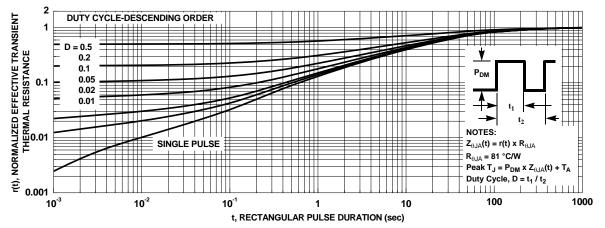
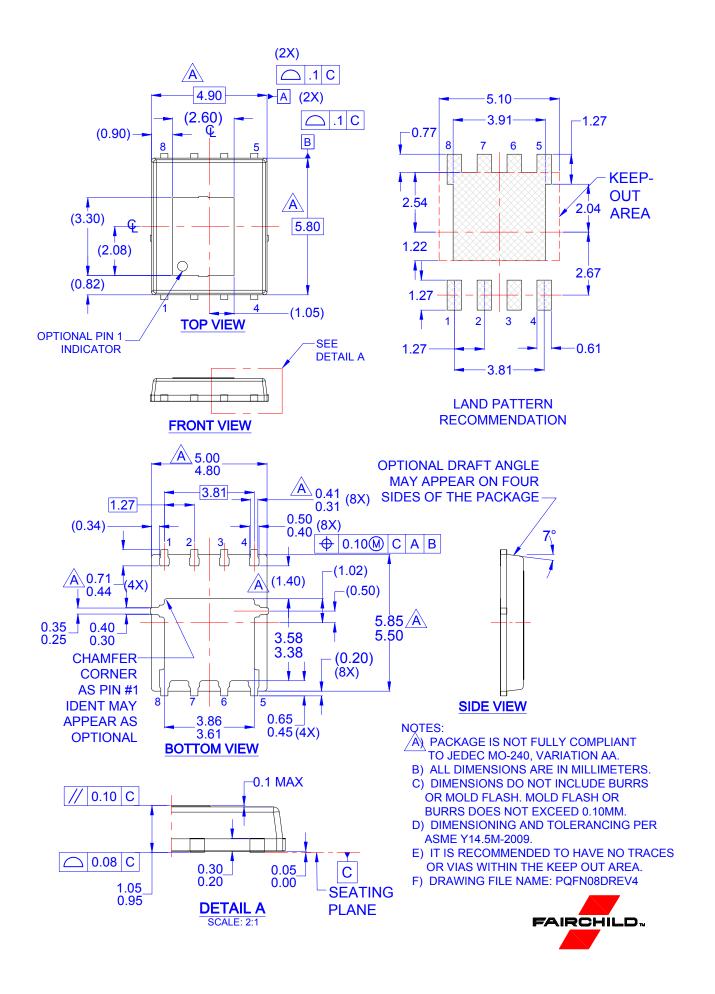


Figure 13. Junction-to-Ambient Transient Thermal Response Curve



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