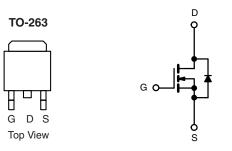


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Vishay Siliconix

# Automotive N-Channel 40 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	40			
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.0040			
$R_{DS(on)}(\Omega)$ at $V_{GS} = 4.5 \text{ V}$	0.0055			
I <sub>D</sub> (A)	50			
Configuration	Single			



N-Channel MOSFET

#### **FEATURES**

- TrenchFET® Power MOSFET
- Package with Low Thermal Resistance
- 100 % R<sub>q</sub> and UIS Tested
- AEC-Q101 Qualified<sup>d</sup>
- Material categorization:
  For definitions of compliance please see <a href="https://www.vishay.com/doc?99912">www.vishay.com/doc?99912</a>



HALOGEN

FREE

ORDERING INFORMATION	
Package	TO-263
Lead (Pb)-free and Halogen-free	SQM50N04-4m0L-GE3

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-Source Voltage		$V_{DS}$	40	V	
Gate-Source Voltage		$V_{GS}$	± 20	V	
Continuous Drain Current <sup>a</sup>	T <sub>C</sub> = 25 °C	l <sub>D</sub>	50		
Continuous Drain Current	T <sub>C</sub> = 125 °C		50		
Continuous Source Current (Diode Conduction)a	I <sub>S</sub>	50	А		
Pulsed Drain Current <sup>b</sup>	I <sub>DM</sub>	200			
Single Pulse Avalanche Current		I <sub>AS</sub>	62		
Single Pulse Avalanche Energy		E <sub>AS</sub>	192	mJ	
Maximum Power Dissipation <sup>b</sup>	T <sub>C</sub> = 25 °C	Pn	150	W	
iviaximum rower bissipation	T <sub>C</sub> = 125 °C	r <sub>D</sub>	50	VV	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 175	°C		

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-Ambient	PCB Mount <sup>c</sup>	$R_{thJA}$	40	°C/W	
Junction-to-Case (Drain)		R <sub>thJC</sub>	1	G/W	

#### Notes

- a. Package limited.
- b. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.
- c. When mounted on 1" square PCB (FR-4 material).
- d. Parametric verification ongoing.



PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> :	= 0 V, I <sub>D</sub> = 250 μA	40	-	-	V	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	· V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.5	2.0	2.5	V	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> =	$0 \text{ V}, \text{ V}_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA	
		$V_{GS} = 0 V$	V <sub>DS</sub> = 40 V	-	-	1		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{GS} = 0 V$	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 125 °C	-	-	50	μΑ	
		$V_{GS} = 0 V$	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 175 °C	-	-	150		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	$V_{DS} \ge 5 V$	50	-	-	Α	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A	-	0.0025	0.0040		
Drain-Source On-State Resistancea	D	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A, T <sub>J</sub> = 125 °C	-	-	0.0067		
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A, T <sub>J</sub> = 175 °C	-	-	0.0082	Ω	
	V <sub>GS</sub> = 4.5 V I <sub>D</sub> = 20 A		I <sub>D</sub> = 20 A	-	0.0030	0.0055		
Forward Transconductanceb	9 <sub>fs</sub>	V <sub>DS</sub>	= 15 V, I <sub>D</sub> = 15 A	-	110	-	S	
Dynamic <sup>b</sup>								
Input Capacitance	C <sub>iss</sub>				4880	6100		
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 V$	$V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$	-	560	700	рF	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	250	315		
Total Gate Charge <sup>c</sup>	Qg			-	85	130		
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V	$V_{DS} = 20 \text{ V}, I_{D} = 50 \text{ A}$	-	14	-	nC	
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			-	14	-		
Gate Resistance	R <sub>g</sub>	f = 1 MHz		1	2.15	3.3	Ω	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>				9	14		
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD} = 20 \text{ V}, \text{ R}_{L} = 0.4 \Omega$ $I_{D} \cong 50 \text{ A}, \text{ V}_{GEN} = 10 \text{ V}, \text{ R}_{g} = 1 \Omega$		-	11	17		
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	39	59	ns -	
Fall Time <sup>c</sup>	t <sub>f</sub>			-	11	17		
Source-Drain Diode Ratings and Characteristics <sup>b</sup>								
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	200	Α	
Forward Voltage	V <sub>SD</sub>	I <sub>F</sub> = 50 A, V <sub>GS</sub> = 0 V		_	0.9	1.5	V	

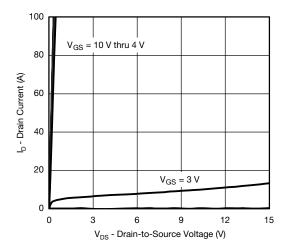
### Notes

- a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

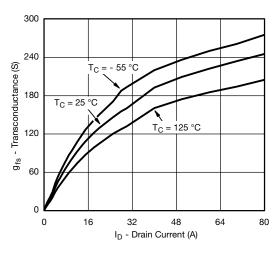
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



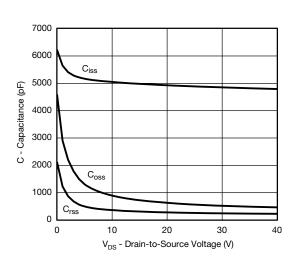
### TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



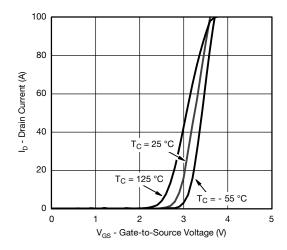
#### **Output Characteristics**



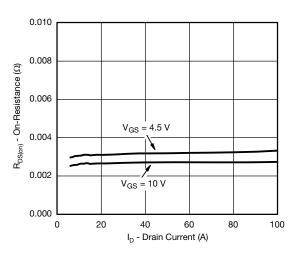
#### Transconductance



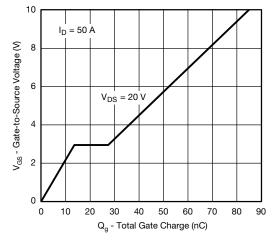
Capacitance



#### **Transfer Characteristics**



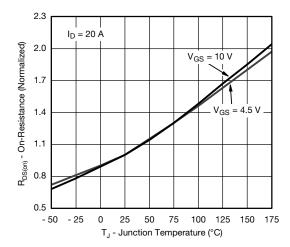
On-Resistance vs. Drain Current



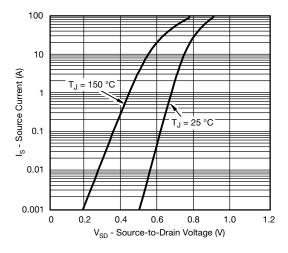
**Gate Charge** 



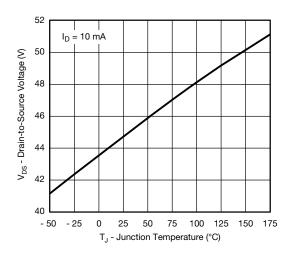
### TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



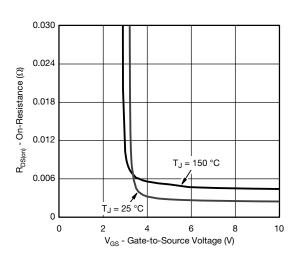
#### On-Resistance vs. Junction Temperature



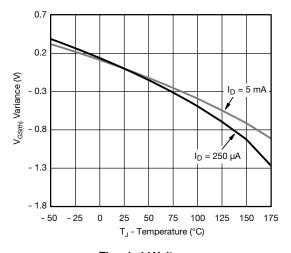
**Source Drain Diode Forward Voltage** 



Drain Source Breakdown vs. Junction Temperature

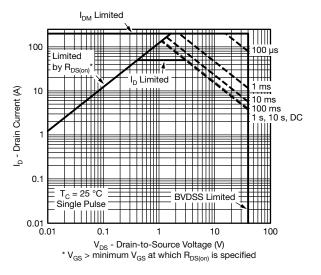


On-Resistance vs. Gate-to-Source Voltage

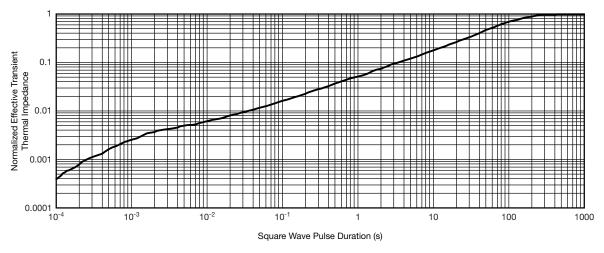


**Threshold Voltage** 

### **THERMAL RATINGS** (T<sub>A</sub> = 25 °C, unless otherwise noted)

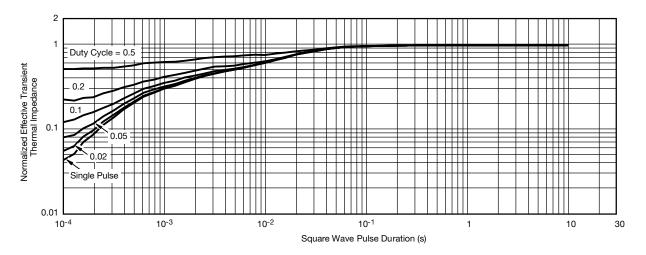


#### Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

### THERMAL RATINGS (T<sub>A</sub> = 25 °C, unless otherwise noted)



#### Normalized Thermal Transient Impedance, Junction-to-Case

#### Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg?66800">www.vishay.com/ppg?66800</a>.

## D<sup>2</sup>PAK / TO-263 and TO-262

Ordering codes for the SQ rugged series power MOSFETs in the D<sup>2</sup>PAK / TO-263 and TO-262 packages:

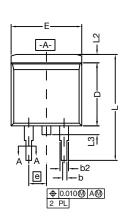
DATASHEET PART NUMBER	OLD ORDERING CODE a	NEW ORDERING CODE
SQM100N04-2m7	SQM100N04-2M7-GE3	SQM100N04-2M7_GE3
SQM100N10-10	SQM100N10-10-GE3	SQM100N10-10_GE3
SQM110N05-06L	SQM110N05-06L-GE3	SQM110N05-06L_GE3
SQM110P06-8m9L	SQM110P06-8M9L-GE3	SQM110P06-8M9L_GE3
SQM120N02-1m3L	SQM120N02-1M3L-GE3	SQM120N02-1M3L_GE3
SQM120N03-1m5L	SQM120N03-1M5L-GE3	SQM120N03-1M5L_GE3
SQM120N04-1m7	SQM120N04-1M7-GE3	SQM120N04-1M7_GE3
SQM120N04-1m7L	SQM120N04-1M7L-GE3	SQM120N04-1M7L_GE3
SQM120N04-1m9	SQM120N04-1M9-GE3	SQM120N04-1M9_GE3
SQM120N06-06	SQM120N06-06-GE3	SQM120N06-06_GE3
SQM120N06-3m5L	SQM120N06-3M5L-GE3	SQM120N06-3M5L_GE3
SQM120N10-09	SQM120N10-09-GE3	SQM120N10-09_GE3
SQM120N10-3m8	SQM120N10-3M8-GE3	SQM120N10-3M8_GE3
SQM120P04-04L	SQM120P04-04L-GE3	SQM120P04-04L_GE3
SQM120P06-07L	SQM120P06-07L-GE3	SQM120P06-07L_GE3
SQM120P10-10m1L	-	SQM120P10_10m1LGE3
SQM200N04-1m1L	SQM200N04-1M1L-GE3	SQM200N04-1M1L_GE3
SQM200N04-1m7L	SQM200N04-1M7L-GE3	SQM200N04-1M7L_GE3
SQM200N04-1m8	SQM200N04-1M8-GE3	SQM200N04-1M8_GE3
SQM25N15-52	SQM25N15-52-GE3	SQM25N15-52_GE3
SQM35N30-97	SQM35N30-97-GE3	SQM35N30-97_GE3
SQM40N10-30	SQM40N10-30-GE3	SQM40N10-30_GE3
SQM40N15-38	SQM40N15-38-GE3	SQM40N15-38_GE3
SQM40P10-40L	SQM40P10-40L-GE3	SQM40P10-40L_GE3
SQM47N10-24L	SQM47N10-24L-GE3	SQM47N10-24L_GE3
SQM50020EL	-	SQM50020EL_GE3
SQM50N04-4m0L	SQM50N04-4M0L-GE3	SQM50N04-4M0L_GE3
SQM50N04-4m1	SQM50N04-4M1-GE3	SQM50N04-4M1_GE3
SQM50P03-07	SQM50P03-07-GE3	SQM50P03-07_GE3
SQM50P04-09L	SQM50P04-09L-GE3	SQM50P04-09L_GE3
SQM50P06-15L	SQM50P06-15L-GE3	SQM50P06-15L_GE3
SQM50P08-25L	SQM50P08-25L-GE3	SQM50P08-25L_GE3
SQM60030E	-	SQM60030E_GE3
SQM60N06-15	SQM60N06-15-GE3	SQM60N06-15_GE3
SQM60N20-35	SQM60N20-35-GE3	SQM60N20-35_GE3
SQM85N15-19	SQM85N15-19-GE3	SQM85N15-19_GE3
SQV120N10-3m8	SQV120N10-3m8-GE3	SQV120N10-3m8_GE3
SQV120N06-4m7L	-	SQV120N06-4m7L_GE3

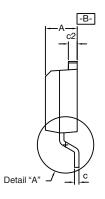
#### Note

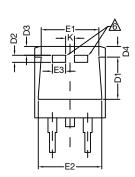
a. Old ordering code is obsolete and no longer valid for new orders



# TO-263 (D<sup>2</sup>PAK): 3-LEAD

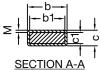








DETAIL A (ROTATED 90°)



⋝:	b     b1	ţ
2:	T /////// 5	
	SECTION A.	Ţ

- 1. Plane B includes maximum features of heat sink tab and plastic.
- 2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- 3. Pin-to-pin coplanarity max. 4 mils.
- 4. \*: Thin lead is for SUB, SYB. Thick lead is for SUM, SYM, SQM.
- 5. Use inches as the primary measurement.

6 This feature is for thick lead.

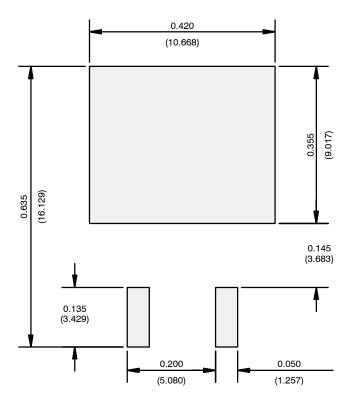
INCHE		HES	MILLIMETERS			
	DIM.	MIN.	MAX.	MIN.	MAX.	
Α		0.160	0.190	4.064	4.826	
	b	0.020	0.039	0.508	0.990	
	b1	0.020	0.035	0.508	0.889	
	b2	0.045	0.055	1.143	1.397	
c*	Thin lead	0.013	0.018	0.330	0.457	
C	Thick lead	0.023	0.028	0.584	0.711	
c1	Thin lead	0.013	0.017	0.330	0.431	
CI	Thick lead	0.023	0.027	0.584	0.685	
	c2	0.045	0.055	1.143	1.397	
	D	0.340	0.380	8.636	9.652	
	D1	0.220	0.240	5.588	6.096	
	D2	0.038	0.042	0.965	1.067	
	D3	0.045	0.055	1.143	1.397	
	D4	0.044	0.052	1.118	1.321	
	Е	0.380	0.410	9.652	10.414	
	E1	0.245	-	6.223	=	
	E2	0.355	0.375	9.017	9.525	
	E3	0.072	0.078	1.829	1.981	
	е	0.100	) BSC	2.54 BSC		
	K	0.045	0.055	1.143	1.397	
L		0.575	0.625	14.605	15.875	
L1		0.090	0.110	2.286	2.794	
L2		0.040	0.055	1.016	1.397	
L3		0.050	0.070	1.270	1.778	
L4		0.010 BSC		0.254 BSC		
	М	-	0.002	-	0.050	
ECN: T13-0707-Rev. K, 30-Sep-13						

DWG: 5843





### RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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Vishay

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Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.

Revision: 02-Oct-12 Document Number: 91000

### **ПОСТАВКА** ЭЛЕКТРОННЫХ КОМПОНЕНТОВ

многоканальный

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001 Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

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### Офис по работе с юридическими лицами:

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E-mail: info@moschip.ru

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moschip.ru moschip.ru\_6 moschip.ru\_4 moschip.ru\_9